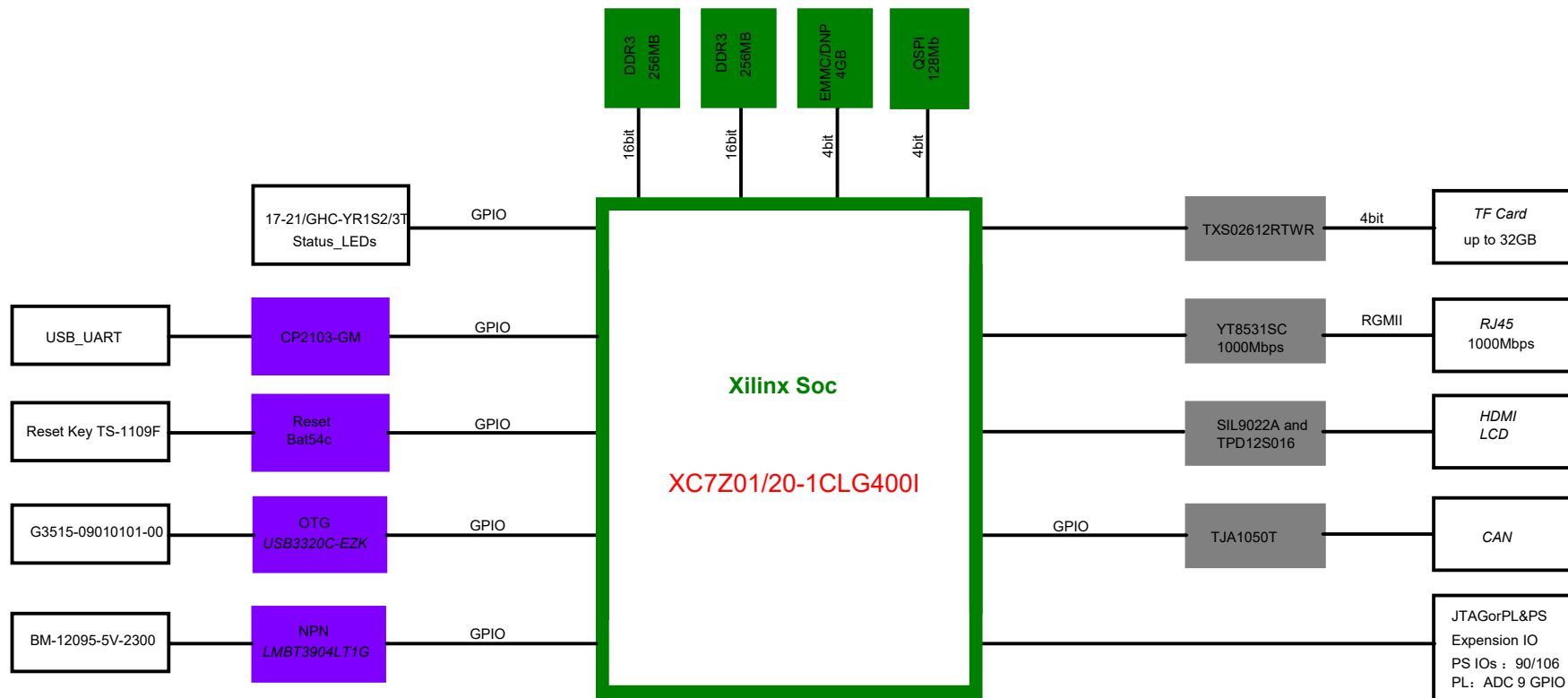
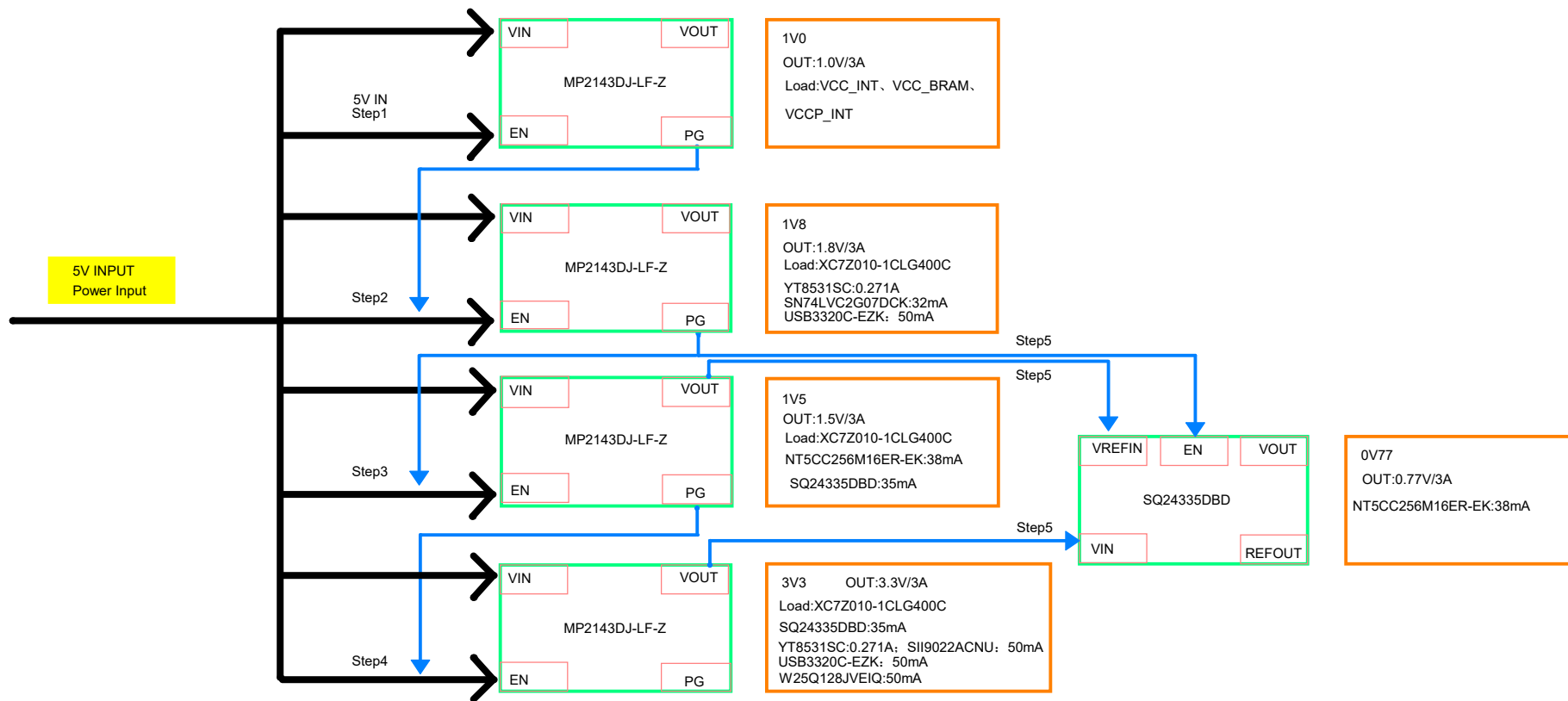
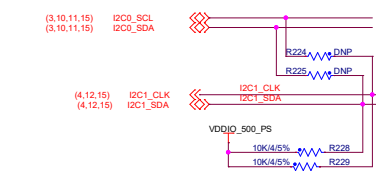
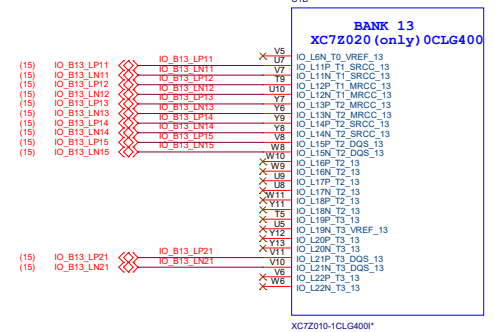
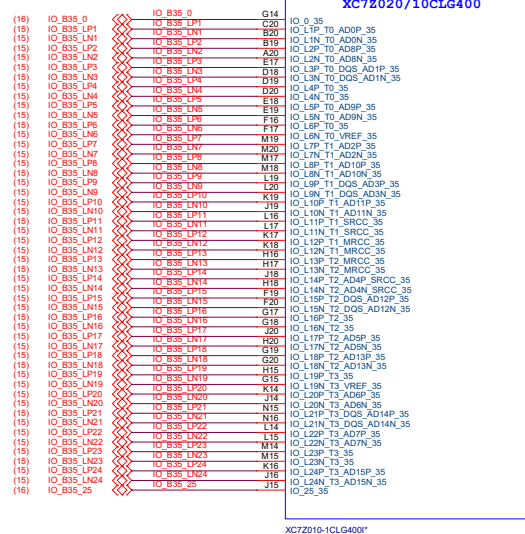
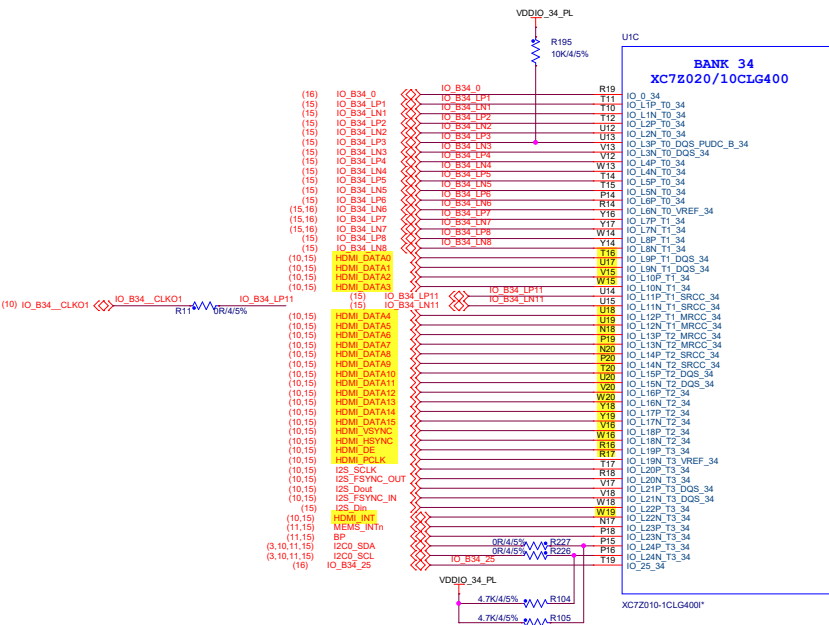
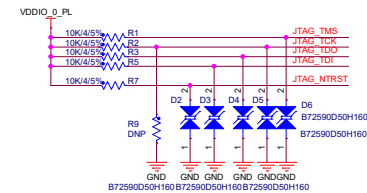
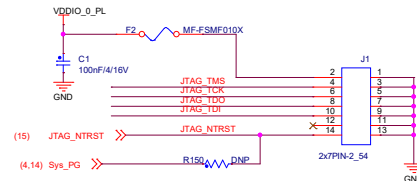
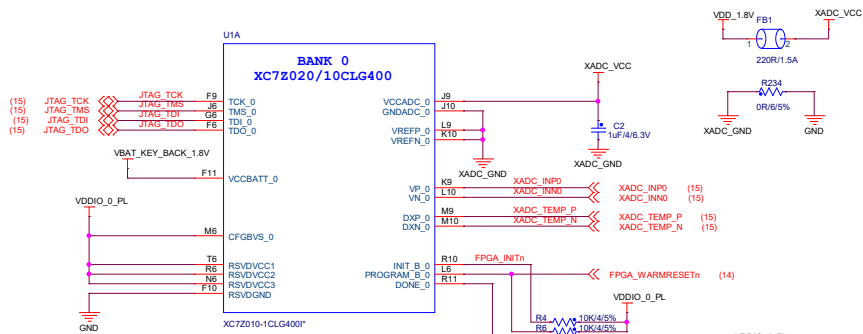


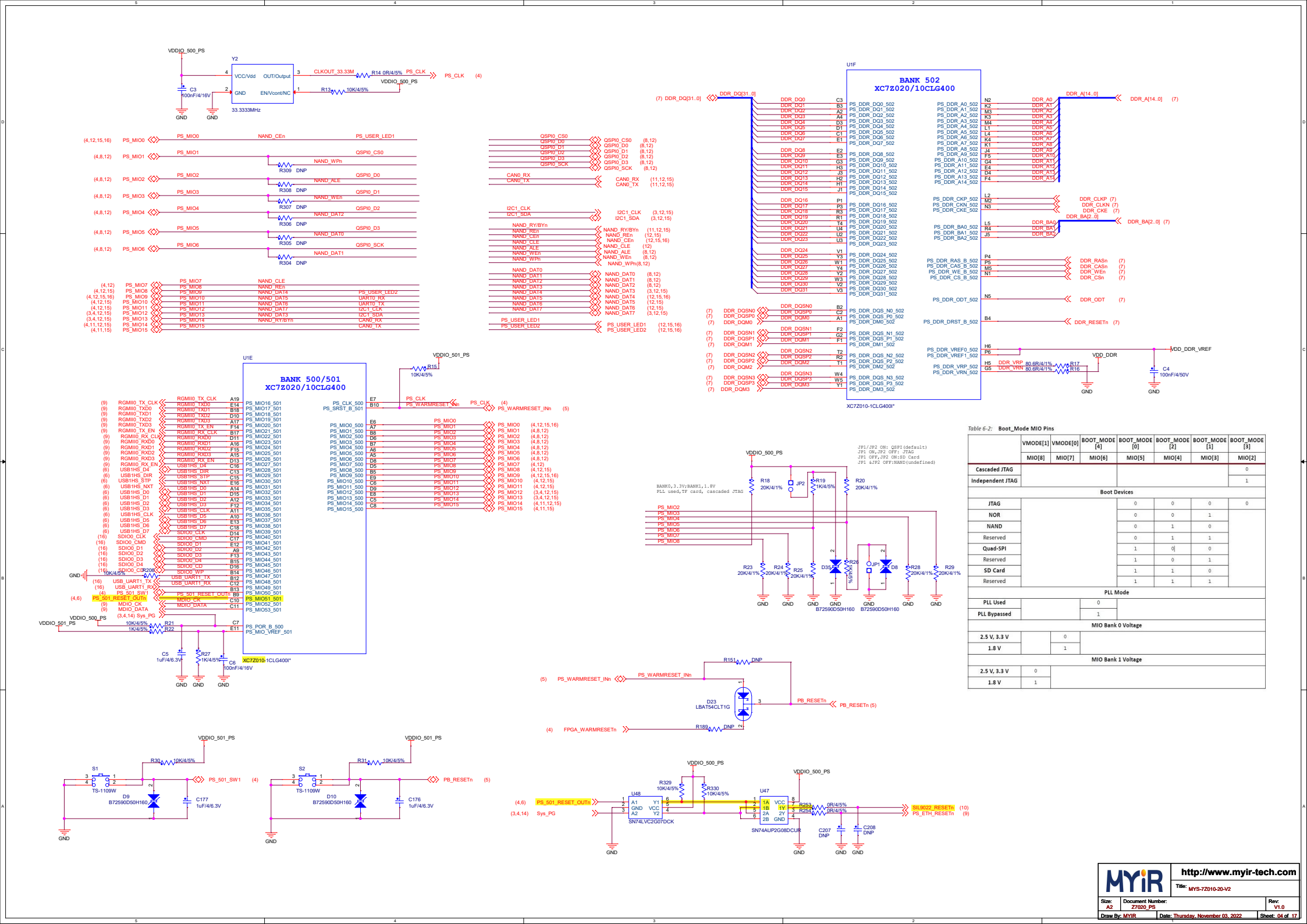
REV	Description	DATE	BY
Ver 1	Initial Release.		

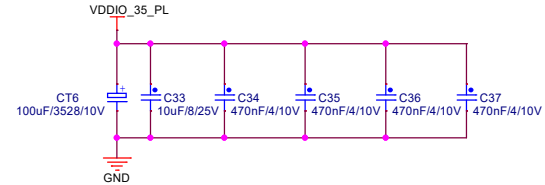
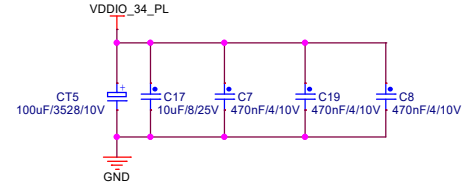
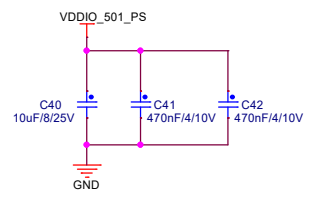
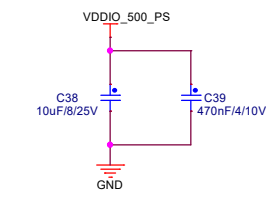
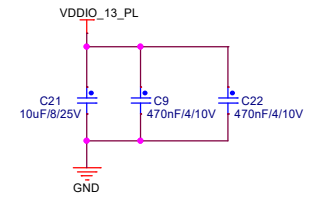
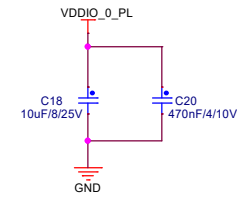
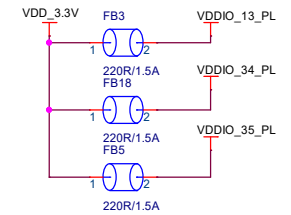
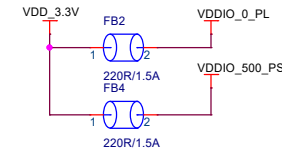
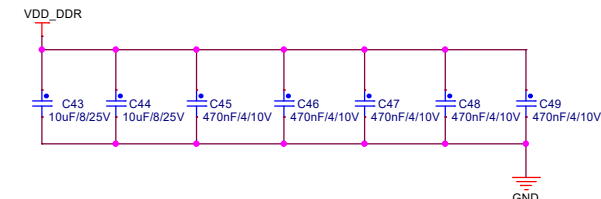
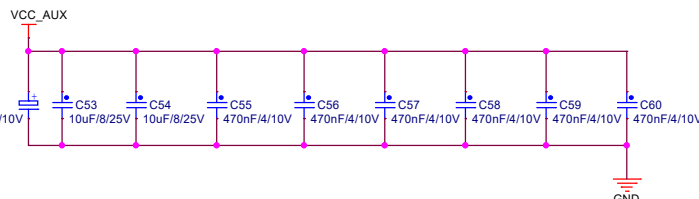
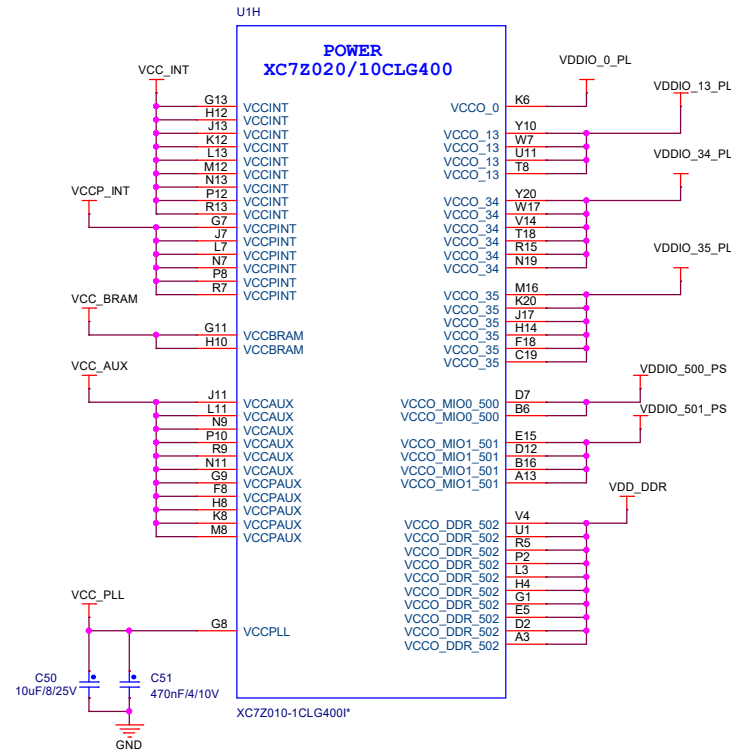
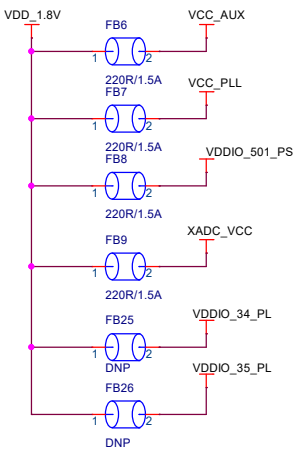
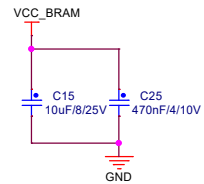
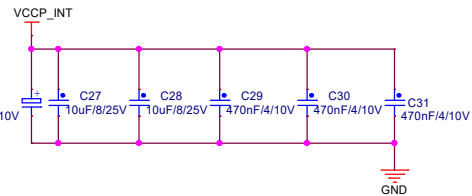
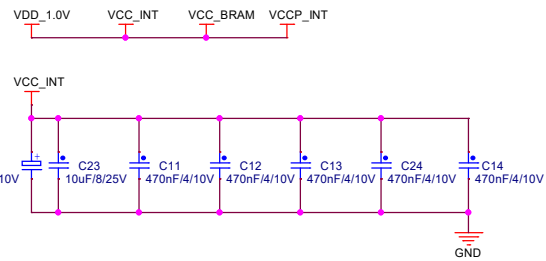
PAGE NO.	SCHEMATIC PAGE
1	TITLE PAGE
2	BLOCK
3	Z7020_PL
4	POWER LOGIC
5	Z7020_PS
6	Z7020_POWER
7	USB OTG
8	DDR3 MEMORY
9	QSPI FLASH
10	10/100/1000 ETHERNET
11	HDMI
12	Sensor: G&T,CAN
13	NAND_FLASH
14	PWR:1.0V&1.5V,VTT
15	Power 1.8V,3.3V&DCin
16	EXP CONN
17	MISC



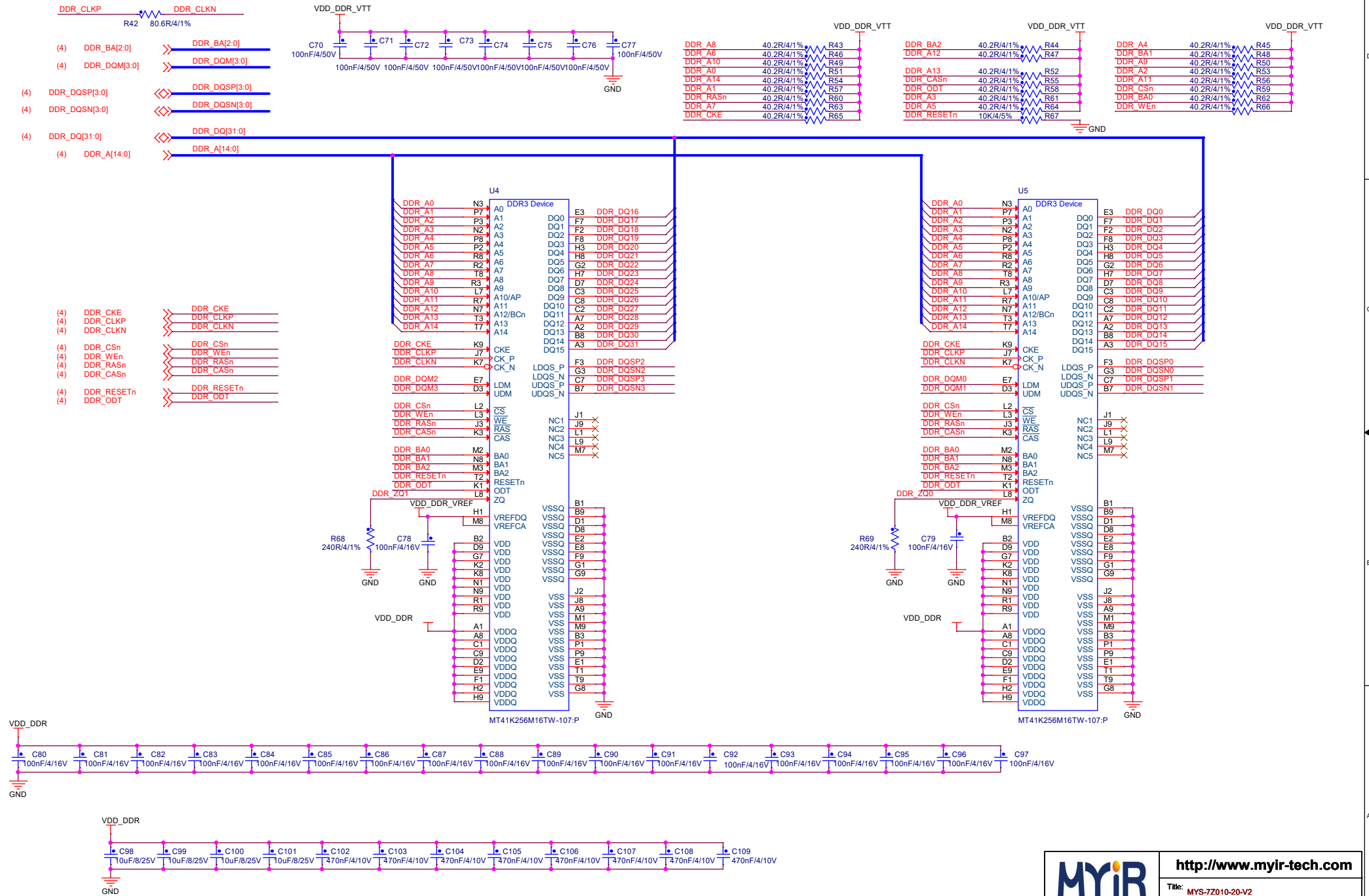


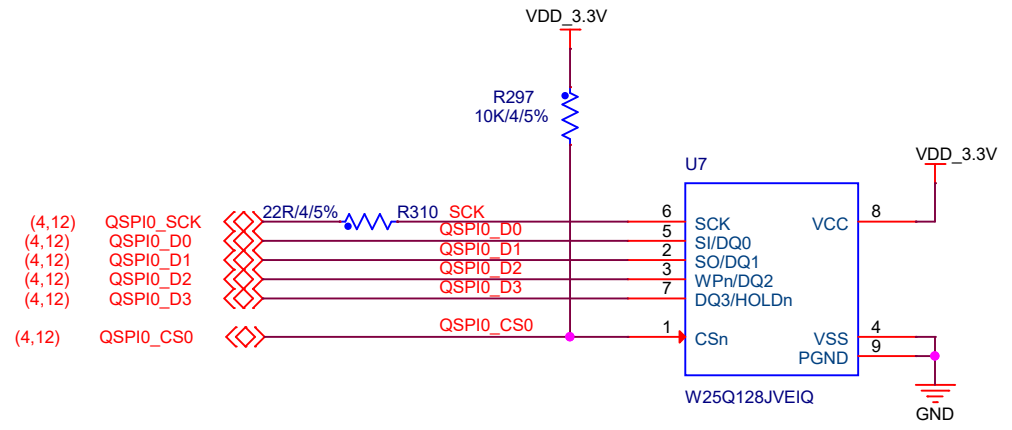
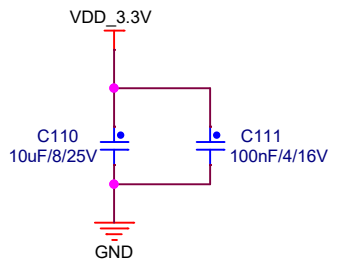




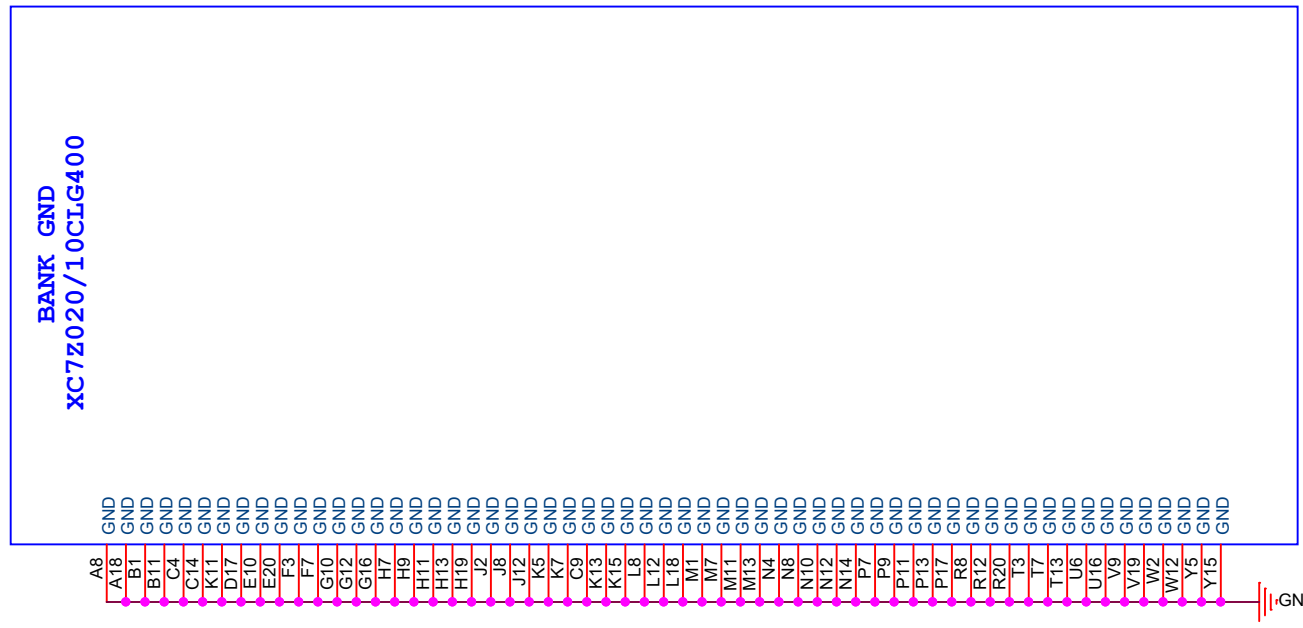


1024MB DDR3 (x32)

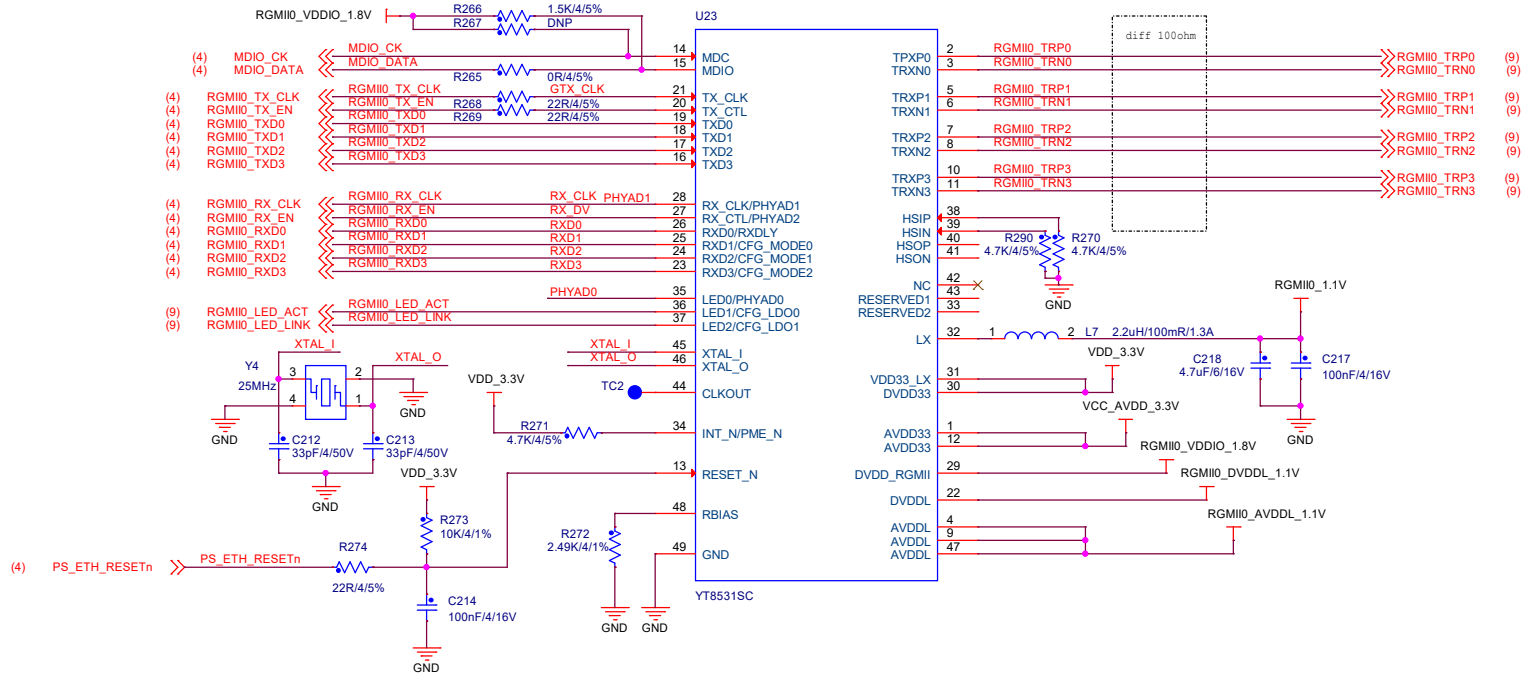




U1G
XC7Z010-1CLG400I*

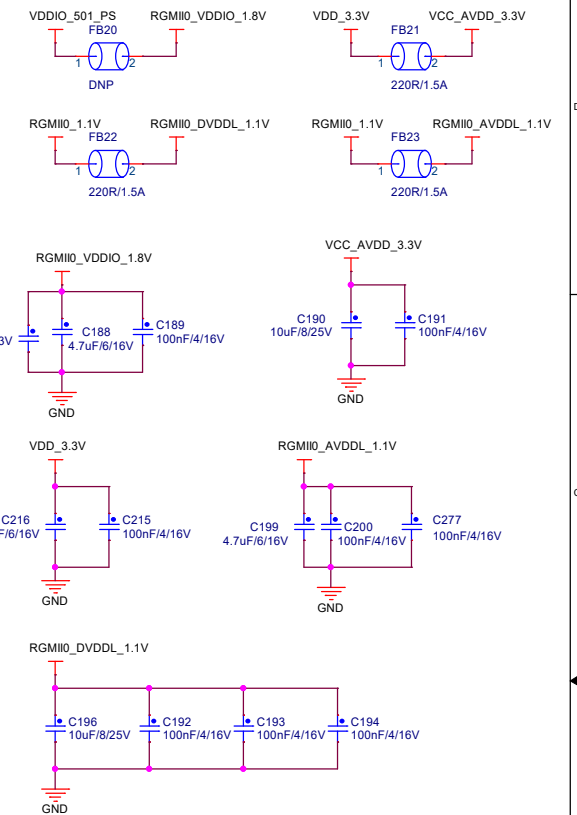
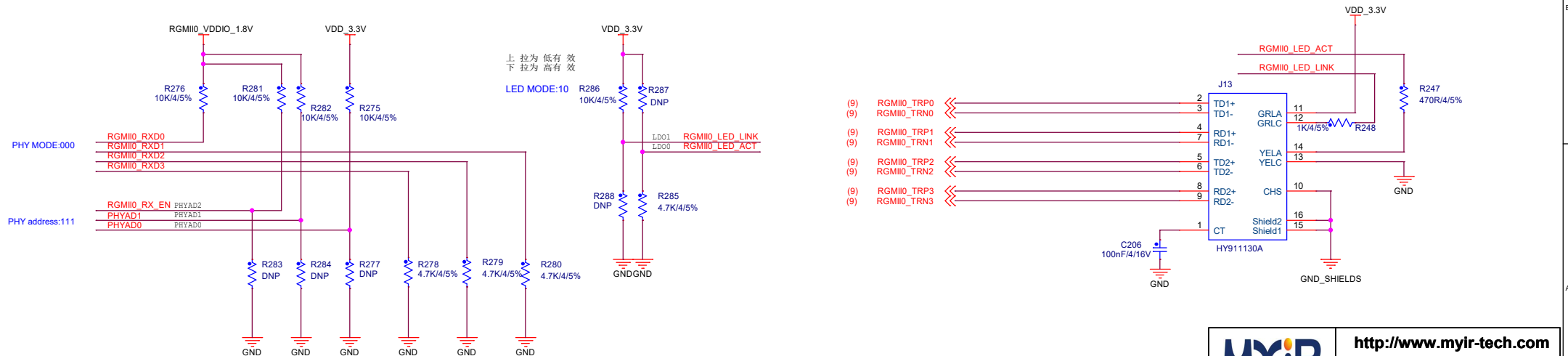


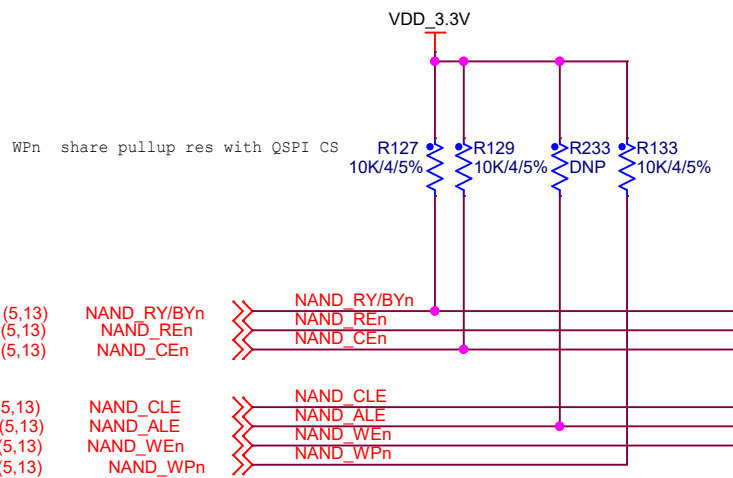
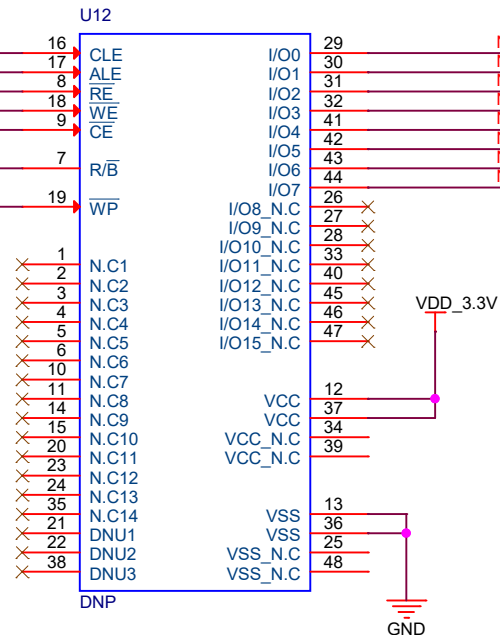
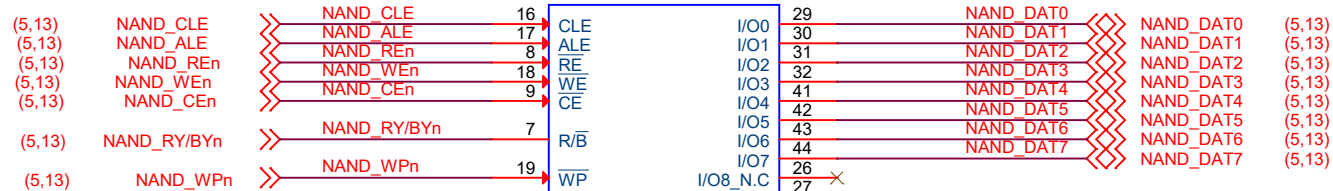
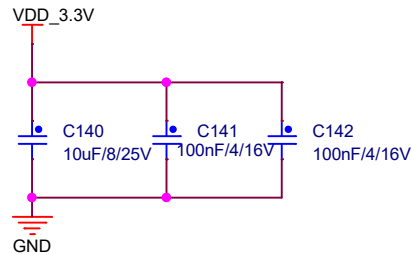
INCREASE MDIO_DATA length 4000mil (shorted by R265)

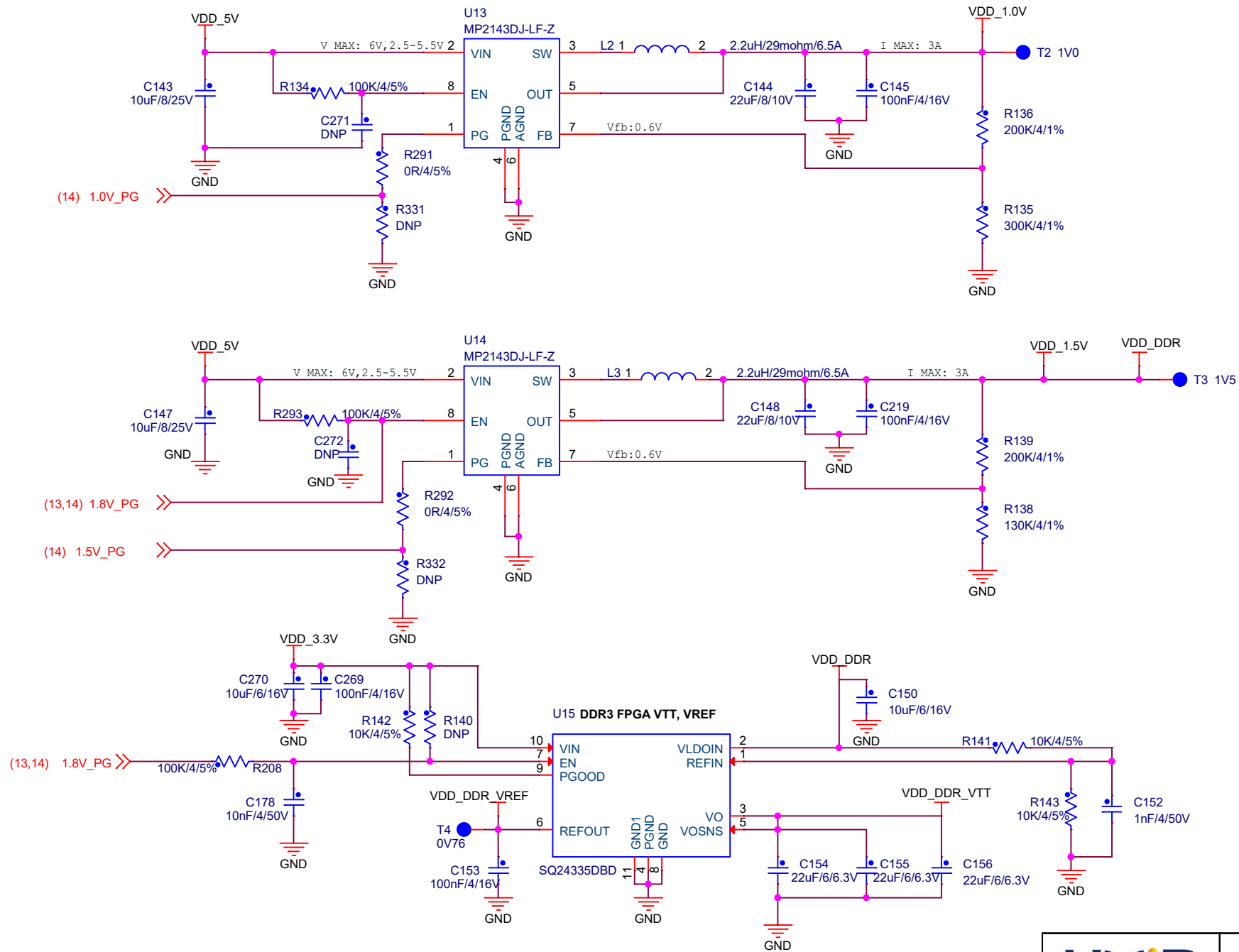


CFG_MODE0	CFG_MODE[2:0]: Operation Mode Configuration. 3'b000: UTP <-> RGMII 3'b001: FIBER <-> RGMII 3'b010: UTP/FIBER <-> RGMII (Media Auto Detection) 3'b011: UTP <-> SGMII 3'b100: SGMII (PHY side) <-> RGMII (MAC side), 3'b101: SGMII (MAC side) <-> RGMII (PHY side) 3'b110: UTP <-> FIBER (Media Conversion auto mode) 3'b111: UTP <-> FIBER (Media Conversion force mode)
CFG_MODE1	
CFG_MODE2	

CFG_LDO[1:0]	Voltage selection for RGMII I/O
2'b00	3.3V
2'b01	2.5V
2'b10 or 2'b11	1.8V







<http://www.myir-tech.com>

Title: MYS-7Z010-20-V2

Size: A4	Document Number: PWR:1.0V&1.5V,VTT	Rev: V1.0
Draw By: MYIR	Date: Thursday, November 10, 2022	Sheet: 13 of 17

