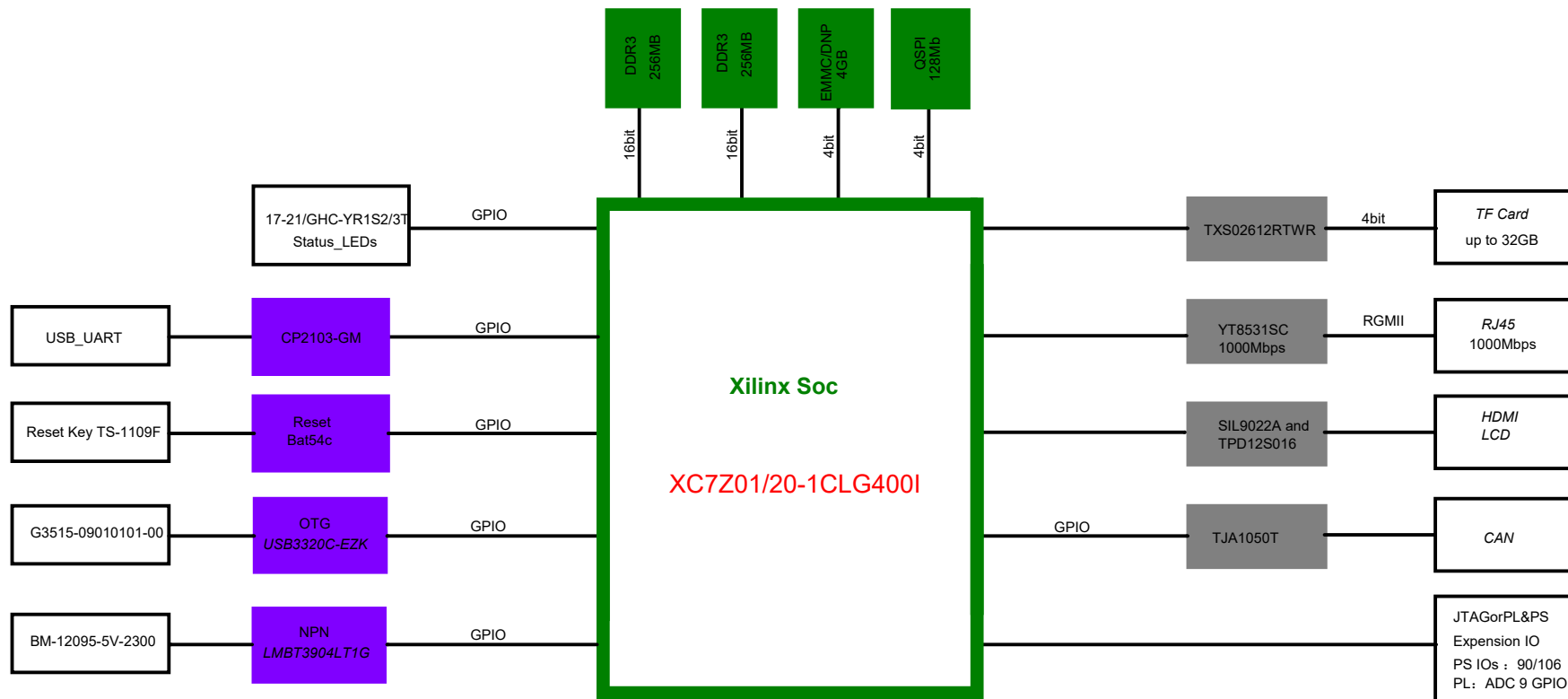
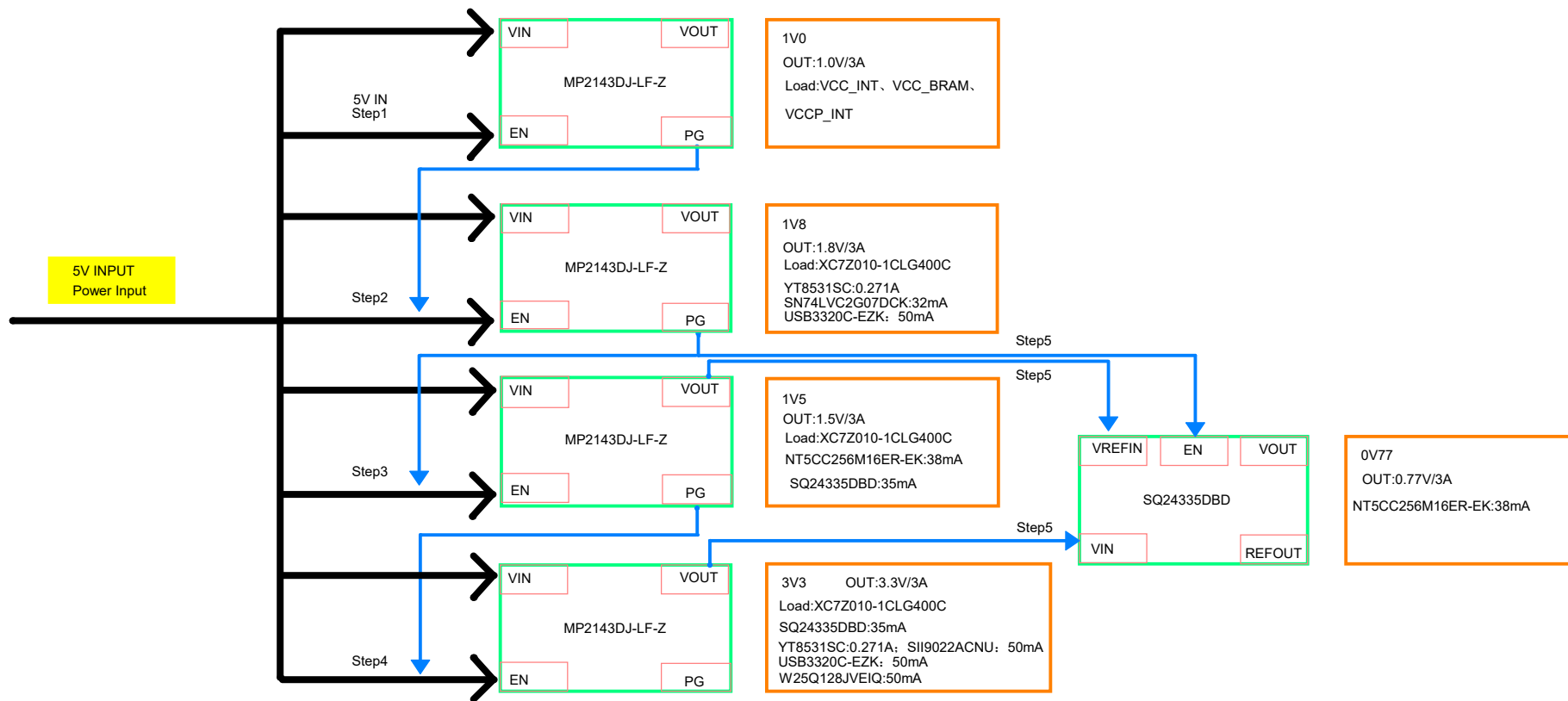


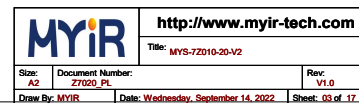
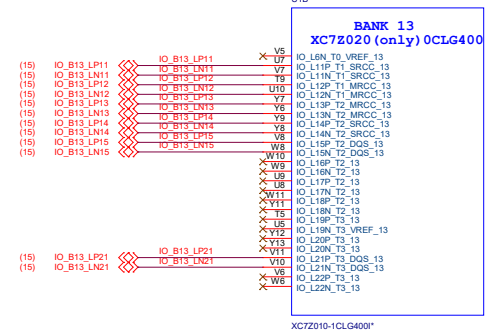
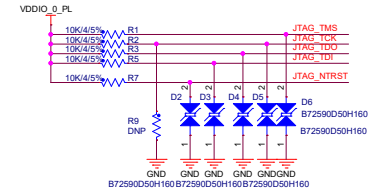
REV	Description	DATE	BY
Ver 1	Initial Release.		

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1	TITLE PAGE
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13	NAND_FLASH
14	PWR:1.0V&1.5V,VTT
15	Power 1.8V,3.3V&DCin
16	EXP CONN
17	MISC







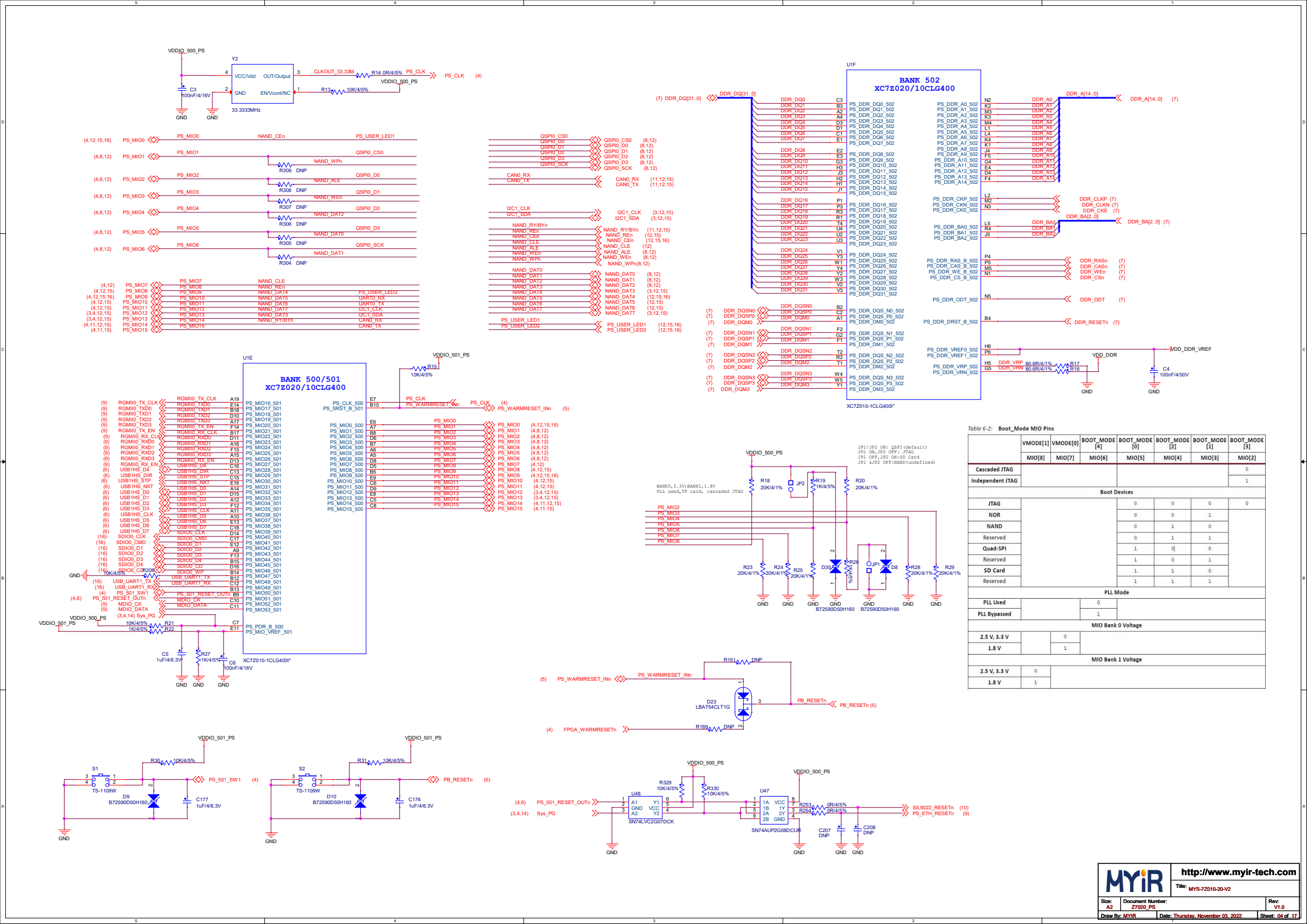
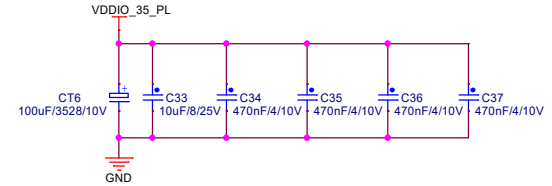
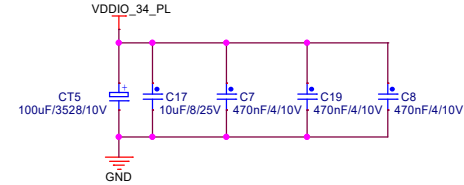
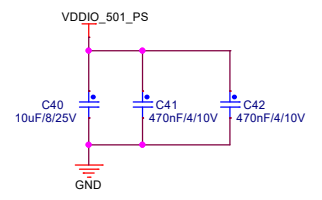
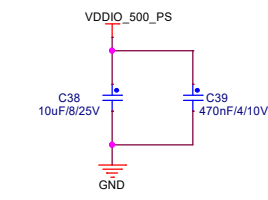
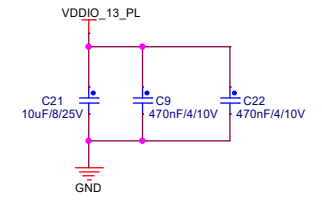
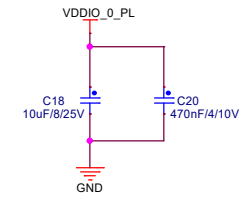
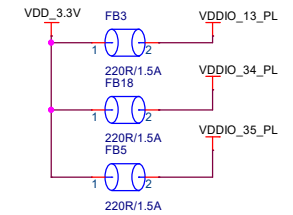
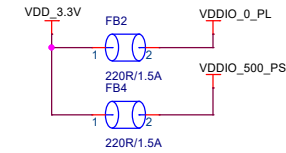
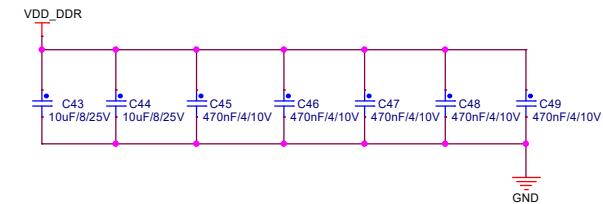
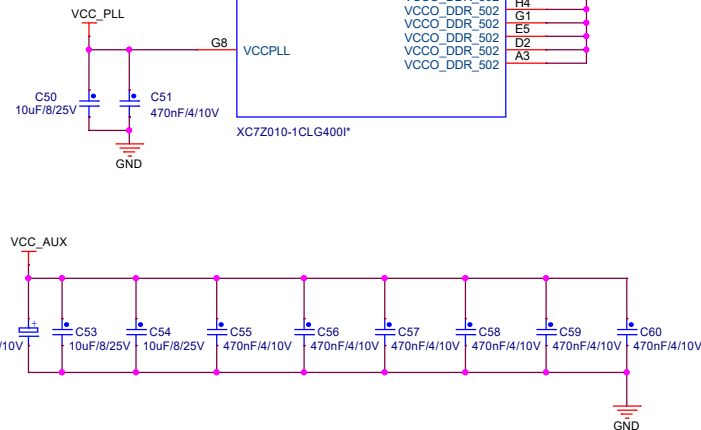
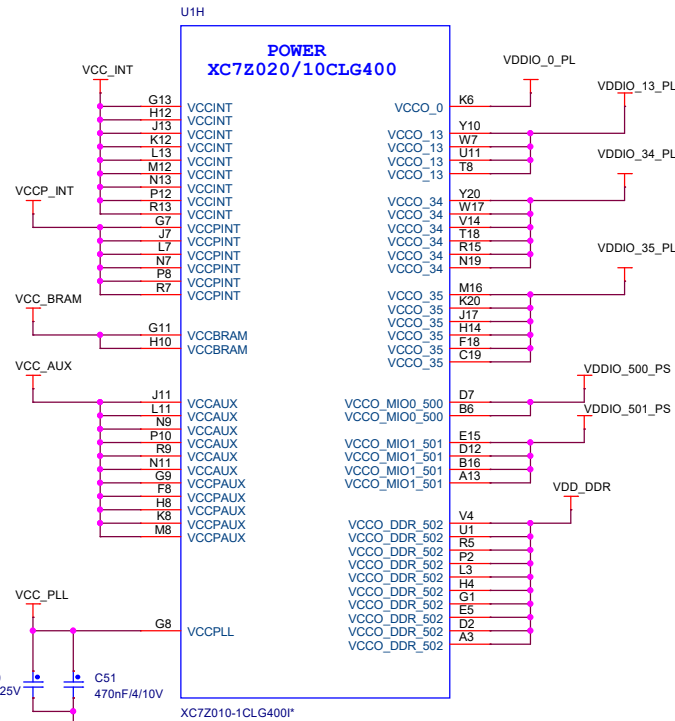
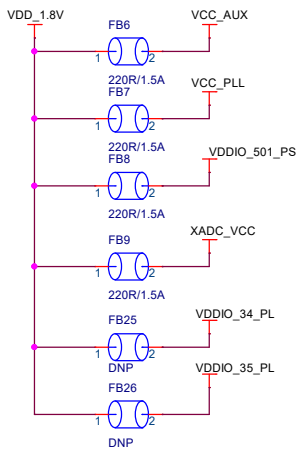
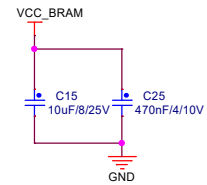
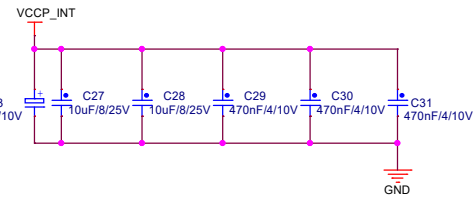
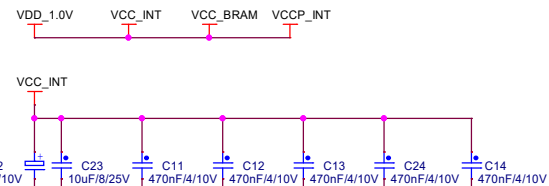


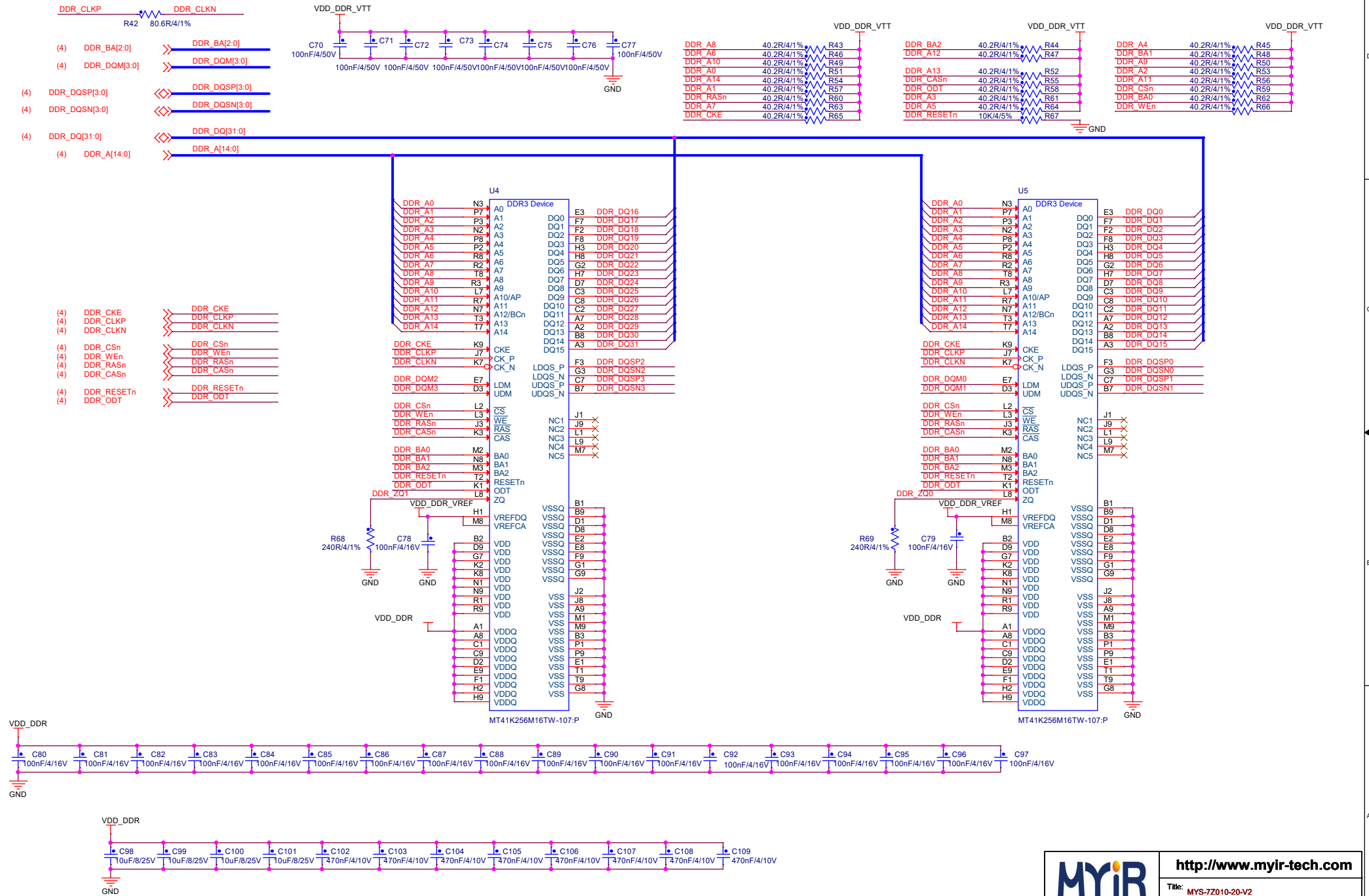
Table 6-2: Boot\_Mode MIO Pins

	VMODE[1]	VMODE[0]	BOOT_MODE [4]	BOOT_MODE [0]	BOOT_MODE [2]	BOOT_MODE [1]	BOOT_MODE [3]
	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]
Cascaded JTAG							0
Independent JTAG							1
Boot Devices							
JTAG				0	0	0	0
NOR				0	0	0	1
NAND				0	1	0	0
Reserved				0	1	1	1
Quad-SPI				1	0	0	0
Reserved				1	0	1	1
SD Card				1	1	0	0
Reserved				1	1	1	1
PLL Mode							
PLL Used				0			
PLL Bypassed				1			
MIO Bank 0 Voltage							
2.5 V, 3.3 V				0			
1.8 V				1			
MIO Bank 1 Voltage							
2.5 V, 3.3 V				0			
1.8 V				1			

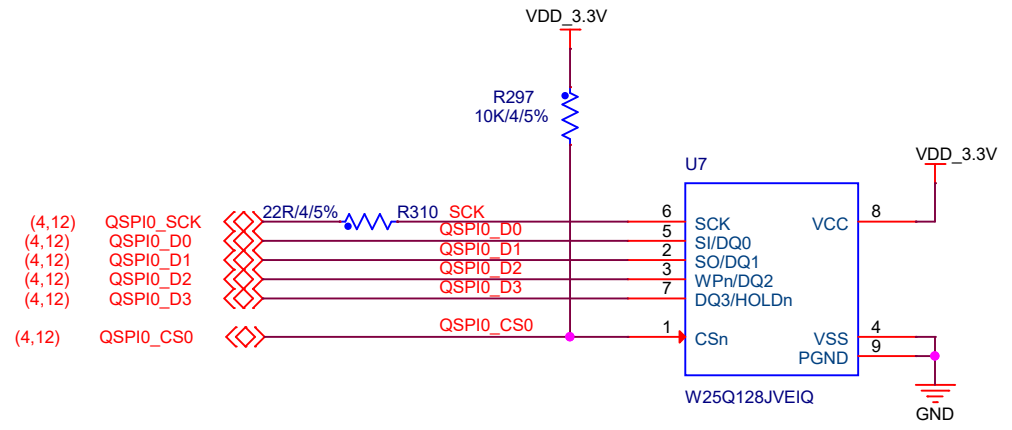
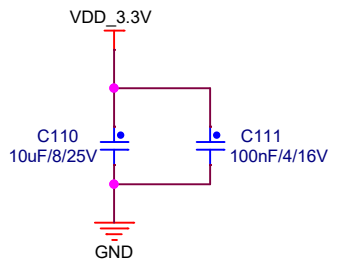




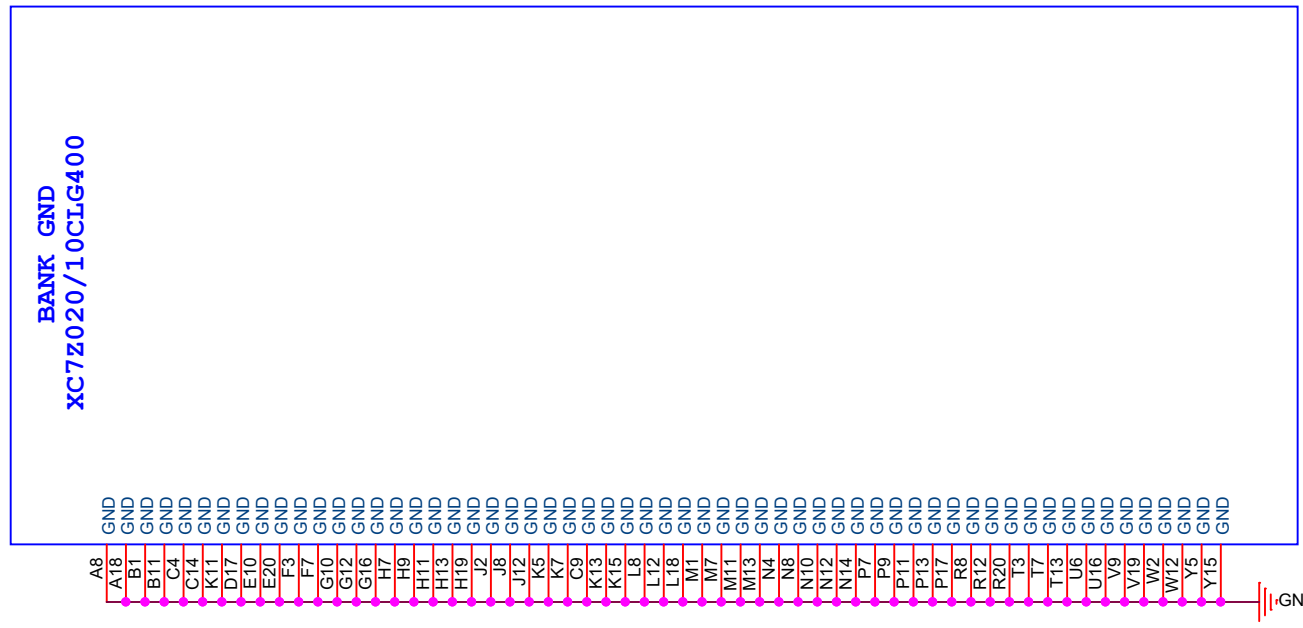
# 1024MB DDR3 (x32)

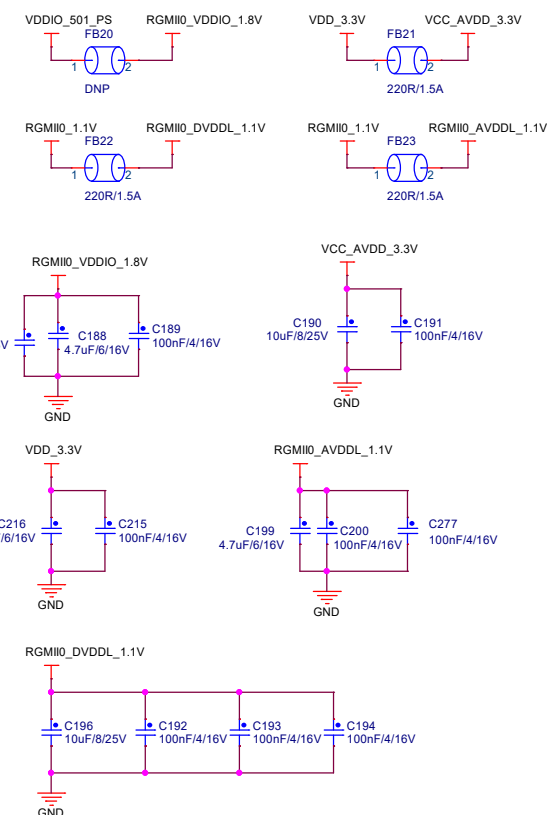






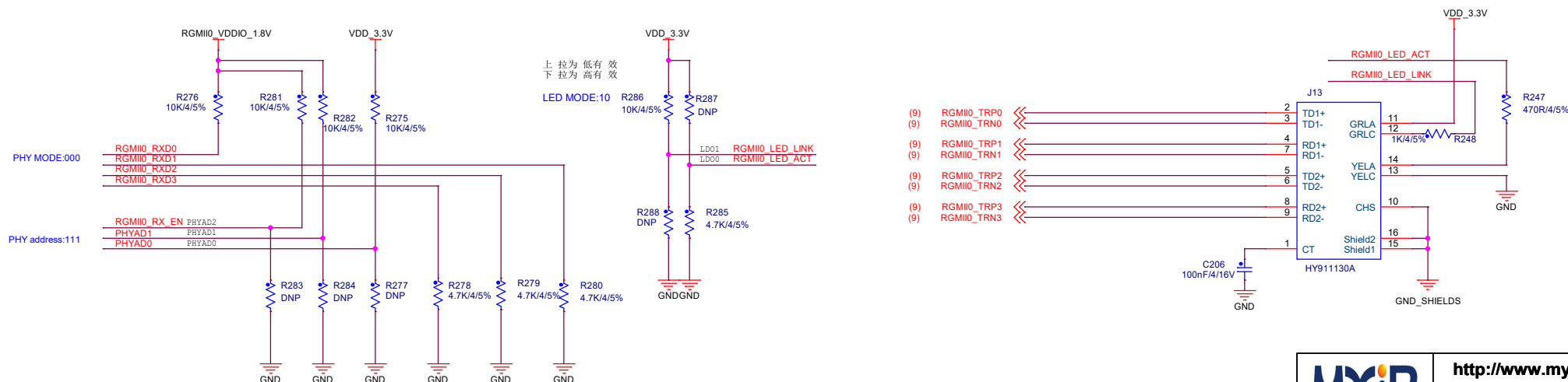
U1G  
XC7Z010-1CLG400I\*



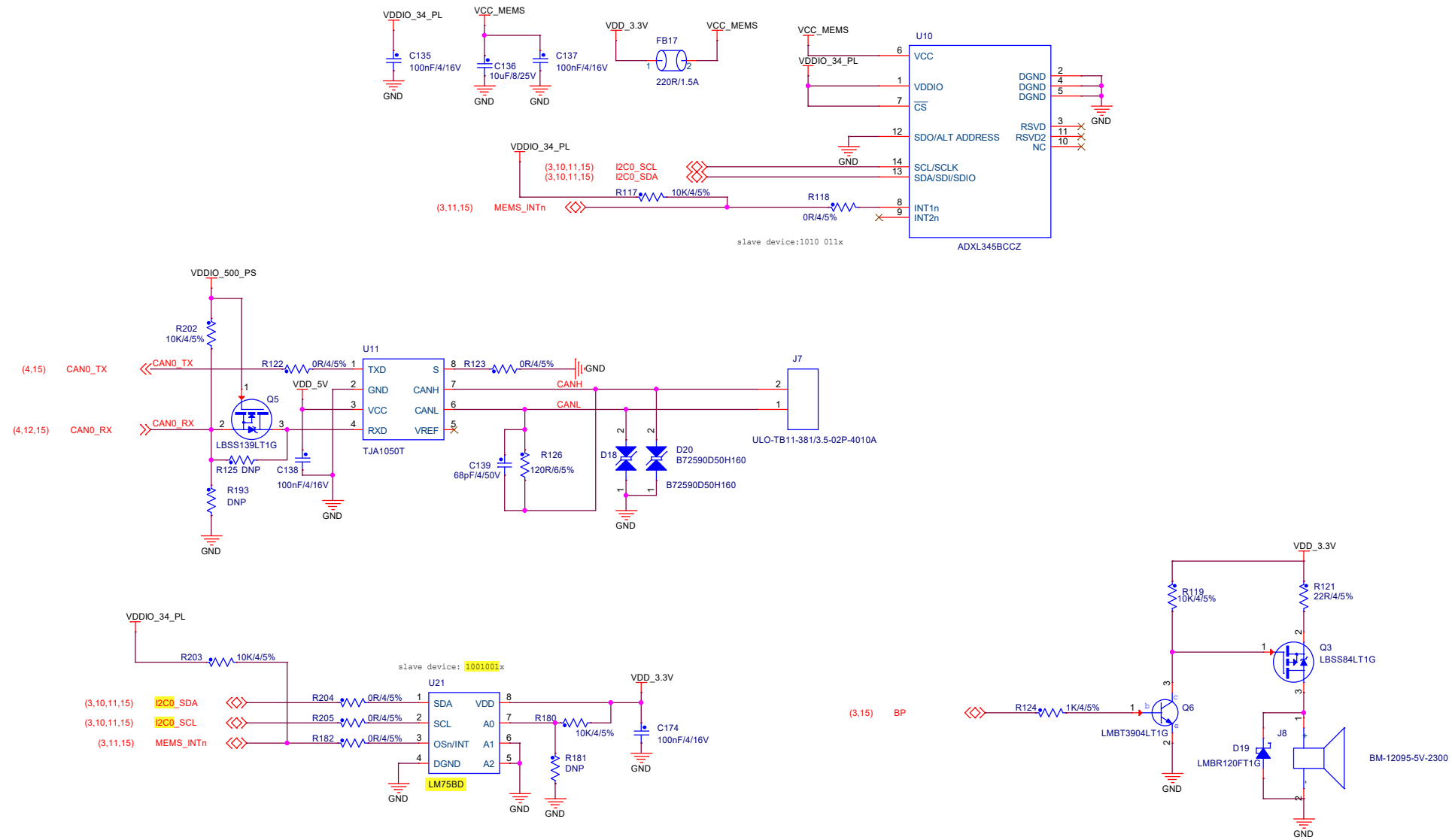


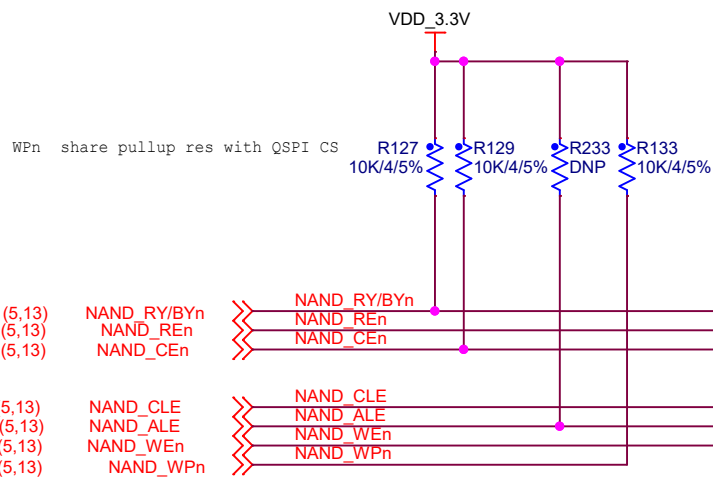
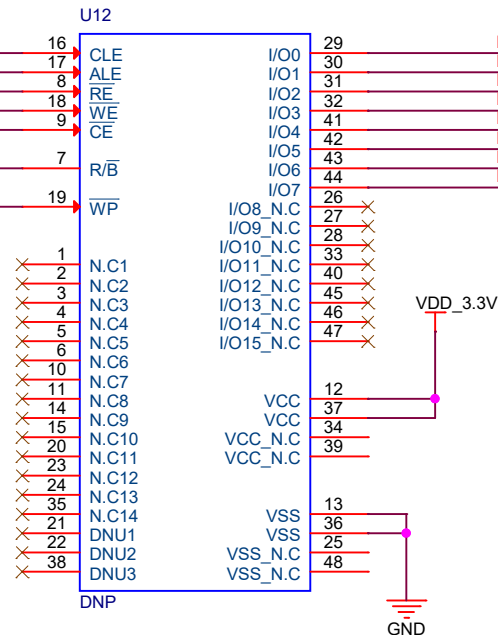
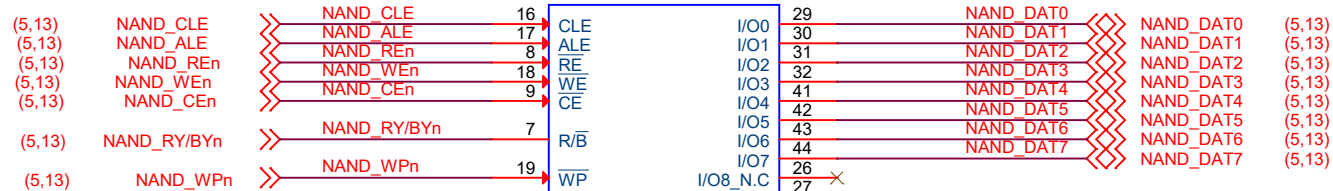
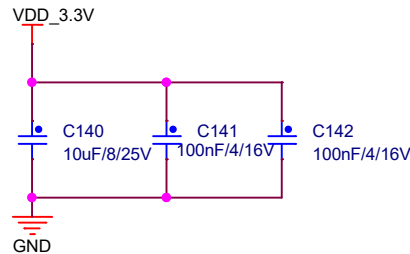
CFG_MODE0	CFG MODE[2:0]: Operation Mode Configuration. 3'b000: UTF <=> RGMII 3'b001: FIBER <=> RGMII 3'b010: UTF/FIBER <=> RGMII (Media Auto Detection)
CFG_MODE1	3'b011: UTF <=> SGMMI 3'b100: SGMMI (PHY side) <=> RGMII (MAC side), 3'b101: RGMII (MAC side) <=> RGMII (PHY side), 3'b110: UTF <=> FIBER (Media Conversion auto mode)
CFG_MODE2	3'b111: UTF <=> FIBER (Media Conversion force mode)

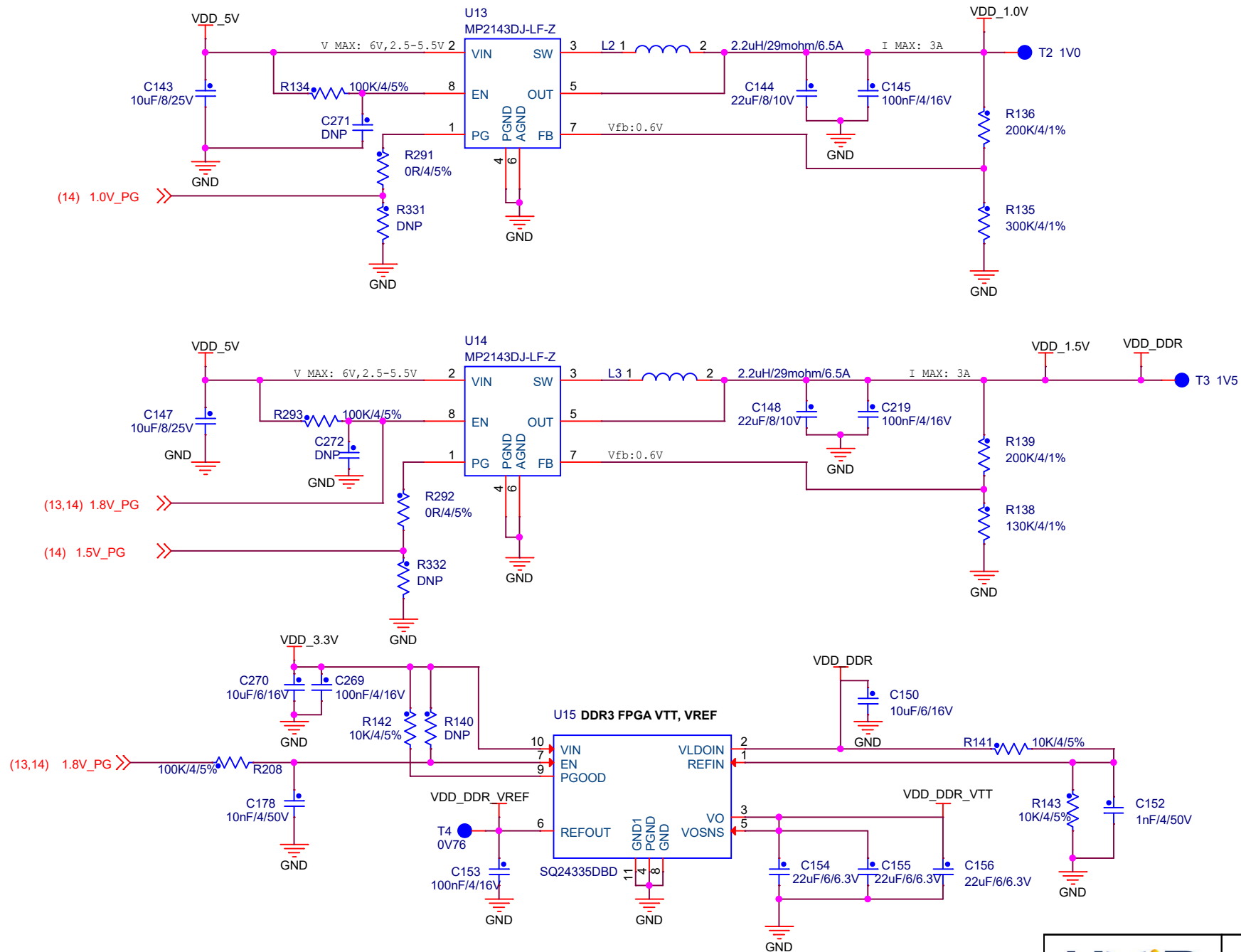
CFG LDO[1:0]	Voltage selection for RGMII I/O
2'b00	3.3V
2'b01	2.5V
2'b10 or 2'b11	1.8V











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