UNIVERSITY OF PATRAS POLYTECHNIC SCHOOL
DEPARTMENT OF COMPUTER ENGINEERING AND INFORMATICS

Checking the Proper Operation of Digital Systems

Laboratory Exercises

Patras, January 2013

LABORATORY EXERCISE 1

1. Perform the synthesis procedure for the combinationalal circuit `c1355.v`, using the implementation library provided to you. Then, using the TetraMax tool, run the Fault Simulation procedure, for all possible stuck-at faults of the circuit, using the test vectors stored in the `c1355_test_set.v` file. Observe the Fault Simulation process step by step, paying attention to the categorization of circuit faults.

2. To what extent the circuit faults were reduced after the fault collapsing process. Save in a list the faults that were not detected by the test vectors of the file you were given.

3. Repeat the above procedure considering this time that stuck-at faults cannot occur in the lines of AOI32D1 cells. What is the reason for the change in test coverage?

4. Repeat the above procedure considering that the possible stuck-at faults are those stored in `c1355_faults.dat file`.

5. For the combinationalal circuit `c7552.v` run the fault simulation procedure, for all possible stuck-at faults of the circuit lines, using the test vectors given in the files `c7552_test_set_10.v`, `c7552_test_set_50.v`, `c7552_test_set_100.v`, `c7552_test_set_1000.v`, `c7552_test_set_5000.v`, `c7552_test_set_10000.v`, `c7552_test_set_100000.v`, `c7552_test_set_1000000.v` and `c7552_test_set_10000000.v`. The above vectors have been obtained in a pseudo-random way, changing the length of the sequence each time. However, in several of the above files the number of stored vectors is much less than what its name indicates file, because the TetraMax tool does not store the vectors that do not detect any faults. After running the Fault Simulation procedure, for the above files, then draw the curve of the fault coverage as a function of the number of vectors. Why is 100% fault coverage not achieved even after the application of the 10,000,000 vectors? How many are there and what are the undetected faults called? Note that the circuit does not contain redundant or other undetectable faults.

LABORATORY EXERCISE 2

1. Using the TetraMax tool, perform the deterministic ATPG procedure for the `s1423.v` sequential circuit, for all possible stuck-at faults of the circuit. Observe the process step by step and especially the results of the DRC process. What rules are violated and why. In addition, observe the results of the ATPG procedure, paying attention to the categorization of circuit faults. What is the reason for the low test coverage rate. Please give reasons for your answer.

2. Perform the ATPG procedure for the combinationalal circuit `c3540.v`, leading the tool to produce test vectors in a deterministic manner for all possible stuck-at faults of the circuit lines. Repeat the process using 10,000, 100,000, and 1,000,000 pseudorandom vectors. Compare the test coverage rates for all cases and comment on the categorization of faults, taking into account each time the length of the pseudo-random sequence. Are there any Random Pattern Resistant faults in the circuit above?

3. For the combinationalal circuit `c7552.v`, perform the deterministic ATPG procedure for each of the following cases:

   - The design requirements are met if the test coverage is at least 97.5%. What do you notice in terms of the resulting test coverage?
   - The total number of test vectors should not exceed 200.
   - The ATPG algorithm's attempts to detect a possible stuck-at error should not exceed 2.

4. For the combinational circuit `c7552.v`, run the Fault Simulation procedure, for all possible stuck-at faults of the circuit lines, using the test vectors stored in the `c7552_test_set.v`. file. After the process is complete, save the list of undetected faults to a file, and then drive the tool to produce test vectors for only these faults. Finally, save the resulting test vectors.

LABORATORY EXERCISE 3

1. For sequential circuit `s5378.v`, lead the Design Compiler tool to create a scan chain, replacing all sequential elements of the circuit with their scan equivalents. Save the new full-scan design after you have verified that it is working correctly during the check phase. In addition, calculate the area and delay overhead of the design that occurred after the chain was inserted. To do this, run a simple mapping of the original design to the implementation technology. What causes the area and delay overhead.

2. For the circuit that emerged after inserting a scan chain, simulate the application of the test vectors, which are stored in the `file s5378.vec`. The first thirty-five (35) columns of the above file correspond to the thirty-five primary inputs of the circuit, while the next one hundred and seventy-nine (179) correspond to the state in which the chain should come (starting from the scan cell closest to the scan input port of the circuit) after applying a test vector. To simulate the operation of the circuit during the control phase, it is necessary to write a Verilog test bench, which will perform the functions of scan chain loading (serial loading of the chain with the new test vector) and parallel capture (normal operation of the circuit for a clock cycle). During simulation, after the end of the application of a vector, update a log file, which will contain the internal state of the chain, as well as a log file, which will contain the responses of the circuit's outputs (except for the scan output port).

LABORATORY EXERCISE 4

1. For the s1423.v `sequential circuit`, lead the Design Compiler tool to create a scan chain, replacing all sequential elements of the circuit with their scan equivalents. Save the new full-scan design after you have verified that it is working correctly during the control phase. Then create the necessary files that determine the operation and timing of the circuit during the control phase, based on the delay of the critical circuit path,.

2. Drive the TetraMax tool to produce test vectors for all possible stuck-at faults of the circuit lines. Pay special attention to the DRC process to make sure that the circuit is fully scan-based (all sequential elements were replaced by their scan equivalents) and works correctly during the scan chain loading and parallel capture phase. Justify the results of the ATPG process, comparing them with the results of the ATPG procedure of Exercise 2 for sequential circuit `s1423.v`.

3. Repeat the synthesis process for the `s1423.v` sequential circuit, replacing all sequential elements of the circuit with their scan equivalents, this time creating two chains of sequential elements. Then run the Fault Simulation procedure for the vectors stored in the `s1423_test_set.v` file. For faults not detected by the Fault Simulation process, generate the required test vectors. What do we achieve by creating more than one chain of sequential elements? Justify your answer by presenting the appropriate results.