2.3.2 Memory map and register boundary addresses

Table 6. Memory map and default device memory area attributes

Region	Boundary address	Arm® Cortex®-M7	Arm® Cortex®-M4	Type	Attributes	Execute never
External devices	0xD0000000 - 0xD3FFFFFF	FMC SDRAM bank 2 (or Reserved in case of FMC remap)		Device	-	Y
	0xCC000000 - 0xCFFFFFFF	FMC SDRAM bank 1 (or remap of FMC NOR/PSRAM/SRAM 4 bank 1)				
	0xC8000000 - 0xCBFFFFFF	FMC SDRAM bank 1 (or remap of FMC NOR/PSRAM/SRAM 3 bank 1)				
	0xC4000000 - 0xC7FFFFFF	FMC SDRAM bank 1 (or remap of FMC NOR/PSRAM/SRAM 2 bank 1)				
	0xC0000000 - 0xC3FFFFFF	FMC SDRAM bank 1 (or remap of FMC NOR/PSRAM/SRAM 1 bank 1)				
	0xA0000000 - 0xBFFFFFFF	Reserved				
External Memories	0x90000000 - 0x9FFFFFFF	QUADSPI		Normal	Write-through	N
	0x80000000 - 0x8FFFFFFF	FMC NAND Flash memory				
	0x70000000 - 0x7FFFFFFF	Reserved (or remap of FMC SDRAM bank 2)			Write-Back Write Allocate	
	0x6C000000 - 0x6FFFFFFF	FMC NOR/PSRAM/SRAM 4 bank 1 (or remap of FMC SDRAM bank 1)				
	0x68000000 - 0x6BFFFFFF	FMC NOR/PSRAM/SRAM 3 bank 1 (or remap of FMC SDRAM bank 1)				
	0x64000000 - 0x67FFFFFF	FMC NOR/PSRAM/SRAM 2 bank 1 (or remap of FMC SDRAM bank 1)				
	0x60000000 - 0x63FFFFFF	FMC NOR/PSRAM/SRAM 1 bank 1 (or remap of FMC SDRAM bank 1)				
Peripherals	0x40000000 - 0x5FFFFFFF	Peripherals (refer to *Table 7: Register boundary addresses*)		Device	-	Y

Table 6. Memory map and default device memory area attributes (continued)

Region	Boundary address	Arm® Cortex®-M7	Arm® Cortex®-M4	Type	Attributes	Execute never
RAM	0x38801000 - 0x3FFFFFFF	Reserved		Normal	Write-Back Write Allocate	N
	0x38800000 - 0x38800FFF	Backup SRAM				
	0x38010000 - 0x387FFFFF	Reserved				
	0x38000000 - 0x3800FFFF	SRAM4				
	0x30048000 - 0x37FFFFFF	Reserved				
	0x30040000 - 0x30047FFF	SRAM3				
	0x30020000 - 0x3003FFFF	SRAM2				
	0x30000000 - 0x3001FFFF	SRAM1				
	0x24080000 - 0x2FFFFFFF	Reserved				
	0x24000000 - 0x2407FFFF	AXI SRAM				
	0x20020000 - 0x23FFFFFF	Reserved				
	0x20000000 - 0x2001FFFF	DTCM	Reserved			

Table 6. Memory map and default device memory area attributes (continued)

Region	Boundary address	Arm® Cortex®-M7	Arm® Cortex®-M4	Type	Attributes	Execute never
Code	0x1FF20000 - 0x1FFFFFFF	Reserved		Normal	Write-through	N
	0x1FF00000 - 0x1FF1FFFF	System Memory	Reserved			
	0x10048000 - 0x1FEFFFFF	Reserved				
	0x10040000 - 0x10047FFF	SRAM3 (Alias)(1)				
	0x10020000 - 0x1003FFFF	SRAM2 (Alias)(1)				
	0x10000000 - 0x1001FFFF	SRAM1 (Alias)(1)				
	0x08200000 - 0x0FFFFFFF	Reserved				
	0x08100000 - 0x081FFFFF	Flash memory bank 2(2)				
	0x08000000 - 0x080FFFFF	Flash memory bank 1(3)				
	0x00010000 - 0x07FFFFFF	Reserved				
	0x00000000 - 0x0000FFFF	ITCM	VTOR REMAP(4)			

1. Alias to maintain Arm® Cortex®-M4 Harvard architecture.
2. Flash memory bank 2 boundary is limited to 0x08100000 - 0x0817FFFF on STM32H745xG/STM32H747xG.
3. Flash memory bank 1 boundary is limited to 0x08000000 - 0x0807FFFF on STM32H745xG/STM32H747xG.
4. Selectable boot memory alias.

All the memory map areas that are not allocated to on-chip memories and peripherals are considered “Reserved”. For the detailed mapping of available memory and register areas, refer to the following table.

The following table gives the boundary addresses of the peripherals available in the devices.

Table 7. Register boundary addresses(1)

Boundary address	Peripheral	Bus	Register map
0x58027000 - 0x580273FF	RAMECC3	AHB4 (D3)	*Section 3.4: RAMECC registers*
0x58026400 - 0x580267FF	HSEM		*Section 11.4: HSEM registers*
0x58026000 - 0x580263FF	ADC3		*Section 26.7: ADC common registers*
0x58025800 - 0x58025BFF	DMAMUX2		*Section 18.6: DMAMUX registers*
0x58025400 - 0x580257FF	BDMA		*Section 17.6: BDMA registers*
0x58024C00 - 0x58024FFF	CRC		*Section 22.4: CRC registers*
0x58024800 - 0x58024BFF	PWR		*Section 7.8: PWR registers*
0x58024400 - 0x580247FF	RCC		*Section 9.7: RCC registers*
0x58022800 - 0x58022BFF	GPIOK		*Section 12.4: GPIO registers*
0x58022400 - 0x580227FF	GPIOJ		*Section 12.4: GPIO registers*
0x58022000 - 0x580223FF	GPIOI		*Section 12.4: GPIO registers*
0x58021C00 - 0x58021FFF	GPIOH		*Section 12.4: GPIO registers*
0x58021800 - 0x58021BFF	GPIOG		*Section 12.4: GPIO registers*
0x58021400 - 0x580217FF	GPIOF		*Section 12.4: GPIO registers*
0x58021000 - 0x580213FF	GPIOE		*Section 12.4: GPIO registers*
0x58020C00 - 0x58020FFF	GPIOD		*Section 12.4: GPIO registers*
0x58020800 - 0x58020BFF	GPIOC		*Section 12.4: GPIO registers*
0x58020400 - 0x580207FF	GPIOB		*Section 12.4: GPIO registers*
0x58020000 - 0x580203FF	GPIOA		*Section 12.4: GPIO registers*

Table 7. Register boundary addresses[1] (continued)

Boundary address	Peripheral	Bus	Register map
0x58005800 - 0x580067FF	Reserved	APB4 (D3)	Reserved
0x58005400 - 0x580057FF	SAI4		*Section 54.6: SAI registers*
0x58004C00 - 0x58004FFF	IWDG2		*Section 48.4: IWDG registers*
0x58004800 - 0x58004BFF	IWDG1		*Section 48.4: IWDG registers*
0x58004000 - 0x580043FF	RTC & BKP registers		*Section 49.6: RTC registers*
0x58003C00 - 0x58003FFF	VREF		*Section 28.3: VREFBUF registers*
0x58003800 - 0x58003BFF	COMP1 - COMP2		*Section 29.7: COMP registers*
0x58003000 - 0x580033FF	LPTIM5		*Section 45.7: LPTIM registers*
0x58002C00 - 0x58002FFF	LPTIM4		*Section 45.7: LPTIM registers*
0x58002800 - 0x58002BFF	LPTIM3		*Section 45.7: LPTIM registers*
0x58002400 - 0x580027FF	LPTIM2		*Section 45.7: LPTIM registers*
0x58001C00 - 0x58001FFF	I2C4		*Section 50.7: I2C registers*
0x58001400 - 0x580017FF	SPI6		*Section 53.11: SPI/I2S registers*
0x58000C00 - 0x58000FFF	LPUART1		*Section 52.7: LPUART registers*
0x58000400 - 0x580007FF	SYSCFG		*Section 13.3: SYSCFG registers*
0x58000000 - 0x580003FF	EXTI		*Section 21.6: EXTI registers*
0x52009000 - 0x520093FF	RAMECC1	AHB3 (D1)	*Section 3.4: RAMECC registers*
0x52008000 - 0x52008FFF	Delay Block SDMMC1		*Section 25.4: DLYB registers*
0x52007000 - 0x52007FFF	SDMMC1		*Section 58.10: SDMMC registers*
0x52006000 - 0x52006FFF	Delay Block QUADSPI		*Section 25.4: DLYB registers*
0x52005000 - 0x52005FFF	QUADSPI control registers		*Section 24.5: QUADSPI registers*
0x52004000 - 0x52004FFF	FMC control registers		*Section 23.7.6: NOR/PSRAM controller registers*, *Section 23.8.7: NAND flash controller registers*, *Section 23.9.5: SDRAM controller registers*
0x52003000 - 0x52003FFF	JPEG		*Section 35.5: JPEG codec registers*
0x52002000 - 0x52002FFF	Flash interface registers		*Section 4.9: FLASH registers*
0x52001000 - 0x52001FFF	Chrom-Art (DMA2D)		*Section 19.5: DMA2D registers*
0x52000000 - 0x52000FFF	MDMA		*Section 15.5: MDMA registers*
0x51000000 - 0x510FFFFF	GPV		*Section 2.2.4: AXI interconnect registers*
0x50003000 - 0x50003FFF	WWDG1	APB3 (D1)	*Section 47.5: WWDG registers*
0x50001000 - 0x50001FFF	LTDC		*Section 33.7: LTDC registers*
0x50000000 - 0x50000FFF	DSIHOST		*Section 34.15: DSI Host registers*, *Section 34.16: DSI Wrapper registers*

Table 7. Register boundary addresses[1] (continued)

Boundary address	Peripheral	Bus	Register map
0x48023000 - 0x480233FF	RAMECC2	AHB2 (D2)	*Section 3.4: RAMECC registers*
0x48022800 - 0x48022BFF	Delay Block SDMMC2		*Section 25.4: DLYB registers*
0x48022400 - 0x480227FF	SDMMC2	AHB2 (D2)	*Section 58.10: SDMMC registers*
0x48021800 - 0x48021BFF	RNG		*Section 36.7: RNG registers*
0x48021400 - 0x480217FF	HASH		*Section 38.7: HASH registers*
0x48021000 - 0x480213FF	CRYPTO		*Section 37.7: CRYP registers*
0x48020000 - 0x480203FF	DCMI		*Section 32.5: DCMI registers*
0x40080000 - 0x400BFFFF	USB2 OTG_FS	AHB1 (D2)	*Section 60.14: OTG_HS registers*
0x40040000 - 0x4007FFFF	USB1 OTG_HS		*Section 60.14: OTG_HS registers*
0x40028000 - 0x400293FF	ETHERNET MAC		*Section 61.11: Ethernet registers*
0x40024400 - 0x400247FF	ART control registers		-
0x40022000 - 0x400223FF	ADC1 - ADC2		*Section 26.7: ADC common registers*
0x40020800 - 0x40020BFF	DMAMUX1		*Section 18.6: DMAMUX registers*
0x40020400 - 0x400207FF	DMA2		*Section 16.5: DMA registers*
0x40020000 - 0x400203FF	DMA1		*Section 16.5: DMA registers*
0x40017400 - 0x400177FF	HRTIM	APB2 (D2)	*Section 39.5: HRTIM registers*
0x40017000 - 0x400173FF	DFSDM1		*Section 31.7: DFSDM channel y registers (y=0..7)*, *Section 31.8: DFSDM filter x module registers (x=0..3)*
0x40016000 - 0x400163FF	SAI3		*Section 54.6: SAI registers*
0x40015C00 - 0x40015FFF	SAI2		*Section 54.6: SAI registers*
0x40015800 - 0x40015BFF	SAI1		*Section 54.6: SAI registers*
0x40015000 - 0x400153FF	SPI5		*Section 53.11: SPI/I2S registers*
0x40014800 - 0x40014BFF	TIM17		*Section 43.6: TIM16/TIM17 registers*
0x40014400 - 0x400147FF	TIM16		*Section 43.6: TIM16/TIM17 registers*
0x40014000 - 0x400143FF	TIM15		*Section 43.5: TIM15 registers*
0x40013400 - 0x400137FF	SPI4		*Section 53.11: SPI/I2S registers*
0x40013000 - 0x400133FF	SPI1 / I2S1		*Section 53.11: SPI/I2S registers*
0x40011400 - 0x400117FF	USART6		*Section 51.8: USART registers*
0x40011000 - 0x400113FF	USART1		*Section 51.8: USART registers*
0x40010400 - 0x400107FF	TIM8		*Section 40.4: TIM1/TIM8 registers*
0x40010000 - 0x400103FF	TIM1		*Section 40.4: TIM1/TIM8 registers*

Table 7. Register boundary addresses[1] (continued)

Boundary address	Peripheral	Bus	Register map
0x4000AC00 - 0x4000D3FF	CAN Message RAM	APB1 (D2)	*Section 59.5: FDCAN registers*
0x4000A800 - 0x4000ABFF	CAN CCU		*Section 59.5: FDCAN registers*
0x4000A400 - 0x4000A7FF	FDCAN2		*Section 59.5: FDCAN registers*
0x4000A000 - 0x4000A3FF	FDCAN1		*Section 59.5: FDCAN registers*
0x40009400 - 0x400097FF	MDIOS		*Section 57.4: MDIOS registers*
0x40009000 - 0x400093FF	OPAMP		*Section 30.6: OPAMP registers*
0x40008800 - 0x40008BFF	SWPMI		*Section 56.6: SWPMI registers*
0x40008400 - 0x400087FF	CRS		*Section 10.8: CRS registers*
0x40007C00 - 0x40007FFF	UART8		*Section 51.8: USART registers*
0x40007800 - 0x40007BFF	UART7		*Section 51.8: USART registers*
0x40007400 - 0x400077FF	DAC1		*Section 27.7: DAC registers*
0x40006C00 - 0x40006FFF	HDMI-CEC		*Section 62.7: HDMI-CEC registers*
0x40005C00 - 0x40005FFF	I2C3		*Section 50.7: I2C registers*
0x40005800 - 0x40005BFF	I2C2		*Section 50.7: I2C registers*
0x40005400 - 0x400057FF	I2C1		*Section 50.7: I2C registers*
0x40005000 - 0x400053FF	UART5		*Section 51.8: USART registers*
0x40004C00 - 0x40004FFF	UART4		*Section 51.8: USART registers*
0x40004800 - 0x40004BFF	USART3		*Section 51.8: USART registers*
0x40004400 - 0x400047FF	USART2		*Section 51.8: USART registers*
0x40004000 - 0x400043FF	SPDIFRX		*Section 55.5: SPDIFRX interface registers*
0x40003C00 - 0x40003FFF	SPI3 / I2S3		*Section 53.11: SPI/I2S registers*
0x40003800 - 0x40003BFF	SPI2 / I2S2		*Section 53.11: SPI/I2S registers*
0x40002C00 - 0x40002FFF	WWDG2		*Section 47.5: WWDG registers*
0x40002400 - 0x400027FF	LPTIM1		*Section 45.7: LPTIM registers*
0x40002000 - 0x400023FF	TIM14		*Section 41.4: TIM2/TIM3/TIM4/TIM5 registers*
0x40001C00 - 0x40001FFF	TIM13		*Section 41.4: TIM2/TIM3/TIM4/TIM5 registers*
0x40001800 - 0x40001BFF	TIM12		*Section 41.4: TIM2/TIM3/TIM4/TIM5 registers*
0x40001400 - 0x400017FF	TIM7		*Section 44.4: TIM6/TIM7 registers*
0x40001000 - 0x400013FF	TIM6		*Section 44.4: TIM6/TIM7 registers*
0x40000C00 - 0x40000FFF	TIM5		*Section 41.4: TIM2/TIM3/TIM4/TIM5 registers*
0x40000800 - 0x40000BFF	TIM4		*Section 41.4: TIM2/TIM3/TIM4/TIM5 registers*
0x40000400 - 0x400007FF	TIM3		*Section 41.4: TIM2/TIM3/TIM4/TIM5 registers*
0x40000000 - 0x400003FF	TIM2		*Section 41.4: TIM2/TIM3/TIM4/TIM5 registers*

1. Accessing a reserved area results in a bus error. Accessing undefined memory space in a peripheral returns zeros.