STM32H755xI Functional overview

MSv39740V7 SRAM2 128 Kbyte SRAM3 32 Kbyte AHB1 AHB2 APB1 APB2 Ξ D2-to-D3 AHB **CPU** Cortex-M4 snq-Q snq-S USBHS2 USBHS1 32-bit AHB bus matrix **D2 domain** SDMMC2 APB4 Ethernet MAC Figure 5. STM32H755xI bus matrix DMA2 SRAM4 64 Kbyte Backup SRAM 4 Kbyte DMA2_PERIPH AHB4 DMA2_MEM DMA1 DMA1_PERIPH Mam_IAMQ 32-bit AHB bus matrix D3 domain BDMA D1-to-D2 AHB D1-to-D3 AHB Flash B Up to 1 Mbyte Flash A Up to 1 Mbyte AXI SRAM 512 Kbyte QUADSPI FMC AHB3 APB3 0x50000000 - 0x57FFFFFF and 0x60000000 - 0xDFFFFFFF Note 1: The address ranges are: 0x38000000 - 0x3FFFFFF and 0x58000000 - 0x5FFFFFF AXI

Master interface

APB Slave interface LTDC Slave interface 0x24000000 - 0x2407FFFF, Note 2: The address ranges are: 0x08000000 - 0x081FFFFF, DMA2D 64-bit AXI bus matrix D1 domain MDMA TCM AHB SDMMC1 **CPU** Cortex-M7 ЯВНА I\$ D\$ 16KB Bus multiplexer AHBS - 32-bit bus 64-bit bus D2-to-D1 AHB ART Legend 0