Description STM32H755xI

MII / RMII MDIO as AF To APB1-2 peripherals (200MHz) AHB1 ETHER DMA² SDMMC: OTG FS OTG H MAC Corte M4 DMA FIFO DMA/ FIFO FIFO DMA AXI/AHB12 (200MHz) JTDO/SWD, JTDO Î Î Î 1 MB $\overline{\mathbb{Q}}$ 00 $\widehat{\mathbb{I}}$ JTRST, JTDI JTCK/SWCLE FLASH 1 MB 32-bit AHB BUS-MATRIX TRACECK TRACED[3:0] FLASH DMA 512 KB AXI Mux1 128 KB 128 KB 32 KB RNG FMC ADC1 Up to 20 analog inputs common to ADC1 & 2 HASH FMC_signals 3DES/AES CHROM-ART (DMA2D) Quad-SPI LCD_R[7:0], LCD_G[7:0], LCD_B[7:0], LCD_HSYNC, LCD_VSYNC, LCD_DE, LCD_CLK CLK, CS,D[7:0] 4 channels, ETR as AF ŧΑΧ LCD-TFT FIFO T. 16b ТІМЗ 4 channels, ETR as AF \square TIM7 WWDG1 JPEG 16b < TIM4 4 channels, ETR as AF 4 channels, SDMMC_D[7:0],SDMMC_D[7:3,1]Dif SDMMC_D0dir, SDMMC_D2dir CMD, CMDdir, CK, Ckin, CKlo as AF_ SWPMI FIFO SDMMC1 ⇒ 16b TIM12 2 channels as AF 2 channels as A 1 channel as AF (instruction cache ⇒ 16b TIM13 1 channel as AF TIM14 RX, TX, SCK, CTS, RTS as AF

RX, TX, SCK, CTS, RTS as AF

RX, TX, SCK

CTS, RTS as AF AHB2 (200MHz) USART2 HSYNC, VSYNC, PUIXCLK, D[13:0] USART3 HRTIM1_CH[A..E]X
HRTIM1_FLT[5:1].
HRTIM1_FLT[5:1]. in, SYSFL]
DFSDM1_CKOUT.
DFSDM1_DATAIN[0:7],
DFSDM1_CKIN[0:7]. UART4 RX. TX as AF HRTIM1 RX, TX as AF UART5 DFSDM1 \Box UART7 RX, TX as AF \Box SAI3 SD, SCK, FS, MCLK as AF RX, TX as AF RX, TX as Ar

MOSI, MISO, SCK, NSS/SDO,
SDI, CK, WS, MCK, as AF

MOSI, MISO, SCK, NSS/SDO,
SDI, CK, WS, MCK, as AF

SCL, SDA, SMBAL as AF SD, SCK, FS, MCLK as AF SPI2/I2S2 SD, SCK, FS, MCLK, D[3:1], CK[2:1] as AF SPI3/I2S3 SAI1 I2C1/SMBUS SCL, SDA, SMBAL as AF MOSI, MISO, SCK, NSS as AF SPI5 10 KB SRAM 1 compl. chan (TIM17_CH1N), 1 chan. (TIM17_CH1, BKIN as AF TIM17 Mux2 I2C2/SMBUS Л. 1 compl. chan (TIM16_CH1N), 1 chan. (TIM16_CH1, BKIN as AF DAP TIM16 I2C3/SMBUS SCL, SDA, SMBAL as AF 2 compl. chan (TIM15_CH1[1:2]N), 2 chan. (TIM_CH15[1:2], BKIN as AF MDIOS MDC. MDIO. \Box 7 MOSI, MISO, SCK, NSS as AF 32-bit AHB BUS-MATRIX RAM FDCAN1 IWDG1 MOSI, MISO, SCK, NSS / SDO, SDI, CK, WS, MCK, as AF SPI/I2S1 FDCAN2 TX RX IJ IWDG2 0 64 KB SRAM RX, TX, SCK, CTS, RTS as AF 🔇 USART6 SPDIFRX1 IN[1:4] as AF RX, TX, SCK, CTS, RTS as AF USART1 אדג 4 compl. chan. (TIM1_CH1[1:4]N), 4 chan. (TIM1_CH1[1:4]ETR, BKIN as AF 4 compl. chan.(TIM8_CH1[1:4]N), 4 chan. (TIM8_CH1[1:4], ETR, BKIN as AE_ CEC as AF HDMI-CEC \square DAC1_OUT, DAC2_OUT as AF DAC1&2 **HSEM** \square TIM8/PWM LPTIM1_IN1, LPTIM1_IN2, LPTIM1_OUT as AF CRC OPAMP1&2 Up to 17 analog inputs common to ADC1 and 2 COPAMPX VINM WWDG2 OPAMPx_VINP OPAMPx_VOUT as AF ADC3 VDD = 1.62 to 3.6V VDD33USB = 3.0 to 3.6V VSS Tem, sensor RCC Reset & GPIO PORTA.. J Voltage regulator 3.3 to 1.2V PA..J[15:0] < control VDDMMC33 = 1.8 to 3.6V VDDSMPS, VSSSMPS VLXSMP, VFBSMPS, SMPS step-dov GPIO PORTK SD, SCK, FS, MCLK, PDM_DI/CK[4:1] as AE COMPX_INP, COMPX_INM, COMPX_OUT as AE XTAL 32 kHz OSC32_IN OSC32_OUT RTC_TS
RTC_TAMP[1:3]
RTC_OUT
RTC_REFIN COMP1&2 S RTC Backup registers LPTIM5_OUT as AF LPTIM5 VRFF 4 MHz CSI S LPTIM4 LPTIM4_OUT as AF SYSCFG 48 MHz HS**I**48 R0 LPTIM3 LPTIM3_OUT as AF EXTI WKUP HSI ◀ 64 MHz HSI RC 12C4 XTAL OSC 4-48 MHz SC_OSC_OUT MISO, MOSI, SCK, NSS as AF SPI6 LPUART1 LPTIM2 UPPLY SUPERVISION VDDA, VSSA NRESET WKUP[6:1] POR/PDR/BOR MSv43742V16

Figure 1. STM32H755xl block diagram

