East west University

Course Name : VLSI circuit ~~design~~ and system

Course code : EEE 416

Experiment-3: Two input NOR gate Schematic, Symbol and layout generation.

Submitted to:

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Introduction: In this lab we will design a 2 input NOR gate and design its symbol and layout in this experiment we will use the study of our previous lab (NAND gate design) to implemet this lab.

Methodology: we will use cadence virtuoso software for this experiment. The technology node is 45nm. we will draw the schematic, Symbol and generate the layout tool. Firstly, we will check the output wave form and compare it with the truth table of logic NOR gate. Then, we will start our design layout. To check the layout we will run LVS and DRC. If, no error shown we can say that our layout design is completed.

Circuit diagram of NOR gate in Cadence Virtuoso:

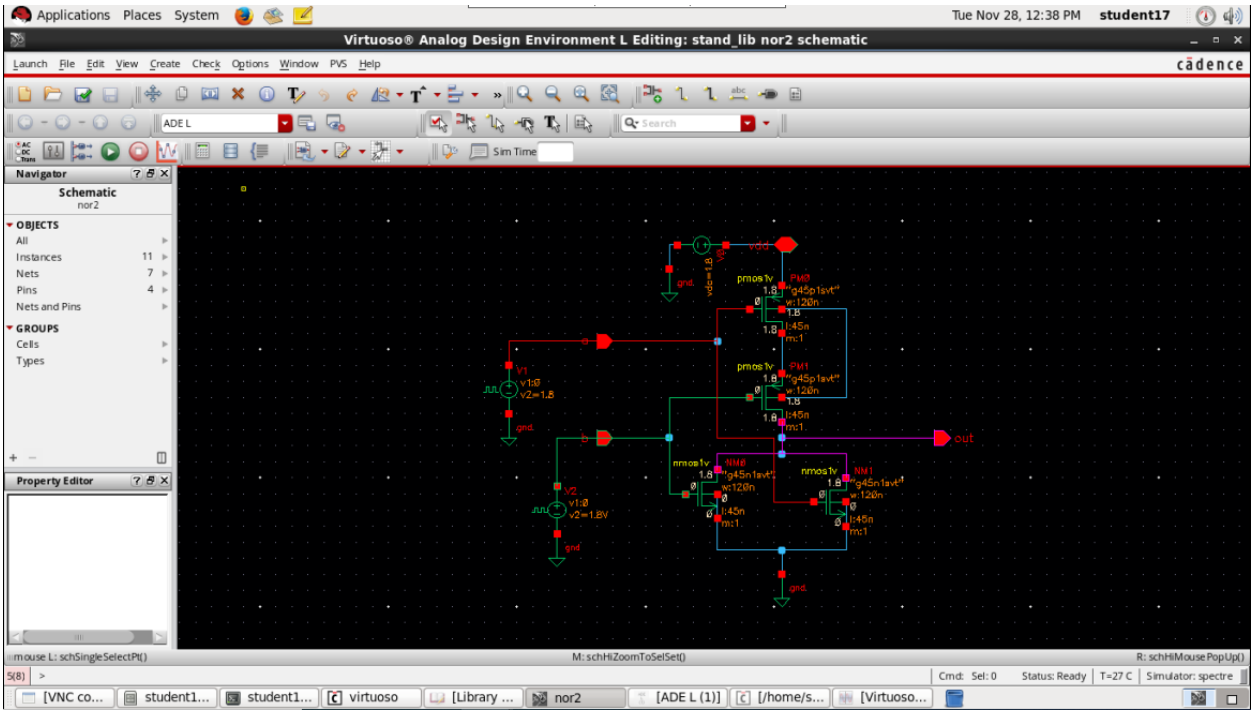

Figure-01: Schematic diagram of a 2-input NOR gate using MOS.

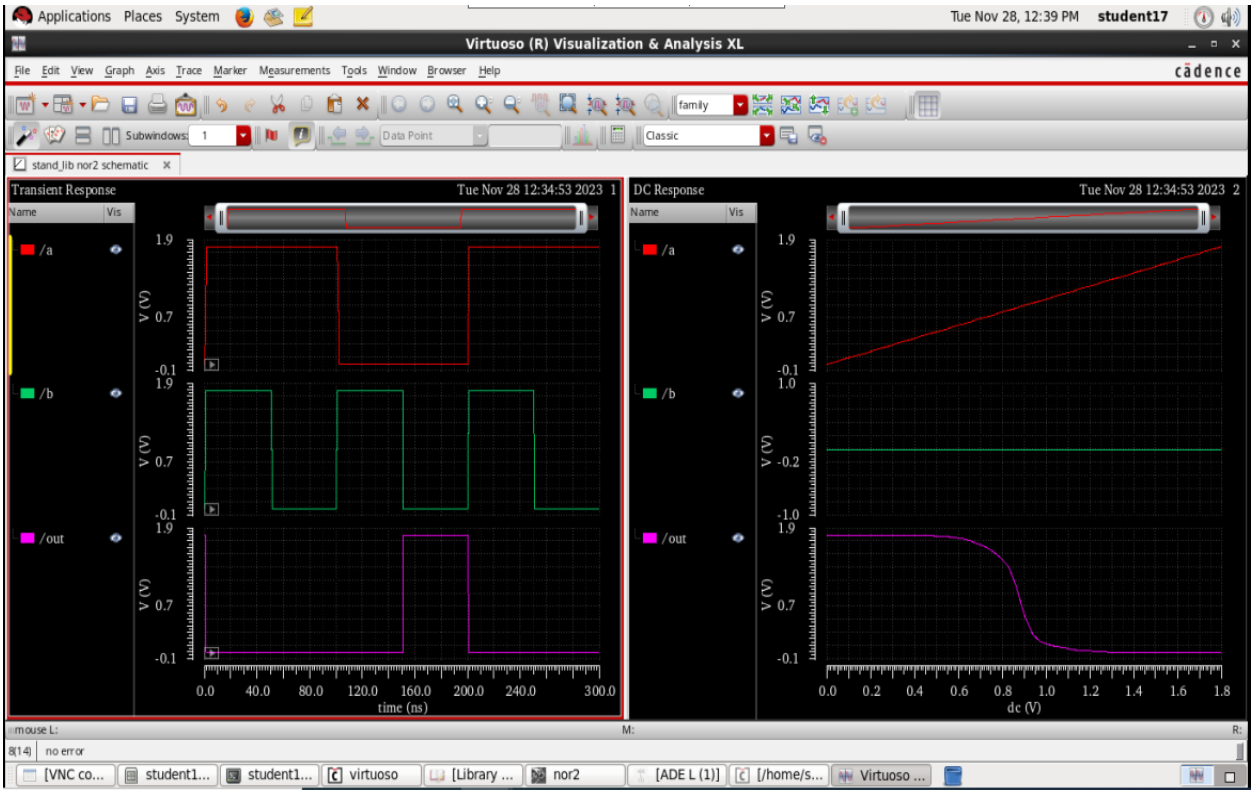

Figure-02: Output waveform of our designed circuit.

Specification for the output waveform:

we configured the voltage source in following way

V_{DC} = DC Voltage 1.8 V

Vpulse (connected to a) = voltage 1 = 0 V
voltage 2 = 1.8 V
period = 200n
Pulse width = 100n

Vpulse (connected to b) = voltage 1 = 0 V
voltage 2 = 1.8 V
period = 100n
pulse width = 50n

Then we plotted the waveform using transient analysis and stop time 300ns

Truth table for NOR gate:

Input		output
A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

Our output satisfied the truth table.

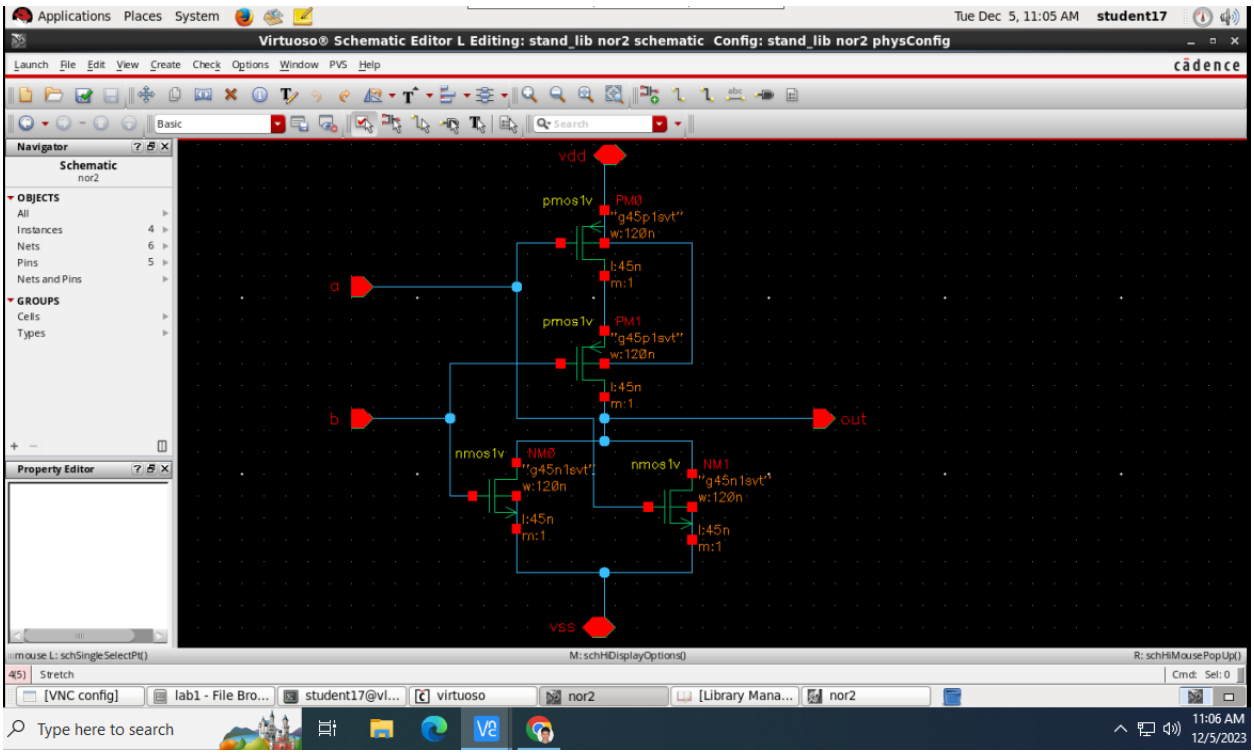

Figure-03: Circuit diagram before designing the symbol and layout.

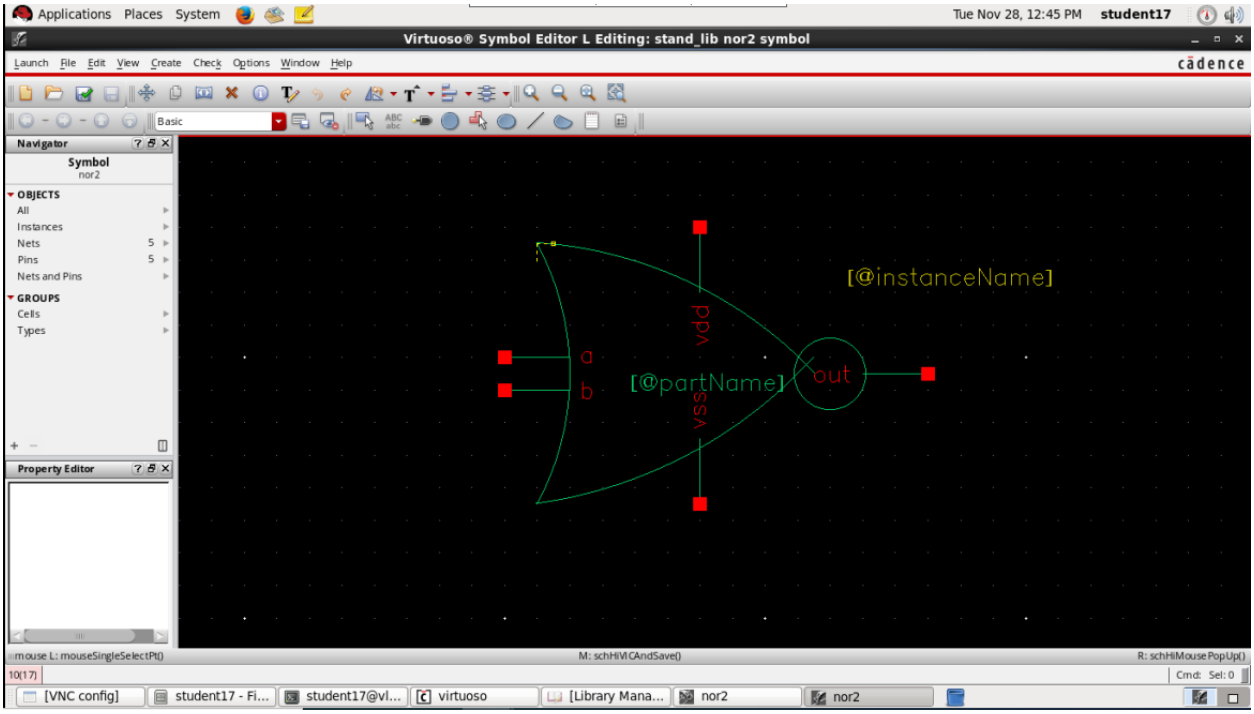

Figure-04: User defined symbol of a 2-input NOR gate.

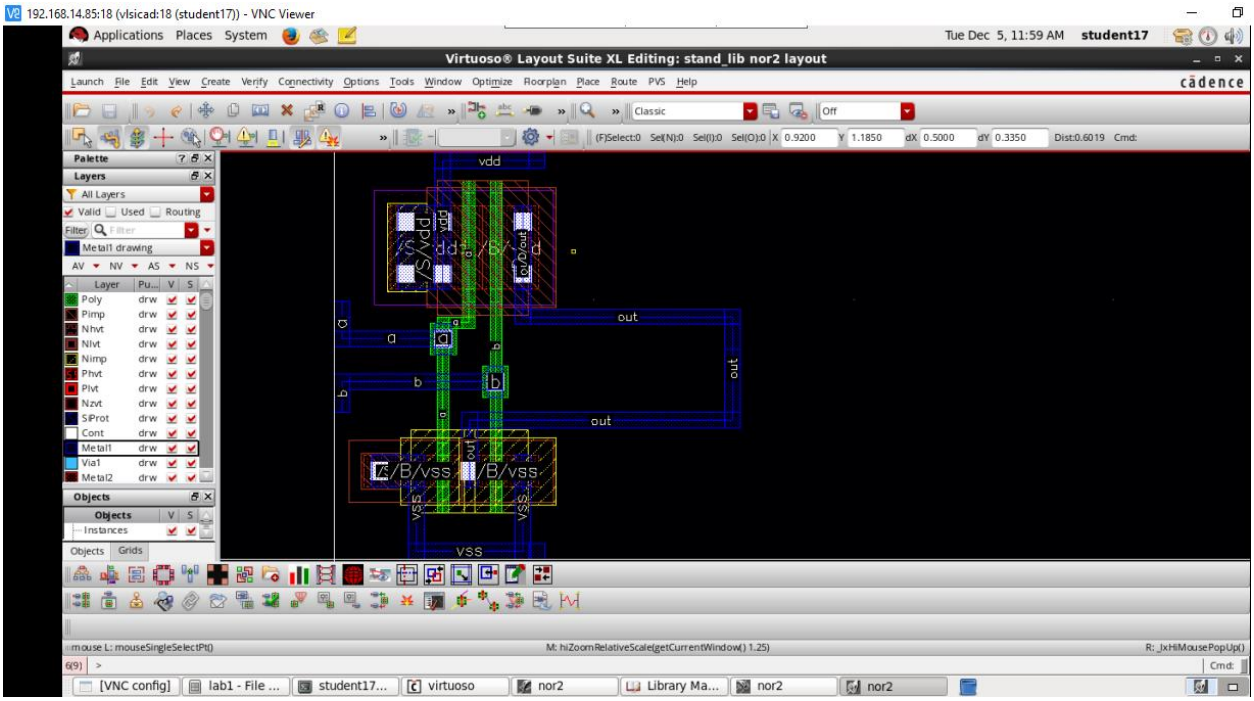

Figure-05: Complete routing of the layout.

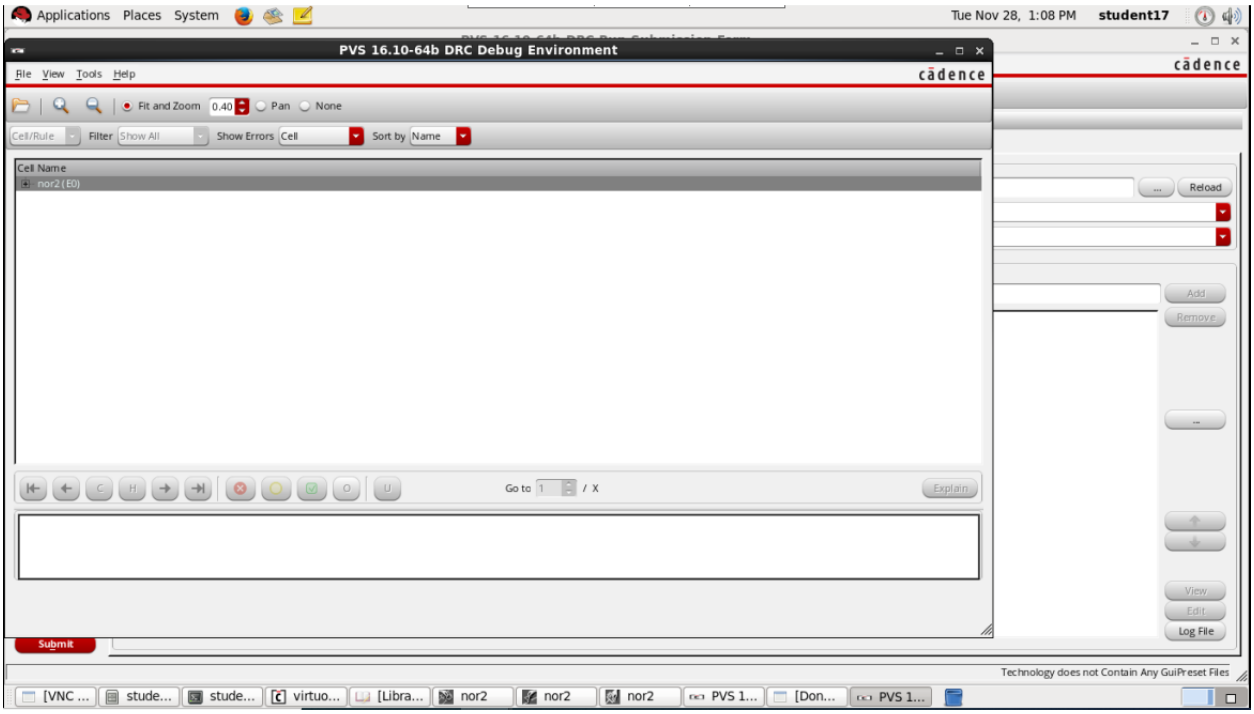

Figure-06: Completed DRS. No error in DRS.

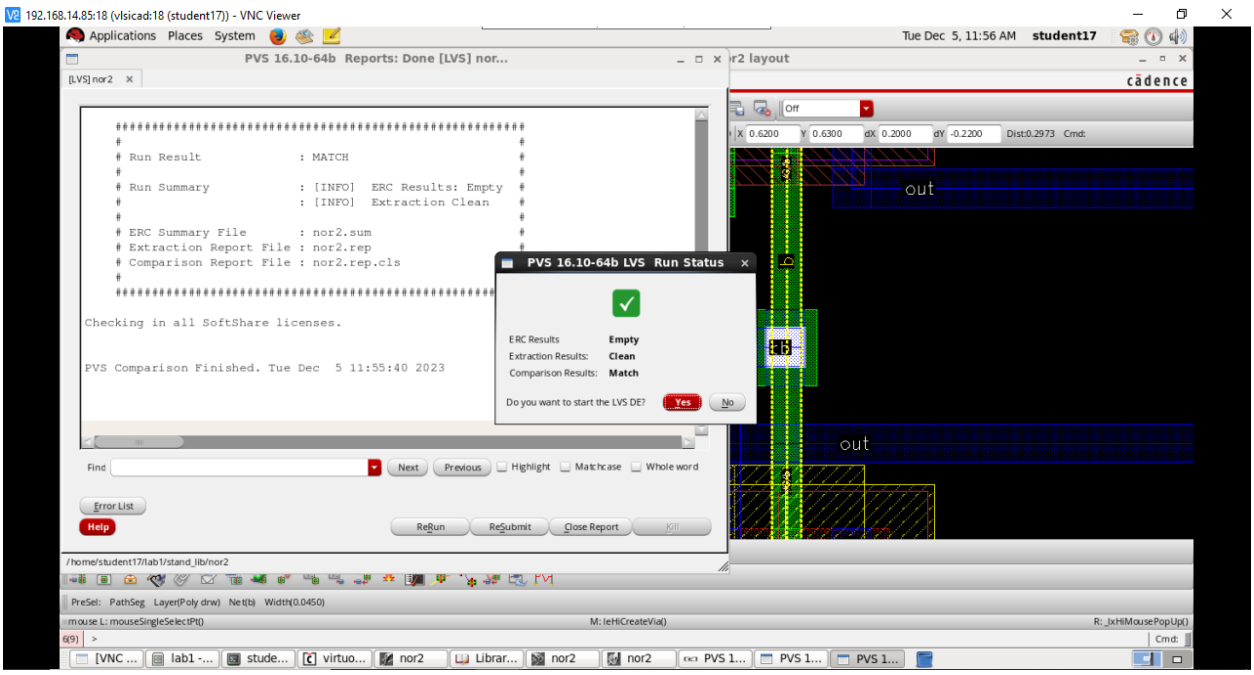

Figure-07: Checking LVS. No error in LVS.

Conclusion : Overall, the experiment was successful and the layout followed the design rule as both DRC and LVS showed no error.