CSE 3203 CT 4 Assignment
Roll No: 1803163

Assignment Problem:
Build CPU based on following requirements:

1. **Word Size of CPU = 4**
2. **ALU Operations = XOR, ADD, ROR**
3. **Register Number = 4**
4. **Size of RAM = 7**
5. **Word size of ISA and RAM = 15**
6. **CPU Instructions = Register Mode, Immediate Mode, JMP, JG**

Solution:
Simulator Design:

1. **ALU Circuit (Top to Bottom all circuits):**

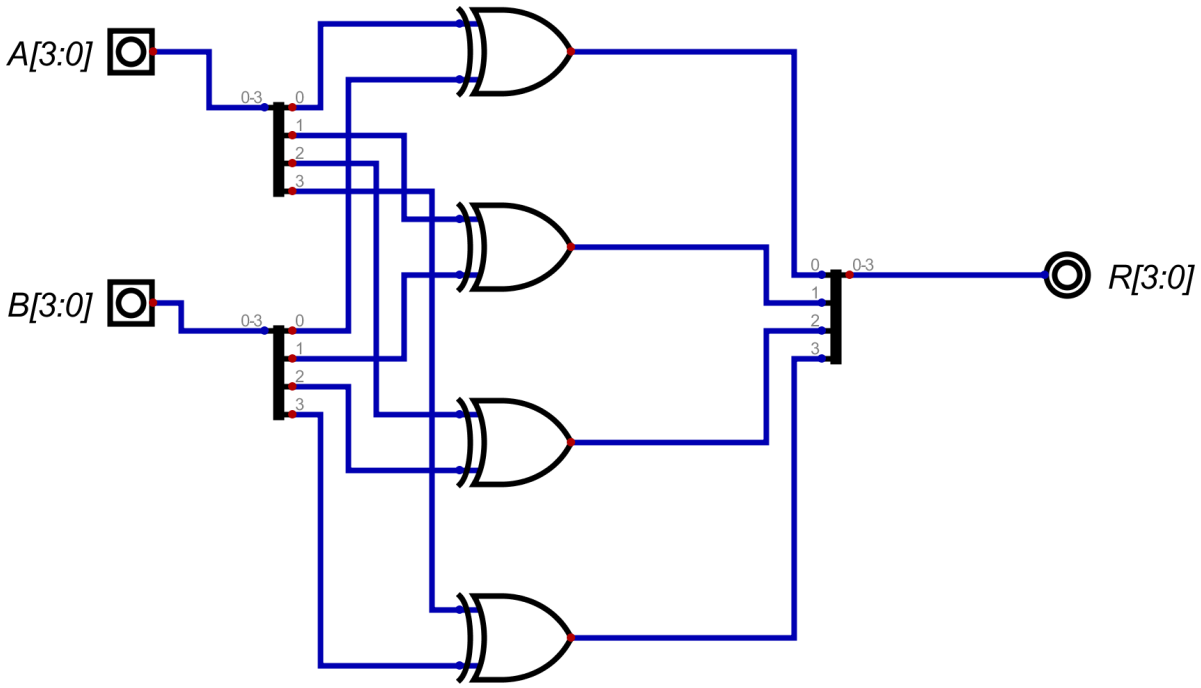

Figure: 4bit XOR

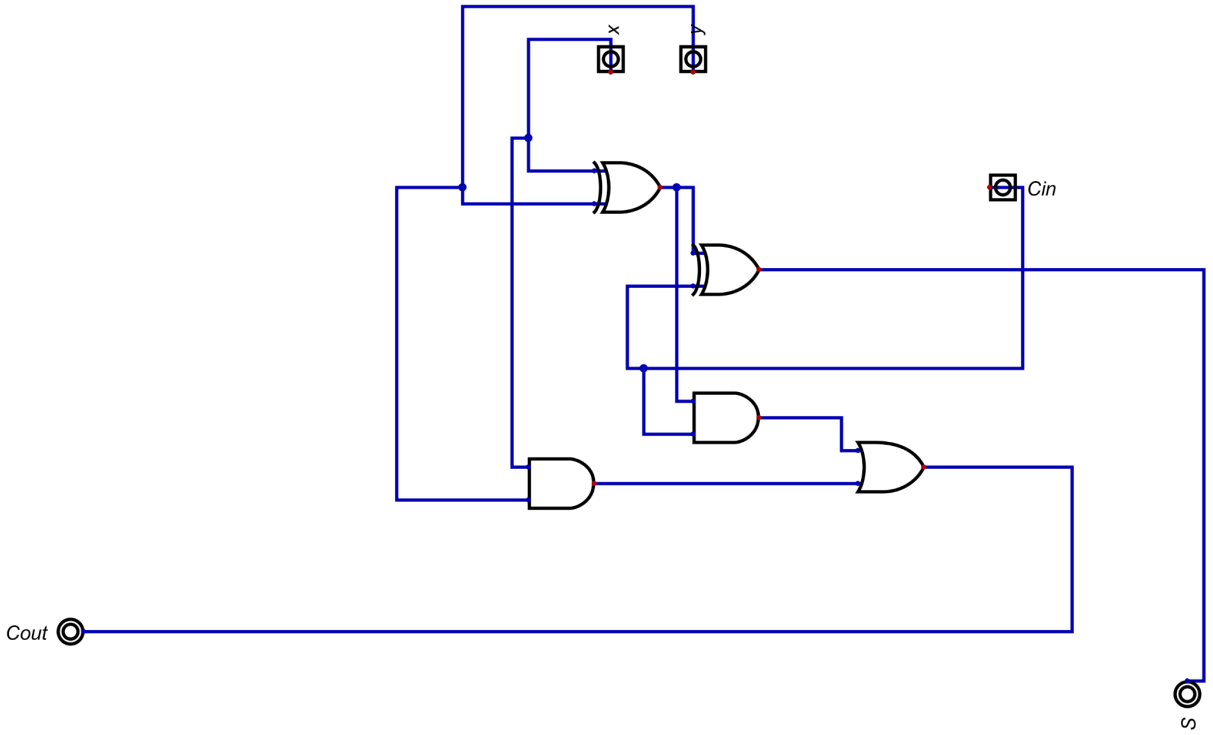

Figure: Full Adder

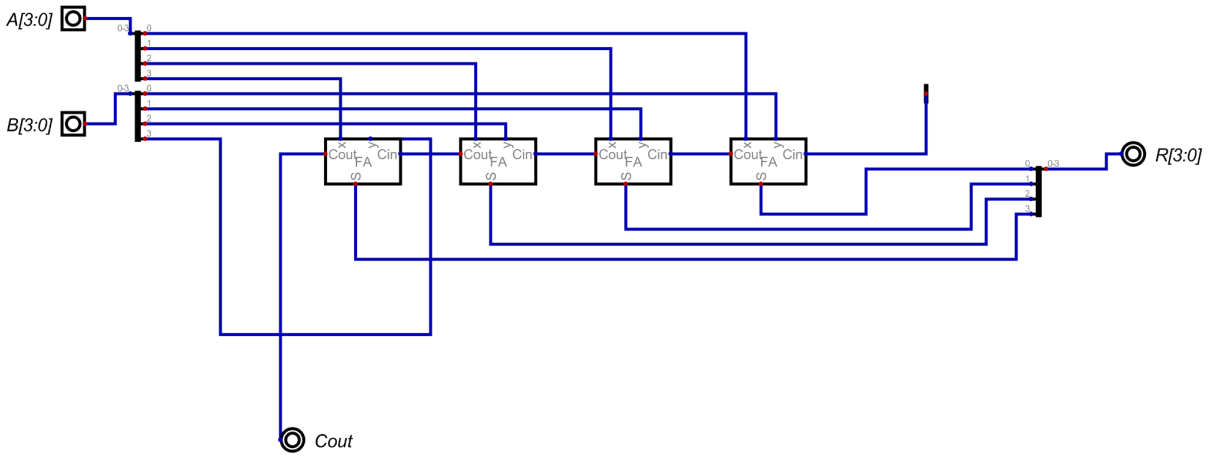

Figure: 4bit Adder

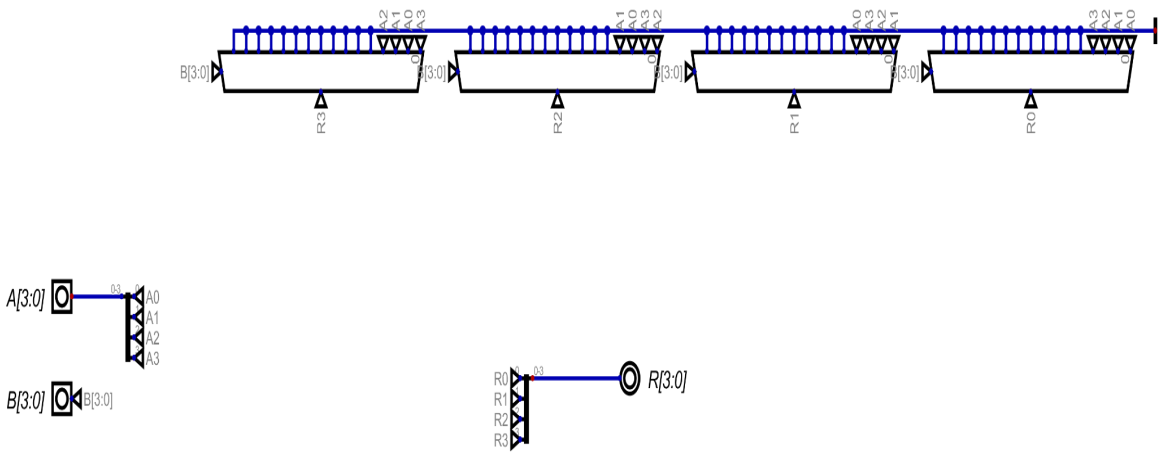

Figure: 4bit ROR

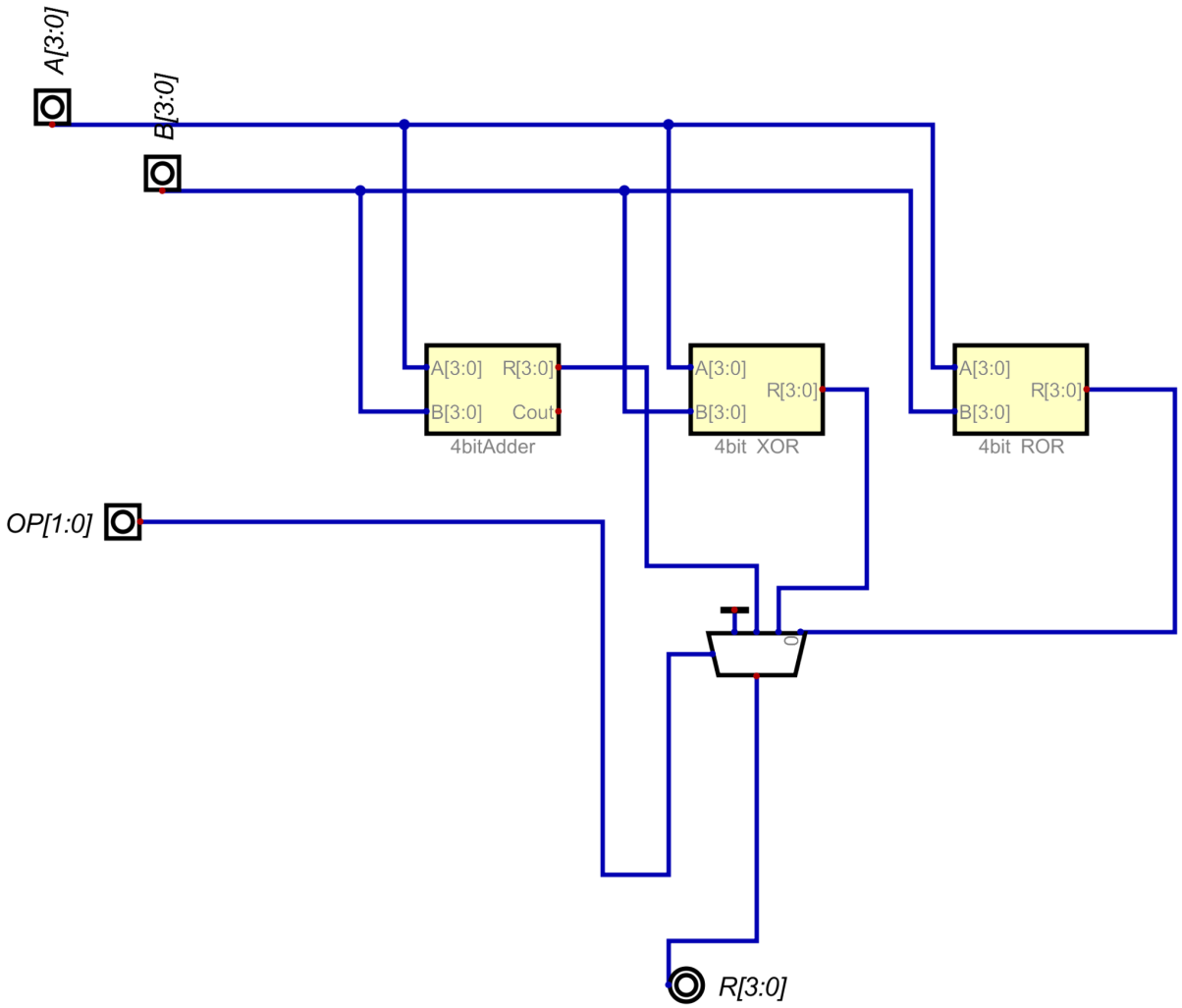

Figure: 4bit ALU

2. **Register Set Circuit (Top to Bottom all circuits):**

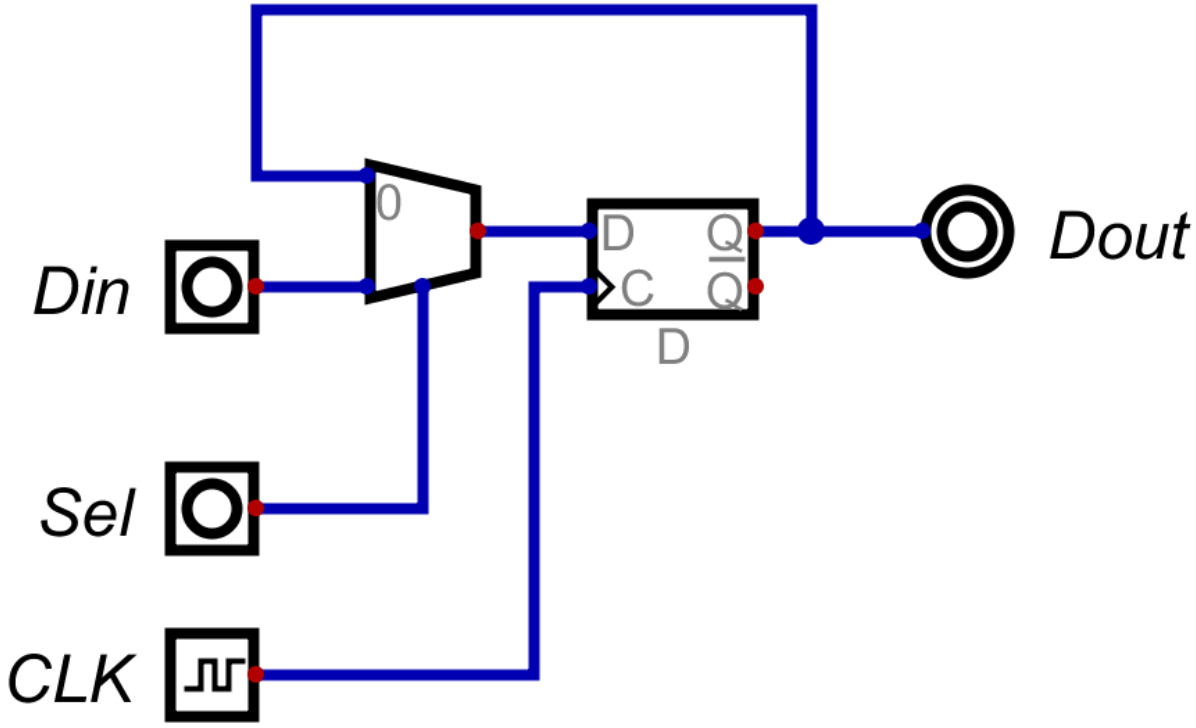

Figure: 1bit Register

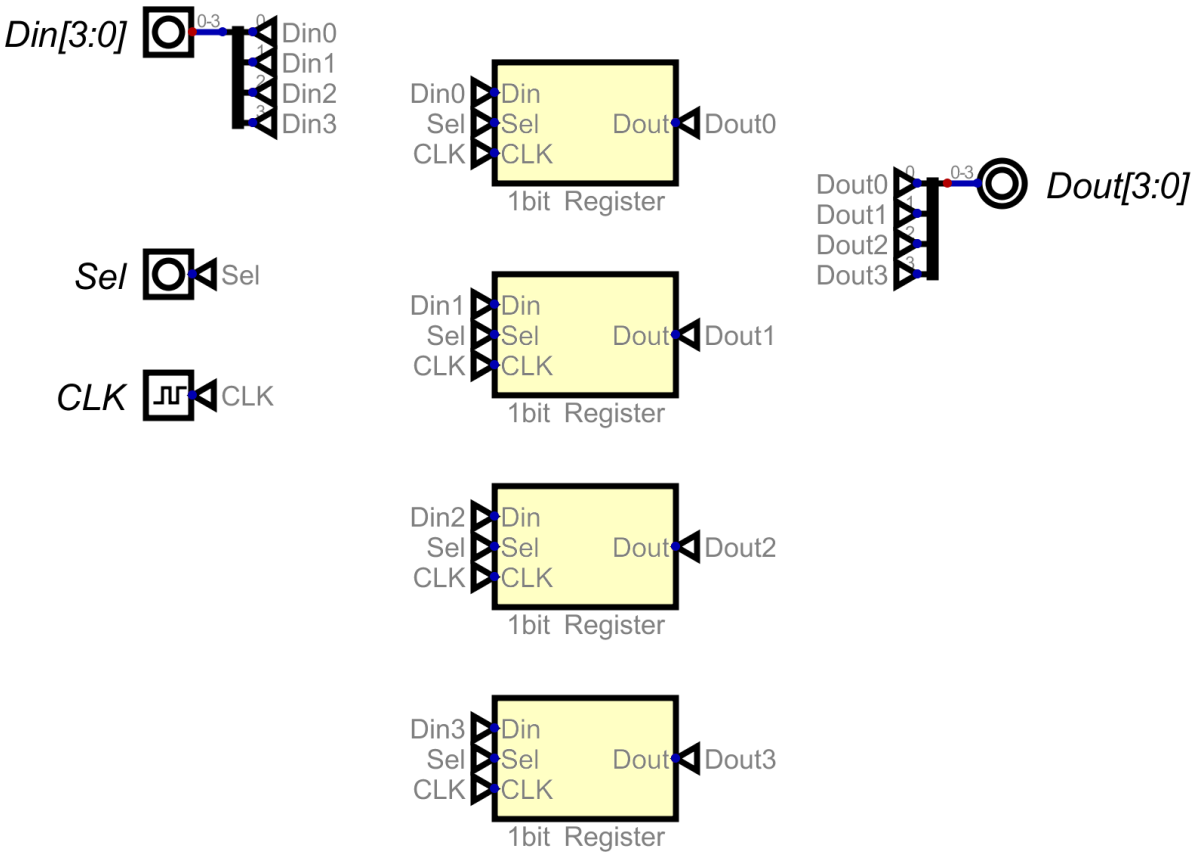

Figure: 4bit Register

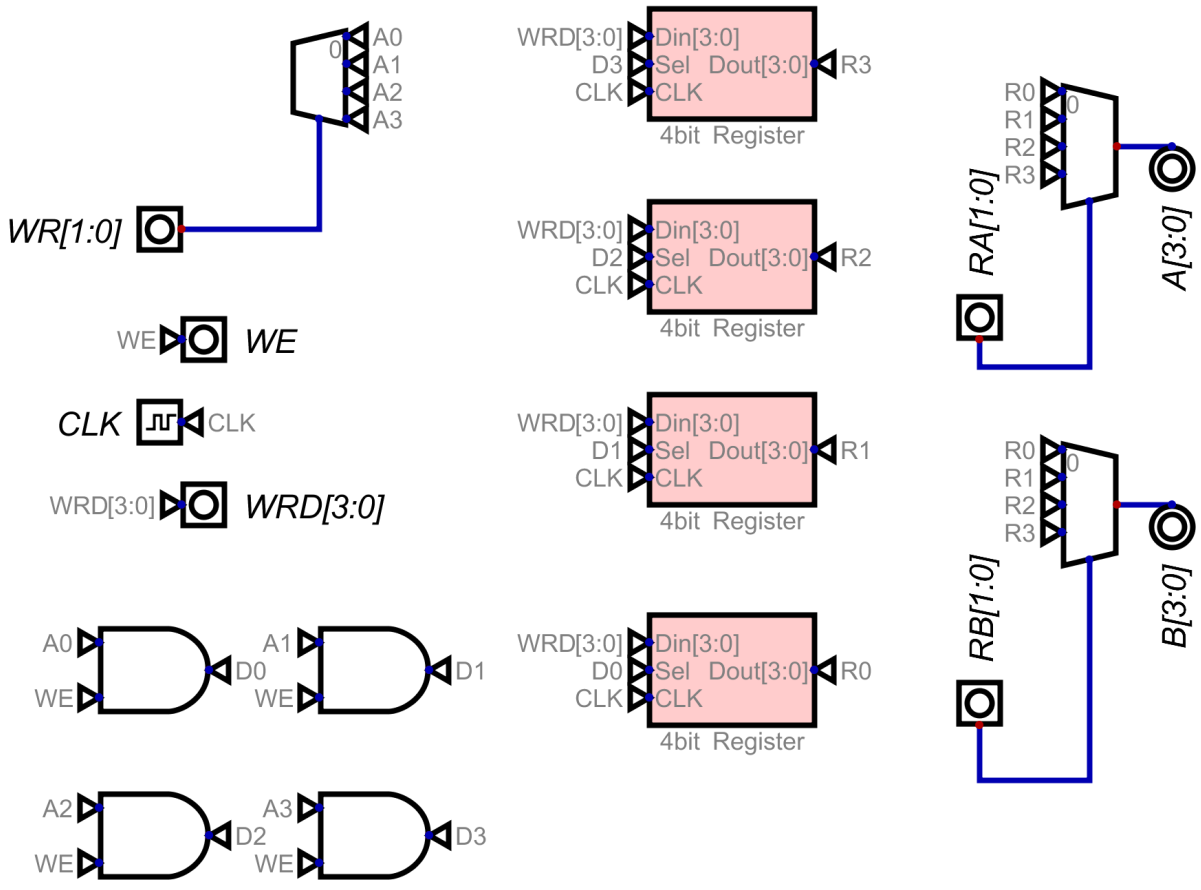

Figure: 4bit register_set

3. RAM Circuit (Top to Bottom all circuits):

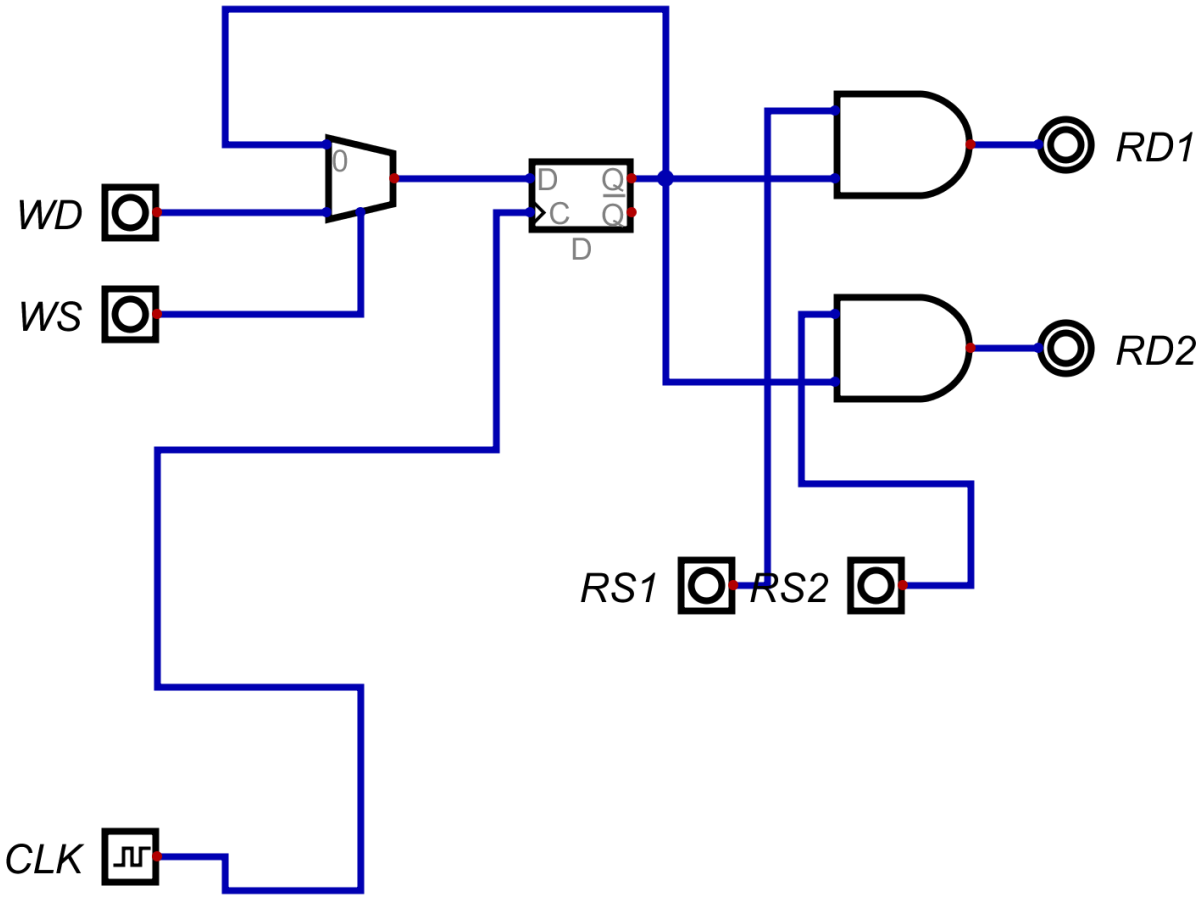

Figure: 1X1 SRAM

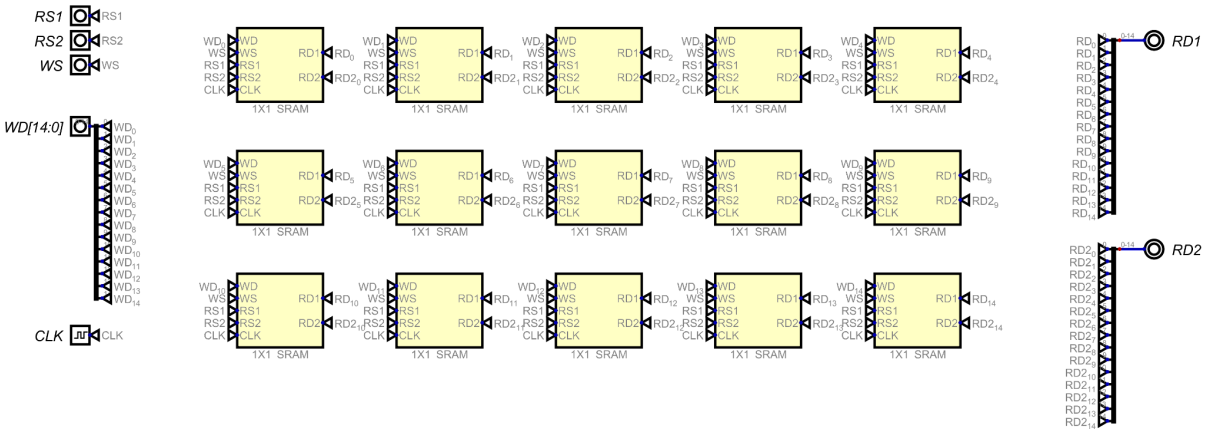

Figure: 1X15 SRAM

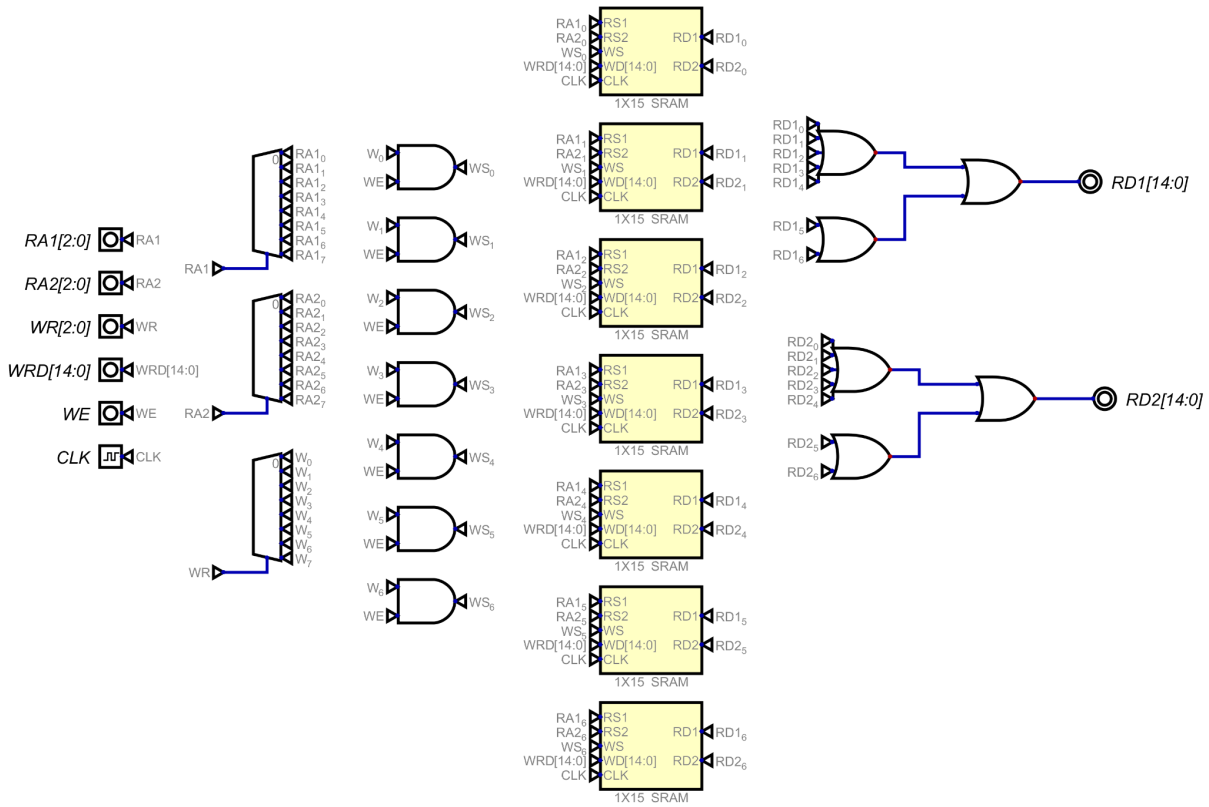

Figure: 7X15 SRAM

4. ISA:

Opcode (4 bit)		Register 1	Register 2	Assembly Example
Type (2 bits)	**Operations (2 bits)**	**2 bits**	**2 bits**	
00	00 (ROR)	00-11(R0-R3)	00-11(R0-R3)	ROR R0, R1
	01 (XOR)	00-11(R0-R3)	00-11(R0-R3)	XOR R2, R3
	10 (ADD)	00-11(R0-R3)	00-11(R0-R3)	ADD R0, R1

ISA(Register Mode)

Opcode (4 bit)		Register 1	Constant	Assembly Example
Type (2 bits)	Operations (2 bits)	2 bits	4 bits	
01	00 (ROR)	00-11(R0-R3)	0000-1111 (0-15)	ROR R0, 1
	01 (XOR)	00-11(R0-R3)	0000-1111 (0-15)	XOR R2, 2
	10 (ADD)	00-11(R0-R3)	0000-1111 (0-15)	ADD R0, 3

ISA(Immediate Mode)

Opcode (4 bit)		Address	Register 1	Assembly Example
Type (2 bits)	Operations (2 bits)	3 bits	2 bits	
10	00 (JMP)	00-11(R0-R3)	00-11(0-3)	JMP LABEL
	01(JG)	00-11(R0-R3)	00-11(0-3)	JG LABEL

ISA(Branching)

5. CPU (Top to Bottom all circuits):

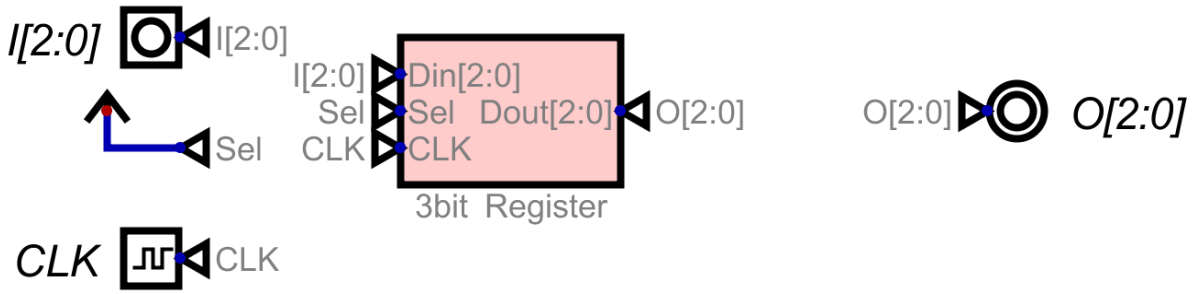

Figure: Program Counter

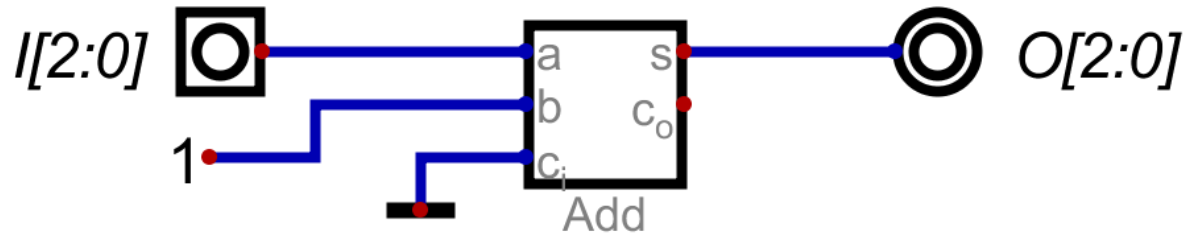

Figure: AddOne Circuit

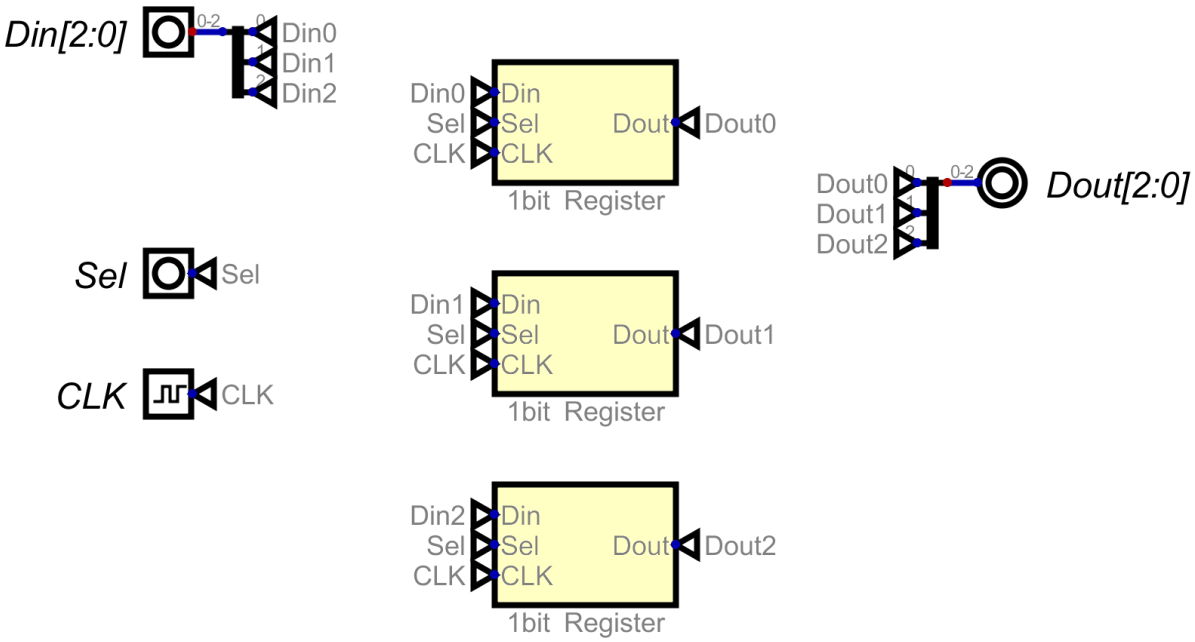

Figure: 3bit Register

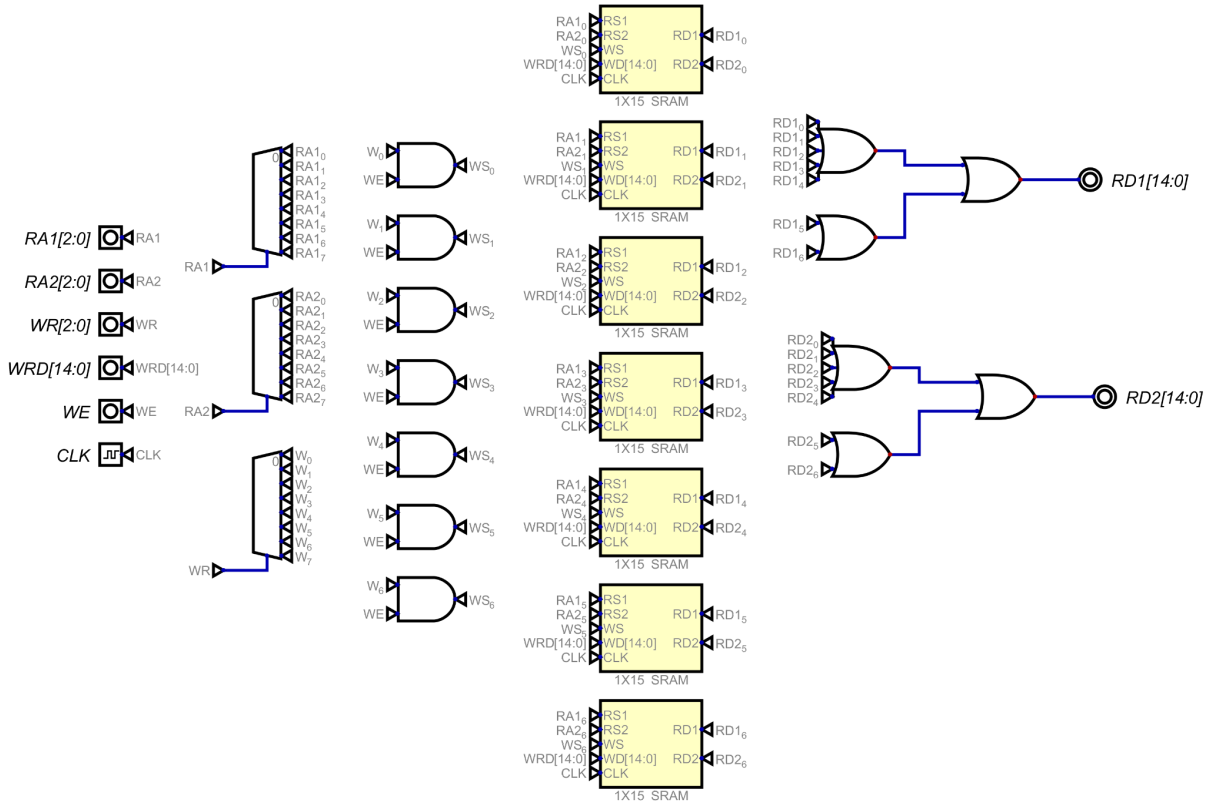

Figure: 7X15 SRAM

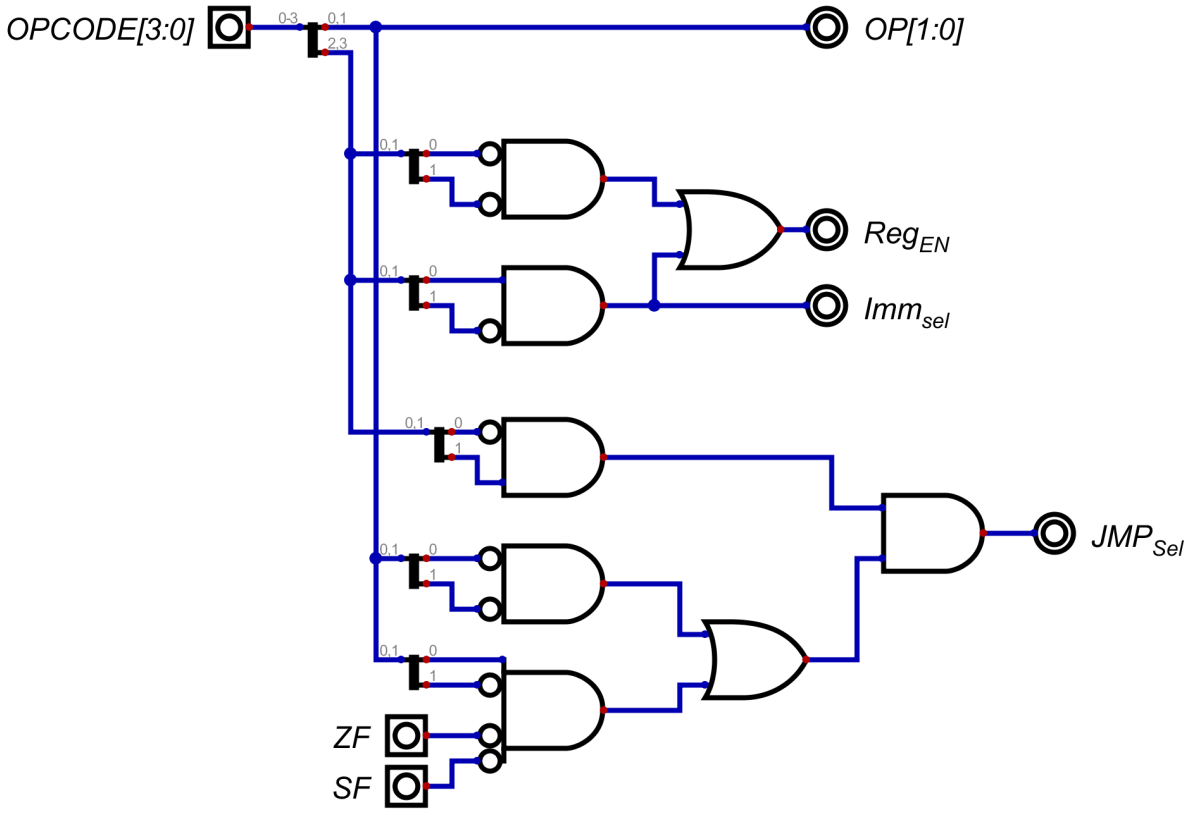

Figure: Control unit

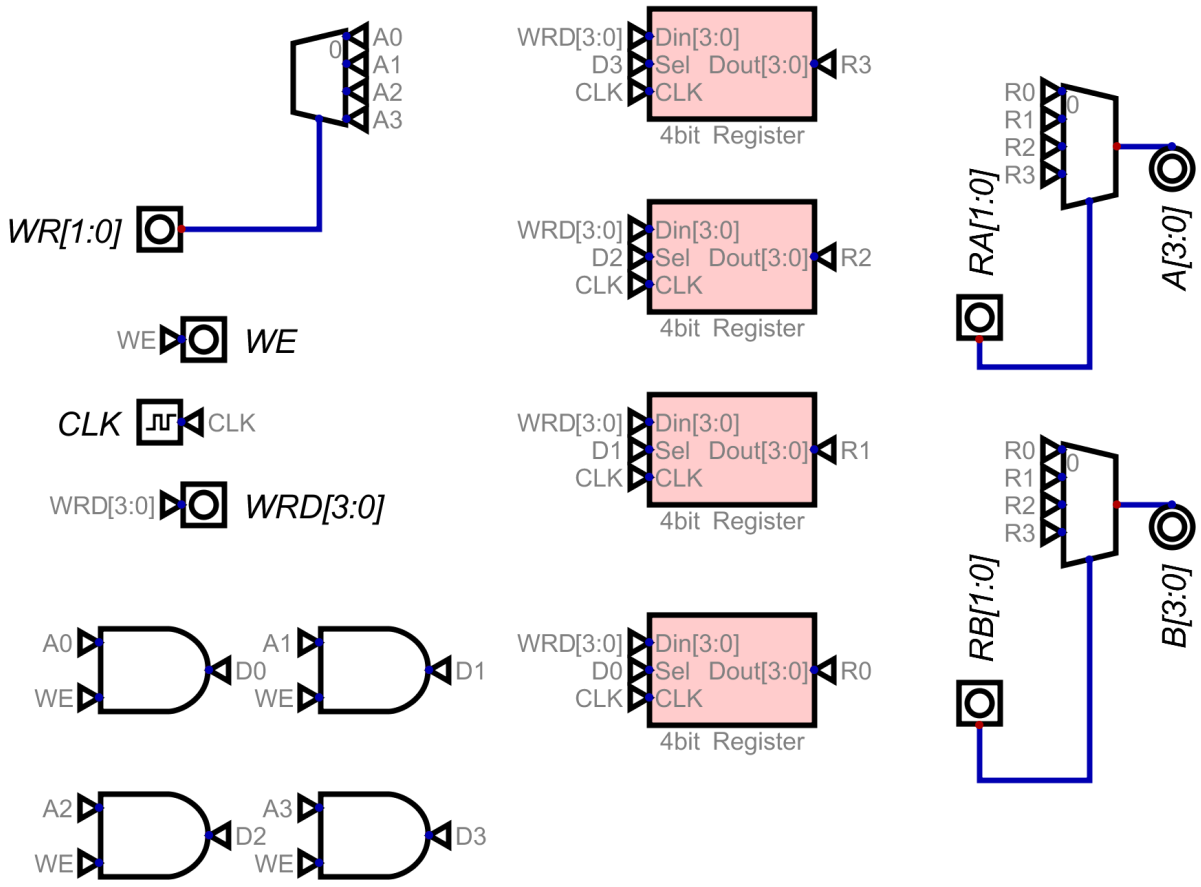

Figure: 4bit register_set

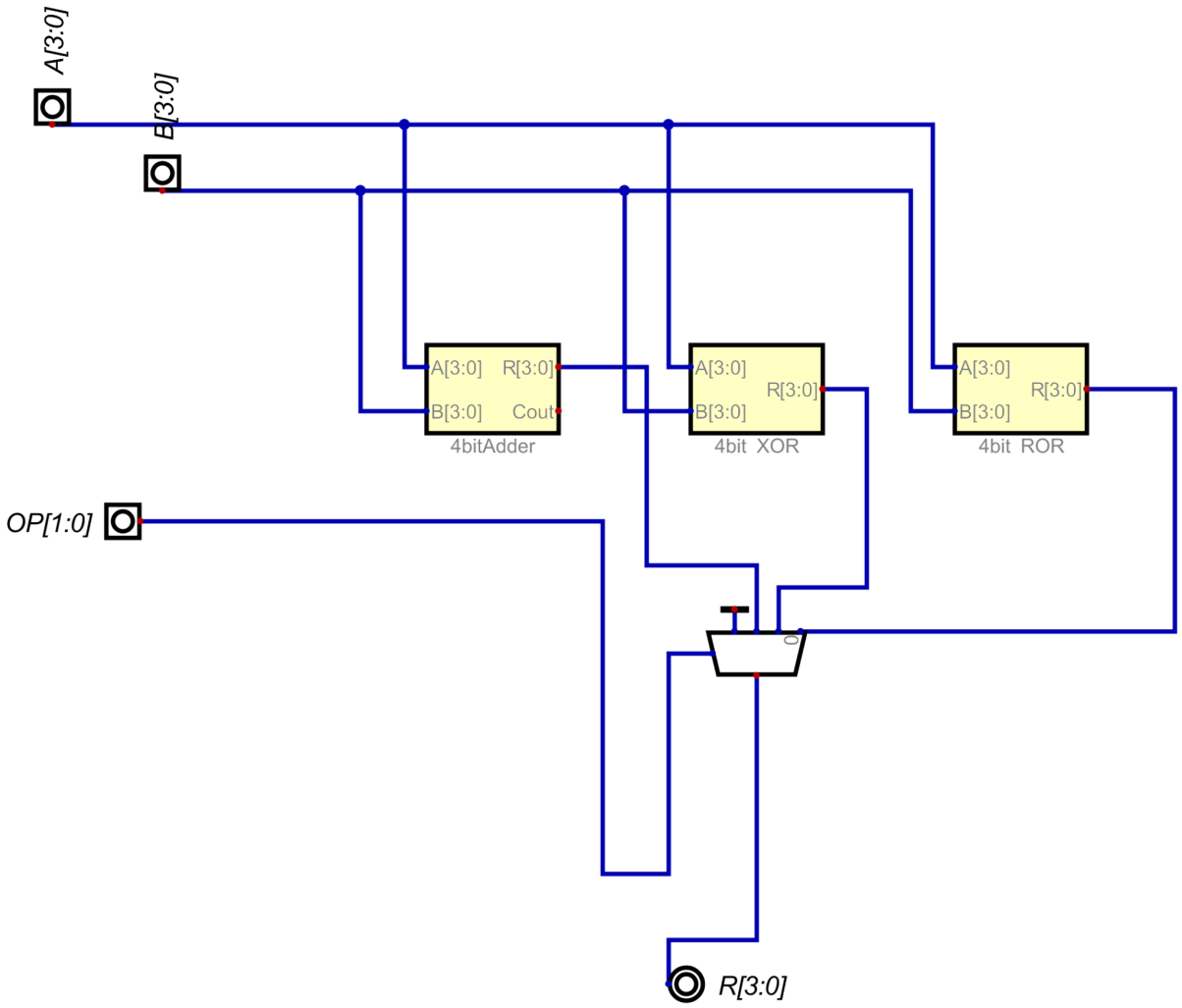
A[3:0]
B[3:0]
A[3:0]
R[3:0]
B[3:0]
Cout
4bitAdder
A[3:0]
R[3:0]
B[3:0]
4bit XOR
A[3:0]
R[3:0]
B[3:0]
4bit ROR
OP[1:0]
R[3:0]

Figure: ALU

Register Mode : 2 bit (type of OP=00) + 2 bit OP + 2 bit (Ra) + 2 bit (Rb) + 7 bit (Don't care) | Total 15 bit
Immediate Mode : 2 bit (type of OP=01) + 2 bit OP + 2 bit (Ra) + 4 bit (Rb) +5 bit (Don't care) | Total 15 bit
XOR (OP = 01), ADD (OP = 10), ROR (OP = 00)
JMP Mode : 2 bit (type of OP=10) + 2 bit OP + 3 bit (Ra)
JMP (OP=00), JG (OP=01)

0 XOR R0,R0 -> 0b000100000000000
1 XOR R1,R1 -> 0b000101010000000
2 JMP REPEAT-> 0b100011000000000
3 START:
ADD R0,01 -> 0b011000000100000
4 ADD R1,06 -> 0b011001011000000
5 ROR R1,R0 -> 0b000001000000000
6 REPEAT:
JG START -> 0b100101100000000

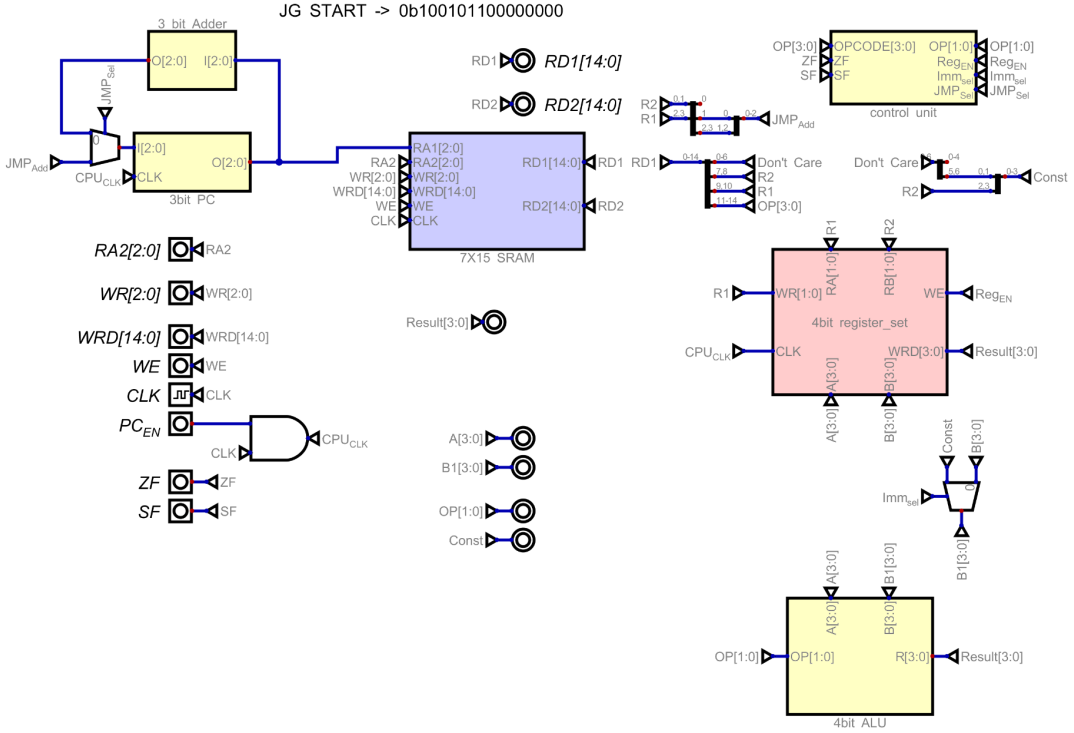

Figure: CPU

Verilog Code:

1. **ALU Circuit (Top to Bottom all circuits):**

2. **Register Set Circuit (Top to Bottom all circuits):**

3. **RAM Circuit (Top to Bottom all circuits):**

4. **CPU (Top to Bottom all circuits):**