RAJSHAHI UNIVERSITY OF ENGINEERING AND TECHNOLOGY

LAB REPORT - 06

COURSE NAME: SESSIONAL BASED ON CSE 2103
COURSE CODE: CSE 2104

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7.1) Experiment Name: Verify SR Flip-Flop by using NOR & NAND Latch.

Objectives:

- To know the characteristics of SR flip-flop.
- To know how to draw SR flip-flop using NOR and NAND latch.
- To generate the truth table of SR flip-flop using of NOR & NAND latch.
- To verify the output of SR flip-flop.

Theory: SR flip-flop is the simplest possible memory element which is formed by two NAND gates or two NOR gates.The inputs S and R are known as the SET and RESET inputs.The outputs Q and Q' are complements of each other.They are referred to as the normal and complementary outputs.

Usually,SR flip-flop is formed by NOR gates.

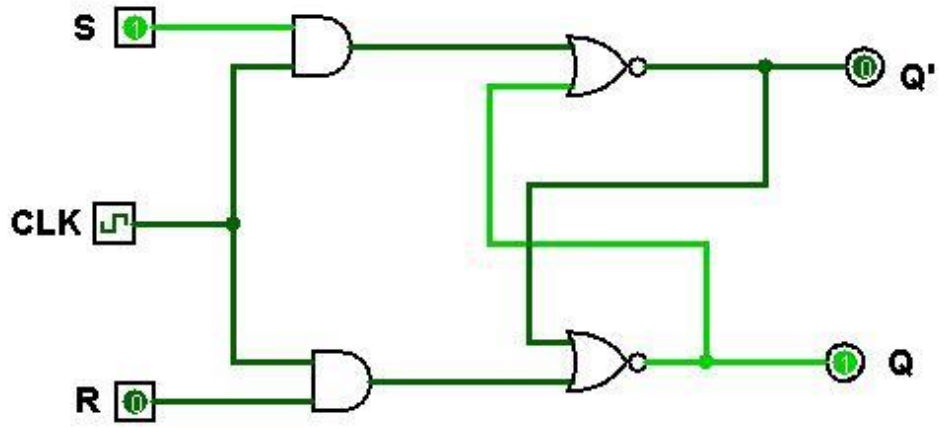
Summary of the NORlatch:

1. SET = 0, RESET = 0—Normal resting state, outputs remain in state they were in prior to input.
2. SET = 1, RESET = 0—Output will go to Q= 1 and remains there, even after SET returns HIGH.
3. SET = 0, RESET = 1—Will produce = 0 LOW and remains there, even after RESET returns HIGH.
4. SET = 1, RESET = 1—Tries to set and clear the latchat the same time, and produces $Q=\overline{Q}=1$.
   Output is unpredictable, and this input condition should not be used.

Experimental Analysis:

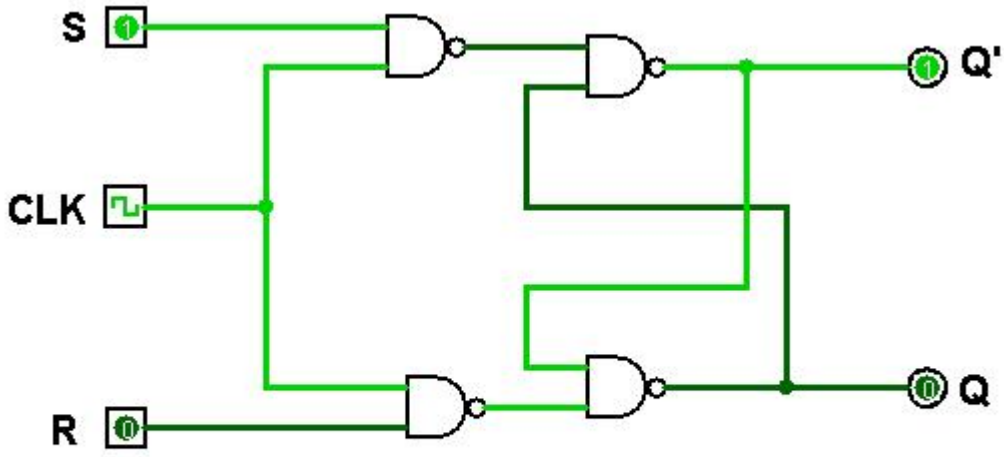
- **Circuit Diagram:**

7.1.1- Verifying SR Flip-Flop by using NOR Latch :



7.1.1: SR FF using NOR Latch

7.1.2- Verifying SR Flip-Flop by using NAND Latch :



7.1.2: SR FF using NAND Latch

- **Truth Table:**

S	R	Q
0	0	Unchanged
0	1	0
1	0	1
1	1	Invalid

Conclusion: In this experiment,we discussed about SR Flip-Flop by using NOR & NAND Latch.The main drawback of SR flip flop is invalid output when both inputs are high.

7.2) Experiment Name: Verify JK Flip-Flop by using NOR & NAND Latch.

Objectives:

- To know the characteristics of JK flip-flop.
- To know how to draw JK flip-flop using NOR and NAND latch.
- To generate the truth table of JK flip-flop using of NOR & NAND latch.
- To verify the output of JK flip-flop.

Theory: J-K flip-flop is the most versatile of the basic flip-flops which is formed by two NAND gates or two NOR Gates.It has two data inputs J and K & clock pulse input. It has no undefined state.

Usually,JK flip-flop is formed by NOR gates.

Summary of the NORlatch:

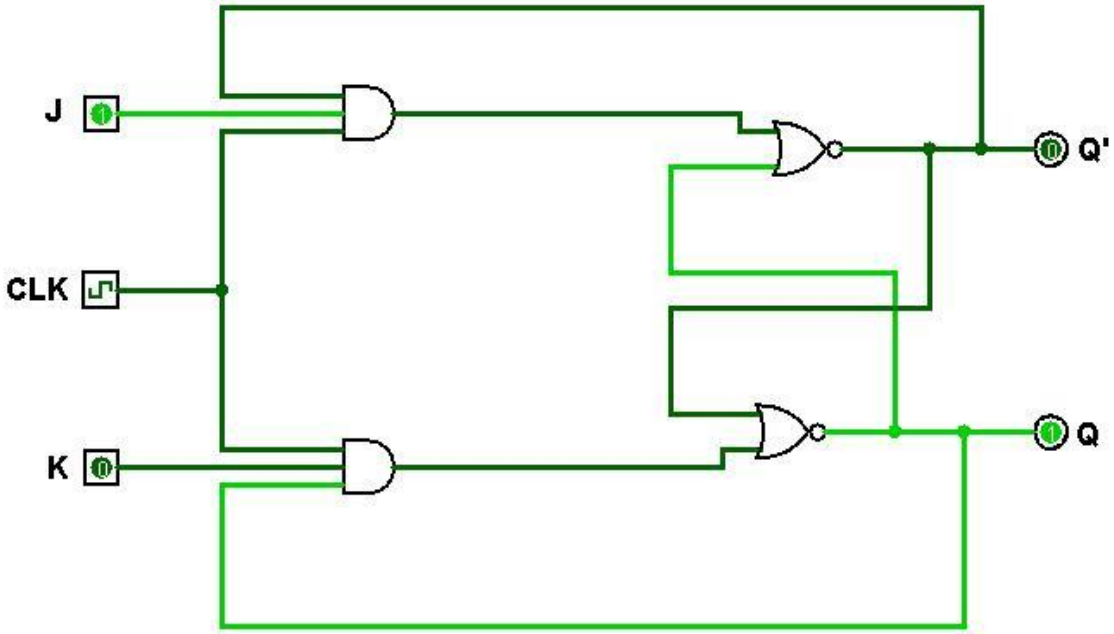
1. SET = 0, RESET = 0—Normal resting state, outputs remain in state they were in prior to input.
2. SET = 1, RESET = 0—Output will go to Q = 1 and remains there, even after SET returns HIGH.
3. SET = 0, RESET = 1—Will produce = 0 LOW and remains there, even after RESET returns HIGH.

4. SET = 1, RESET = 1—Output is toggled to the opposite state.

Experimental Analysis:

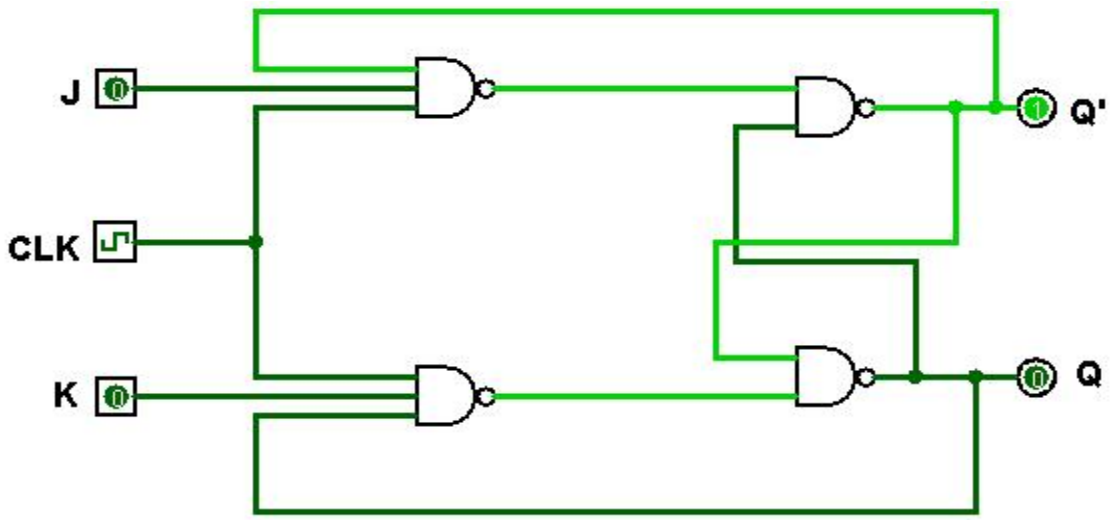
- **Circuit Diagram:**

7.2.1- Verifying JK Flip-Flop by using NOR Latch :



7.2.1: JK FF using NOR Latch

7.2.2- Verifying JK Flip-Flop by using NAND Latch :



7.2.2: JK FF using NAND Latch

- **Truth Table:**

J	K	Q
0	0	Unchanged
0	1	0
1	0	1
1	1	Toggled

Conclusion: In this experiment,we discussed about JK Flip-Flop by using NOR & NAND Latch.In JK flip-flop,there is no ambiguous output & all outputs are valid.

7.3) Experiment Name: Verify D Flip-Flop by using NOR & NAND Latch.

Objectives:

- To know the characteristics of D flip-flop.
- To know how to draw D flip-flop using NOR and NAND latch.
- To generate the truth table of D flip-flop using of NOR & NAND latch.
- To verify the output of D flip-flop.

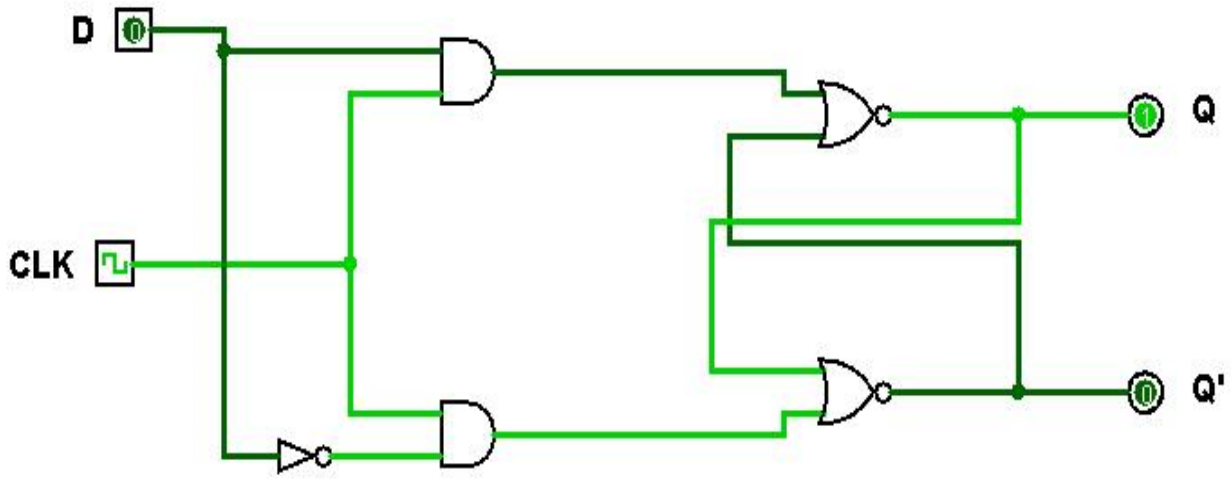
Theory: The D-type flip-flop is a modified Set-Reset flip-flop with the addition of an inverter to prevent the S and R inputs from being at the same logic level.

Output changes to the value of the input at either the positive-or negative-going clock trigger.

Experimental Analysis:

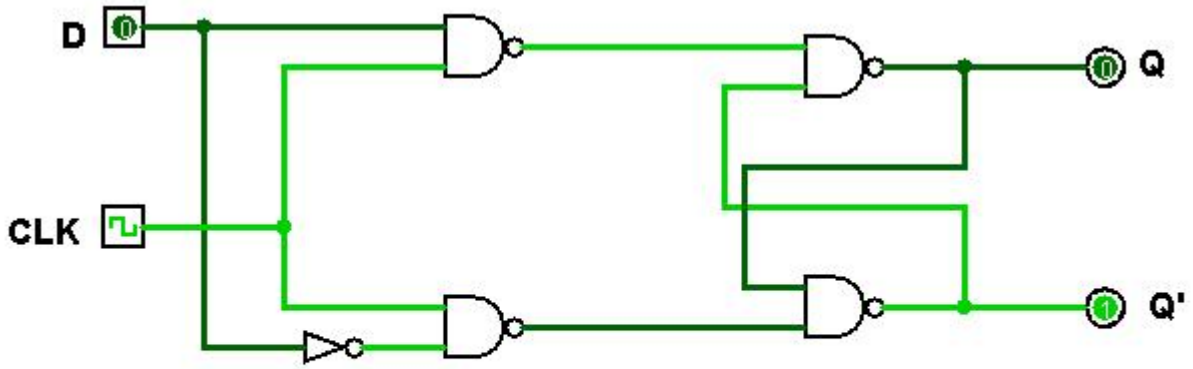
- **Circuit Diagram:**

7.3.1- Verifying D Flip-Flop by using NOR Latch :



7.3.1: D FF using NOR Latch

7.3.2- Verifying D Flip-Flop by using NAND Latch :



7.3.2: D FF using NAND Latch

- **Truth Table:**

D	Q
0	0
1	1

Conclusion: In this experiment,we discussed about D Flip-Flop by using NOR & NAND Latch**.**Whenever the clock signal is LOW, the input is never going to affect the output state.The clock has to be high for the inputs to get active.

7.4) Experiment Name: Verify T Flip-Flop by using NOR & NAND Latch.

Objectives:

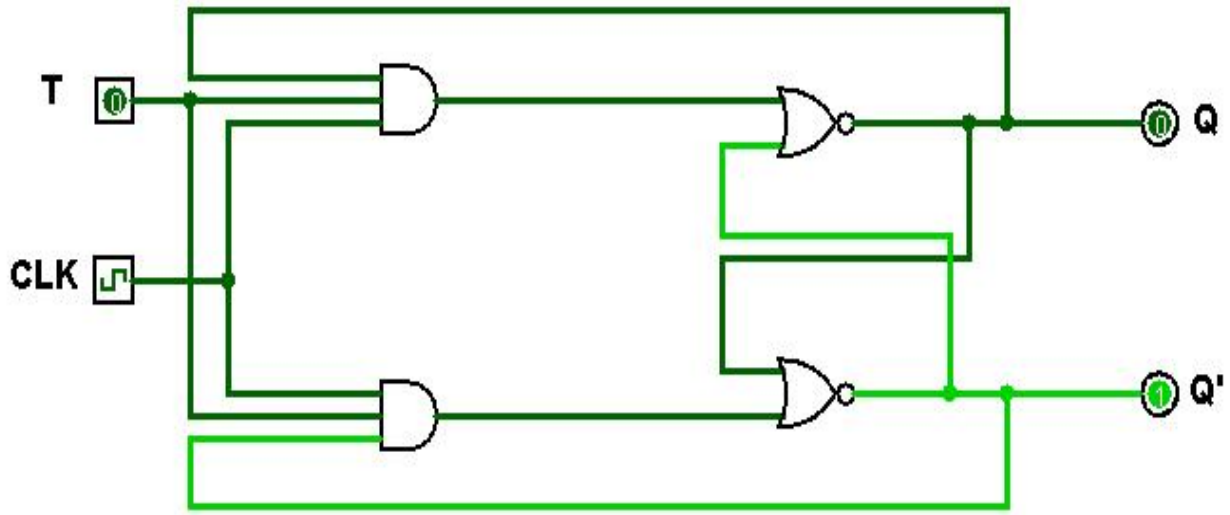
- To know the characteristics of T flip-flop.
- To know how to draw T flip-flop using NOR and NAND latch.
- To generate the truth table of T flip-flop using of NOR & NAND latch.
- To verify the output of T flip-flop.

Theory: T flip flop is modified form of JK flip-flop making it to operate in toggling region. A T flip flop is constructed by connecting J and K inputs,creating a single input called T. Hence why a T flip flop is also known as a single input JK flip flop..

Experimental Analysis:

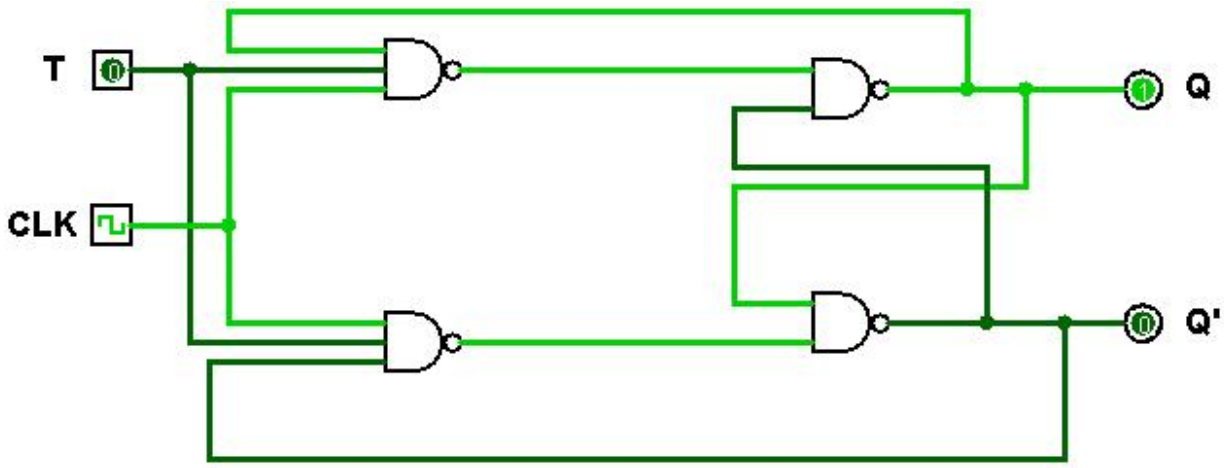
- **Circuit Diagram:**

7.4.1- Verifying T Flip-Flop by using NOR Latch :



7.4.1: T FF using NOR Latch

7.4.2- Verifying T Flip-Flop by using NAND Latch :



7.4.2: T FF using NAND Latch

- **Truth Table:**

T	Q
0	Unchanged
1	Toggled

Conclusion: In this experiment,we discussed about T Flip-Flop by using NOR & NAND Latch**.**Whenever the clock signal is LOW, the input is never going to affect the output state. The clock has to be high for the inputs to get active.