RAJSHAHI UNIVERSITY OF ENGINEERING AND TECHNOLOGY LAB REPORT - 03

COURSE NAME: SESSIONAL BASED ON CSE 2103 COURSE CODE: CSE 2104

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4.1) Experiment Name: Implement Various Logic Functions (For Example F(a, b, c, d) = SOP(0, 2, 3, 4, 6, 10, 14, 15)).

Objectives:

- To learn about Boolean algebra.
- To understand what are combinational logic circuits.
- To learn about canonical & standard form.
- To learn about using the sum-of-products method to design a logic circuit based on a design truth table.
- To learn about how to simplify Boolean expression.
- To learn about maxterm & minterm & how to findout these.

Theory: Digital circuit operates using digital signals. These signals have discrete binary values: zero and one. Zero signifies the false state while one signifies the true state. Boolean algebra is a type of algebra that helps to represent binary numbers and binary variables. Canonical form is a method of representing Boolean functions of Boolean algebra while standard form is a simplified version of canonical form.

Minterm: A product term in which all the variables appear exactly once, either complemented or uncomplemented. Denoted by m_j , where j is the decimal equivalent of the minterm's corresponding binary combination (b_i) .

Maxterm: A sum term in which all the variables appear exactly once, either complemented or Uncomplemented. Denoted by M_j , where j is the decimal equivalent of the maxterm's corresponding binary combination (b_i) .

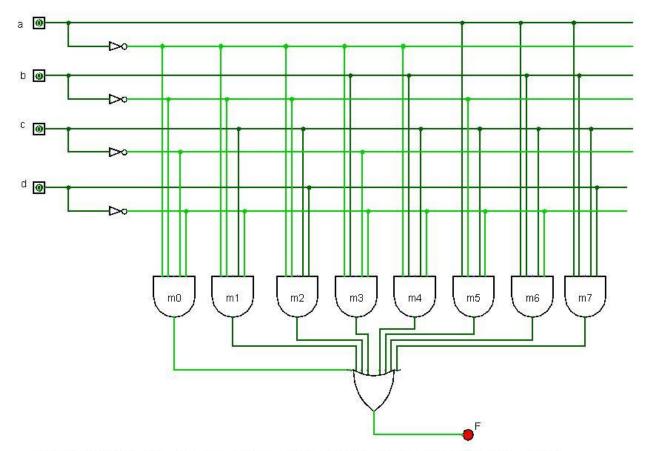
Truth Table notation for Minterms and Maxterms:

×	У	z	Minterm	Maxterm
0	0	0	$x'y'z' = m_0$	x+y+z = M ₀
0	0	1	$x'y'z = m_1$	x+y+z' = M ₁
0	1	0	x'yz' = m ₂	x+y'+z = M ₂
0	1	1	x'yz = m ₃	x+y'+z'= M ₃
1	0	0	xy'z' = m ₄	x'+y+z = M ₄
1	0	1	$xy'z = m_5$	x'+y+z' = M ₅
1	1	0	xyz' = m ₆	$x'+y'+z = M_6$
1	1	1	xyz = m ₇	$x'+y'+z' = M_7$

Experimental Analysis:

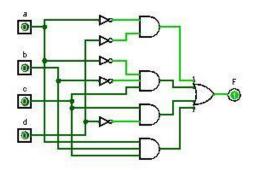
• Circuit Diagram:

4.1.1- Drag & drop circuit diagram:



4.1.1-(Drag & drop) Implement Various Logic functions (For example F(a,b,c,d) = SOP(0,2,3,4,6,10,14,15)

4.1.2-Analyse circuit diagram:



4.1.2-(Analyse) Implement Various Logic functions (For example F(a,b,c,d) = SOP(0,2,3,4,6,10,14,15)

)

• Truth Table:

a	b	С	d	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

Conclusion: In this experiment, we discussed about canonical form, it's characteristics and diagram.

4.2) Experiment Name: Verify the result of simplified version of F in 1.

Objectives:

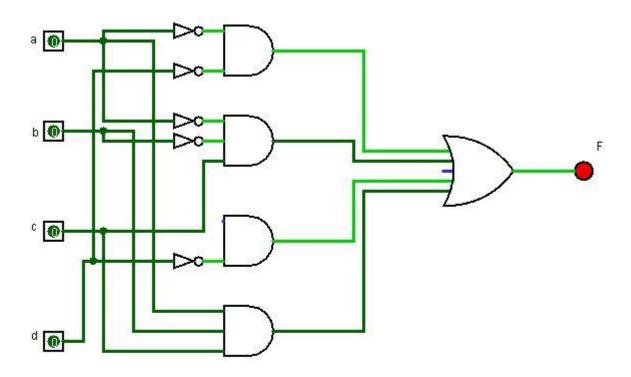
- To learn about how to simplify Boolean expression.
- To learn about how to use rules of Boolean expression.

Theory: In Boolean algebra simplification, a Boolean expression is translated to another form with less number of terms and operations.

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Simplification: abed + abed + abed
 +abcd +abcd +abcd + abcd
00) = abd+abcd+abcd+abcd+abcd+abcd
   tabed [: c+c=1]
 =) a & (6+bc) + a 5 cd + a b cd + a 5 cd
   + abcd +abcd.
=) at (6+c)+ a ocd + a ocd + a ocd
   + abcd + abcd
=) ad (5+c+6c)+abcd+abcd+abcd+abcd
= ad } (5+c+b) (5+c+b)y + abcd + abcd
 tabeatabed.
=) az + abcd +abcd +abcld+2)
=) ad +abcd +abcd +abc
=) ad + abcd +ac( 0 b + 6 d)
=) ad + abcd + acd +abc.
=) 7 (a + ac) + a 5 cd + abc
→ d(a+c)+ a 5 cd+abc
=) ad + cd + abcd +abc
=) ad + e ) ( + a t) ( a+ d) / rab
=) ad + c (d+ab) +abc
=) AJ+cJ+Abc+abc
```

Experimental Analysis:

• Circuit Diagram:



4.2-Verify the result of simplified version of F in 1.

• Truth Table:

a	b	С	d	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

Conclusion: We can say that the result of simplified version of F in 1 is verified.