

**RAJSHAHI UNIVERSITY OF ENGINEERING AND TECHNOLOGY**  
**LAB REPORT - 01**

COURSE NAME: SESSIONAL BASED ON CSE 2103  
COURSE CODE: CSE 2104

**SUBMITTED TO-**

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SUBMISSION DATE -2 FEBRUARY, 2021

**Experiment Name:** Verify the Basic NOT gate for all input combinations.

**Objectives:**

- To study and understand the NOT gate.
- To implement the logic circuit operation using NOT gate.
- To write the Boolean expression for NOT gate.
- To draw the diagram of NOT gate.
- To generate the truth-table of NOT gate.

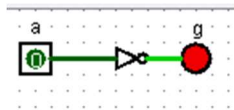
**Theory:** The gate which is a single input and output gate is called **NOT** gate. This gate is also known as inverter because it performs the inversion of the applied binary signal. If we give 0 as input, it converts it to 1 and vice-versa. Suppose Z is output and A is input then we express the NOT gate as:  $Z = \bar{A}$ .

The complement value is generated by the NOT gate.

**Experimental Analysis:**

• **Circuit Diagram:**

When the input signal is 0, the output is 1.



On the other hand, when the input signal is 0, the output is 1.



• **Truth Table:**

a	g
0	1
1	0

**Conclusion:** In this experiment, we discussed about NOT gate operation. From the truth table, we came to know that a NOT gate always has high (logical 1) output when its input is low (logical 0). Conversely, it always has low (logical 0) output when the input is high (logical 1).

**Experiment Name:** Verify the Basic AND gate (up to 5 Inputs) for all input combinations.

**Objectives:**

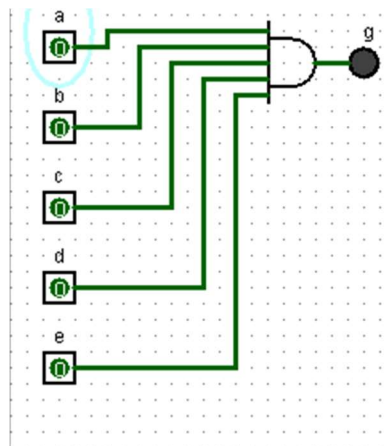
- To study and understand the AND gate.
- To implement the logic circuit operation using AND gate.
- To write the Boolean expression for AND gate.
- To draw the diagram of AND gate.
- To generate the truth-table of AND gate.

**Theory:** The basic digital logic gate that implements logical conjunction is called **AND** gate. The output of this gate will be high if all the input signals are high and the output of this gate will be low if all the input signals are low. Suppose Z is output and A,B are the two inputs, then we can represent the AND gate as:  $Z = A \wedge B$

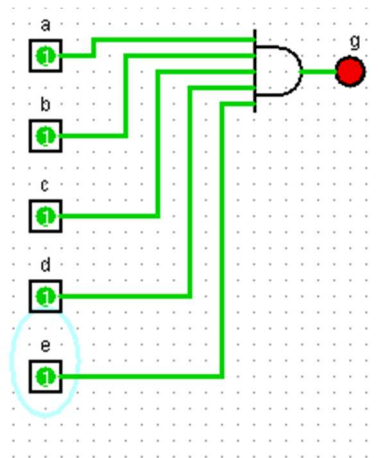
**Experimental Analysis:**

- **Circuit Diagram:**

When all the inputs are 0, the output is 0.



When all the inputs are 1, the output is 1.



- **Truth Table:**

a	b	c	d	e	g
0	0	0	0	0	x
0	0	0	0	1	x
0	0	0	1	0	x
0	0	0	1	1	x
0	0	1	0	0	x
0	0	1	0	1	x
0	0	1	1	0	x
0	0	1	1	1	x
0	1	0	0	0	x
0	1	0	0	1	x
0	1	0	1	0	x
0	1	0	1	1	x
0	1	1	0	0	x
0	1	1	0	1	x
0	1	1	1	0	x
0	1	1	1	1	x
1	0	0	0	0	x
1	0	0	0	1	x
1	0	0	1	0	0
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	0	1	0
1	0	1	1	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	0	0	1	0
1	1	0	1	0	0
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	0	1	0
1	1	1	1	0	0
1	1	1	1	1	1

**Conclusion:** In this experiment, we discussed about AND gate operation. From the truth table, we came to know that an AND gate operates on logical multiplication rules.

**Experiment Name:** Verify the Basic OR gate (up to 5 Inputs) for all input combinations.

**Objectives:**

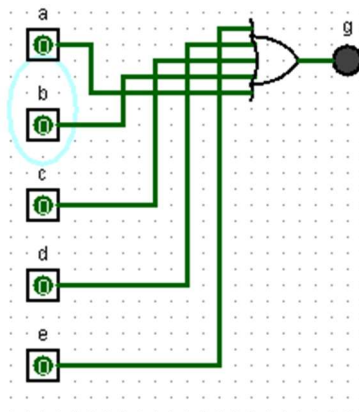
- To study and understand the OR gate.
- To implement the logic circuit operation using OR gate.
- To write the Boolean expression for OR gate.
- To draw the diagram of OR gate.
- To generate the truth-table of OR gate.

**Theory:** The digital logic gate that implements logical disjunction is called **OR** gate. The output of this gate will be high if at least one of the input signals is high and the output of this gate will be low if all the input signals are low. Suppose Z is output and A,B are the two inputs, then we can represent the OR gate as:  $Z = A+B$

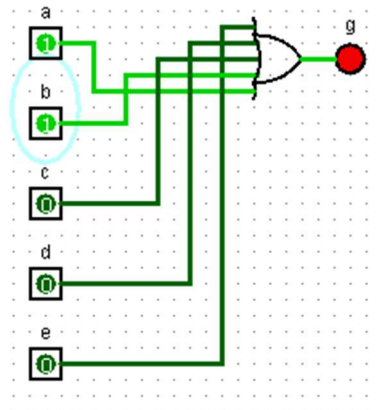
**Experimental Analysis:**

- **Circuit Diagram:**

When all the inputs are 0, the output is 0.



When at least one of the inputs is 1, the output is 1.



- **Truth Table:**

a	b	c	d	e	g
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	1
0	0	0	1	1	1
0	0	1	0	0	1
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	0	1	1
0	1	0	1	0	1
0	1	0	1	1	1
0	1	1	0	0	1
0	1	1	0	1	1
0	1	1	1	0	1
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	0	1	1
1	1	0	1	0	1
1	1	0	1	1	1
1	1	1	0	0	1
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	1

**Conclusion:** In this experiment, we discussed about OR gate operation. From the truth table, we came to know that an OR gate operates on logical addition rules.

**Experiment Name:** There are given four input signals. Display the output of AND gate and NOT gate connected in series with the output of AND gate.

**Objectives:**

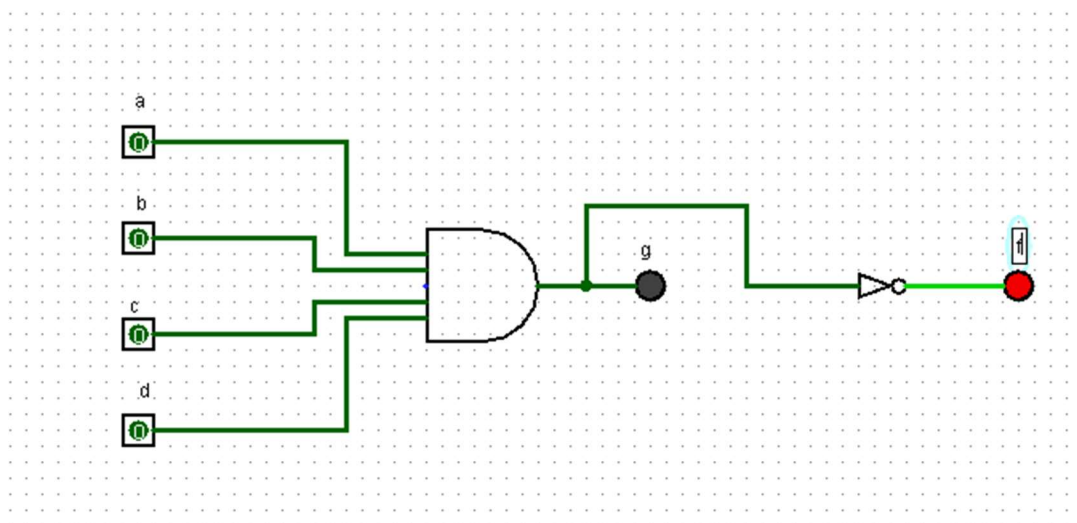
- To study and understand the combination of AND and NOT gate.
- To implement the logic circuit operation using AND and NOT gate.
- To draw the diagram of the circuit by drag and drop.
- To analyse the circuit.
- To generate the truth-table of combination gate.

**Theory:** A logic gate which produces an output which is false only if all its inputs are true is called NAND (NOT-AND) gate. Suppose Z is the output and A, B are the two inputs then we can represent the NAND gate as :  $Z = \sim(A \wedge B)$

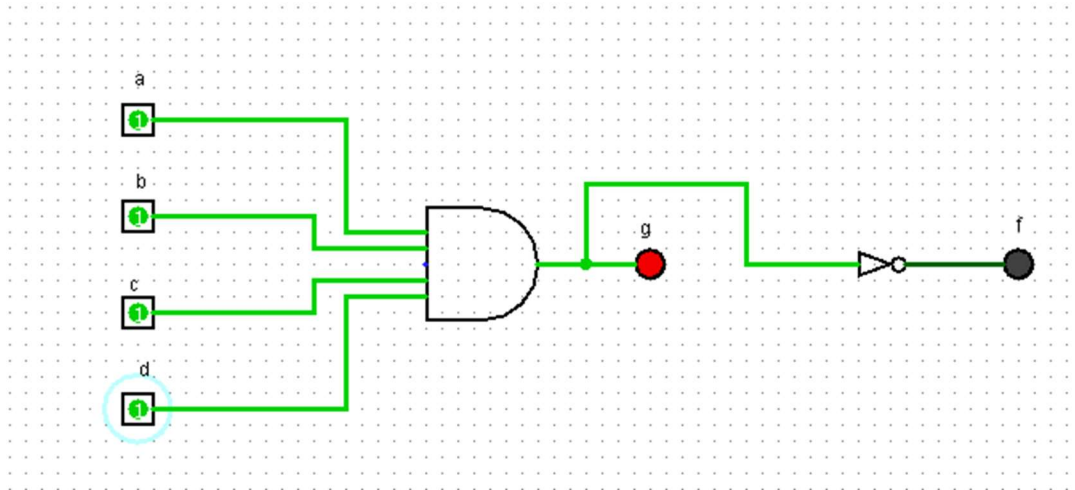
**Experimental Analysis:**

- **Circuit Diagram:**

When all the inputs are 0, the output is 1.



When all the inputs are 1,the output is 0.



- **Truth Table:**

a	b	c	d	g	f
0	0	0	0	0	1
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	0	1
1	0	0	0	0	1
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	0	1
1	1	0	0	0	1
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	1	0

**Conclusion:** In this experiment, we discussed about NAND gate. From the truth table, we came to know that NAND gate's output is complement to the output of an AND gate. Besides, a low output(0) is found only if all the inputs to the gate are high(1) and if any input is low(0), a high output(1) results.