RAJSHAHI UNIVERSITY OF ENGINEERING AND TECHNOLOGY

LAB REPORT - 04

COURSE NAME: SESSIONAL BASED ON CSE 2103
COURSE CODE: CSE 2104

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SUBMISSION DATE -3 JULY,2021

5.1) Experiment Name: Verify the Half Adder Circuit.

Objectives:

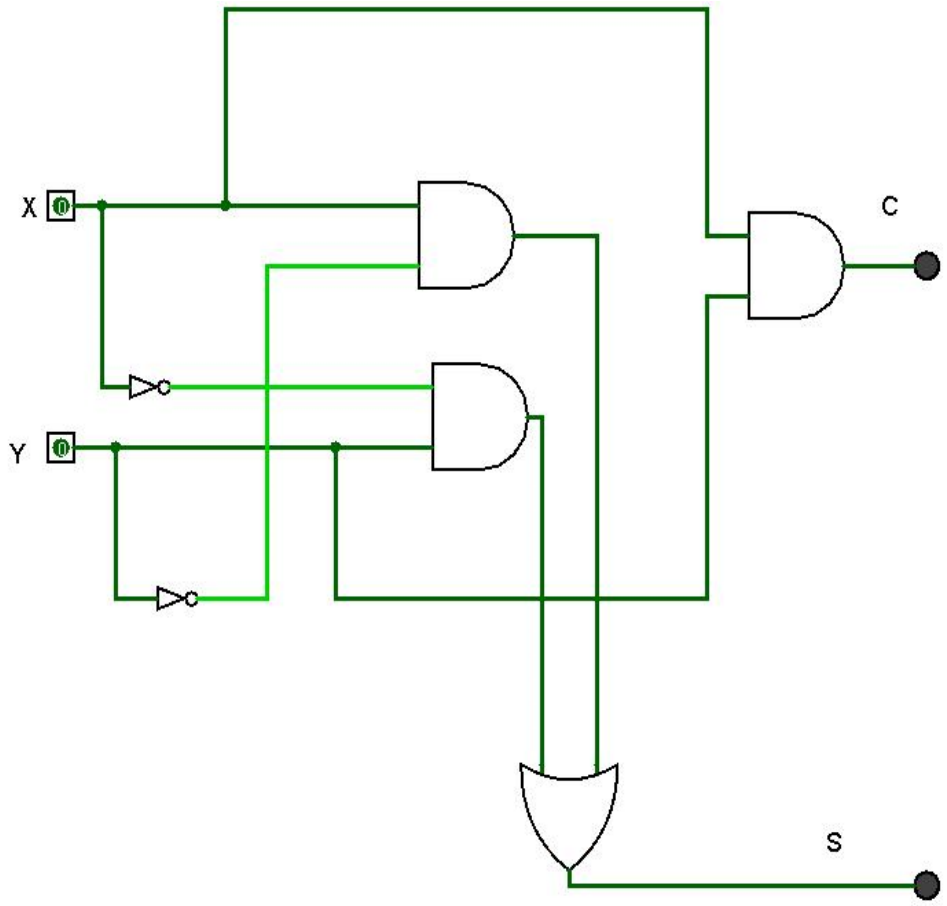
- To learn the properties of Half Adder Circuit.
- To know the different implementation ways of Half Adder Circuit.
- To draw the diagram of Half Adder Circuit.
- To write the Boolean expression for Half Adder Circuit.
- To generate the truth table of a Half Adder Circuit.

Theory: A combinational circuit that performs the addition of two bits is called a Half Adder Circuit.The Half Adder is able to add two single binary digits and provide the output plus a carry value.It has two inputs x and y, and two outputs S (sum) and C (carry).The common representation uses a XOR gate and an AND gate.
Using basic gates:
S = x^y + xy^
C = xy
Using the universal gates:
S = x ⊕ y
C = xy

Experimental Analysis:

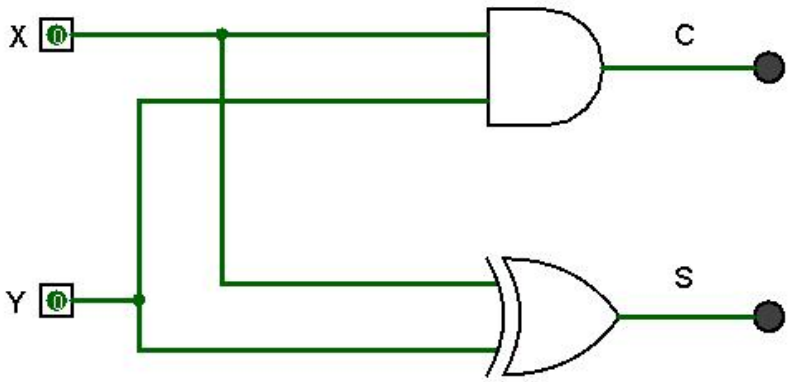
- **Circuit Diagram:**

5.1.1- The Half Adder Circuit(Using Basic Gates)



5.1.1 The Half Adder Circuit(using the basic gates)

5.1.2- The Half Adder Circuit(Using Universal Gates)



5.1.2 The Half Adder Circuit(using the universal gates)

- **Truth Table:**

X	Y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Conclusion: In this experiment,we discussed about Half Adder Circuit using both basic gates and universal gates.The truth table shows the exact result in both ways of implementation.

5.2) Experiment Name: Verify the Full Adder Circuit.

Objectives:

- To learn the properties of Full Adder Circuit.
- To know the different implementation ways of Full Adder Circuit.
- To draw the diagram of Full Adder Circuit.
- To write the Boolean expression for Full Adder Circuit.
- To generate the truth table of a Full Adder Circuit.

Theory: A combinational circuit that is able to add three single binary digits and provide the output and a carry value is called a Full Adder Circuit. It has three inputs x,yand z, and two outputs S (sum) and C (carry).The common representation uses three AND gate,an OR gate and a XOR gate.

Using basic gates:

S = x^y^z + x^yz^ + xy^z^ + xyz

C = xy + xz + yz

Using the universal gates:

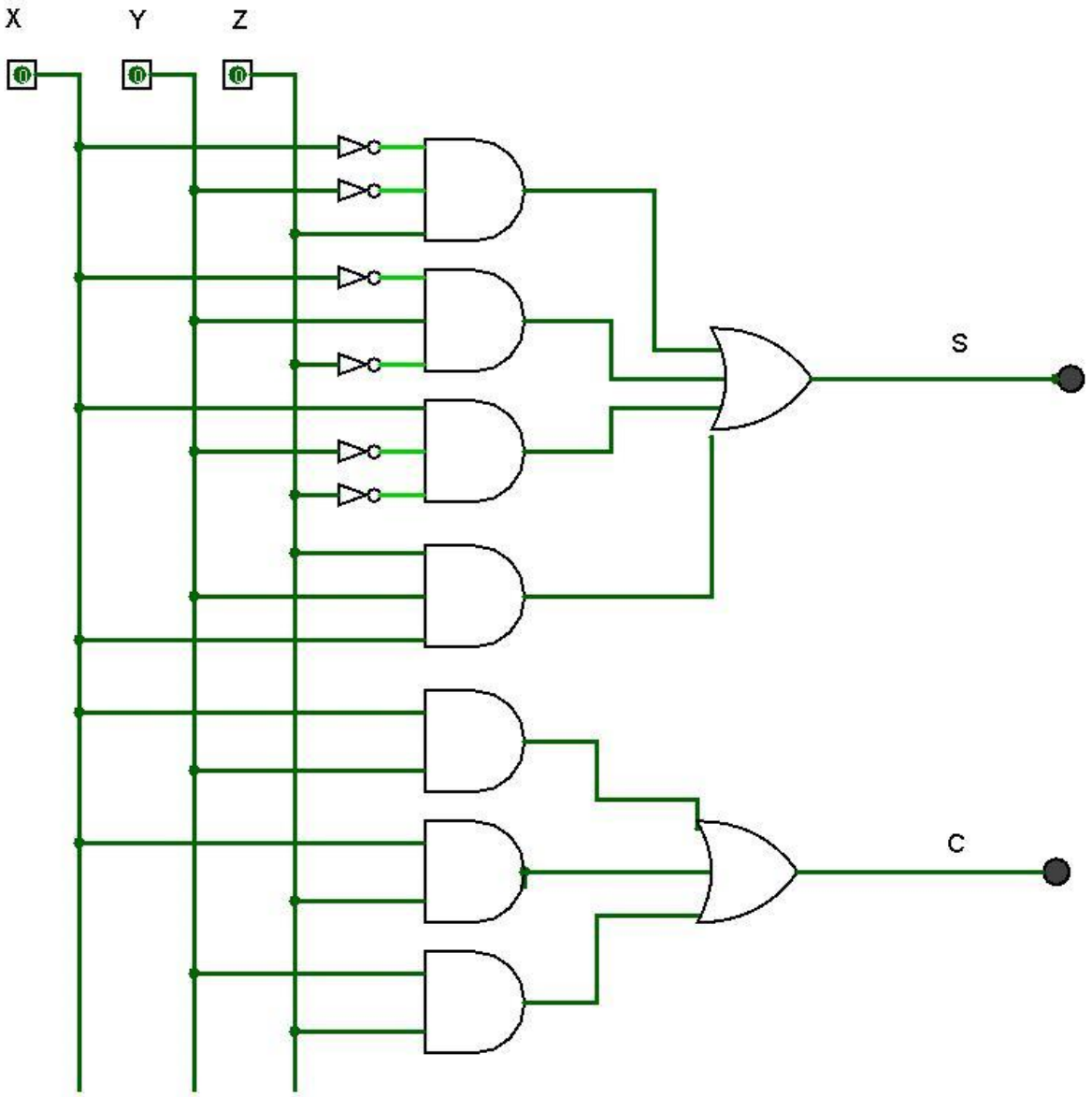
S = (x ⊕ y) ⊕ z

C = xy + yz + zx

Experimental Analysis:

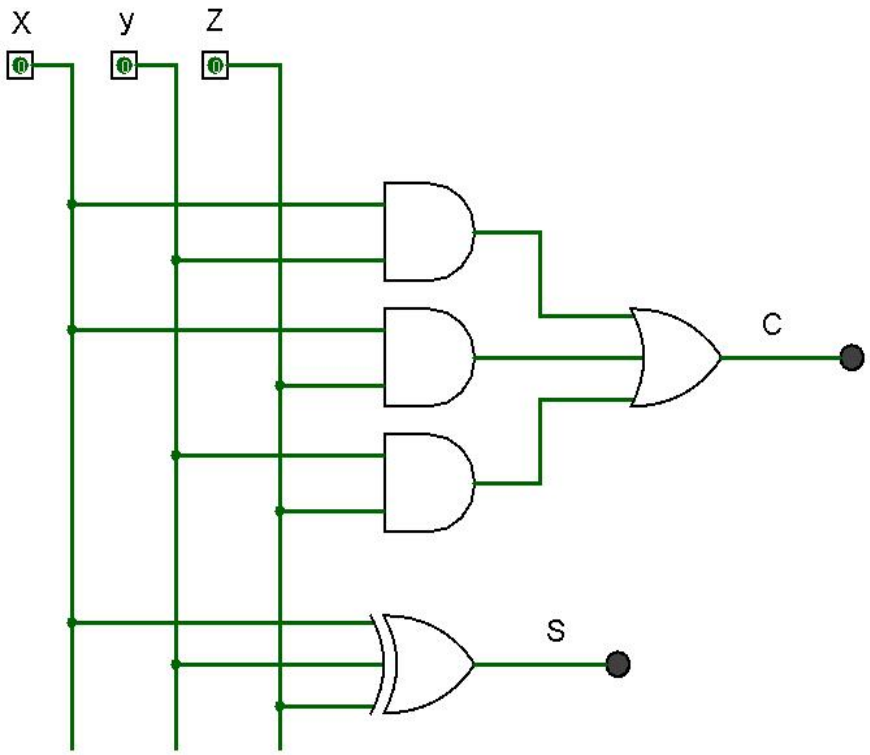
- **Circuit Diagram:**

5.2.1- The Full Adder Circuit(Using Basic Gates)



5.2.1 The Full Adder Circuit(using the basic gates)

5.1.2- The Full Adder Circuit(Using Universal Gates)



5.2.2 The Full Adder Circuit(using the universal gates)

- **Truth Table:**

X	Y	Z	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Conclusion: In this experiment,we discussed about Full Adder Circuit using both basic gates and universal gates.The truth table shows the exact result in both ways of implementation.

5.3) Experiment Name: Implement the Full Adder Circuit by using Half Adder Circuit and verify the result.

Objectives:

- To draw the diagram of Full Adder Circuit using Half Adder Circuit.
- To generate the truth table of a Full Adder Circuit.
- To verify the result of the implemention.

Theory: A combinational circuit that is able to add three single binary digits and provide the output and a carry value is called a Full Adder Circuit. It has three inputs x,yand z, and two outputs S (sum) and C (carry).The common representation uses three AND gate,an OR gate and an XOR gate.

Using basic gates:

S = x^y^z + x^yz^ + xy^z^ + xyz

C = xy + xz + yz

Using the universal gates:

S = (x ⊕ y) ⊕ z

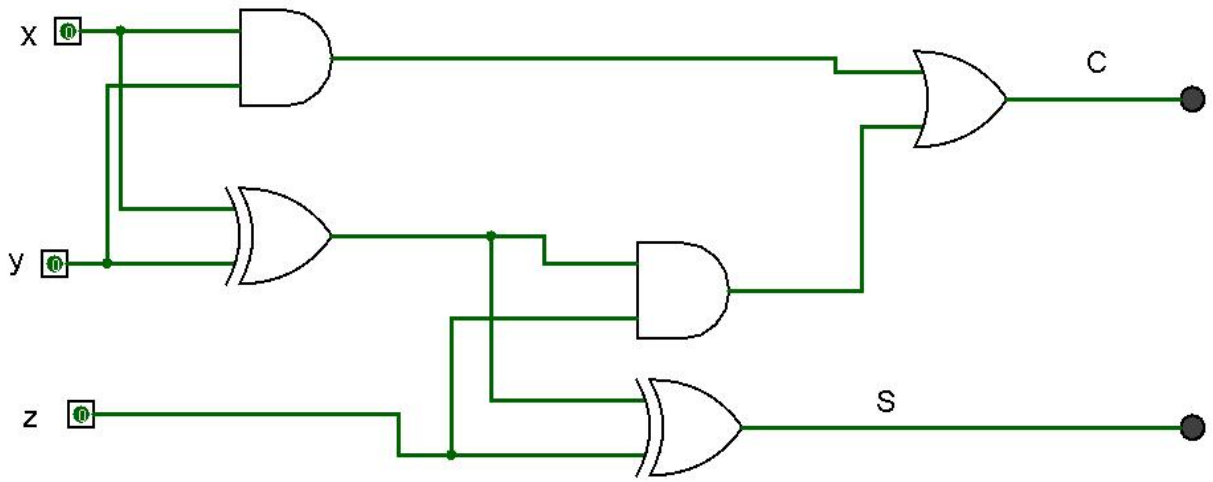
C = xy + yz + zx

A Full Adder Circuit can be respented using two Half Adder Circuits and an OR gate.

Experimental Analysis:

- **Circuit Diagram:**

5.3- The Full Adder Circuit Using Half Adder Circuit



5.3 The Full Adder Circuit by Using Half Adder

Truth Table:

X	Y	Z	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Conclusion: In this experiment,we discussed about Full Adder Circuit using Half Adder Circuit.The truth table shows the exact result of implementation.