RAJSHAHI UNIVERSITY OF ENGINEERING AND TECHNOLOGY

LAB REPORT - 07

COURSE NAME: SESSIONAL BASED ON CSE 2103
COURSE CODE: CSE 2104

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SUBMISSION DATE -7 AUGUST,2021

8.1) Experiment Name: Verify SR Flip-Flop by using Module.

Objectives:

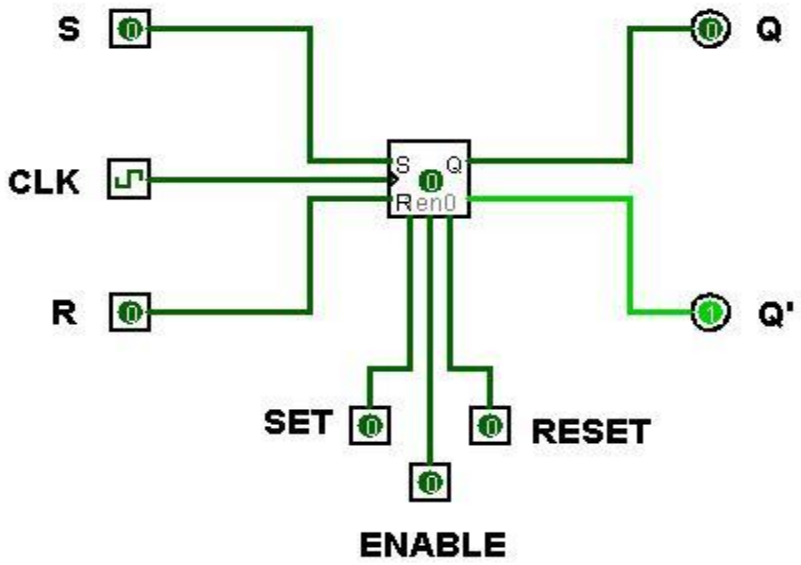
- To know the characteristics of SR flip-flop.
- To know how to draw SR flip-flop using Module.
- To generate the truth table of SR flip-flop using Module.
- To verify the output of SR flip-flop.

Theory: SR flip-flop is the simplest possible memory element which is formed by two NAND gates or two NOR gates.The inputs S and R are known as the SET and RESET inputs.The outputs Q and Q' are complements of each other.They are referred to as the normal and complementary outputs.
In case of SR FF using module in Logisim,when the clock triggers,the value is remembered by the flip-flop & that remains unchanged when S and R are both 0, becomes HIGH if the S input is HIGH and becomes LOW if the R input is HIGH.When both inputs are 1, the value in the flip flop remains unchanged in logisim.

Experimental Analysis:

- **Circuit Diagram:**

8.1- Verifying SR Flip-Flop by using Module :



8.1: SR FF using module

- **Truth Table:**

S	R	Q
0	0	Unchanged
0	1	0
1	0	1
1	1	Invalid

Conclusion: In this experiment,we discussed about SR Flip-Flop by using Module.Logism shows same output as the table.

8.2) Experiment Name: Verify JK Flip-Flop by using Module.

Objectives:

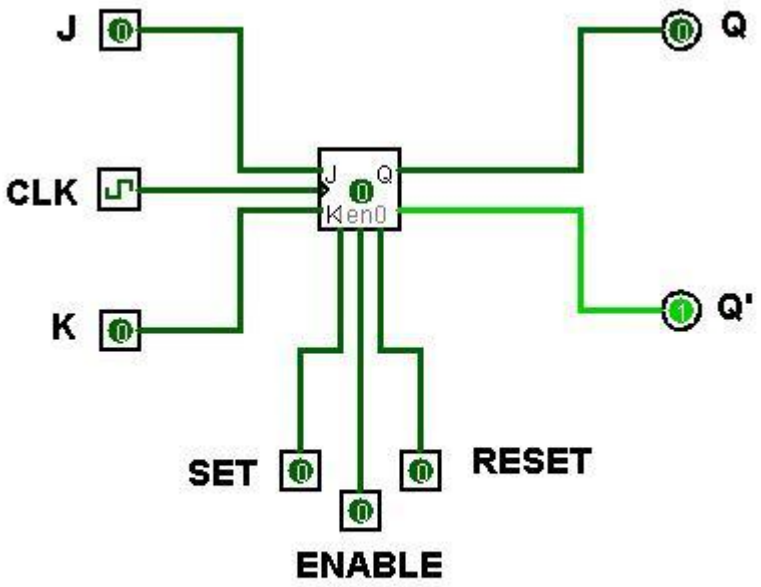
- To know the characteristics of JK flip-flop.
- To know how to draw JK flip-flop using Module.
- To generate the truth table of JK flip-flop using Module.
- To verify the output of JK flip-flop.

Theory: J-K flip-flop is the most versatile of the basic flip-flops which is formed by two NAND gates or two NOR Gates.It has two data inputs J and K & clock pulse input. It has no undefined state.
In case of JK flip-flop module in Logisim,when the clock triggers,the value is remembered by the flip-flop toggles if the J and K inputs are both HIGH,remains the same if the inputs are both LOW,if they are different,then the value becomes HIGH if the K input is LOW and HIGH if the J input is HIGH.

Experimental Analysis:

- **Circuit Diagram:**

8.2- Verifying JK Flip-Flop by using Module :



8.2: JK FF using module

- **Truth Table:**

J	K	Q
0	0	Unchanged
0	1	0
1	0	1
1	1	Toggled

Conclusion: In this experiment,we discussed about JK Flip-Flop by using Module. Logism shows same output as the table.

8.3) Experiment Name: Verify D Flip-Flop by using Module

Objectives:

- To know the characteristics of D flip-flop.
- To know how to draw D flip-flop using Module.
- To generate the truth table of D flip-flop using Module.
- To verify the output of D flip-flop.

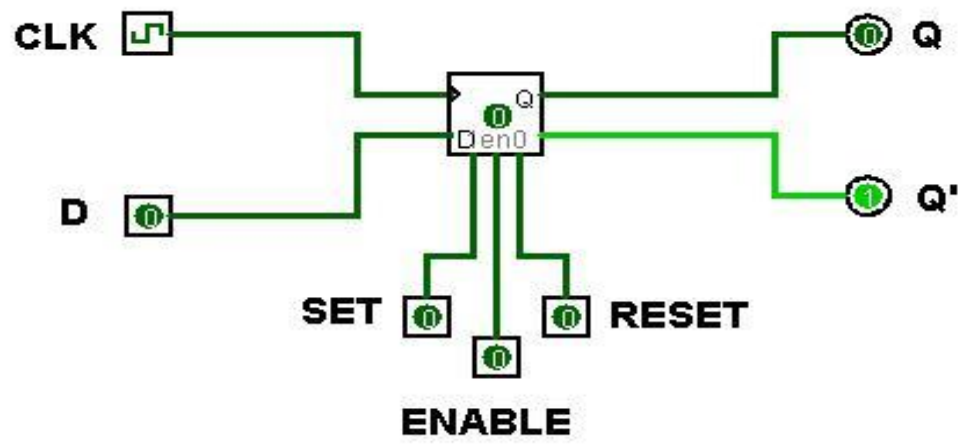
Theory: The D-type flip-flop is a modified Set-Reset flip-flop with the addition of an inverter to prevent the S and R inputs from being at the same logic level.

Output changes to the value of the input at either the positive-or negative-going clock trigger.

Experimental Analysis:

- **Circuit Diagram:**

8.3- Verifying D Flip-Flop by using Module :



8.3: D FF using module

- **Truth Table:**

D	Q
0	0
1	1

Conclusion: In this experiment,we discussed about D Flip-Flop by using Module.Whenever the clock signal is LOW, the input is never going to affect the output state.

7.4) Experiment Name: Verify T Flip-Flop by using NOR & NAND Latch.

Objectives:

- To know the characteristics of T flip-flop.

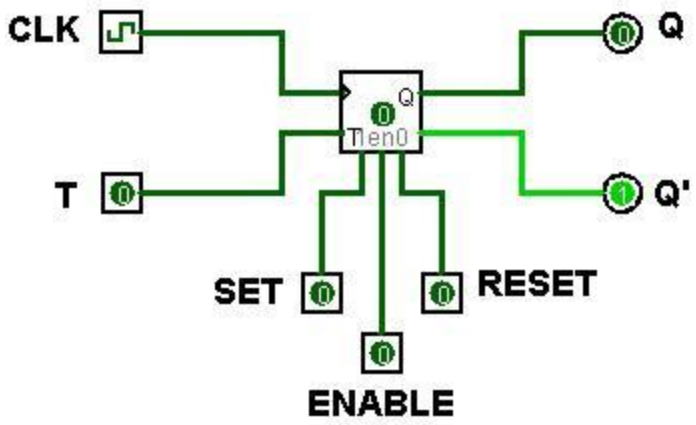
- To know how to draw T flip-flop using Module.
- To generate the truth table of T flip-flop by using Module.
- To verify the output of T flip-flop.

Theory: T flip flop is modified form of JK flip-flop making it to operate in toggling region. A T flip flop is constructed by connecting J and K inputs,creating a single input called T. Hence why a T flip flop is also known as a single input JK flip flop.

Experimental Analysis:

- **Circuit Diagram:**

8.4- Verifying T Flip-Flop by using Module:



8.4: T FF using module

- **Truth Table:**

T	Q
0	Unchanged
1	Toggled

Conclusion: In this experiment,we discussed about T Flip-Flop by using NOR & NAND Latch**.**Whenever the clock signal is LOW, the input is never going to affect the output state.