RAJSHAHI UNIVERSITY OF ENGINEERING AND TECHNOLOGY

LAB REPORT - 08

COURSE NAME: SESSIONAL BASED ON CSE 2103
COURSE CODE: CSE 2104

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9.1) Experiment Name: Design a 3-bit Asynchronous Counter by using JK Flip-Flops.

Objectives:

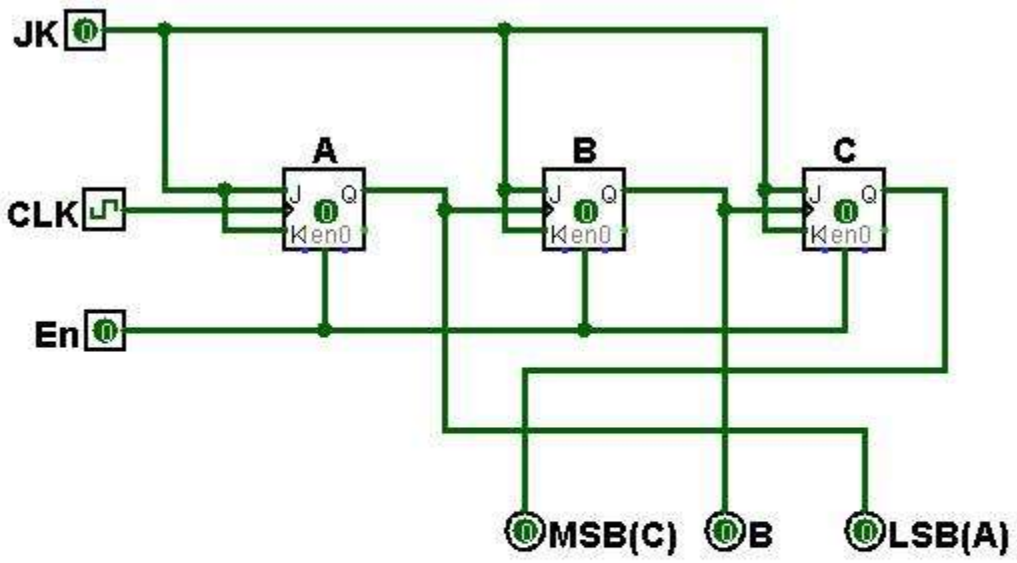
- To know the characteristics of a 3-bit Asynchronous Counter
- To know how to draw a 3-bit Asynchronous Counter by using JK Flip-Flops.
- To generate the truth table of 3-bit Asynchronous Counter by using JK Flip-Flops.
- To verify the output of 3-bit Asynchronous Counter.

Theory: Asynchronous counters are those whose output is free from the clock signal because the flip flops in asynchronous counters are supplied with different clock signals.Asynchronous stands for the absence of synchronization.

Experimental Analysis:

- **Circuit Diagram:**

9.1- Designing a 3-bit Asynchronous Counter by using JK Flip-Flops :



9.1: 3-bit Asynchronous Counter using JK FF

- **Circuit Excitation Table:**

Present State			Next State			Flip-Flop Input					
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	X	0	0	X	1	X
0	0	1	0	1	0	X	1	1	X	X	1
0	1	0	0	1	1	X	X	X	0	1	X
0	1	1	1	0	0	X	X	X	1	X	1
1	0	0	0	0	0	1	0	0	X	0	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X	X

Conclusion: In this experiment,we discussed about a 3-bit Asynchronous Counter by using JK Flip-Flops.An Asynchronous counter can count $\mathbf{2^n - 1}$ possible counting states.

9.2) Experiment Name: Design a 3-bit Synchronous Counter by using various Flip-Flops.

Objectives:

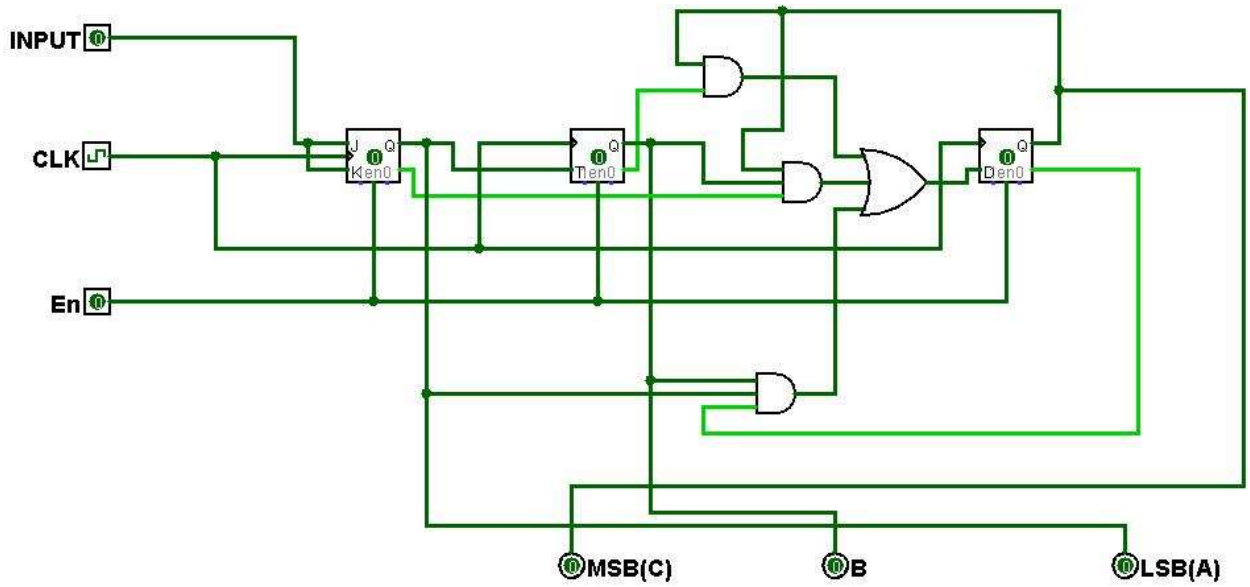
- To know the characteristics of a 3-bit Synchronous Counter.
- To know how to draw a 3-bit Synchronous Counter by using various Flip-Flops.
- To generate the truth table of 3-bit Synchronous Counter by using various Flip-Flops.
- To verify the output of 3-bit Synchronous Counter.

Theory: Synchrounous generally refers to something which is cordinated with others based on time.Synchronous signals occur at same clock rate and all the clocks follow the same reference clock.In a nutshell,we can say that If the "clock" pulses are applied to all the flip-flops in a counter simultaneously, then such a counter is called as synchronous counter.

Experimental Analysis:

- **Circuit Diagram:**

9.2- Designing a 3-bit Synchronous Counter by using various Flip-Flops :



9.2: 3-bit Synchronous Counter using various(JK,T,D) FF

- **Circuit Excitation Table:**

Present State			Next State			Flip-Flop Input			
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	D_C	T_B	J_A	K_A
0	0	0	0	0	1	0	0	1	X
0	0	1	0	1	0	0	1	X	1
0	1	0	0	1	1	0	0	1	X
0	1	1	1	0	0	1	1	X	1
1	0	0	1	0	1	1	0	1	X
1	0	1	1	1	0	1	1	X	1
1	1	0	1	1	1	1	0	1	X
1	1	1	0	0	0	0	1	X	1

Conclusion: In this experiment,we discussed about a 3-bit Synchronous Counter by using various Flip-Flops.