README - 4-Bit ALU Project

Project Title

4-Bit ALU - Digital System Design Project

Overview

This project implements a 4-bit Arithmetic Logic Unit (ALU) in Verilog HDL, designed as part of my learning from the NPTEL Digital System Design course. The ALU performs basic arithmetic and logic operations and is fully testable using simulation tools like ModelSim or Xilinx ISE.

Features

Inputs: A[3:0], B[3:0], Sel[2:0]

Output: Result[3:0]

Supported Operations:

- 000: Addition (A + B)
- 001: Subtraction (A - B)
- 010: Bitwise AND (A & B)
- 011: Bitwise OR (A | B)
- 100: Bitwise XOR (A ^ B)
- 101: Bitwise NOT (~A)
- 110: Increment A
- 111: Decrement A

File Structure

/src/ -> Contains ALU_4bit.v (main module)

/testbench/ -> Contains test_ALU.v (testbench)

/screenshots/ -> Optional waveform outputs

4bit_ALU_Project_Sravani.pdf -> Project report with diagrams and code

README.md -> This file

Tools Used

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- Verilog HDL

- ModelSim / Xilinx ISE / EDAPlayground

- GitHub for version control and sharing

How to Run

1. Clone/download the repo

2. Open the Verilog files in a simulator

3. Compile and run `test_ALU.v`

4. Observe waveform to verify ALU operations

Future Improvements

- 8-bit ALU version

- Pipelined ALU

- Include overflow/carry out flag support

- FPGA implementation with switches and LEDs

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Learning from: NPTEL Digital System Design