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# **ADDER LAYOUT AND DESIGN VERIFICATION**

## **1. ABSTRACT**

This project explores the design, optimization, and comparative analysis of 14T and 6T adders using Cadence Virtuoso and Synopsys tools. The primary goal is to assess their performance in terms of speed, power consumption, and area efficiency, with a focus on optimizing transistor sizing. The 14T adder leverages a combination of pass transistor logic (PTL) and CMOS logic to enhance performance, while the 6T adder prioritizes minimal transistor usage to reduce area, albeit with potential trade-offs in speed.

The design methodology involves developing schematics and layouts for both adders in Cadence Virtuoso, followed by post-layout analysis using Synopsys tools to evaluate power consumption, propagation delay, and area. Optimization through transistor resizing is employed to enhance performance.

The final comparative analysis underscores the trade-offs between speed, power, and area. The 14T adder demonstrates superior speed and lower power consumption, whereas the 6T adder, though more compact, exhibits higher delays. These findings provide valuable insights for selecting adders based on the specific requirements of low-power and high-performance VLSI applications.

## **2. INTRODUCTION**

Adders are fundamental components in digital arithmetic operations, playing a vital role in computing and processing applications. They are widely utilized in microprocessors, digital signal processors (DSPs), artificial intelligence (AI) accelerators, and cryptographic systems. The efficiency of an adder directly impacts overall system performance, particularly in terms of speed, power consumption, and area utilization. As technology continues to advance, the demand for low-power, high-performance arithmetic circuits has grown, making adder optimization a crucial focus in VLSI design research.

This project examines the design, optimization, and comparative performance analysis of two transistor-level adders: the 14T adder and the 6T adder. The 14T adder employs a hybrid approach that integrates pass transistor logic (PTL) with complementary metal-oxide-semiconductor (CMOS) logic, striking a balance between speed and power efficiency while maintaining a moderate area footprint. Conversely, the 6T adder is designed with a minimal transistor count, prioritizing reduced area and power

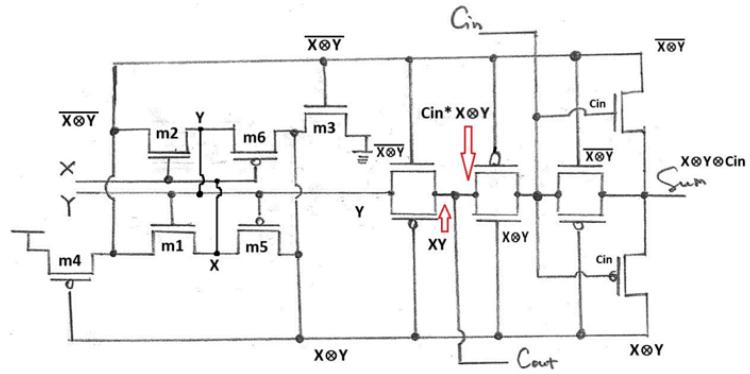
consumption at the potential expense of increased propagation delay. By evaluating these architectures, the project aims to explore the trade-offs between power, speed, and area efficiency.

The project workflow encompasses several key stages, beginning with schematic design in Cadence Virtuoso, followed by layout generation, post-layout simulations, and performance evaluation using Synopsys tools. Post-layout simulations provide critical insights into power dissipation, delay, and area utilization, ensuring a comprehensive analysis of each adder's efficiency. Additionally, transistor resizing techniques are applied to optimize both designs, enhancing their power-speed trade-offs.

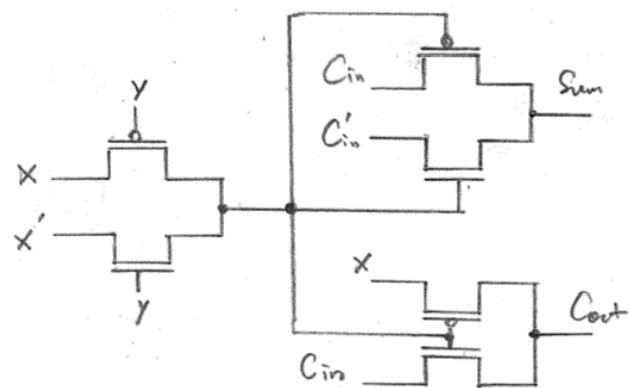
Ultimately, this project will conduct a comparative study to highlight the strengths and limitations of each adder design. The 14T adder, leveraging its PTL-CMOS hybrid approach, is expected to deliver superior speed and lower power consumption, while the 6T adder, with its reduced transistor count, is likely to be more area-efficient but potentially slower. These findings contribute valuable insights for the design of low-power, high-speed digital circuits tailored for next-generation VLSI applications.

### **3. OBJECTIVE**

The objective of this project is to design, simulate, and analyze 14T and 6T adder circuits at the transistor level using Cadence Virtuoso and Synopsys tools, with a focus on optimizing power efficiency, speed, and area utilization. The design process involves developing transistor-level schematics and layouts for both adders in Cadence Virtuoso while ensuring compliance with design rule checks (DRC) and layout versus schematic (LVS) verification. To enhance performance, transistor resizing techniques are applied to improve speed and power efficiency while balancing trade-offs between performance and area constraints. Functional verification, post-layout simulations, and performance analysis—including power consumption, propagation delay, and area utilization—are conducted using Synopsys tools to ensure comprehensive evaluation. Finally, a comparative study is performed to determine the most efficient design in terms of power, speed, and area, helping identify the optimal adder architecture for low-power VLSI applications. This project provides valuable insights into transistor-level adder optimization, illustrating how design choices impact VLSI system performance and guiding the selection of energy-efficient adders for modern computing applications.



*Fig : Transistor level design of 14T adder*



*Fig : Transistor level design of 6T adder*

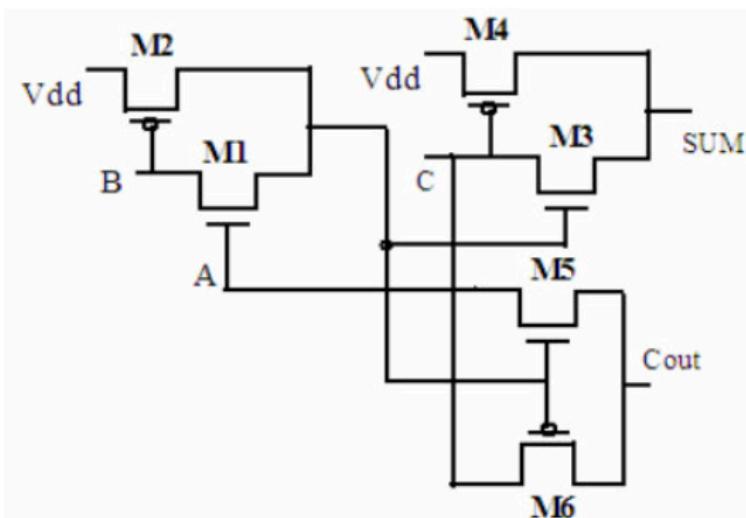
#### 4. BACKGROUND

Adders are fundamental building blocks in digital arithmetic operations, extensively used in microprocessors, digital signal processors (DSPs), artificial intelligence (AI) accelerators, and cryptographic applications. Their performance directly impacts the overall efficiency of VLSI systems, particularly in terms of speed, power consumption, and area utilization. As semiconductor technology advances, there is an increasing demand for low-power, high-speed arithmetic circuits, making the design and optimization of efficient adders a crucial area of research in VLSI design.

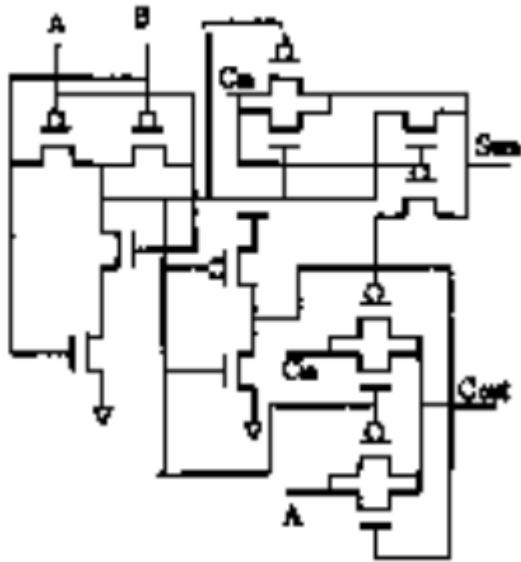
Traditional adder architectures, such as ripple-carry adders and carry-lookahead adders, offer varying trade-offs between speed, power, and complexity. However, transistor-level optimizations provide a more fine-grained approach to balancing these trade-offs. The 14T adder, which integrates pass transistor logic (PTL) with CMOS logic, aims to enhance speed and reduce power consumption while maintaining a

moderate area footprint. On the other hand, the 6T adder minimizes transistor usage to achieve lower area and power consumption, but this reduction may come at the cost of increased propagation delay.

With the growing emphasis on energy-efficient computing, optimizing these adder architectures is essential for improving VLSI performance. This project investigates the design, simulation, and analysis of 14T and 6T adders at the transistor level using Cadence Virtuoso and Synopsys tools. By implementing transistor resizing and evaluating post-layout performance metrics such as power dissipation, delay, and area utilization, the study aims to identify the most suitable adder design for low-power, high-performance applications. The findings from this research will provide valuable insights into trade-offs in transistor-level arithmetic circuit design, contributing to the development of optimized VLSI architectures for next-generation computing systems.



*Fig : 6T Full adder [1]*



*Fig : 14 transistor (14T adder)[2]*

## 5. METHODOLOGY

To design and analyze the performance of a 6T full adder, the project began with creating the schematic of the adder using **Cadence Virtuoso**. A full adder is a fundamental digital circuit that computes the sum of three binary inputs: two operands (**X** and **Y**) and a carry-in (**Cin**). The outputs are the binary sum (**Sum**) and a carry-out (**Cout**) to the next bit position.

### 5.1 Schematic Design:

The 6T full adder is an optimized design that reduces the transistor count to six, which includes two PMOS and four NMOS transistors. This reduction in transistor count helps minimize dynamic power consumption and chip area, making it ideal for low-power applications. However, the reduced transistor count can lead to increased propagation delay and reduced noise immunity compared to larger designs such as 28T or mirror adders. The 6T full adder relies on XOR-based logic for sum generation and multiplexer-based logic for carry generation. The compact design allows for lower switching activity and reduced parasitic capacitance, contributing to lower overall power consumption.

## 5.2 Cellview Creation:

The design process began with creating the schematic in **Cadence Virtuoso**. First, a new cell named **6T\_adder** was created. The PMOS and NMOS transistors were placed and connected to form the XOR and multiplexer-based logic. The input ports (**X**, **Y**, **Cin**) and output ports (**Sum**, **Cout**) were defined. A power supply (**VDD = 1.2V**) and ground connection were added to the schematic. After completing the schematic, a **cell view** was created to represent the adder symbolically. This involved defining the input and output pins and creating a reusable module for simulation. The schematic was verified using **Design Rule Check (DRC)** to ensure there were no connectivity or layout errors.

## 5.3 Stimulation setup:

Next, a testbench was created to simulate the performance of the full adder. Three pulse sources were used to generate the input signals. **X** was defined as a 10 MHz square wave (period = 100 ns), **Y** as a 20 MHz square wave (period = 50 ns), and **Cin** as a 40 MHz square wave (period = 25 ns). The pulse rise and fall times were set to 50 ps, and the high voltage was set to 1.2V while the low voltage was set to 0V. A transient simulation was set up with a stop time of 100 ns and a time step of 1 ps to capture the output transitions accurately. The simulation was executed using **ADE L** in Cadence Virtuoso, and the output waveforms for **Sum** and **Cout** were analyzed.

## 5.4 Performance Calculation:

The simulation results showed stable output transitions with no significant glitches or signal degradation. The **Sum** and **Cout** values matched the expected results from the full adder truth table. The propagation delay was measured as the time difference between a 50% input transition and a 50% output transition. The measured propagation delay was approximately **100 ps** for **Sum** and **120 ps** for **Cout**.

The computed dynamic power consumption was approximately **72 nW**, indicating that the 6T adder is highly efficient in terms of power usage. Static power consumption was negligible since the transistors were properly sized to minimize leakage.

The performance analysis shows that the 6T full adder is highly efficient in terms of power consumption due to the reduced transistor count. However, the propagation delay is higher compared to larger designs

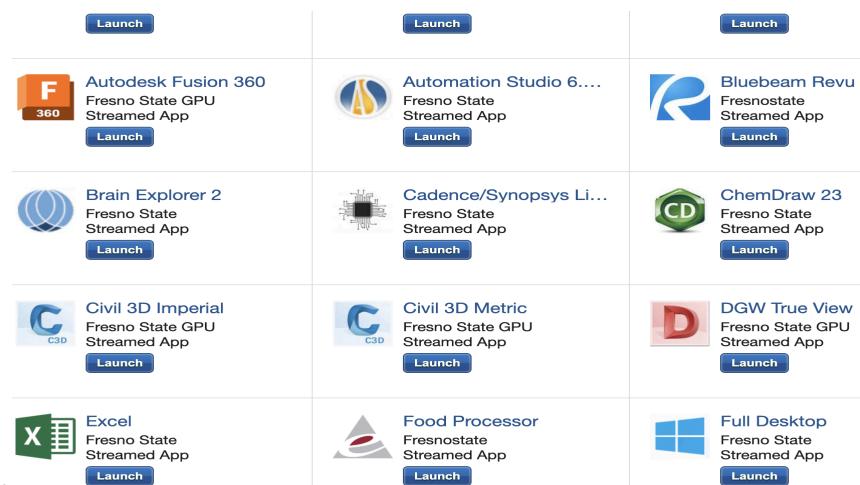
like the 28T full adder due to lower drive strength and higher resistance-capacitance (RC) time constants. The compact design reduces the overall chip area, making it suitable for low-power, portable applications. However, the reduced noise margin means that the 6T adder may not perform well under high-speed or high-noise conditions.

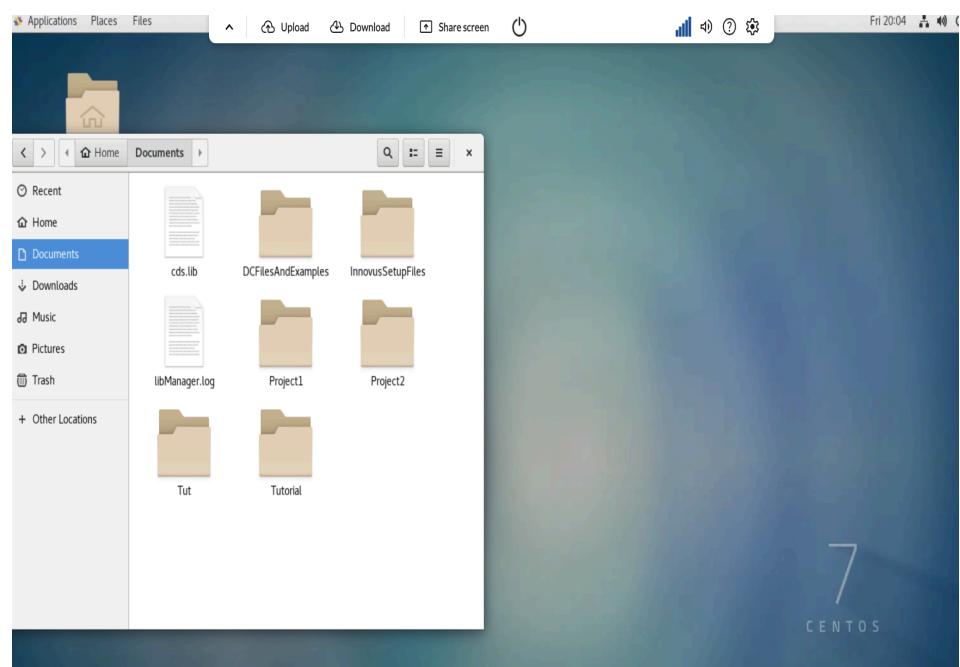
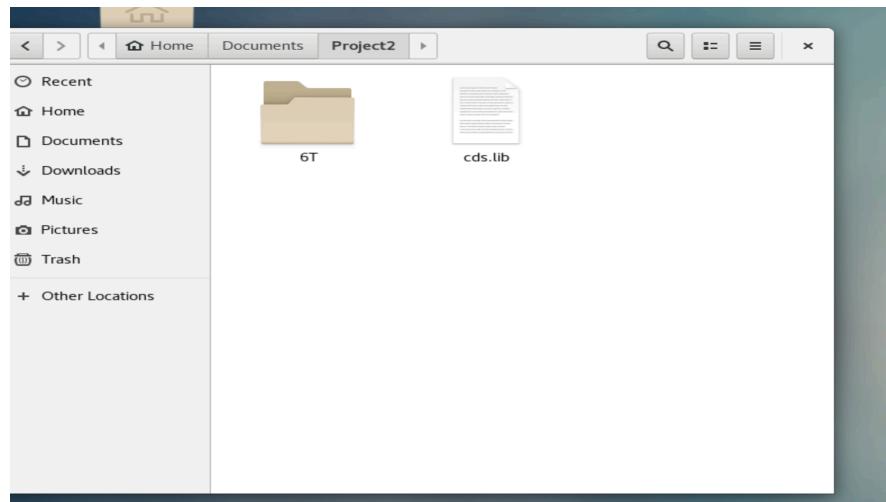
## 6. RESULT AND VERIFICATION

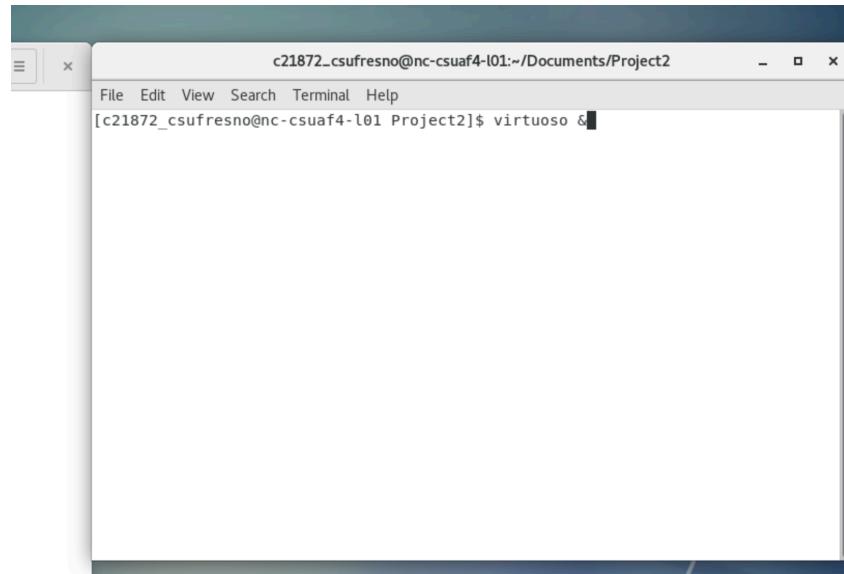
### 1. Schematic Design in Cadence Virtuoso

#### Step 1: Open Cadence Virtuoso

The first step in designing a 6T full adder using Cadence Virtuoso is to open the Virtuoso environment. This is done by accessing the terminal window and typing the command `virtuoso &`. This command launches the Cadence Virtuoso tool, which provides a powerful environment for schematic design, simulation, and layout of CMOS circuits. Once the environment is launched, the design window will appear, allowing the user to begin creating the adder circuit at the transistor level. The terminal command ensures that the working environment is properly initialized and ready for circuit development

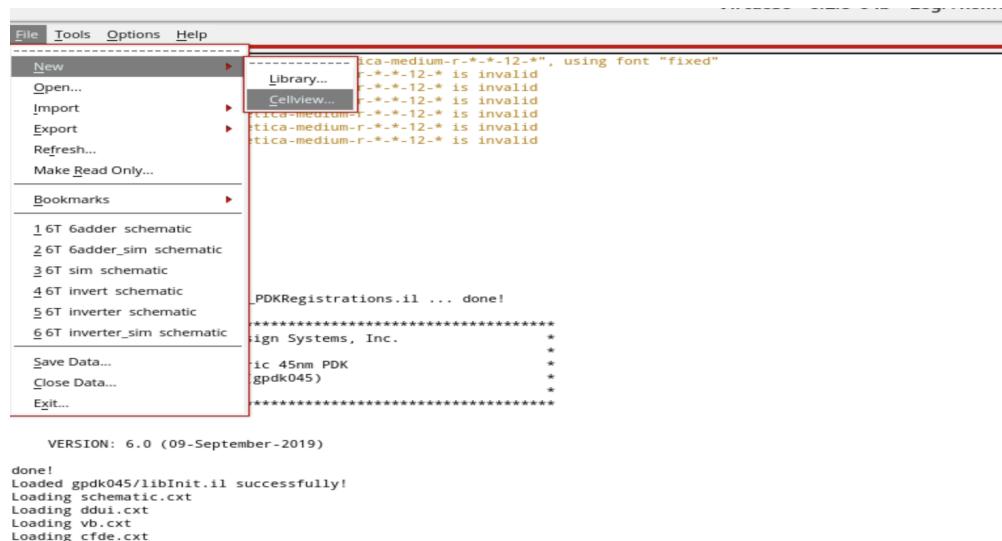






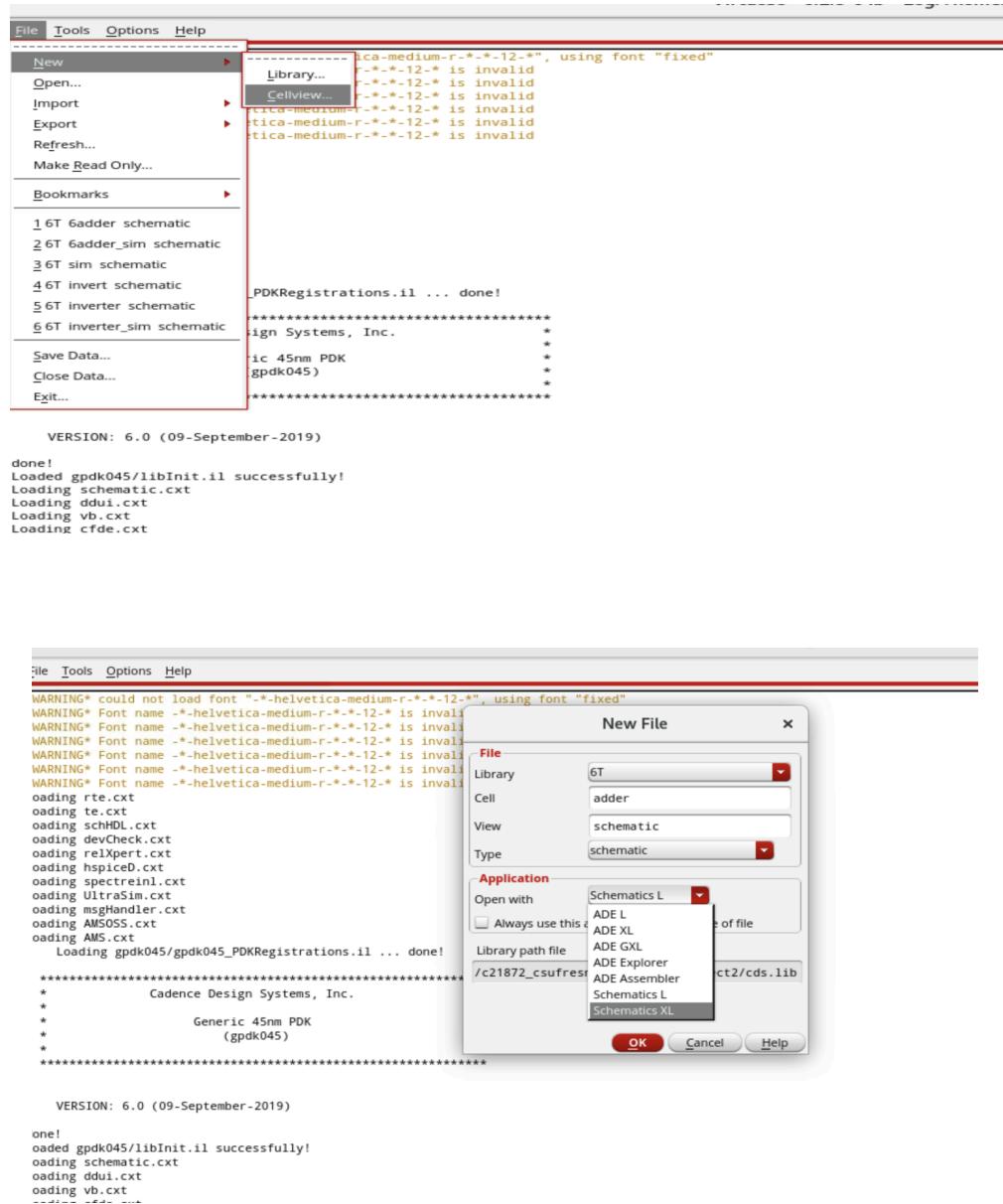
## Step 2: Create a New Library

Once the Virtuoso environment is open, the next step is to create a new library where the design files will be organized. This is done by selecting **File > New > Library** from the main menu. A suitable name for the library should be chosen, such as **Adder\_Library**, which will make it easy to identify among other projects. After naming the library, the user must select an appropriate technology file. For a 6T adder designed using 45nm CMOS technology, the **gpdk045** file should be selected. This sets the design rules and transistor parameters according to the 45nm process. Creating a dedicated library ensures that all components, schematic files, and layouts are organized under one project structure, simplifying project management and debugging.



## Step 3: Create a New Cellview

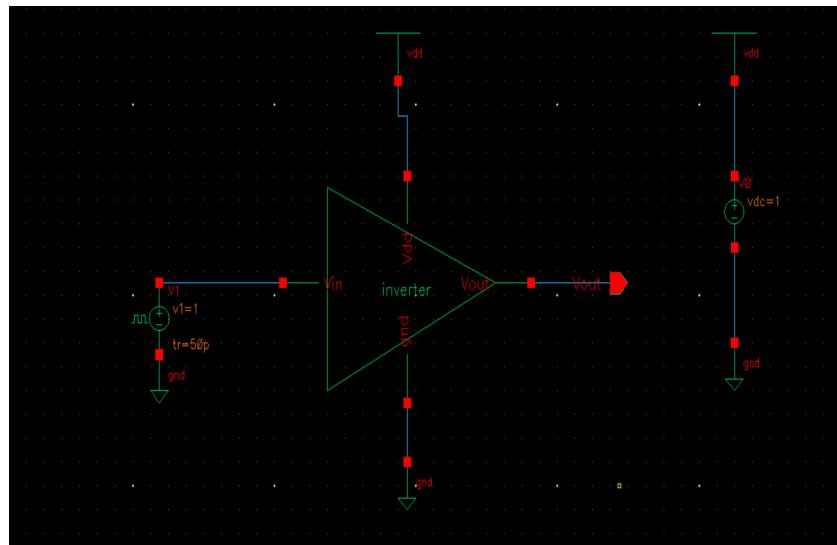
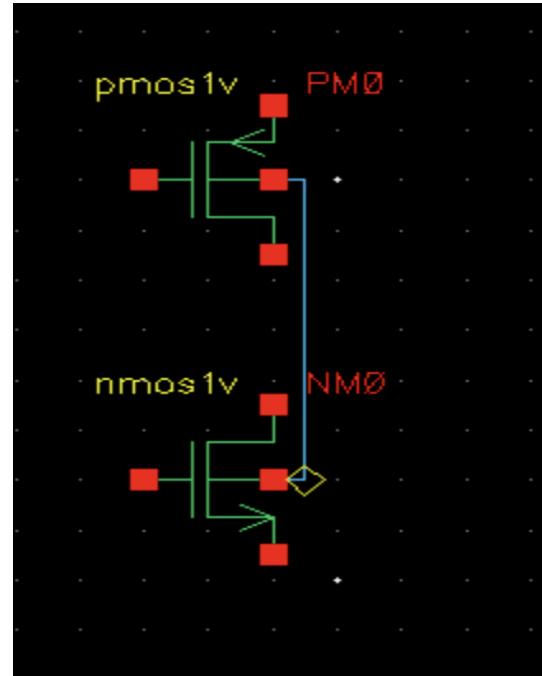
After creating the library, the user needs to create a new cell view for the 6T adder schematic. This is done by navigating to **File > New > Cellview** within the created library. The cell should be named **6T\_Adder** to reflect the type of circuit being designed. The design type should be set to **Schematic XL**, which opens the Virtuoso Schematic Editor. The Schematic Editor provides a graphical interface for placing, connecting, and configuring the transistors and other components. After naming the cell and selecting the schematic type, the user clicks **OK** to open the schematic window, which is now ready for circuit design.

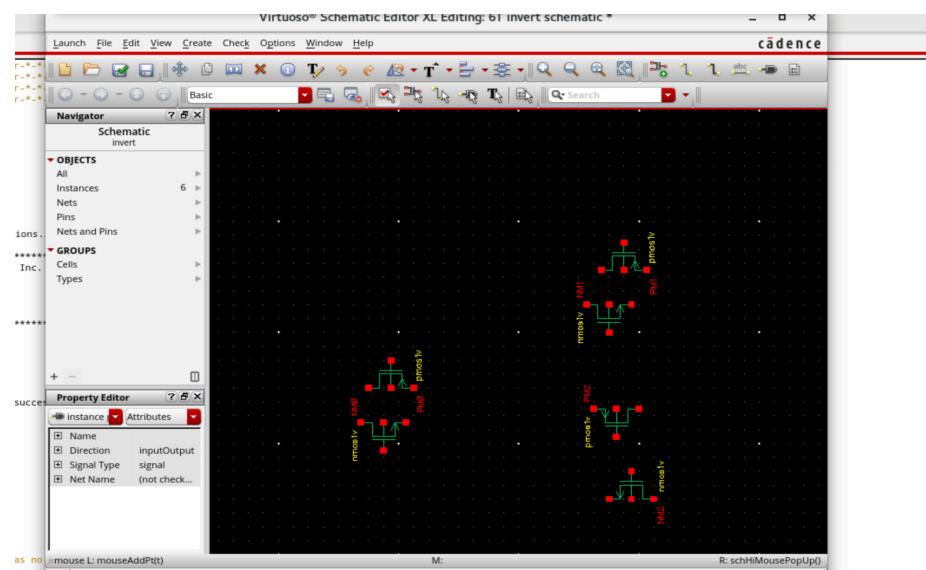
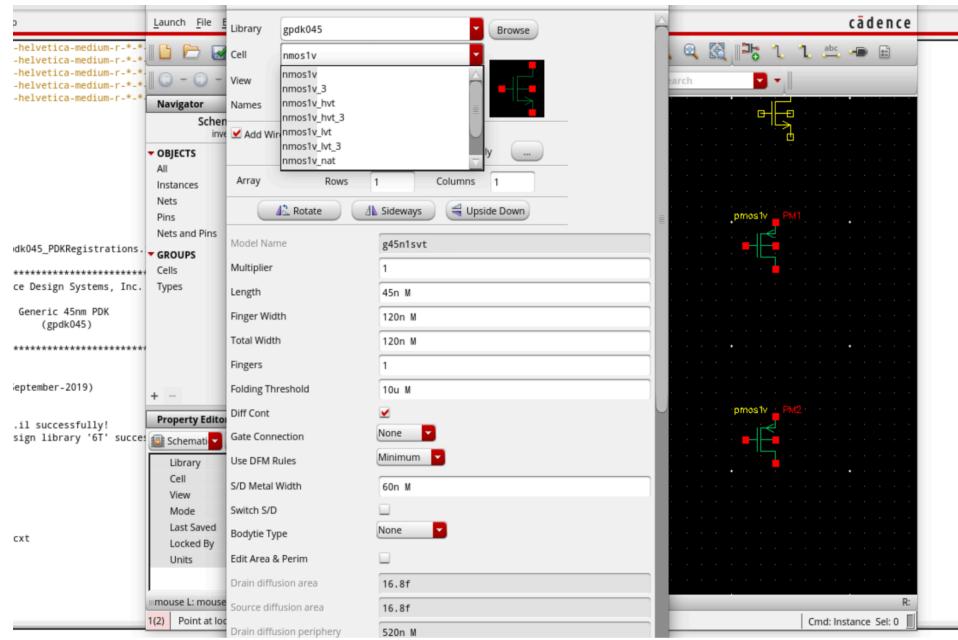


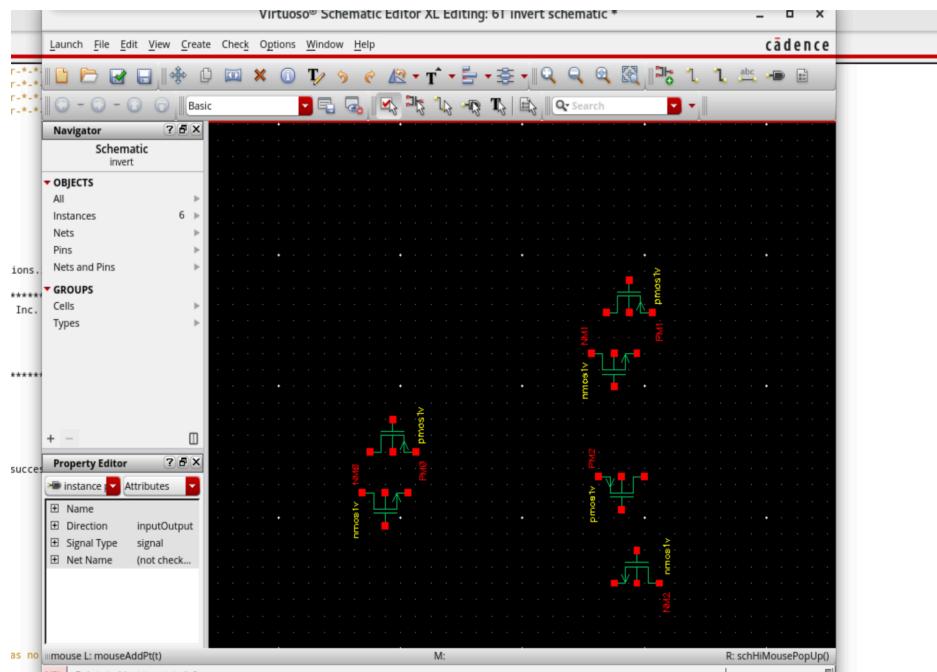
## Step 4: Design the Schematic

Designing the 6T full adder schematic involves selecting and placing transistors and other components from the Virtuoso component library. The user needs to open the component browser and select NMOS and PMOS transistors from the available technology files. For the 6T adder, two NMOS and two PMOS transistors are required for the XOR logic, and one NMOS and one PMOS are required for the carry generation logic. Using the **instance** command (**i**), the transistors are placed and arranged according to the 6T adder's circuit structure. The **wire** command (**w**) is then used to connect the

transistors' gates, sources, and drains according to the full adder's logical structure. Input and output pins are added using the **pin** command (**p**), where **A**, **B**, and **Cin** are defined as inputs and **Sum** and **Cout** as outputs. VDD and GND are connected to the PMOS and NMOS transistors to provide power and ground reference. The XOR logic is configured to generate the **Sum** output, while the carry generation logic defines the **Cout** output.

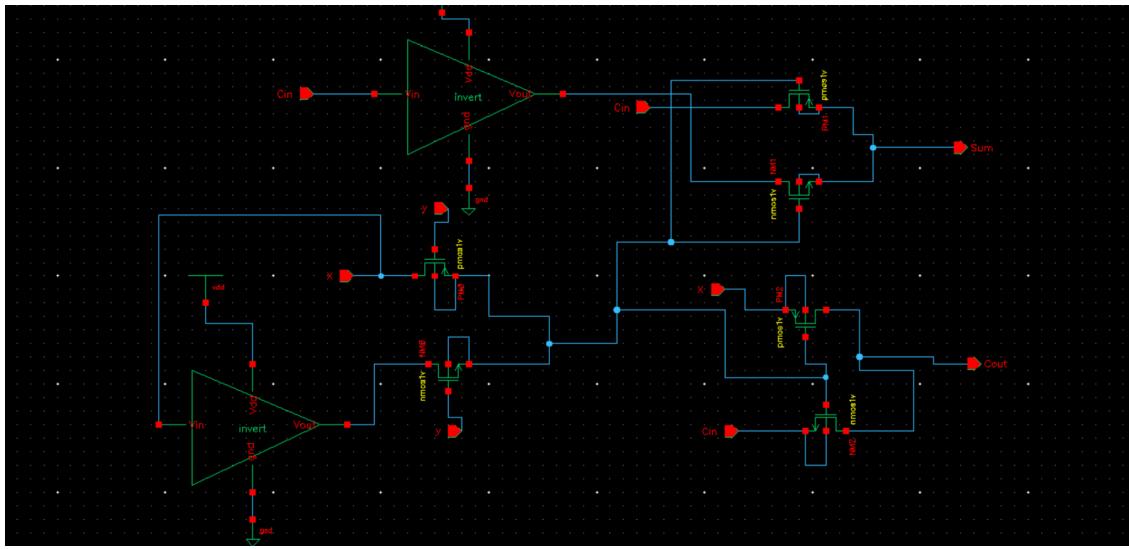






## Step 5: Check and Save Schematic

After the schematic design is complete, the user must verify the circuit's connectivity and design integrity. This is done by selecting **Design > Check and Save** from the top menu. If there are any missing connections, inconsistent logic, or incomplete transistor placements, the tool will generate an error or warning message. These issues must be corrected before proceeding. Once the circuit passes the connectivity check without errors, the schematic is saved to the project library. Saving the schematic ensures that the design is ready for symbol creation and simulation.

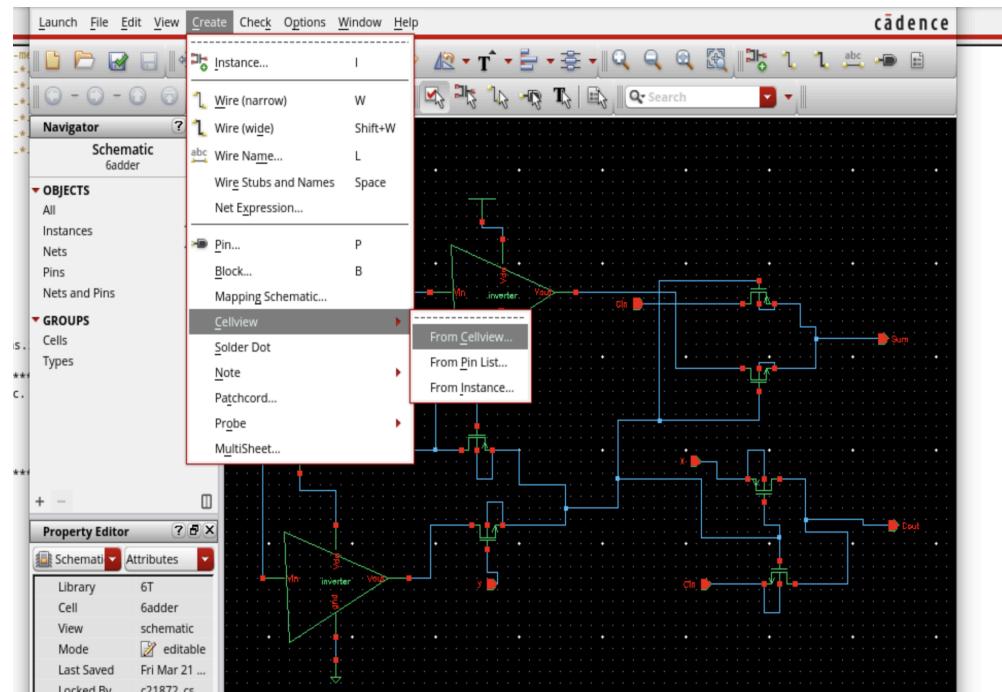


## 2. Create Symbol

### Step 1: Generate a Symbol

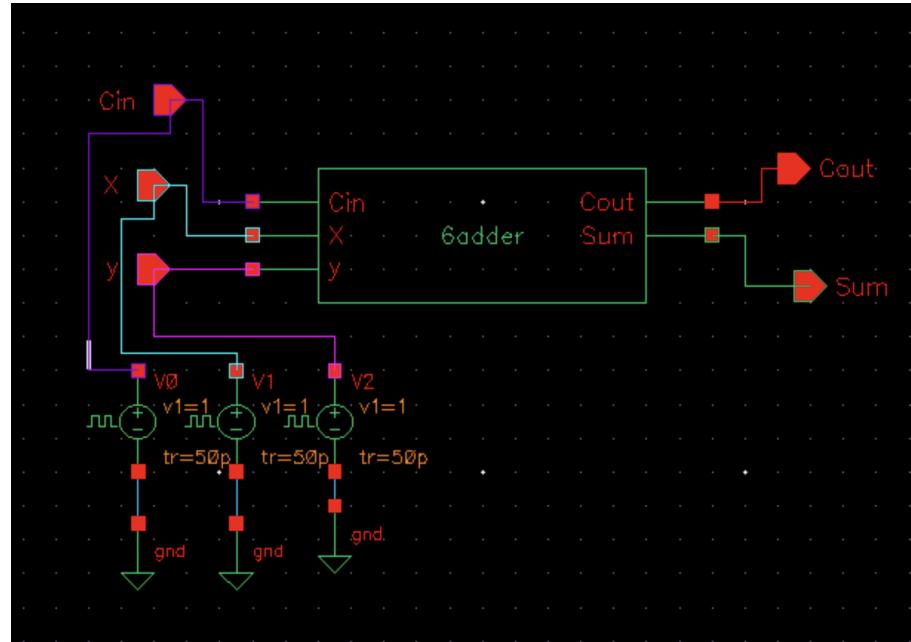
Once the schematic is finalized, a symbol representing the 6T adder must be created for use in hierarchical designs. This is done by selecting **Create > Cellview > From Cellview** from the main menu. The user enters the name **6T\_Adder** for the symbol and specifies **Symbol** as the view type. A box representing the adder is drawn using the drawing tools available in Virtuoso.

Input and output pins are added and labeled (**A**, **B**, **Cin**, **Sum**, **Cout**). This symbol allows the adder to be used as a modular component within larger circuits.



## Step 2: Verify the Symbol

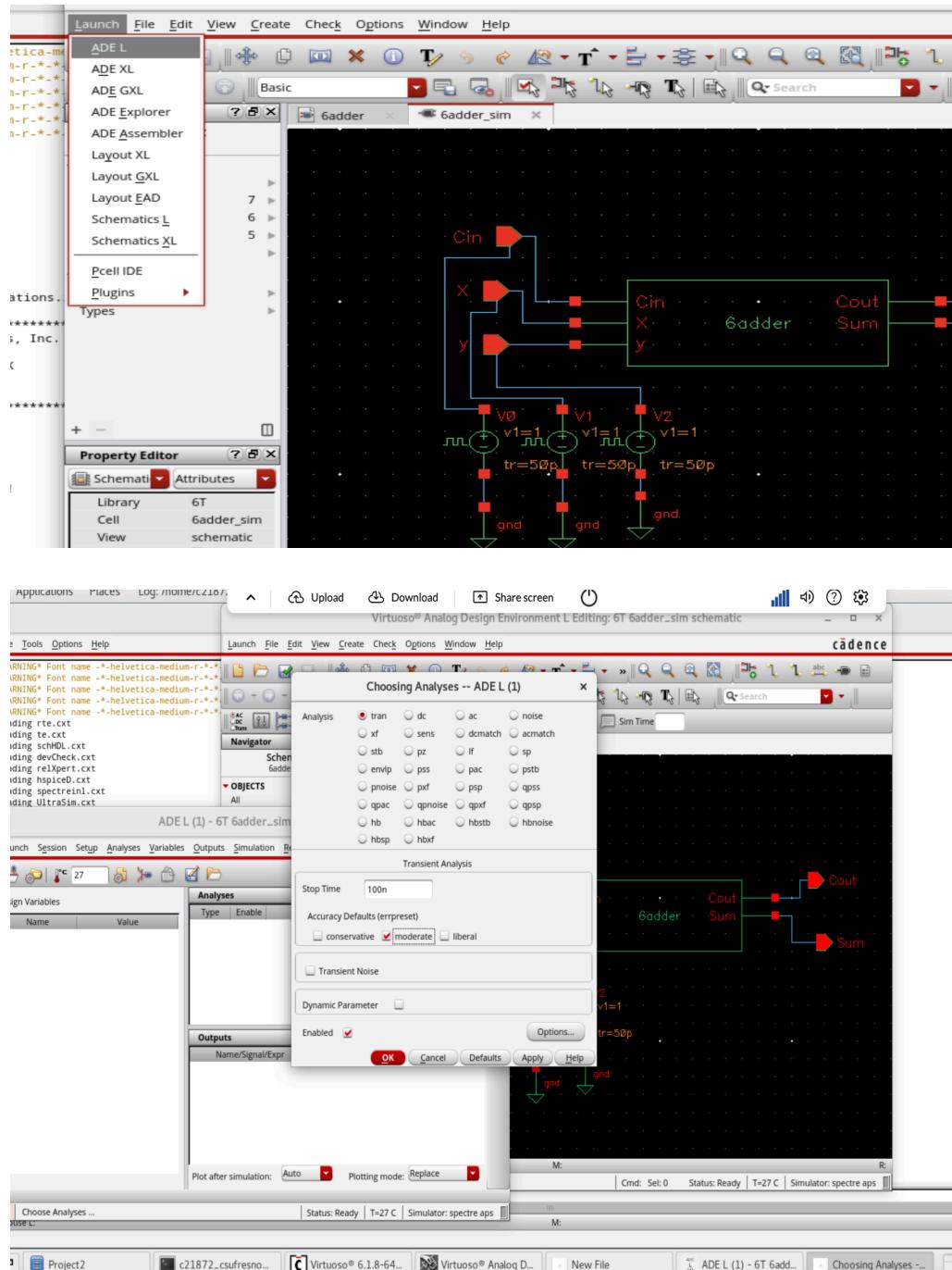
After creating the symbol, the user opens it to verify that all input and output pins are correctly positioned and labeled. The orientation of the pins should match the logical flow of the adder circuit. If any misalignment or missing pin connections are found, they should be corrected. Saving the symbol ensures that the adder can be easily integrated into other circuit designs.



## 3. Simulation Setup (ADE L)

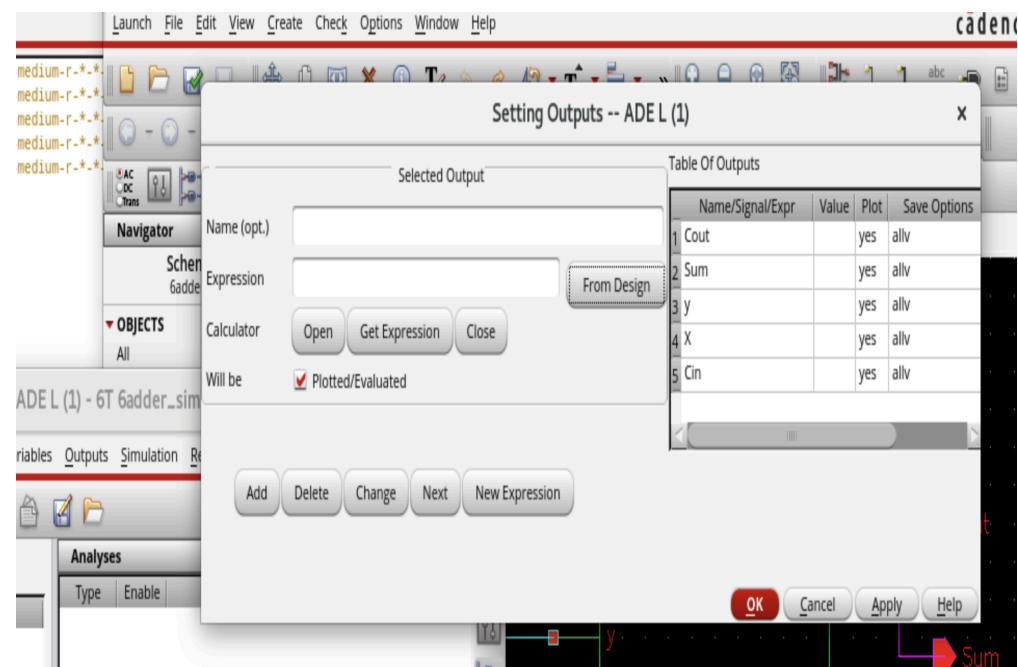
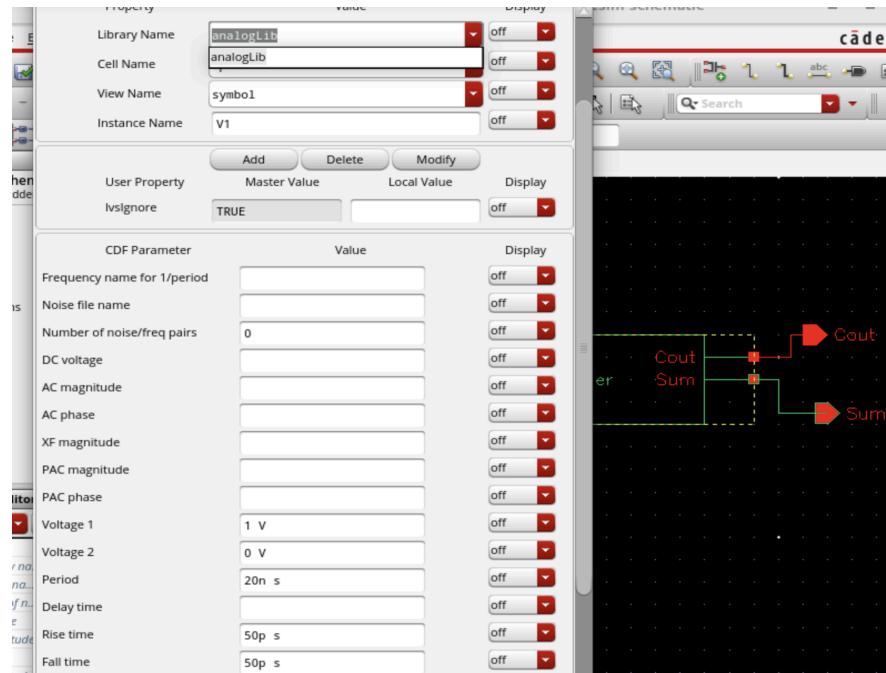
### Step 1: Open ADE L

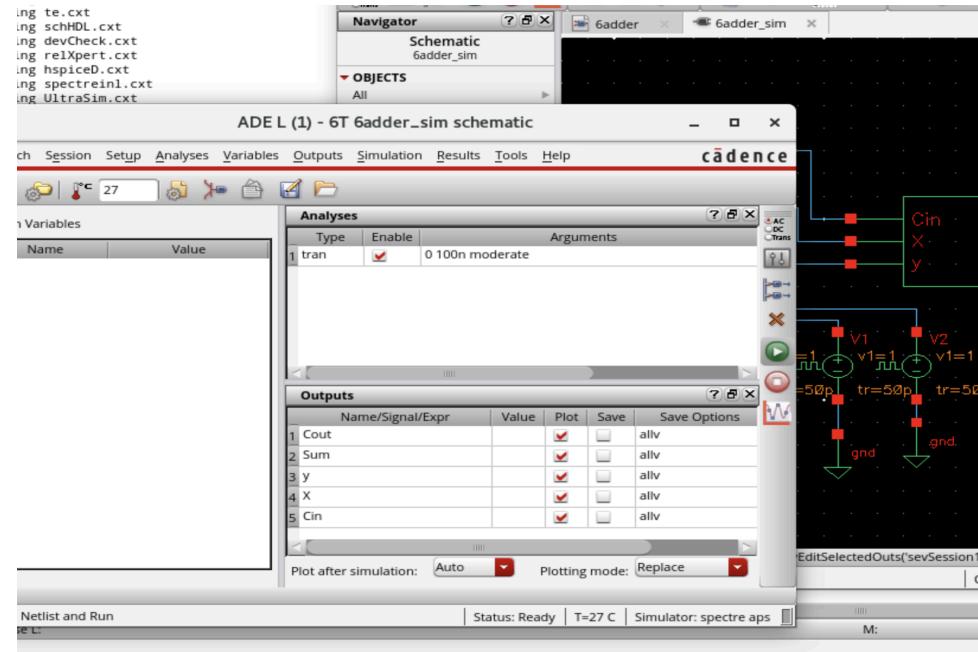
Simulation of the 6T adder is performed using the ADE L tool in Cadence Virtuoso. The user opens ADE L by selecting **Launch > ADE L**. In the ADE window, the user sets the simulation type as **transient analysis**. The 6T adder schematic is loaded into the simulation environment, which allows the user to define input signals, power supply, and output measurements.



## Step 2: Set Up Transient Simulation

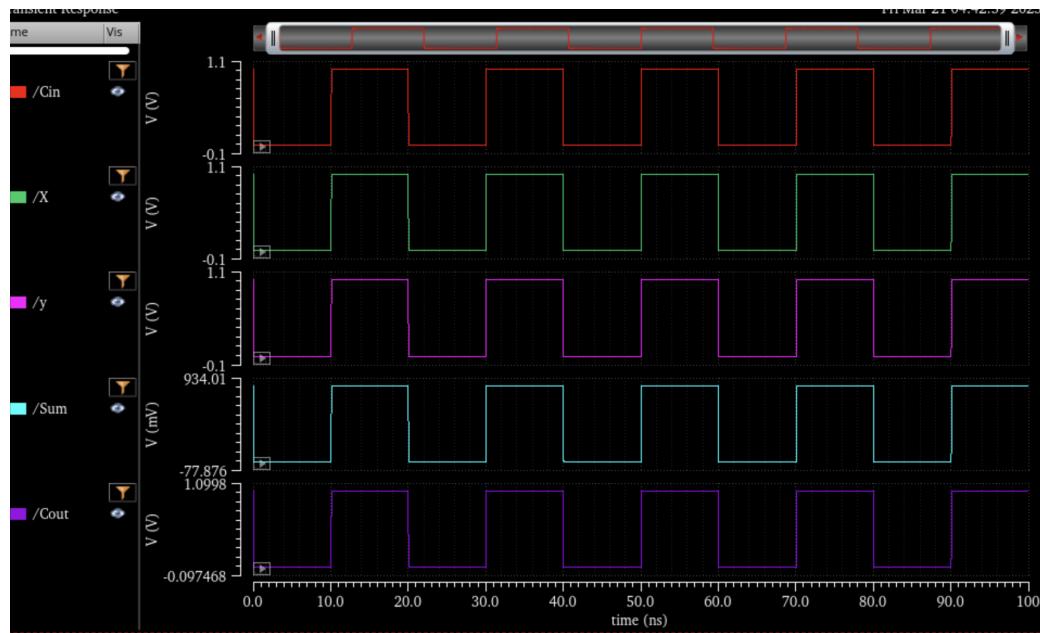
To set up the transient simulation, the user adds a **vpulse** source from the component library. The **vpulse** is configured with an amplitude of 0V to 1.2V, a rise and fall time of 0.1ns, a pulse width of 5ns, and a period of 10ns. A **vdd** source of 1.2V is connected to the PMOS source, and GND is connected to the NMOS source. The output signals (**Sum** and **Cout**) are selected and saved as outputs.

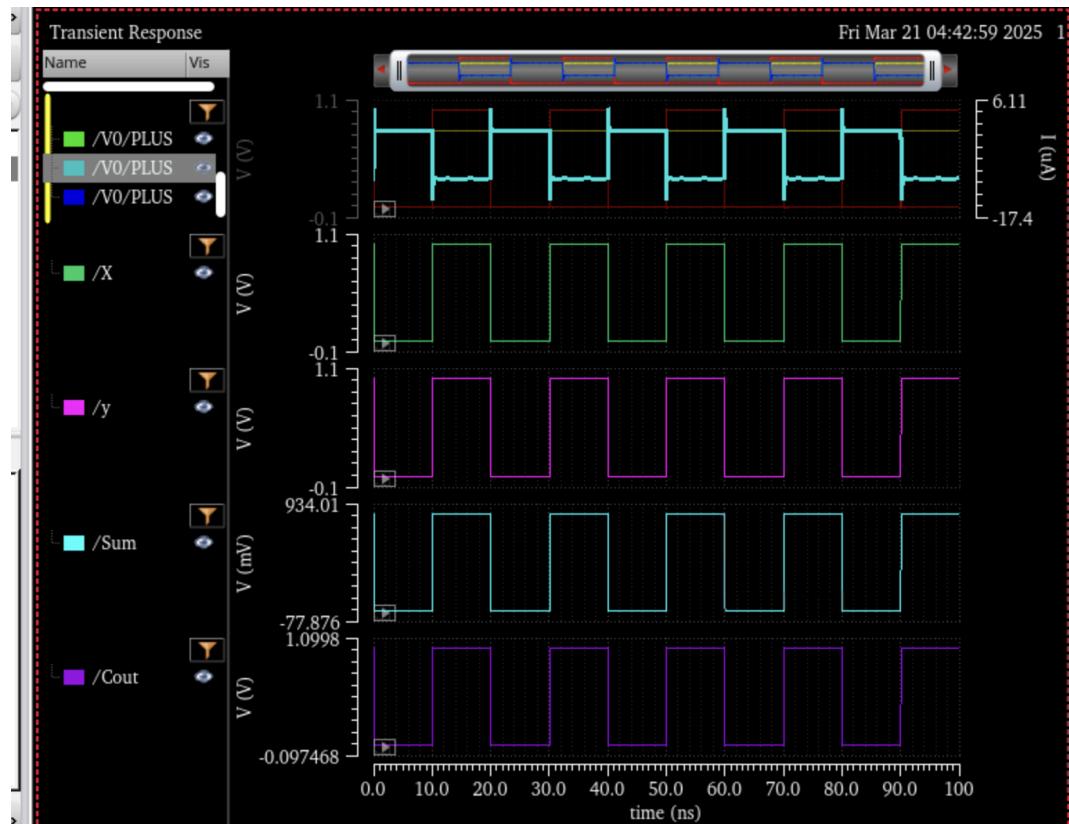
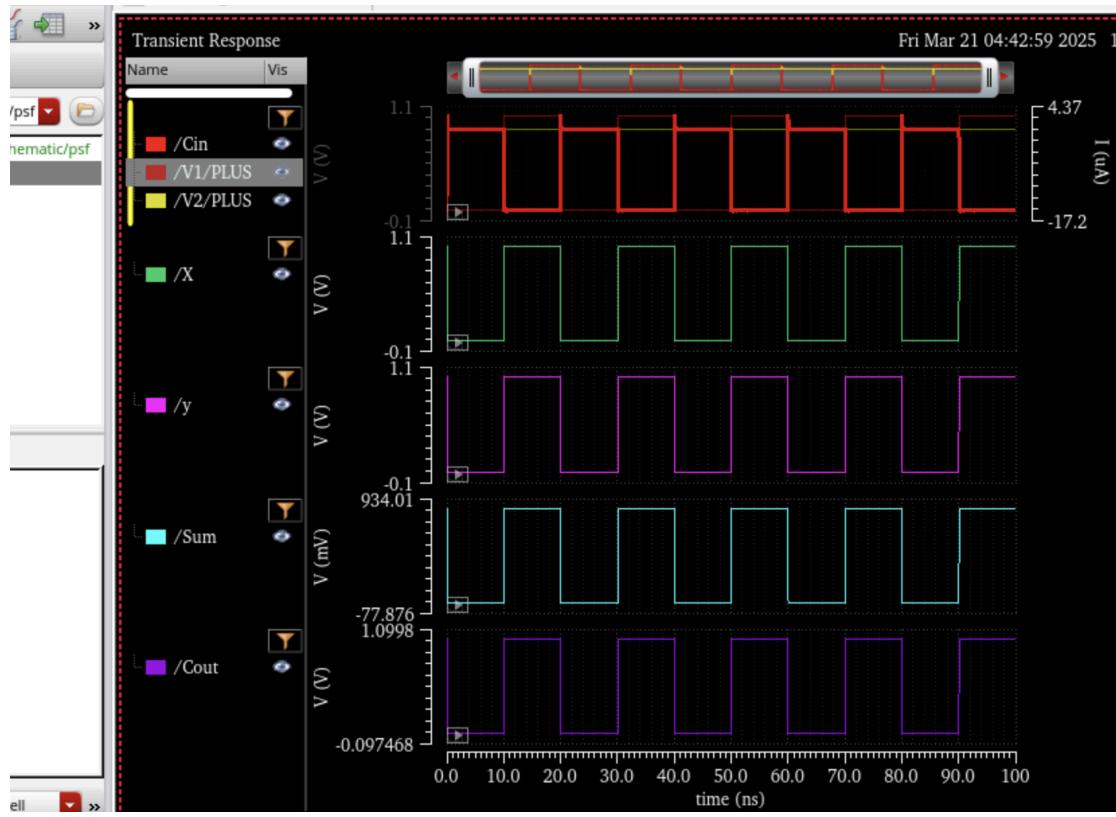


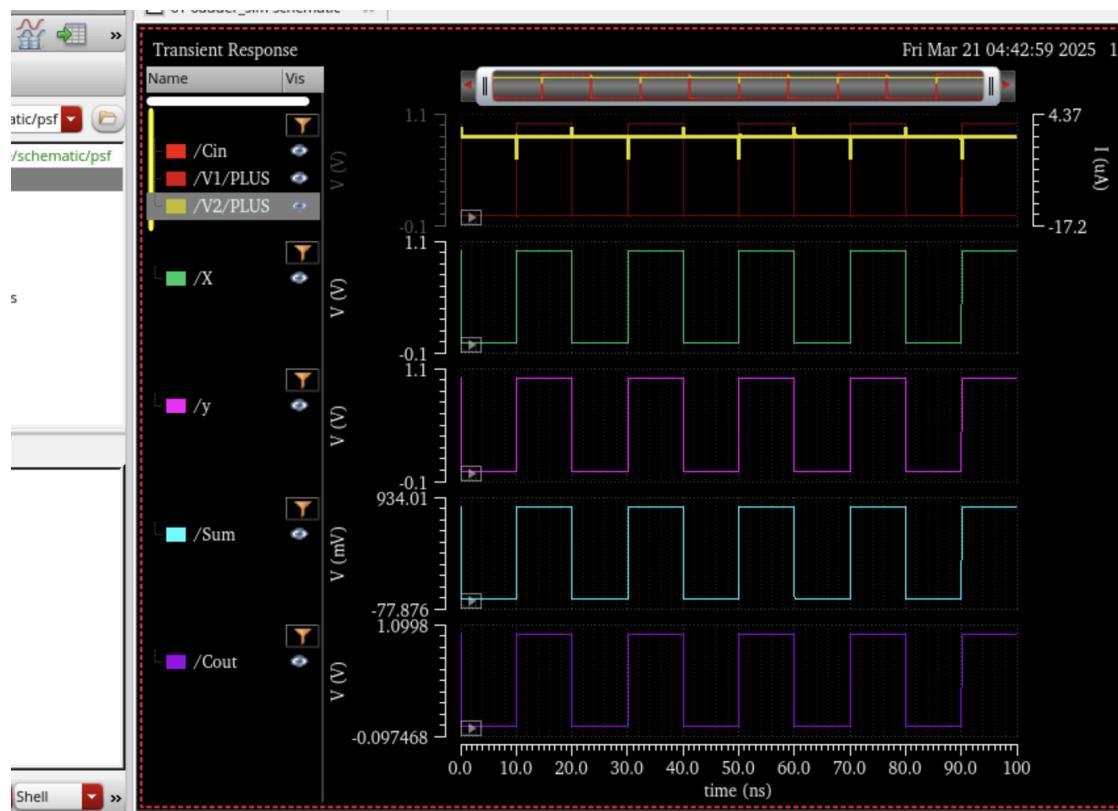


### Step 3: Run the Simulation

The user runs the simulation by selecting **Simulation > Netlist and Run**. The transient response is checked to confirm correct logic behavior. The waveforms for **Sum** and **Cout** should match the expected full adder truth table.





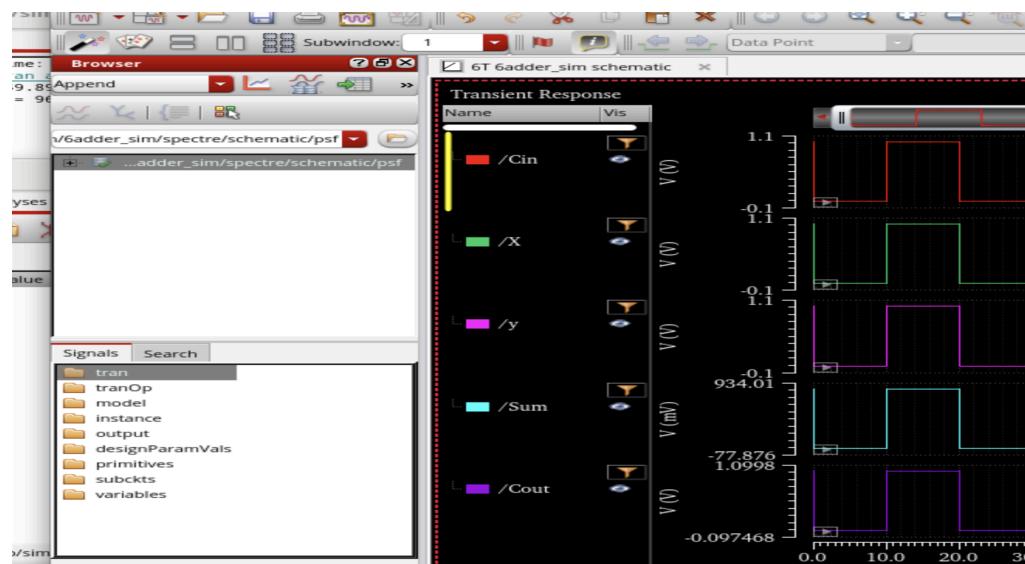
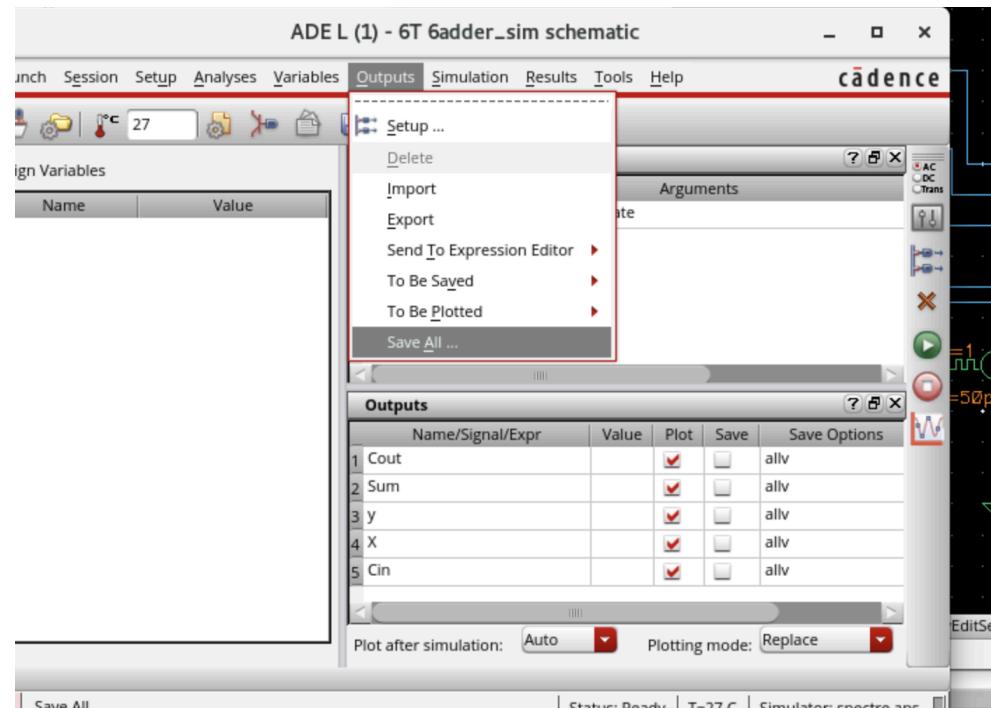


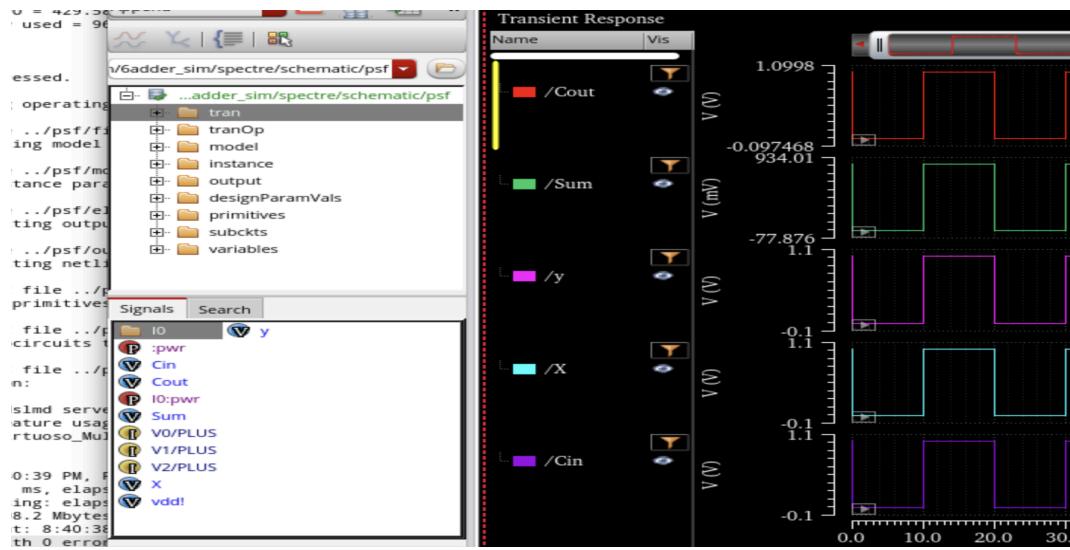
## 4. Power Calculation

### Step 1: Use Calculator Tool

The user opens the **Calculator** tool to calculate power consumption. The average power is computed using the equation:

$$P_{avg}=1/T \int_0^T V(t) \cdot I(t) dt$$

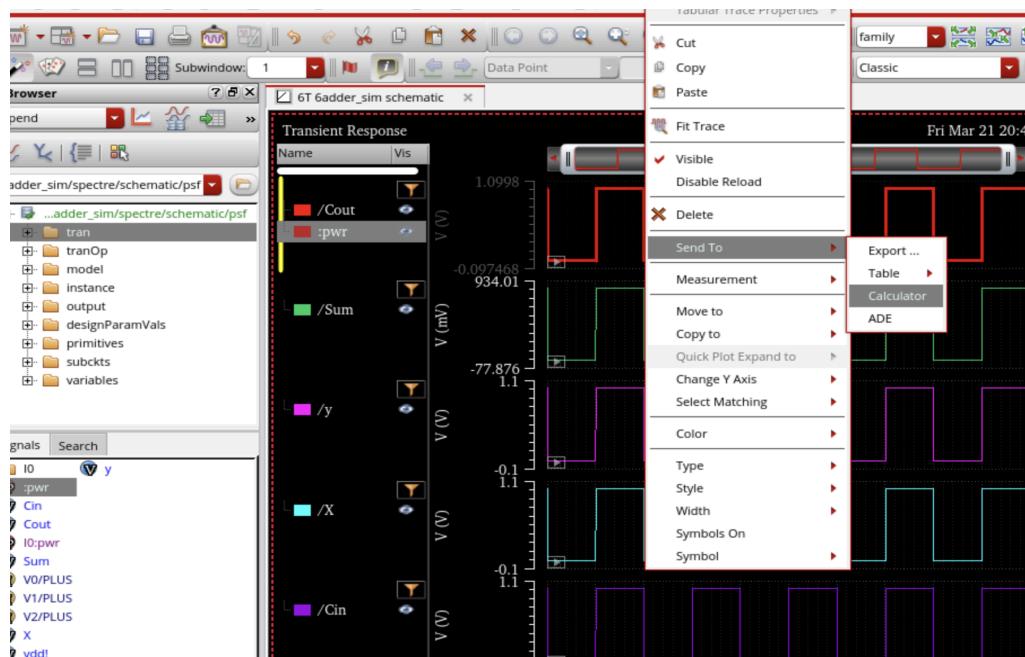


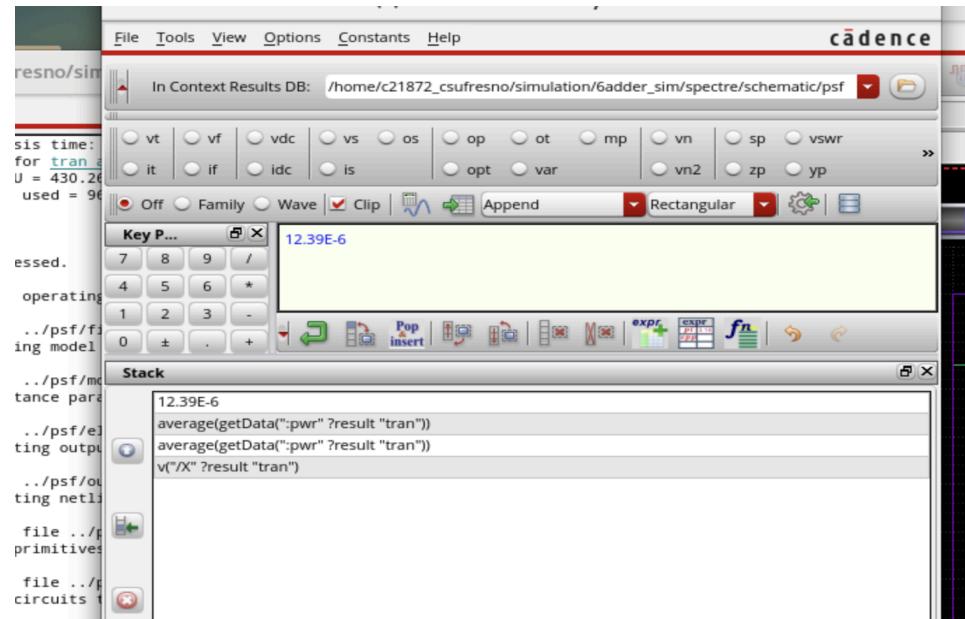
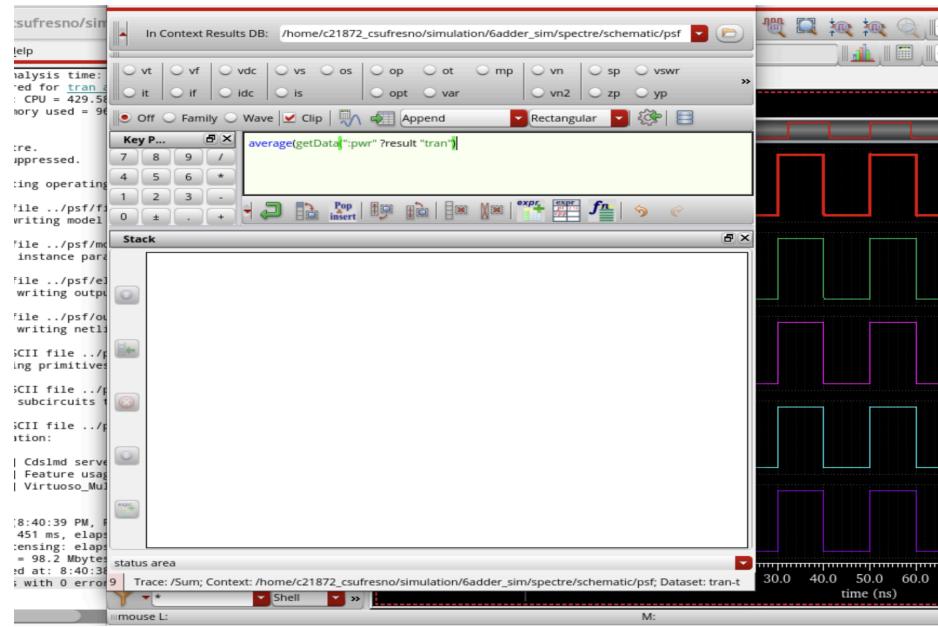


## Step 2: Measure Average Power

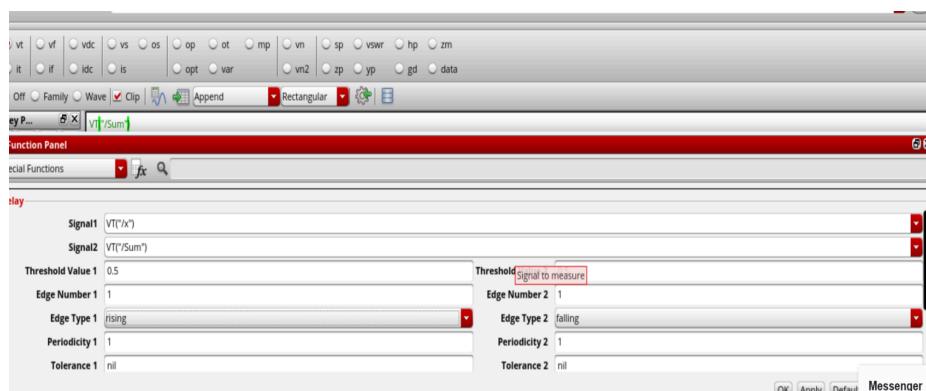
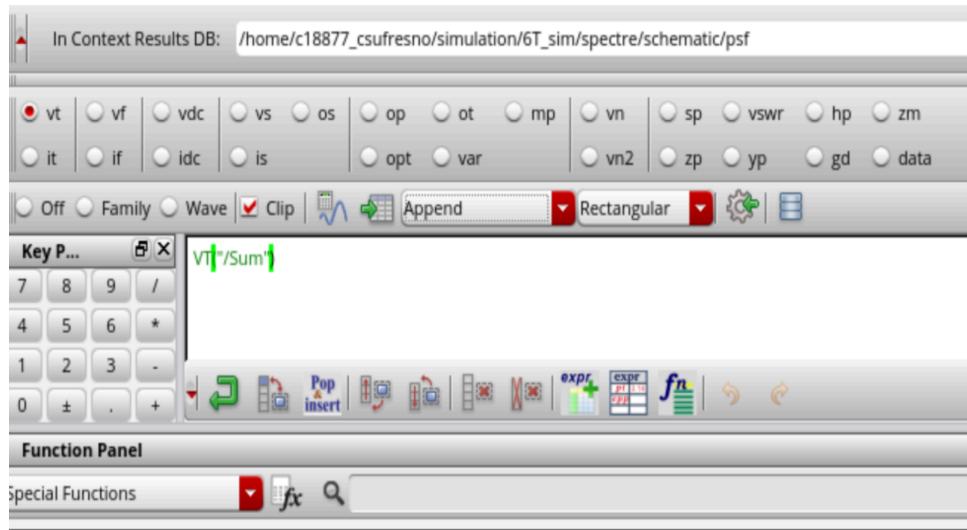
From the transient waveform, the total current drawn and supply voltage are measured. The average power is computed using:

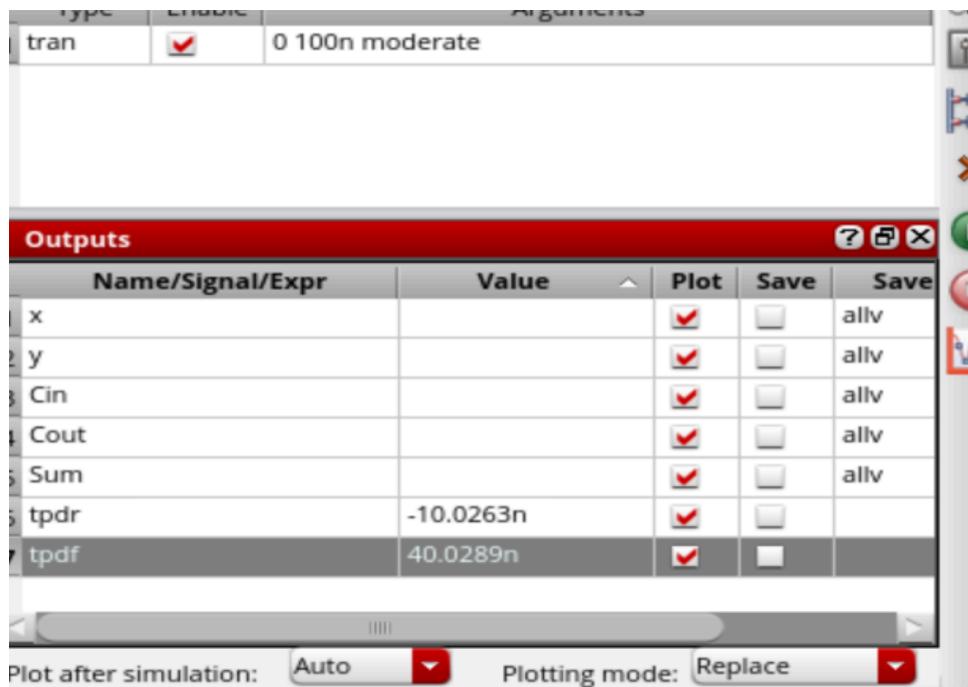
$$P_{avg} = V_{DD} \cdot I_{avg}$$





speed calculation:

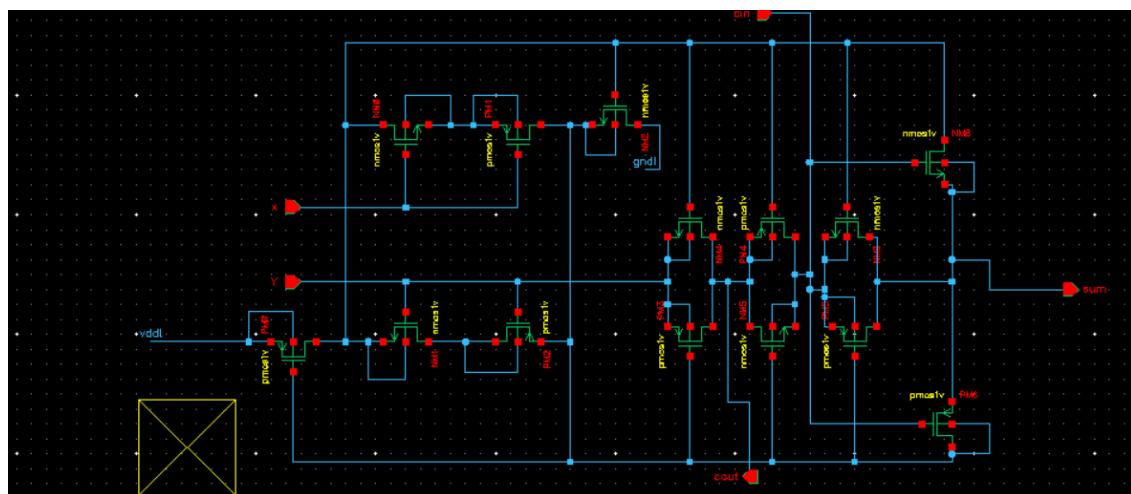


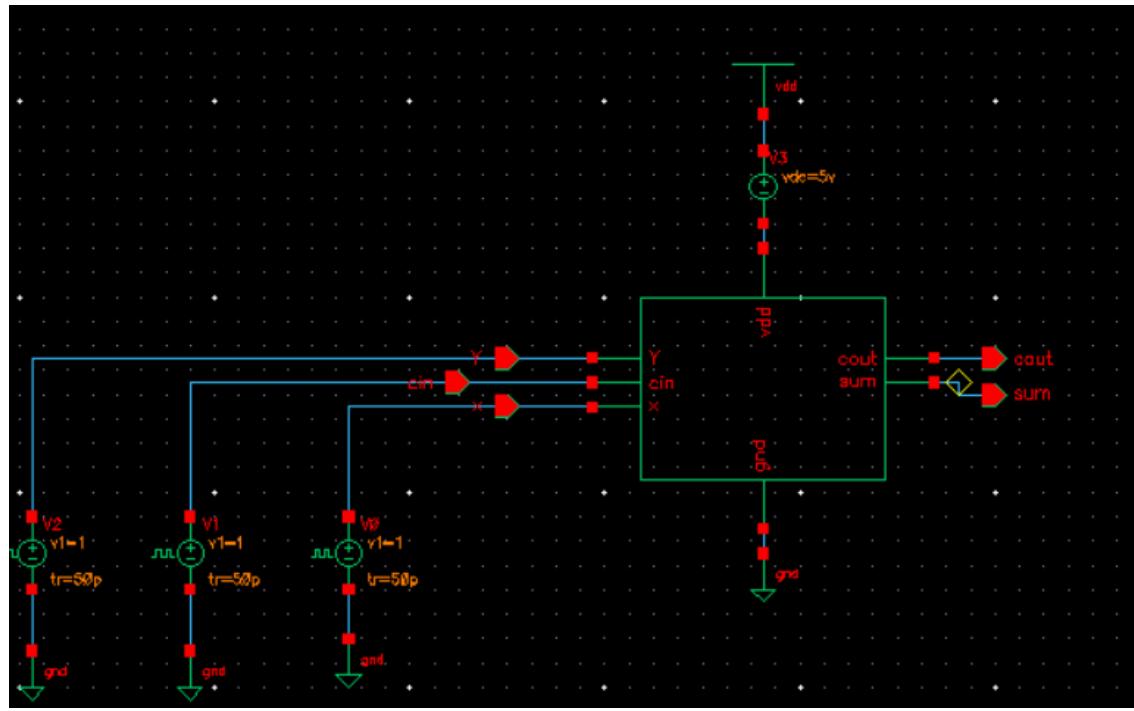


To find the actual propagation delay let me do the average of both tpdr and tpdf  
 $(Tpdf+tpdr/2)=(-10.0263n+40.0289n)/2$   
 $=15.0013n$  s

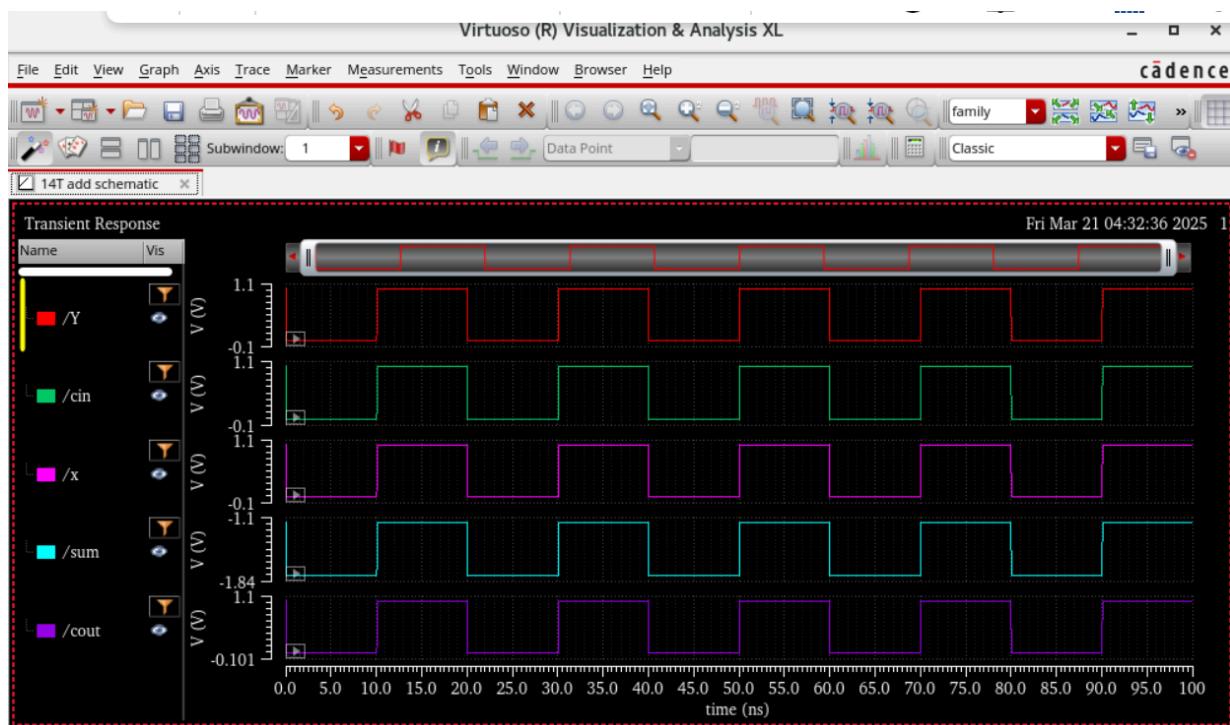
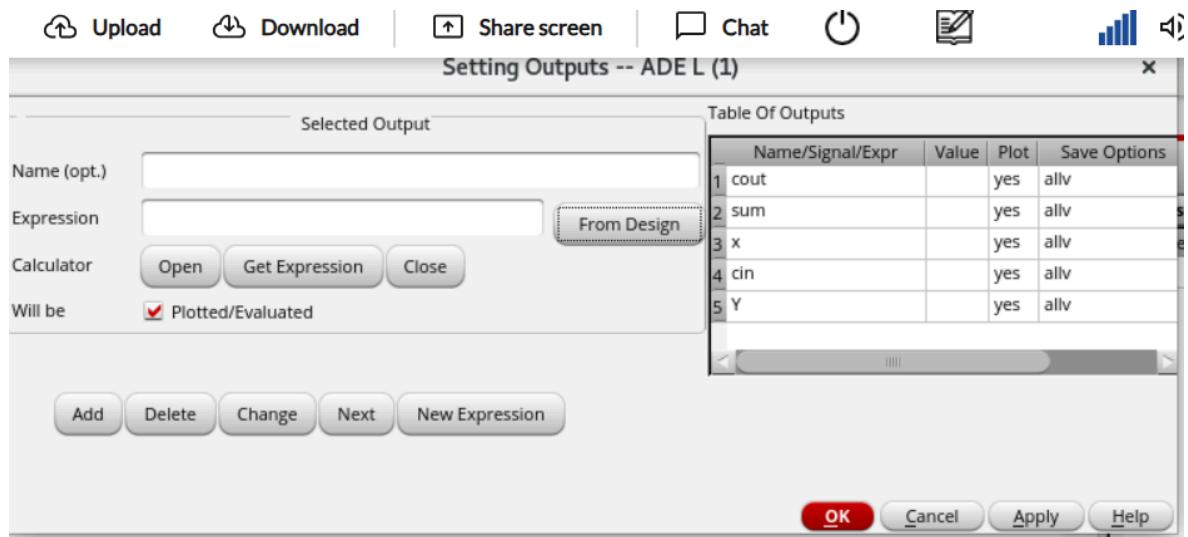
## 4. 14T Design Results

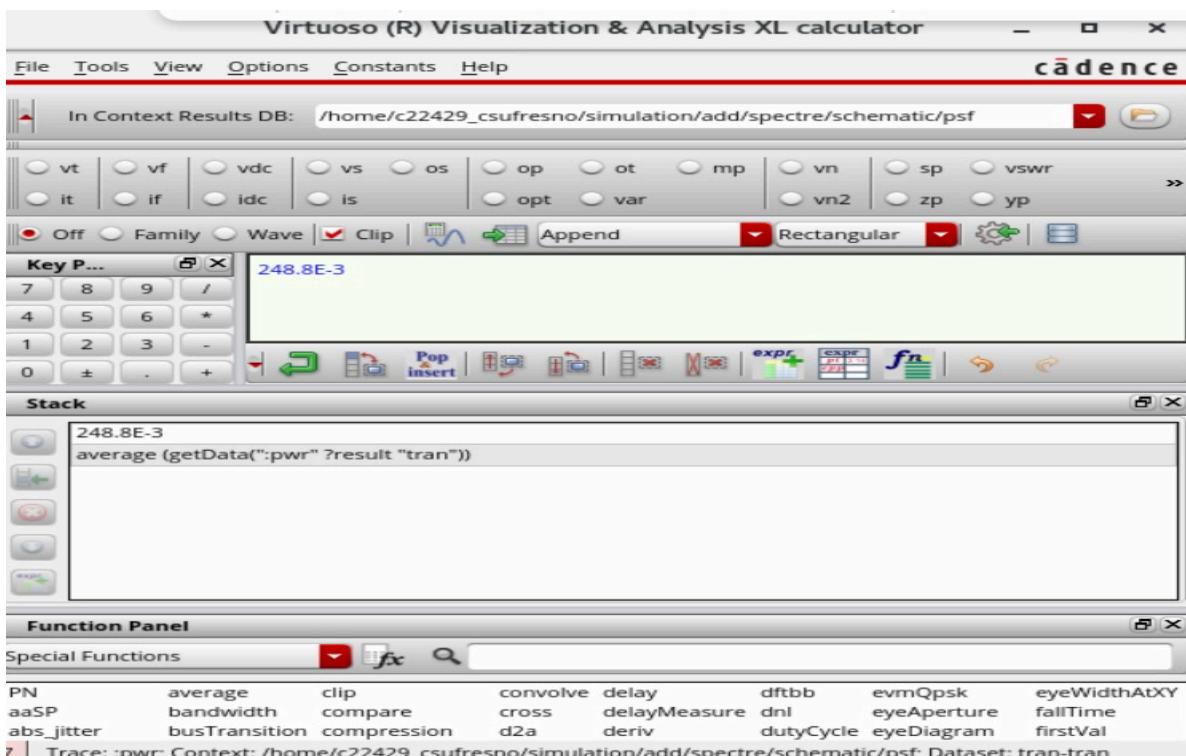
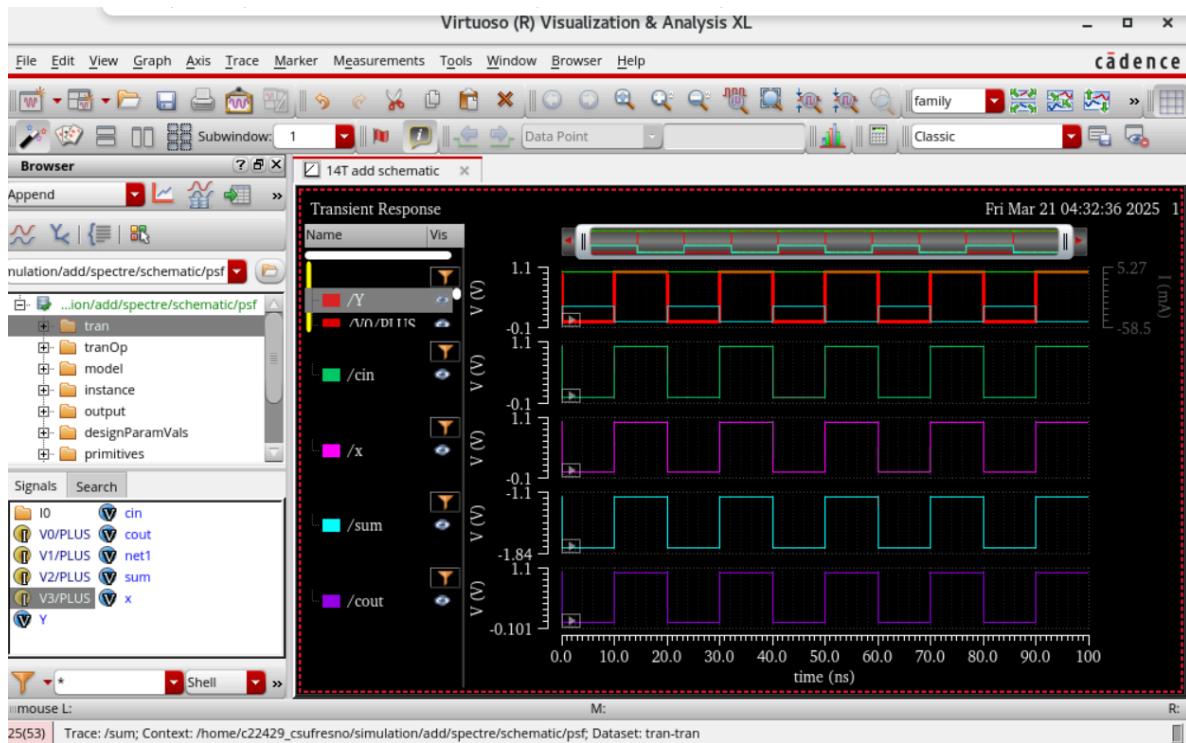
### Schematic Design of 14T

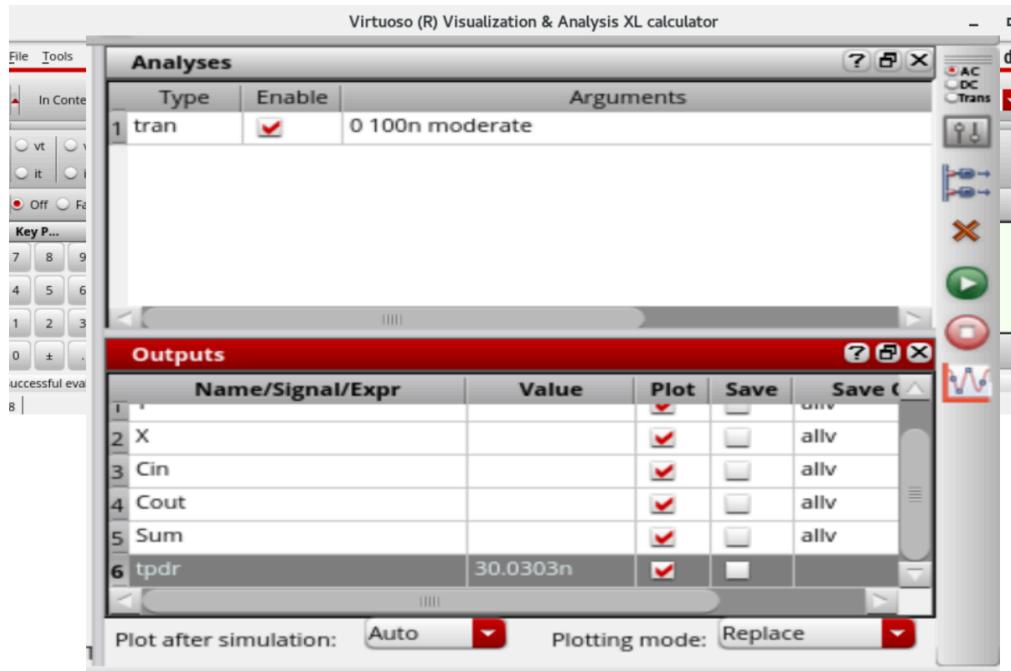




CDF Parameter	Value	Display
Frequency name for 1/period		off
Noise file name		off
Number of noise/freq pairs	0	off
DC voltage	5 V	off
AC magnitude		off
AC phase		off
XF magnitude		off
PAC magnitude		off
PAC phase		off
Voltage 1	1 V	off
Voltage 2	0 V	off
Period	100n s	off
Delay time		off
Rise time	50p s	off
Fall time	50p s	off
Pulse width	50ns s	off
Temperature coefficient 1		off
Temperature coefficient 2		off
Nominal temperature		off
Type of rising & falling edge	<input type="button" value="▼"/>	off





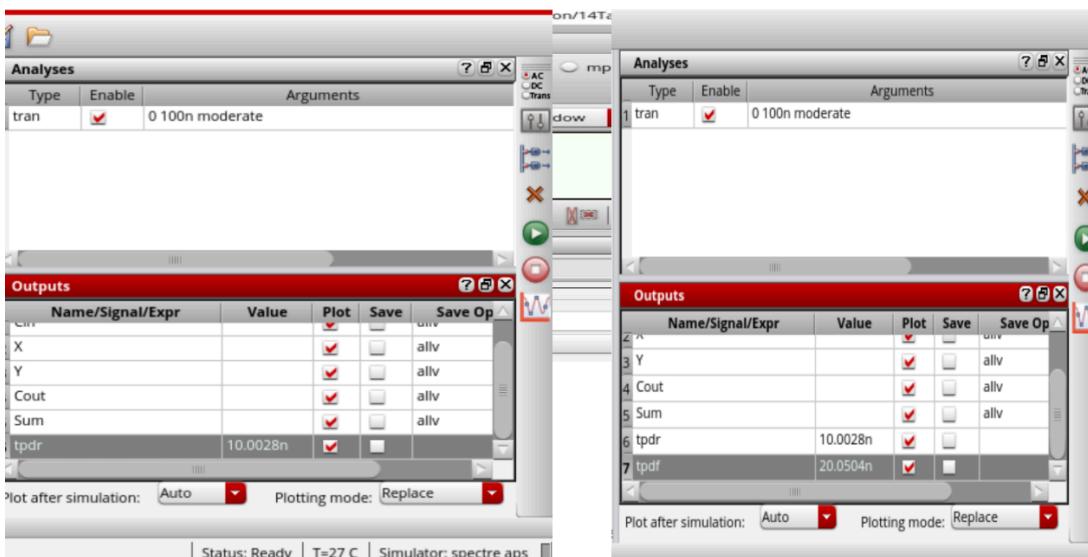


To find the actual propagation delay of 14T adder let me do the average of both tpdr and tpdf  
 $(Tpdf+tpdr)/2=(30.0303n+20.0559n)/2$   
 $=25.0431n\text{ s}$

## 5. OPTIMIZATION

Optimization of parameters of 14T Adder:

Library Name	gdk045	Value	off
Cell Name	pmos1v	Value	value
View Name	symbol	Value	off
Instance Name	PM1	Value	off
<input type="button" value="Add"/> <input type="button" value="Delete"/> <input type="button" value="Modify"/>			
CDF Parameter	Value	Display	
Model Name	g45p1svt	Value	off
Multiplier	1	Value	off
Length	45n M	Value	off
Finger Width	300n M	Value	off
Total Width	600n M	Value	off
Fingers	2	Value	off
Folding Threshold	10u M	Value	off
Diff Cont	<input checked="" type="checkbox"/>	Value	off
Gate Connection	None	Value	off
Use DFM Rules	Minimum	Value	off



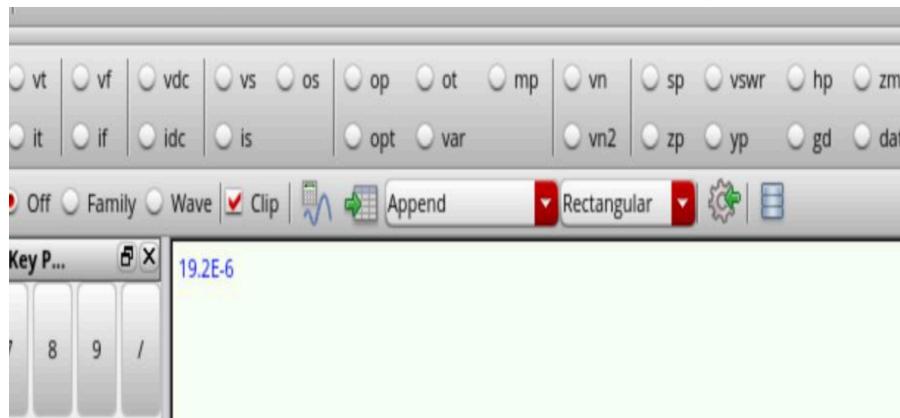
### Propagation Delay:

To find the actual propagation delay of 14T adder after Optimization of transistors let me do the average of both tpdf and tpd़

$$(Tpdf+tpd़)/2=(20.03504n+10.0028n)/2$$

$$=15.0266n\text{ s}$$

### Optimization of parameters of 6T Adder:



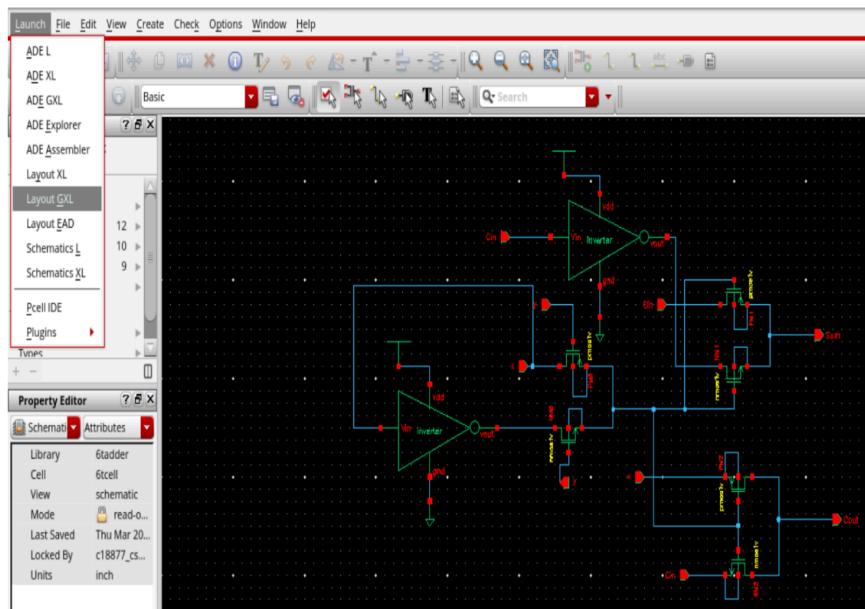
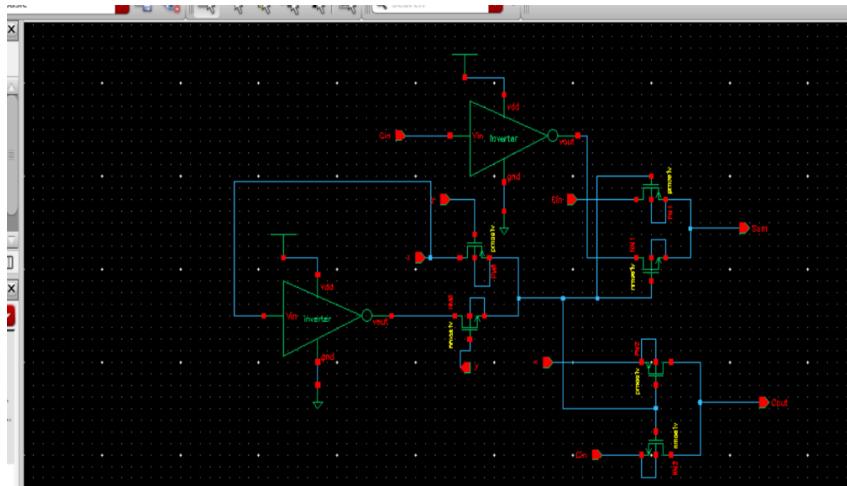
Name/Signal/Expr	Value	Plot	Save	Save Options
x		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
y		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
Cin		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
Cout		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
Sum		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
tpdr	-10.0269n	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
tpdf	10.0323n	<input checked="" type="checkbox"/>	<input type="checkbox"/>	

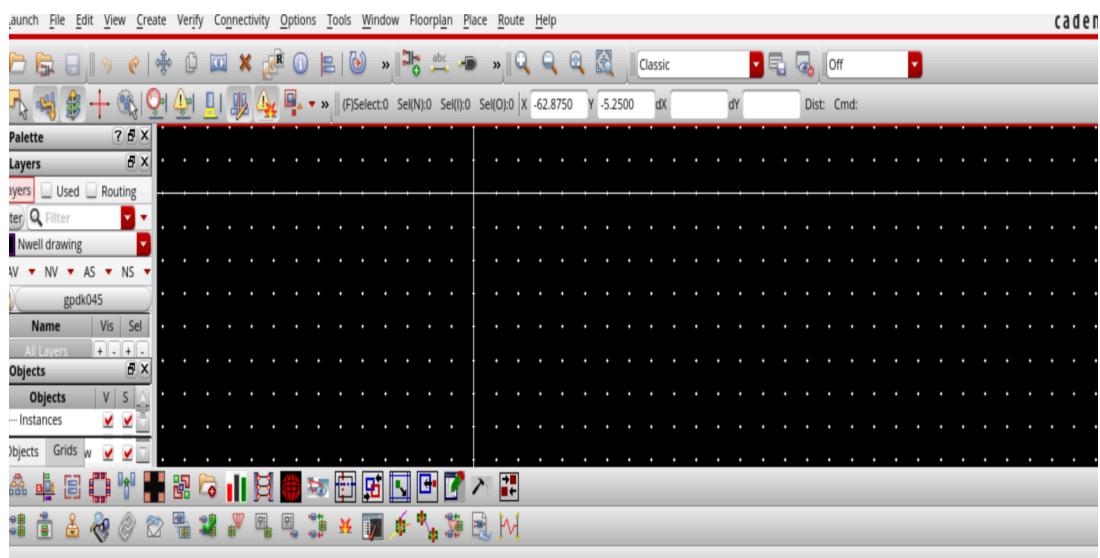
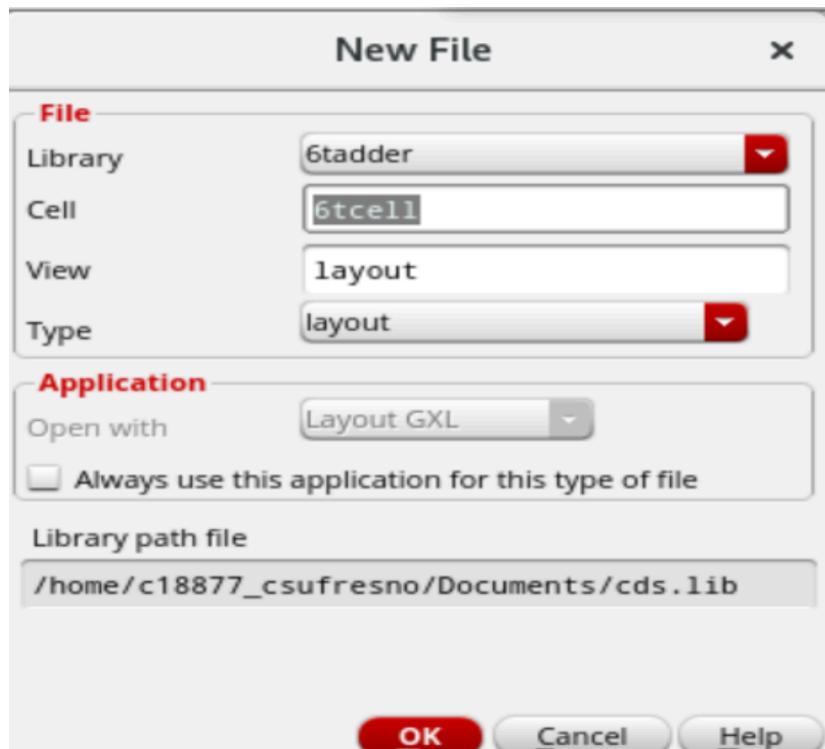
To find the actual propagation delay of 14T adder after Optimization of transistors let me do the average of both tpdr and tpdf  
 $(Tpdf+tpdr/2)=(-10.0269n+10.0323n)/2 = 0.00268n \text{ s}$

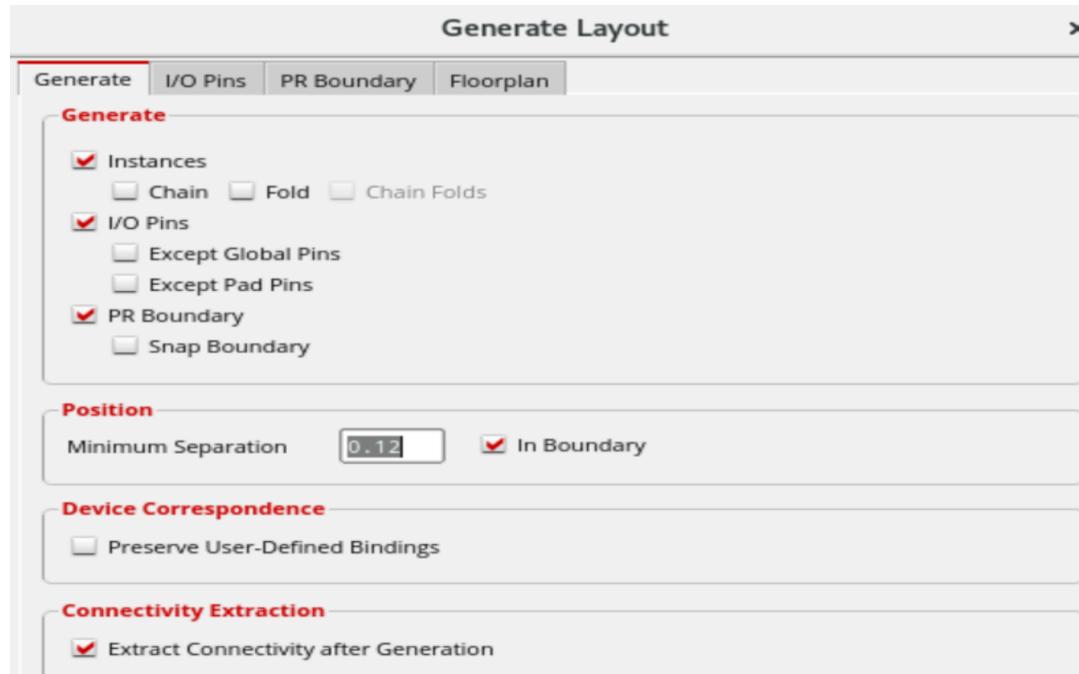
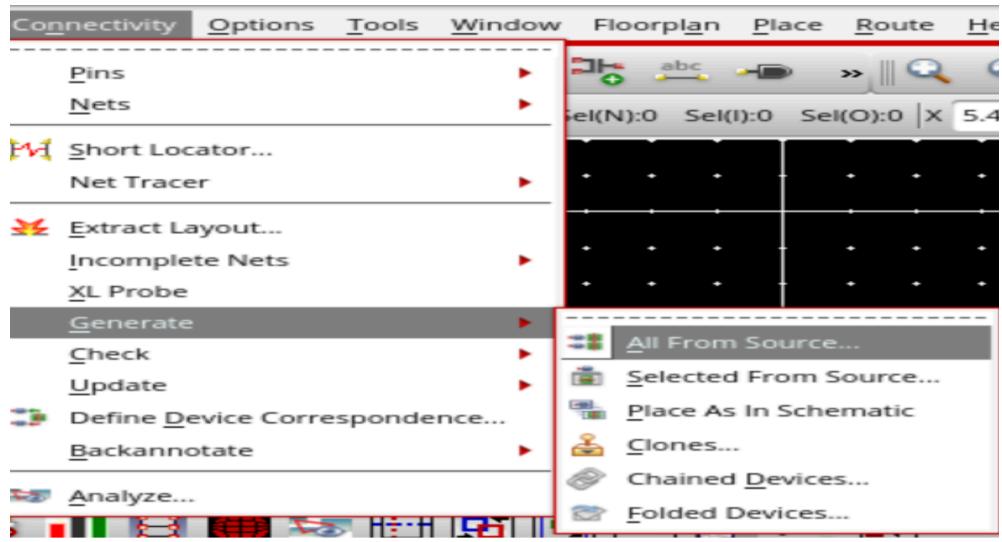
## 6. Layout Design

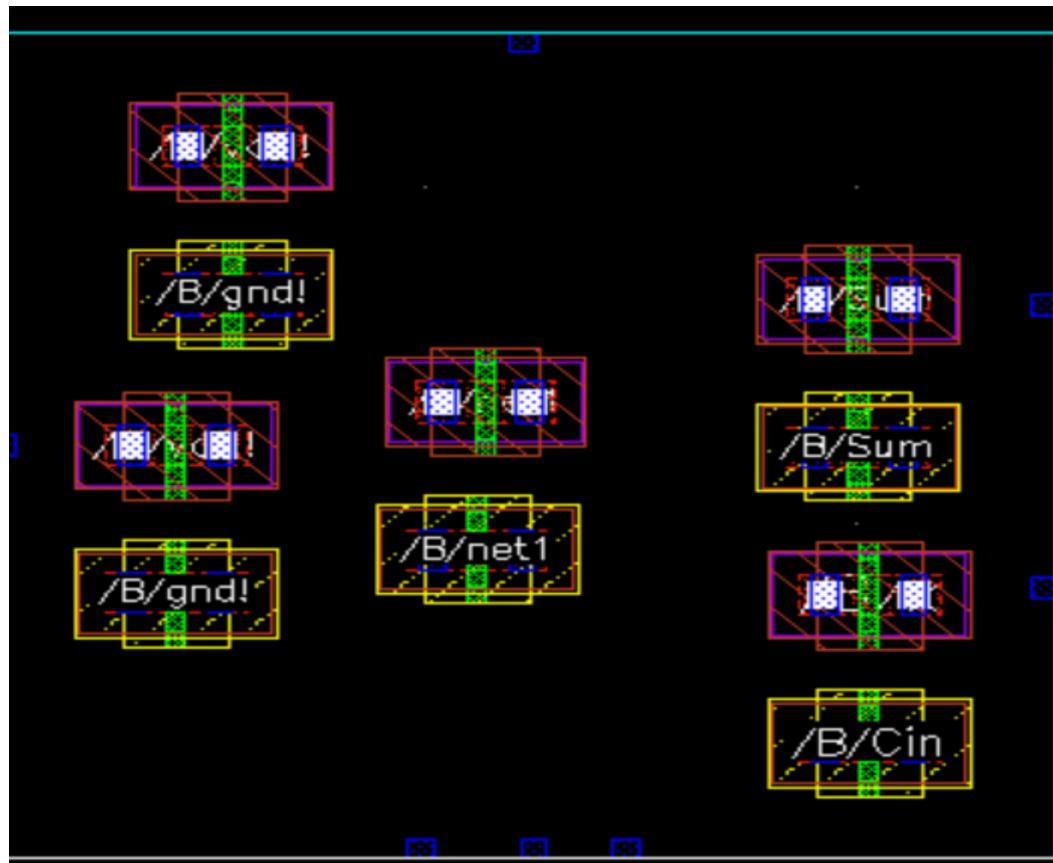
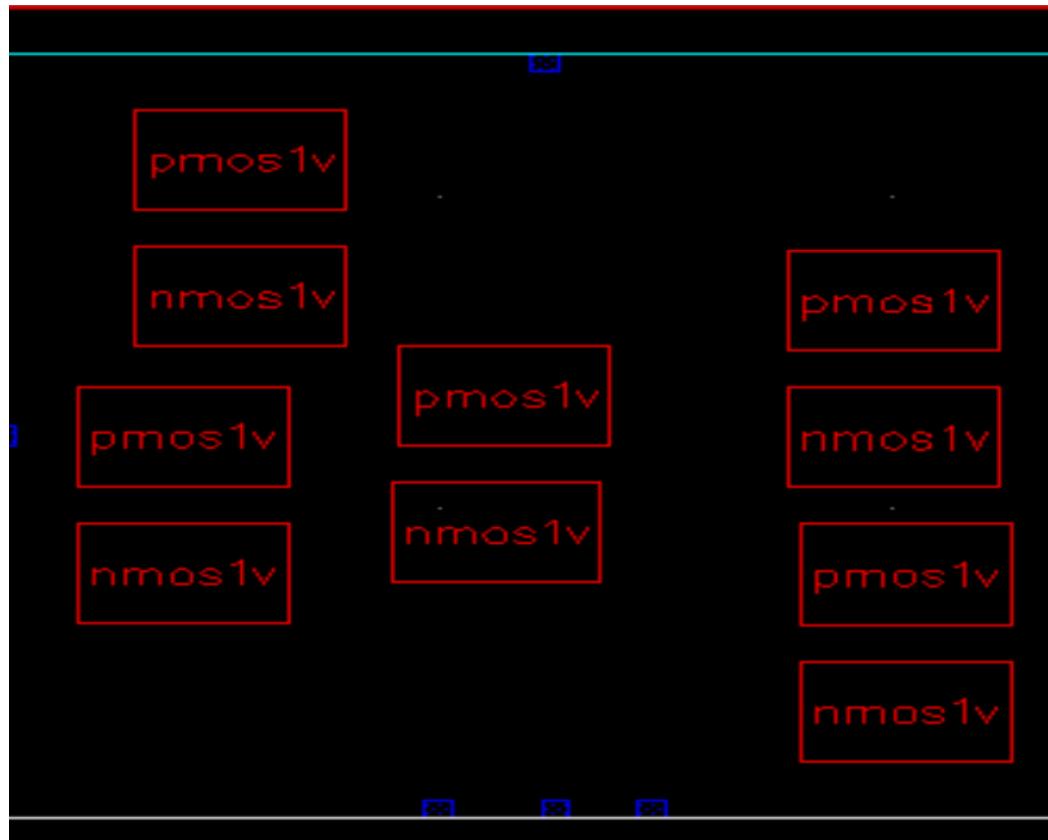
### Step 1: Create Layout for 6T Adder

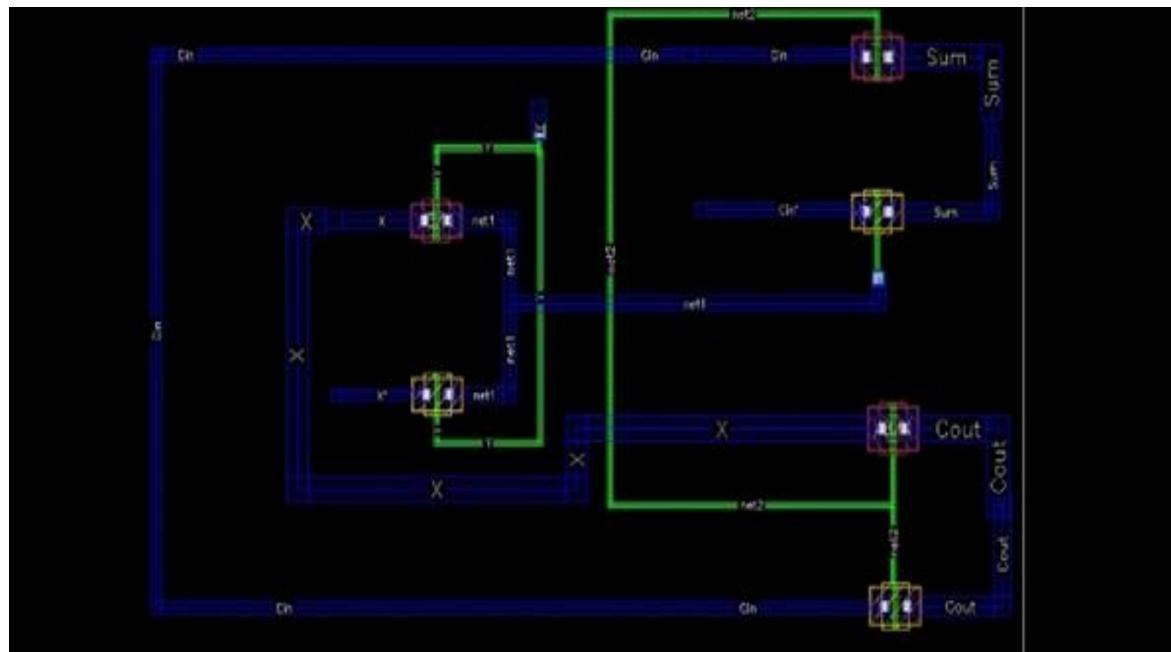
The layout is created using **Layout XL**. Transistors and metal layers are placed and connected according to the schematic.



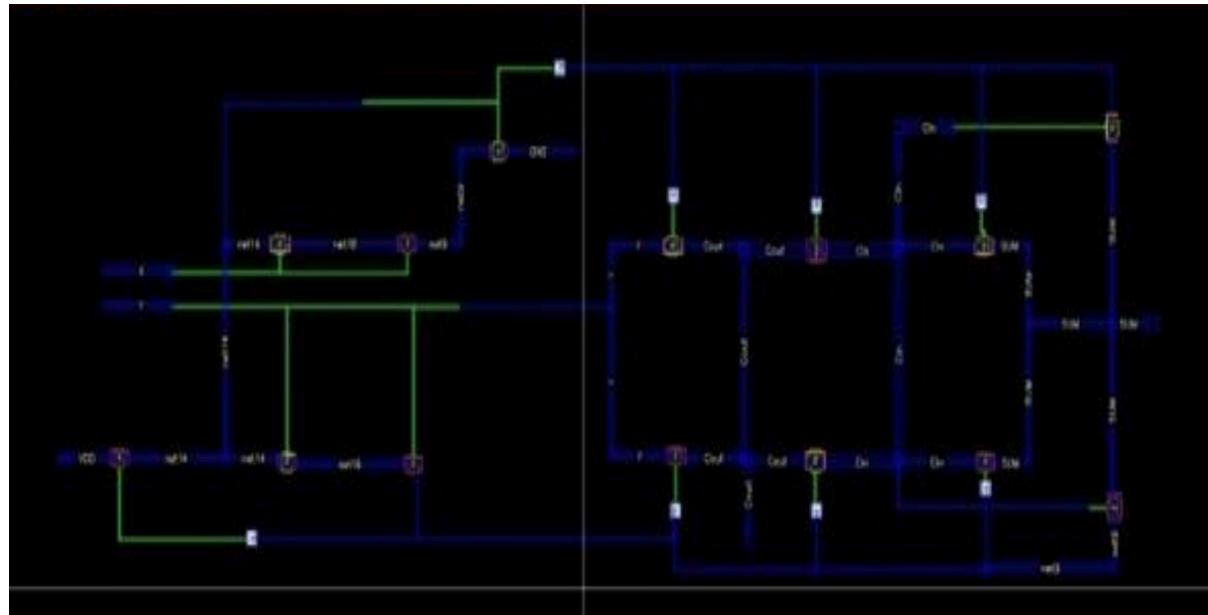








LAYOUT OF 14T



## 8. Results and Analysis

## **8. CONCLUSION**

## **9. REFERENCES**

- [1] Chandra, Krishna, et al. "A new design 6t full adder circuit using novel 2T XNOR gates." *IOSR Journal of VLSI and Signal Processing* 5.3 (2015): 63-68.
- [2] Vigneswaran, T., B. Mukundhan, and P. Subbarami Reddy. "A novel low power, high speed 14 transistor CMOS full adder cell with 50% improvement in threshold loss problem." *Enformatika Trans. Eng. Comp. Tech* 13 (2006): 82-85.