SRAVANI YALAGANAMONI

⋄ +1(408) 590-1165 ⋄ Fresno, CA ⋄ sravaniyalaganamoni@gmail.com ⋄ LinkedIn ⋄

PROFESSIONAL SUMMARY

Graduate student in Computer Engineering with hands-on experience from RTL to GDSII, specializing in low-power design, verification, and test automation. Proficient in Verilog/SystemVerilog, C++, Python, and industry-standard EDA tools (Synopsys & Cadence). Strong interest in CPU microarchitecture, SoC implementation, and hardware verification with emphasis on performance, power, and yield optimization.

EDUCATION

Master of Science in Computer Engineering, California State University, Fresno **GPA: 3.3/4.0** **Aug 2023 - Dec 2025**
Relevant course work: Semiconductor Manufacturing, VLSI Design, VLSI Testing, Machine learning, Cybersecurity, Probability Theory.
Bachelors in Electronics and Communication Engineering, Malla Reddy Engineering Collage, India**.** **June 2018 - May 2022**
Relevant course work: Computer Architecture, Digital System Design, CMOS Design, Microcontrollers and Microprocessors, Electronic device circuits.

TECHNICAL SKILLS

Software& Programming Languages: Verilog, System Verilog, UVM, C++, TCL, Python, Java, JavaScript, C, SQL, Data Structures, MATLAB, MS Excel, MS Word, MS PowerPoint, OOPs, Linux, Git, Agile teamwork, technical documentation & presentation

EDA Tools: Synopsys ICC2, Design Compiler, PrimeTime, VCS, Cadence Innovus, Virtuoso, Modelsim, TetraMAX, Machine learning tools, SPICE, Unit-level Testbench Architecture, Subsystem Feature Verification.

Area of Expertise: Digital & Analog Circuit Design, ASIC/FPGA Synthesis, Place & Route, Static Time Analysis, Power & Noise Analysis, Clock/Power Distribution, RC Extraction & Correlation, SRAM operation principles, PVT variation analysis concepts, CPU & SoC architecture concepts, Pre-silicon verification, UVM, Coverage-driven Verification, Assertion-Based Verification (SVA), Constrained Random Testing, Testplan Development.

Soft Skills: Strong Communication and teamwork skills, facilitating cross-functional collaboration, Proactive initiative in project execution, demonstrating leadership in research-driven design improvements, Analytical skills, Problem-solving.

WORK EXPERIENCE

System Engineer Trainee, VLSI Guru, Hyderabad, India **Dec 2022 – Mar 2023**
• Developed a UVM-based verification environment for an RTL FIFO design, leveraging SystemVerilog OOP concepts for scalable, reusable testbench components.
• Authored a comprehensive testplan, implemented constrained-random testing, and achieved 100% coverage-driven verification closure.
• Integrated SystemVerilog Assertions to monitor FIFO properties and enhance functional bug detection.

Intern, Verzeo, Hyderabad, India **Jun 2022 – Nov 2022**
• Simulated post-silicon validation flow for FIR filter by synthesizing to gate-level netlist and performing functional debug using assertion-based verification (SVA).
• Compared RTL and gate-level simulation results, injected functional bugs, and documented root-cause analysis mimicking post-silicon debug workflow.
• Demonstrated proficiency in using industry-standard tools for pre- and post-silicon validation without requiring hardware.

PROJECTS

Adaptive Test Pattern Generation for SRAM BIST (In Progress)
• Designing an adaptive BIST architecture for SRAMs using fault clustering and gray code/TRN-based test pattern generation.
• Implementing real-time feedback with an automated scoreboard system to enhance test validation and debugging.
• Projected outcomes include >98% fault coverage, 30% reduction in test time, and 25% power savings

Test-Aware Low Power Clock Gating in DSP Blocks
• Designed a 7-tap FIR filter for DSP applications with the goal of reducing power consumption without sacrificing testability.
• Implement clock gating and scan chain insertion to optimize both power efficiency and fault coverage using industry-standard ASIC design tools.
• Developed the design in Verilog, performed functional and post-synthesis verification, applied scan insertion with DFT strategies, and generated ATPG patterns using Synopsys TetraMAX.
• Delivered a fully verified, low-power FIR filter achieving 100% fault coverage, reducing power to 247.8 µW, and maintaining timing closure with 2.59 ns positive slack.

Transistor-Level Design and Optimization of 6T and 14T Adders
• Performed schematic design, layout creation, and post-layout simulation; analyzed power and delay using ADE L.
• Designed and simulated 6T and 14T adders using Cadence Virtuoso, focusing on optimizing power, delay, and area.
• Achieved 99.98% delay reduction in 6T adder and 40.01% improvement in 14T adder through transistor sizing techniques.

Floating-Point Unit (FPU) Synthesis and Physical Design
• Synthesized a Verilog-based Floating-Point Unit (FPU) using Synopsys Design Compiler, achieving optimized area and timing.
• Completed full physical design in Cadence Innovus, including floorplanning, placement, CTS, and routing.
• Achieved post-route timing closure (WNS +0.026 ns, skew <0.09 ns) and verified zero DRC/LVS violations.

CERTIFICATIONS

Design Verification with System Verilog/UVM - Udemy | Cadence RTL-to-GDSII Flow| FPGA Development