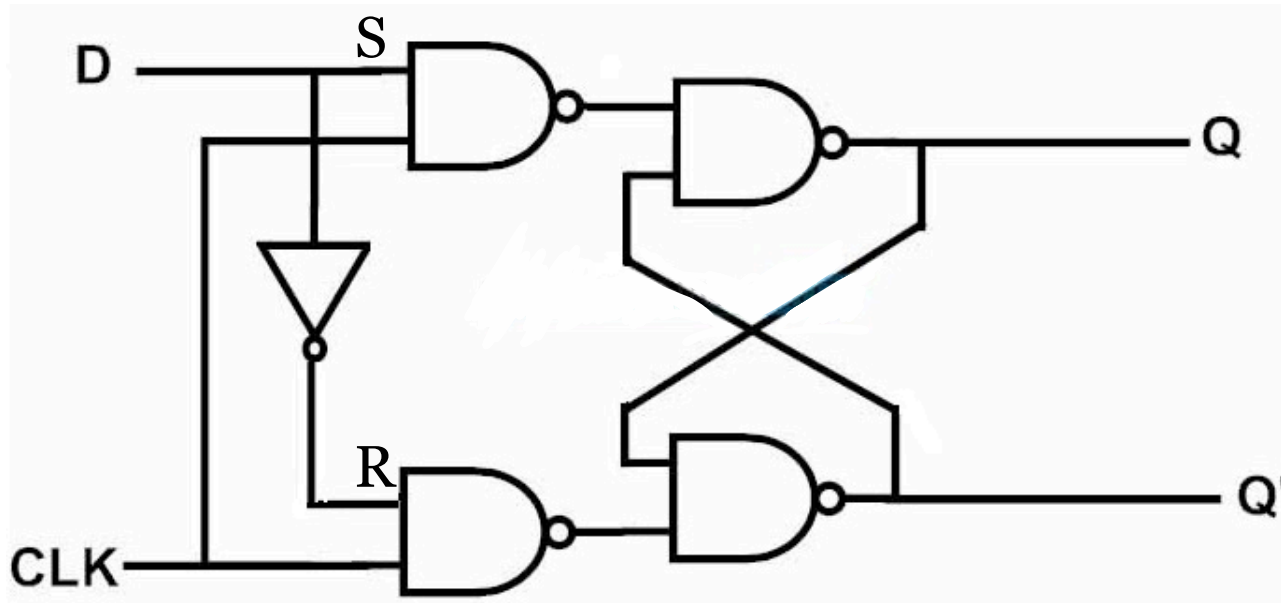
@Sree Vishnu Varthini

Day - 7

Embedded Systems Programming

D FLIPFLOP



A D Flip-Flop (also called a Data or Delay Flip-Flop) is a type of digital storage device that stores one bit of data and is widely used in digital circuits to maintain memory.

Truth Table

D Flip Flop		
Input	**Output**	
D	Q	Q'
0	0	1
1	1	0

REASON FOR CREATION OF D FLIPFLOP

The D flip-flop was designed to simplify the operation of the SR flip-flop and avoid the problem of invalid states. Instead of two inputs (S and R), the D flip-flop uses only one input, called D (Data).

To prevent the invalid state (S = R = 1), the D flip-flop was derived by connecting S and R logically. This is done by:

- Setting S = D
- Setting R = NOT(D) (or D')

This ensures that S and R are never both 1 at the same time.

By connecting D to S and its inverse to R, the D flip-flop operates with just one input (D), making it simpler and avoiding any unpredictable behavior.

Working:

Case 1: D = 0

D = 0 → S remains 0 and R becomes 1

S = 0 → Output of the first NAND gate (N1) becomes 1.

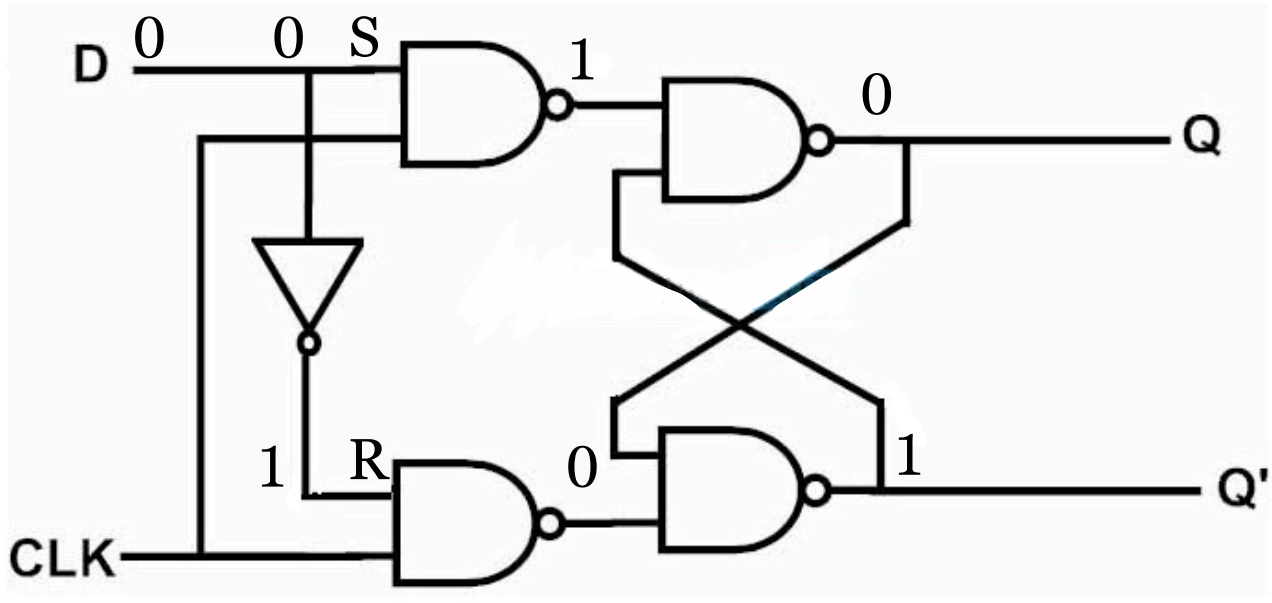
R = 1 → Output of the second NAND gate (N2) becomes 0.

Input to fourth NAND gate (N4) is 0 and so Q' becomes 1.

Due to this, input to third NAND (N3) gate becomes 1 and 1.

So Q becomes 0.

Q' is set to 1, and so Q is set to 0.



Working:

Case 2: D = 1

D = 1 → S remains 1 and R becomes 0

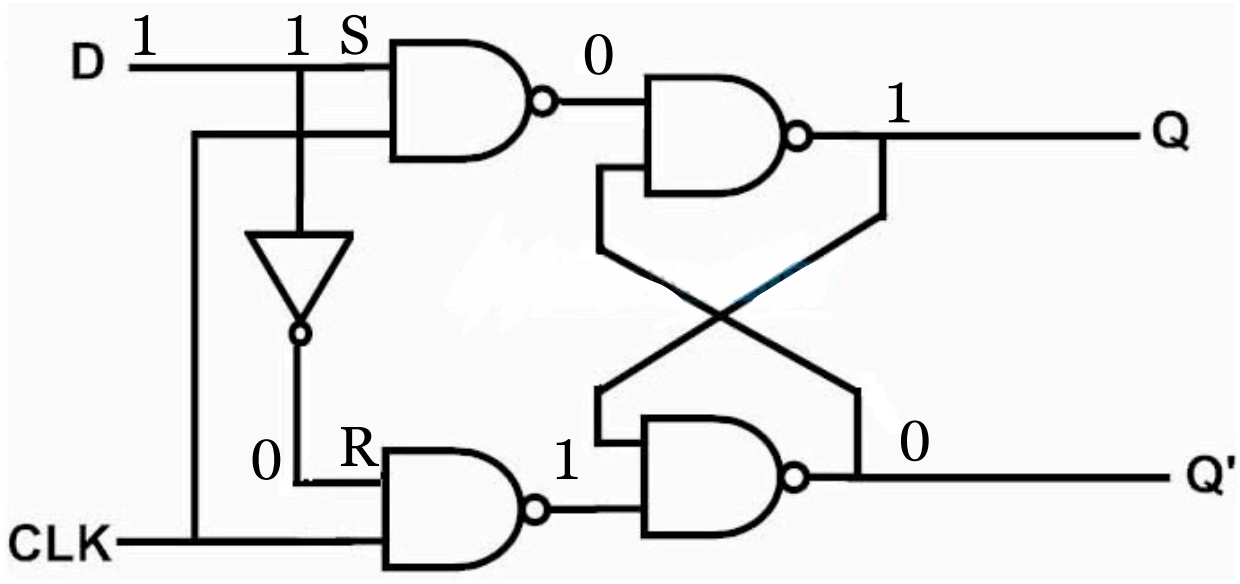
S = 1 → Output of the first NAND gate (N1) becomes 0.

R = 0 → Output of the second NAND gate (N2) becomes 1.

Input to third NAND gate (N3) is 0 and so Q becomes 1.

Due to this, input to fourth NAND (N4) gate becomes 1 and 1. So Q' becomes 0.

Q is set to 1, and so Q' is set to 0.



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