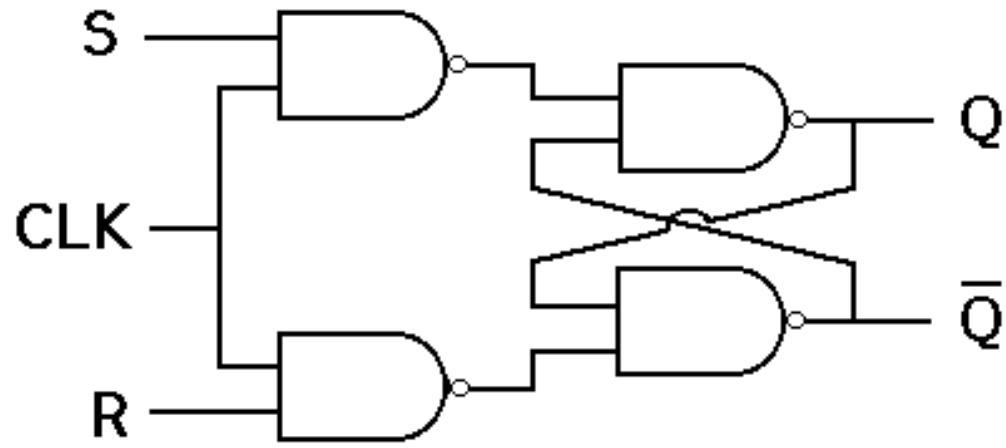
@Sree Vishnu Varthini

Day - 6

Embedded Systems Programming

SR FLIPFLOP



An SR flip-flop, or Set-Reset flip-flop, is a basic memory element in digital electronics. It has two inputs: S (Set) and R (Reset), and two outputs: Q and Q' (the inverse of Q).

Truth Table

S	R	Q_{n+1}
0	0	Q_n(No Change)
0	1	0
1	0	1
1	1	x

Components of SR Flipflop:

Inputs:

- **S (Set):** Sets the output (Q) to 1.
- **R (Reset):** Resets the output (Q) to 0.

Outputs:

- **Q:** Main output of the flip-flop.
- **Q':** Inverse of Q (if Q = 1, then Q' = 0 and vice versa).

Analogy:

Imagine the SR flip-flop as a light switch:

- The Set input (S) turns the light **on** (Q = 1).
- The Reset input (R) turns the light **off** (Q = 0).
- When neither Set nor Reset is pressed (S = 0, R = 0), the light stays in whatever **state it was previously in.**
- If both buttons are pressed at the same time (S = 1, R = 1), the system is confused and enters an **invalid state.**

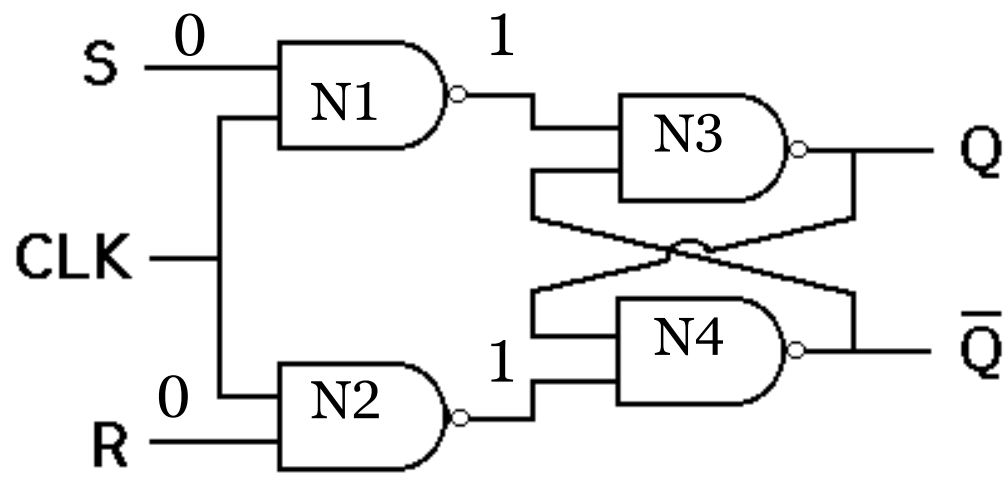
Working:

Case 1: Hold State (S = 0, R = 0)

Outputs of both NAND gates (N1 and N2) become 1.

Inputs of both NAND gates (N3 and N4) are 1, which results in depending on the previous Q values for output.

The flip-flop remains in its current state, with Q and Q' retaining their previous values.



Working:

Case 2: Reset State (S = 0, R = 1)

S = 0 → Output of the first NAND gate (N1) becomes 1.

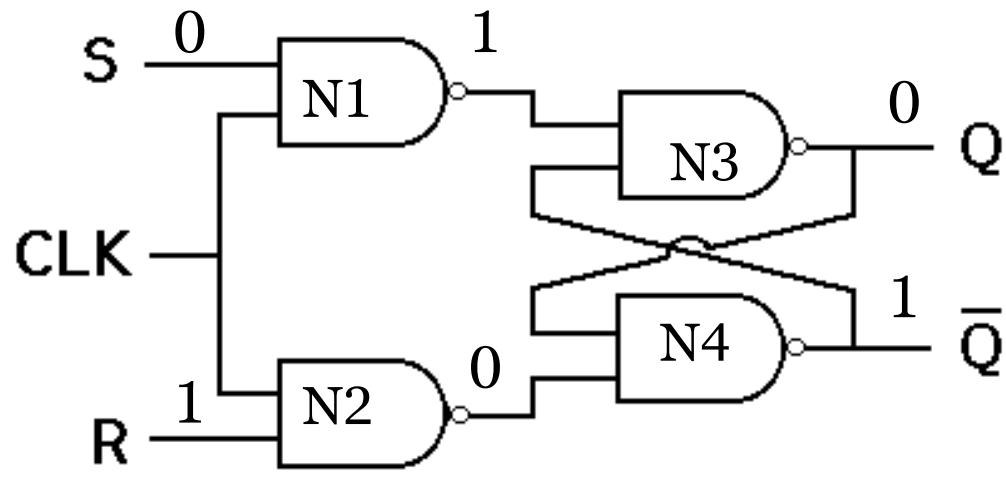
R = 1 → Output of the second NAND gate (N2) becomes 0.

Input to fourth NAND gate (N4) is 0 and so Q' becomes 1.

Due to this, input to third NAND (N3) gate becomes 1 and 1.

So Q becomes 0.

Q' is set to 1, and so Q is set to 0.



Working:

Case 3: Set State (S = 1, R = 0)

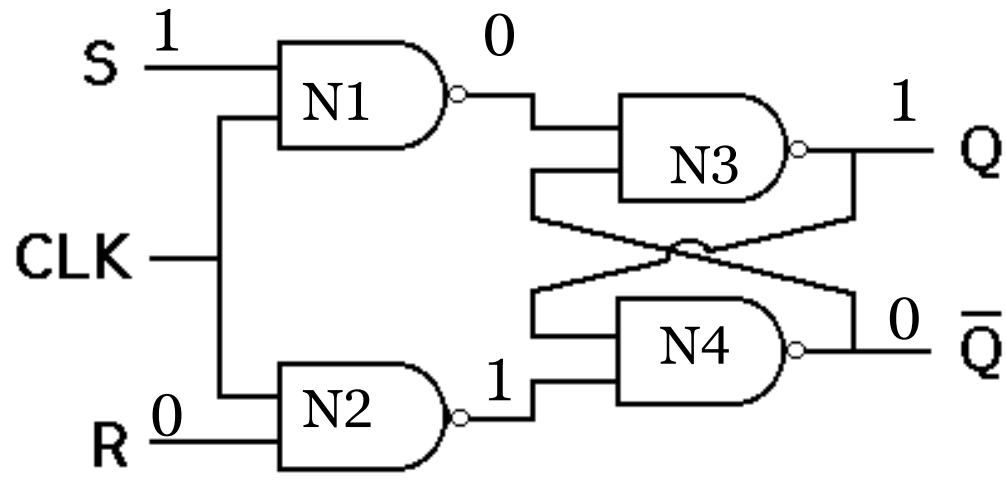
S = 1→ Output of the first NAND gate (N1) becomes 0.

R = 0→ Output of the second NAND gate (N2) becomes 1.

Input to third NAND gate (N3) is 0 and so Q becomes 1.

Due to this, input to fourth NAND (N4) gate becomes 1 and 1. So Q' becomes 0.

Q is set to 1, and so Q' is set to 0.



Working:

Case 4: Invalid State (S = 1, R = 1)

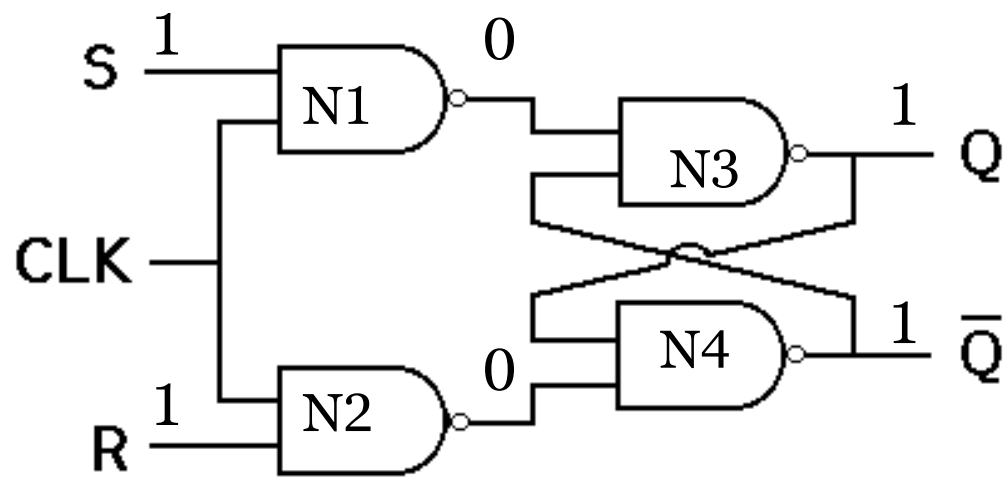
S = 1 → Output of the first NAND gate (N1) becomes 0.

R = 1 → Output of the second NAND gate (N2) becomes 0.

Inputs to both NAND gates (N3 and N4) is 0.

So both outputs, Q and Q', become 1, which is invalid since Q' should be the inverse of Q.

This input should be avoided in practical designs.



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Was it helpful?

follow for more!

P.S. You can access the **Embedded Systems Programming** course by contacting **Balajee Seshadri** Sir through the WhatsApp number provided on his profile.