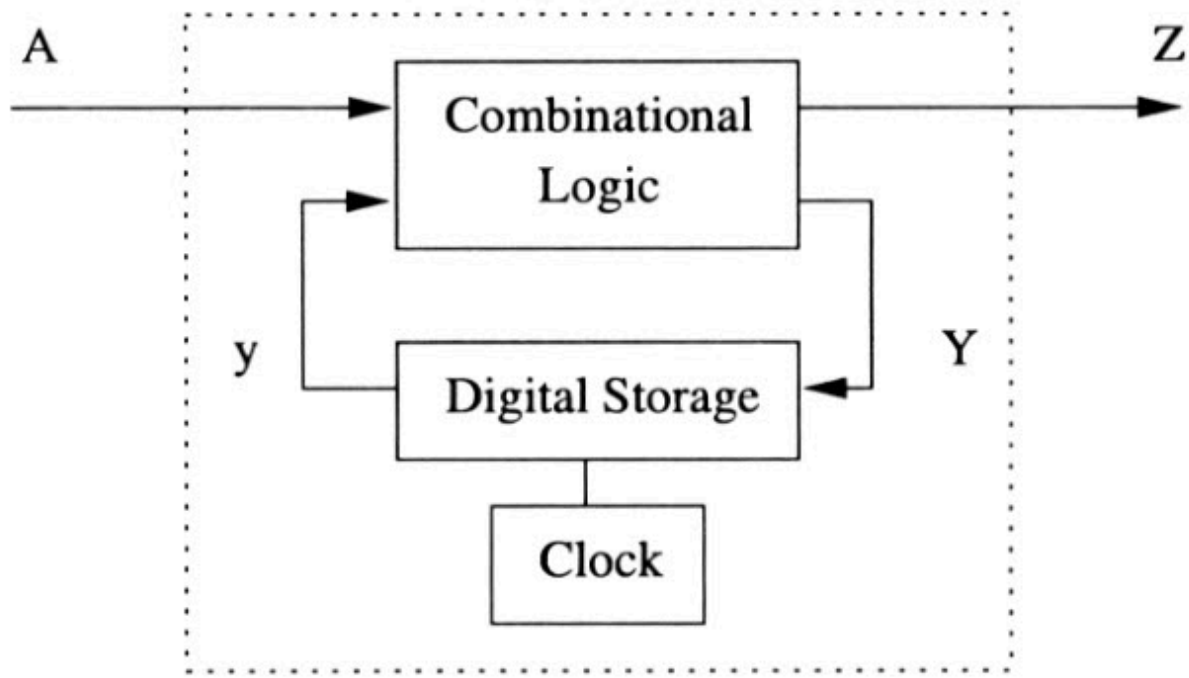
@Sree Vishnu Varthini

Day - 5

Embedded Systems Programming

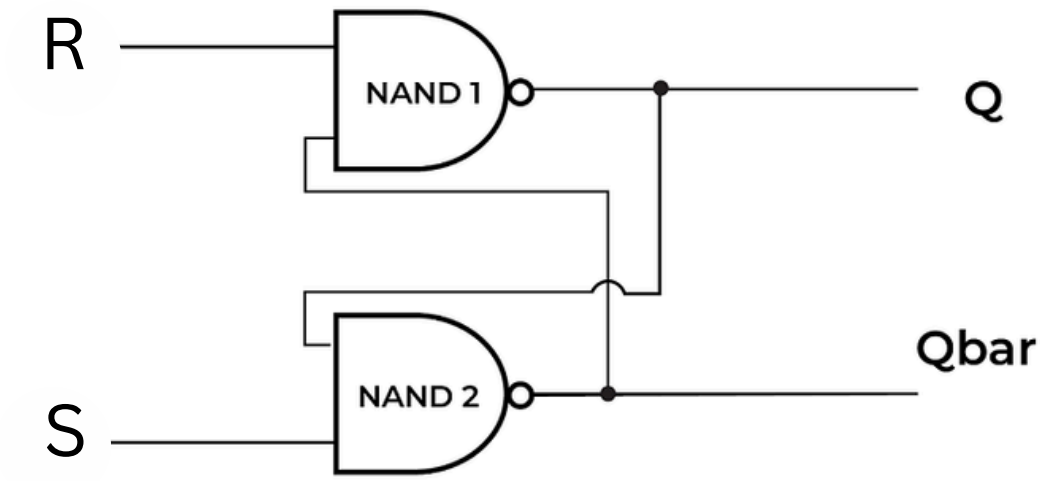
SEQUENTIAL LOGIC



Applications:

- Shift Registers
- Flipflops
- Counters
- Registers

RS LATCH



The SR Latch is one of the simplest types of flip-flops used for storing a single bit of data (either 0 or 1). The name "**SR**" stands for **Set** and **Reset**.

Truth Table:

R	S	Qn+1
0	0	Forbidden
0	1	1
1	0	0
1	1	Hold

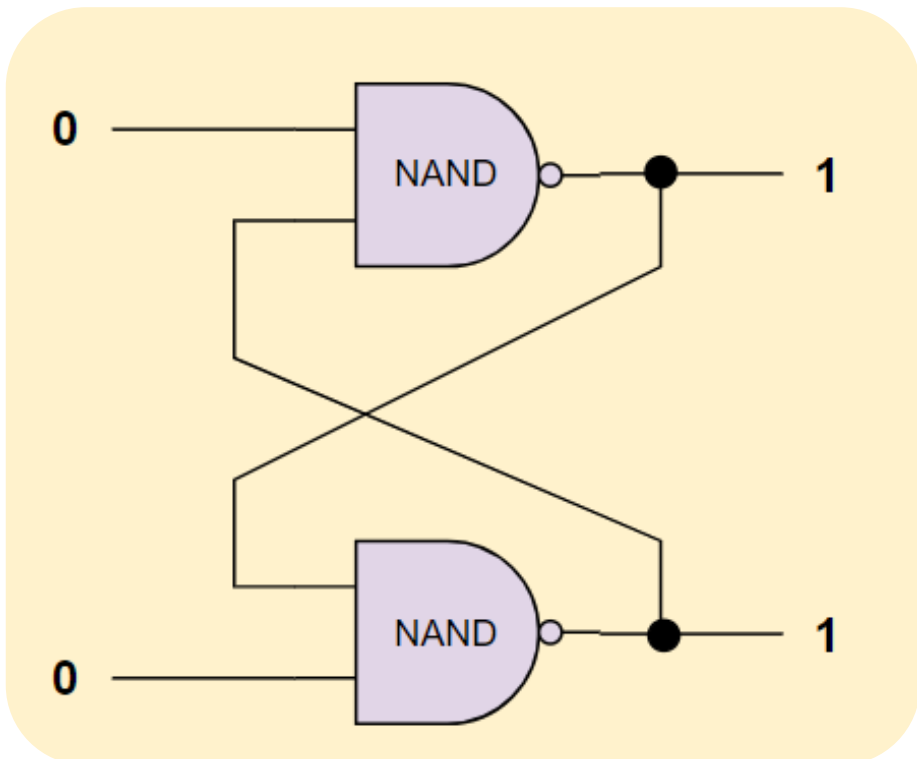
Working:

Case 1: Invalid State (R = 0, S = 0)

R = 0 $\rightarrow$ Output of the first NAND gate (Q) becomes 1.

S = 0 $\rightarrow$ Output of the second NAND gate (Q') becomes 1.

Both outputs, Q and Q', become 1, which is invalid since Q' should be the inverse of Q. This input should be avoided in practical designs.

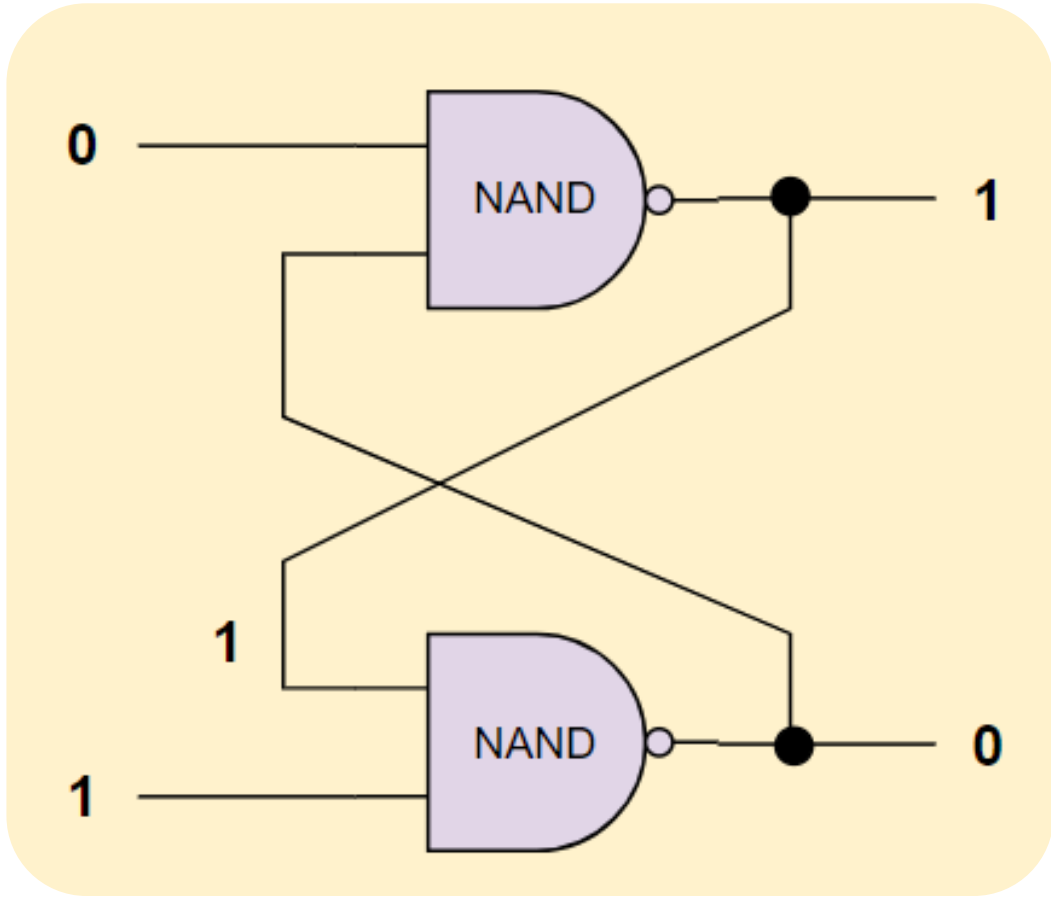


Working:

Case 2: Set State (R = 0, S = 1)

R = 0 → Output of the first NAND gate (Q) becomes 1. Due to this, Output of the second NAND gate (Q') becomes 0.

Q is set to 1, and so Q’ is set to 0.



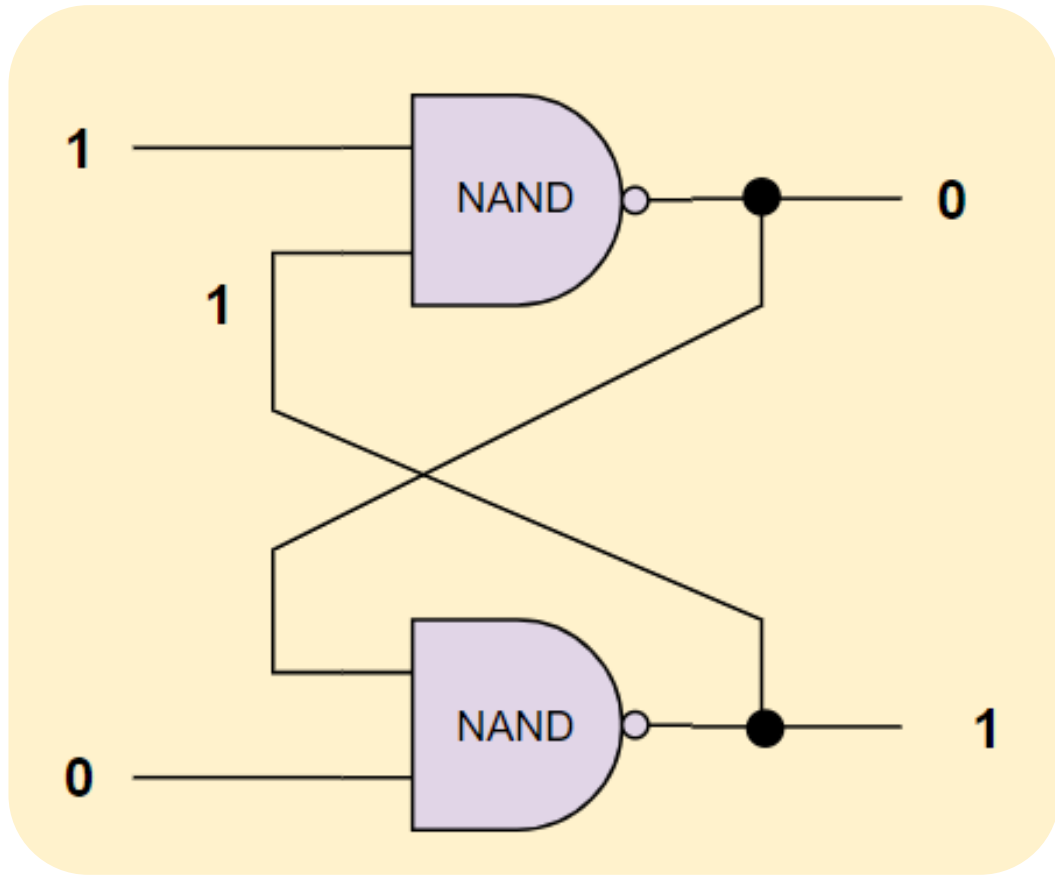
Working:

Case 3: Reset State (R = 1, S = 0)

S = 0 $\rightarrow$ Output of the second NAND gate (Q') becomes 1.

Due to this, Output of the first NAND gate (Q) becomes 0.

Q’ is set to 1, and so Q is set to 0.

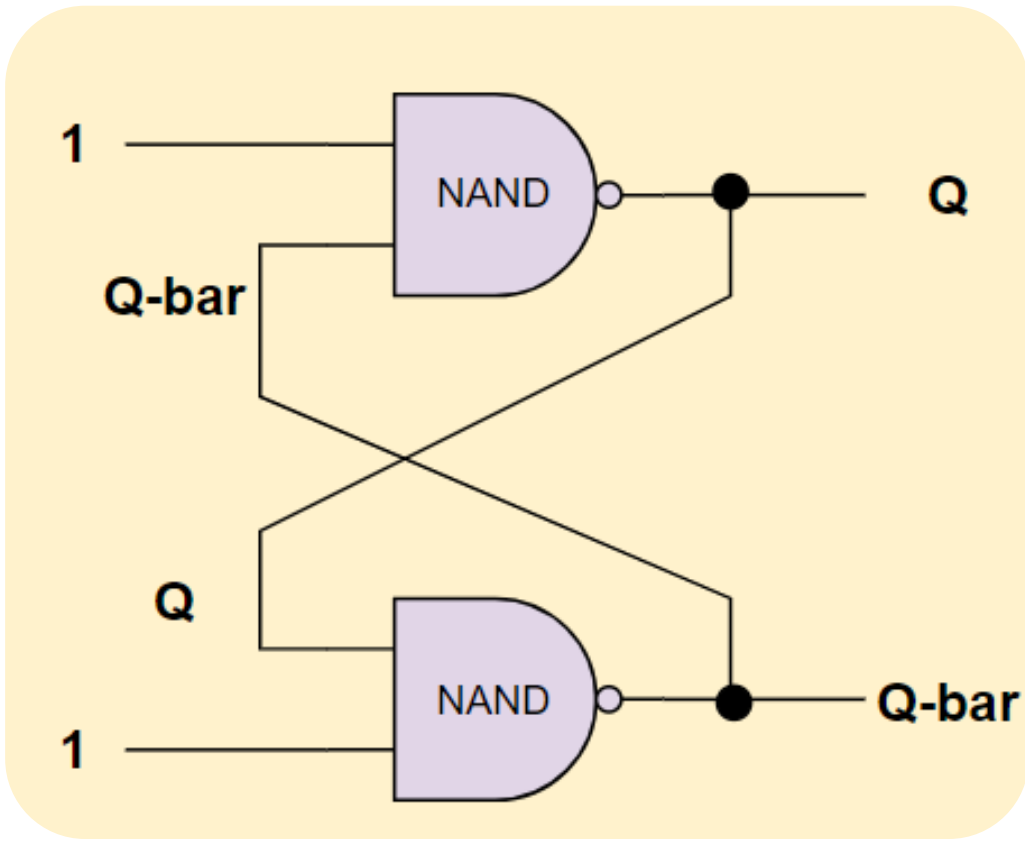


Working:

Case 4: Hold State (R = 1, S = 1)

Inputs of both NAND gates (S and R) are 1, which results in depending on the previous Q values for output.

The flip-flop remains in its current state, with Q and Q' retaining their previous values.



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Was it helpful?

follow for more!

P.S. You can access the **Embedded Systems Programming** course by contacting **Balajee Seshadri** Sir through the WhatsApp number provided on his profile.