NIT JSR & VSD
Circuit Design & Simulation Hackathon

VLSI SYSTEM DESIGN

Performance Analysis of Low-Power Power-on-Reset Circuit using SKY130 PDK Technology

Presented by
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OBJECTIVES

01 Develop a Power-On-Reset (POR) circuit using a **current reference and comparator architecture** to reduce power consumption.

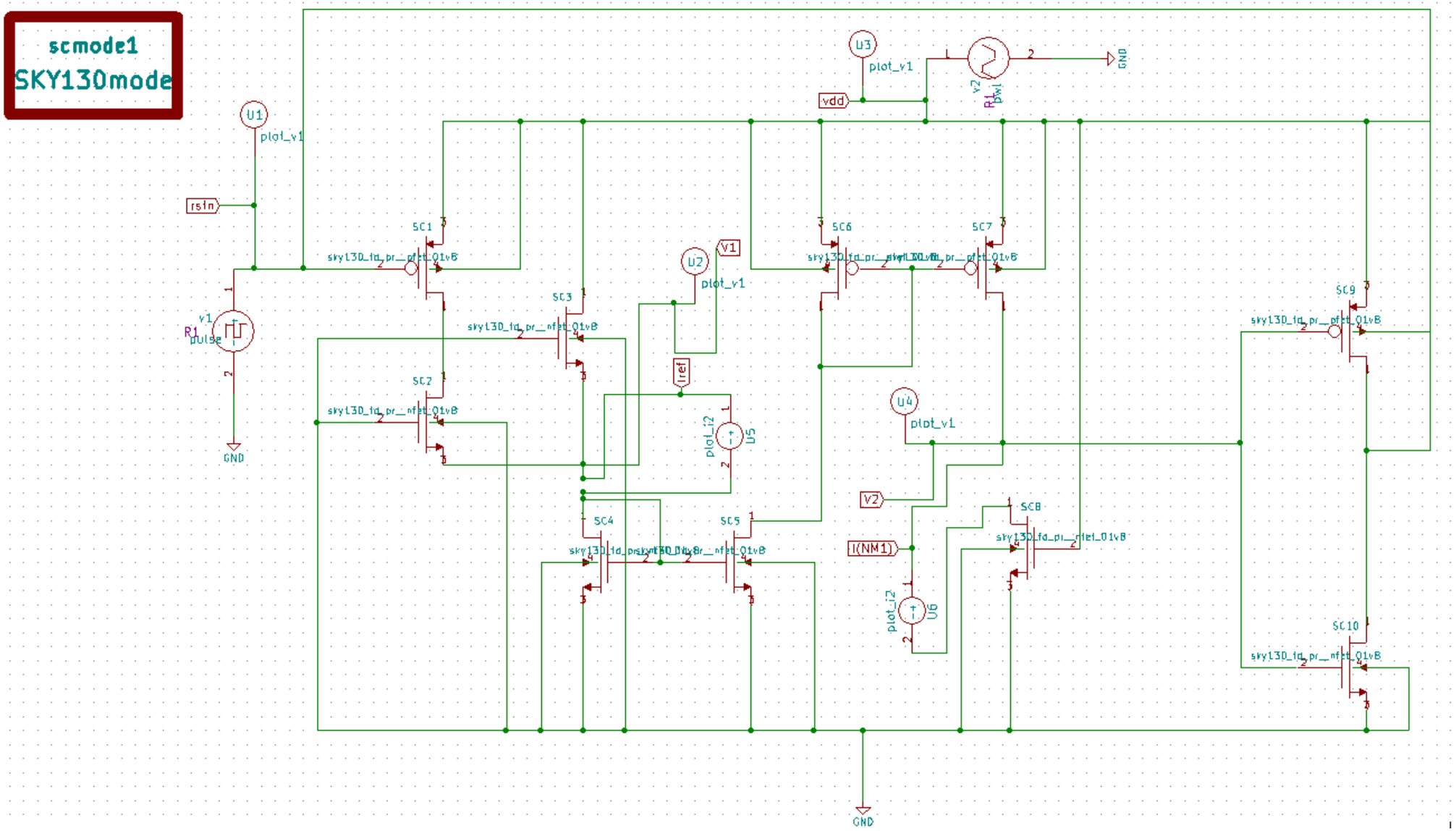
02 Utilize **eSim, Ngspice, and the SKY130 PDK** for the simulation, analysis, and validation of the POR circuit design.

03 To analyze the performance of POR circuit with a focus on **power efficiency** and response time by observing key parameters over time at a **supply voltage of 0.5 V.**

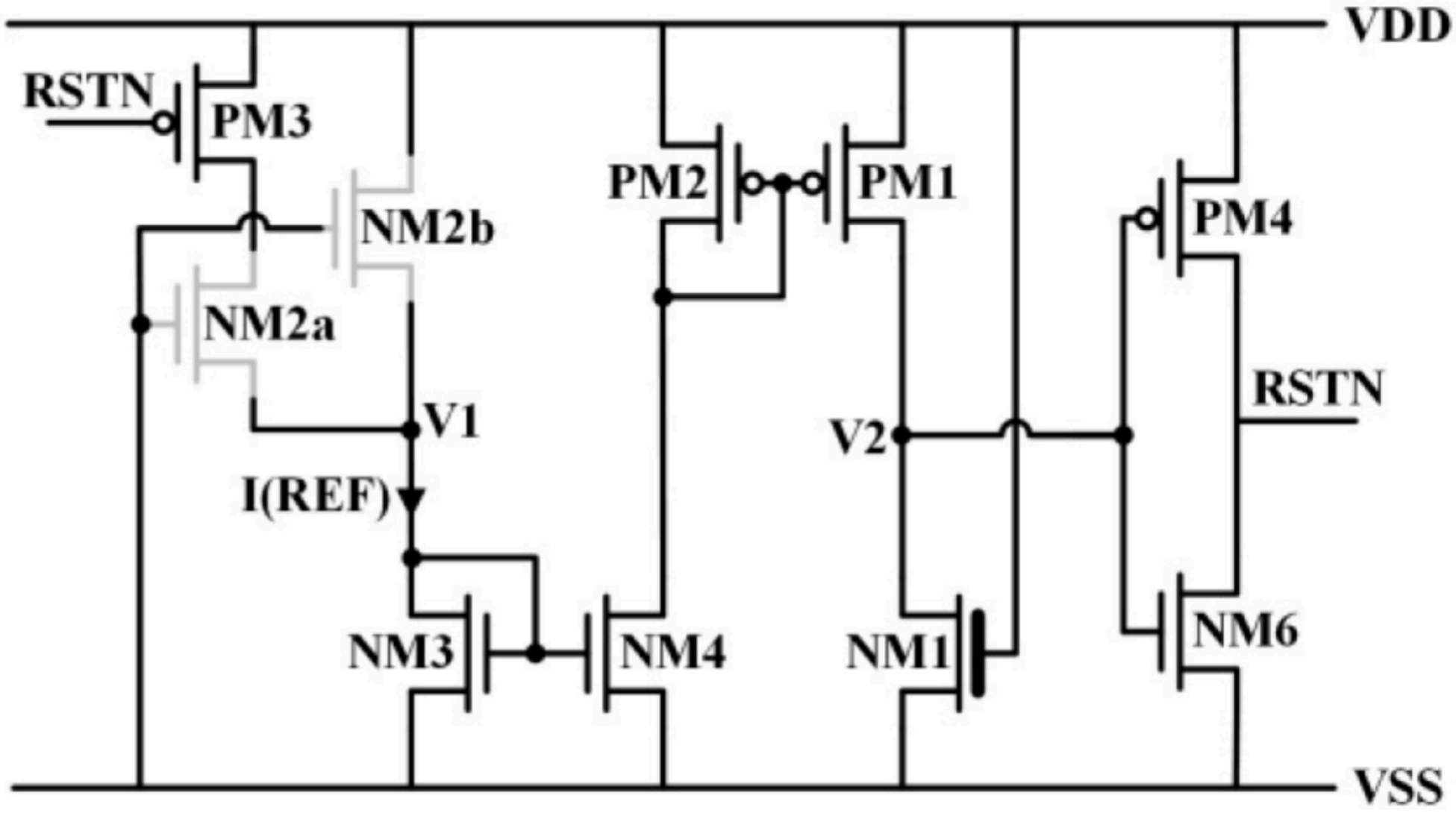
LITERATURE SURVEY

AUTHOR	TITLE	CONTRIBUTION	INFERENCE
H.You, J. Yuan, Z. Yu and S. Qiao	**"An Accurate Low-Power Power on-Reset Circuit in 55-nm CMOS Technology"**, vol. 69, no. 8, pp. 3361 3365, Aug. 2022	An accurate, low-power Power-On-Reset (POR) circuit is designed with a 10-transistor architecture for low-voltage applications.	An accurate, low-power POR circuit with a trip-voltage of 0.45V, 32nW power consumption is achieved
Xinxin Ren, xiaoyu hu, Shushan Qiao	**"An Ultra-Low-Power Reconfigurable Power-On Reset for Multi-Supply Voltages Applications"**, Authorea, Jan. 2023	An ultra-low-power, reconfigurable Power-On-Reset (POR) circuit is designed for multi-supply voltage applications.	A POR circuit with configurable trip-voltages (385.5mV and 775.4mV), ultra-low power consumption (8.5nA and 92.6nA) is achieved.
H. B. Le, X. D. Do, S. G. Lee and S. T. Ryu	**"A Long Reset-Time Power-On Reset Circuit With Brown-Out Detection Capability"**, vol. 58, no. 11, pp. 778-782, Nov. 2011	A compact low-power on-chip power-on reset circuit with a brown-out detection capability is designed.	A compact POR circuit with brown-out detection, consuming 1 μA at 1.8 V and offering a long reset time is implemented.

POR SCHEMATIC

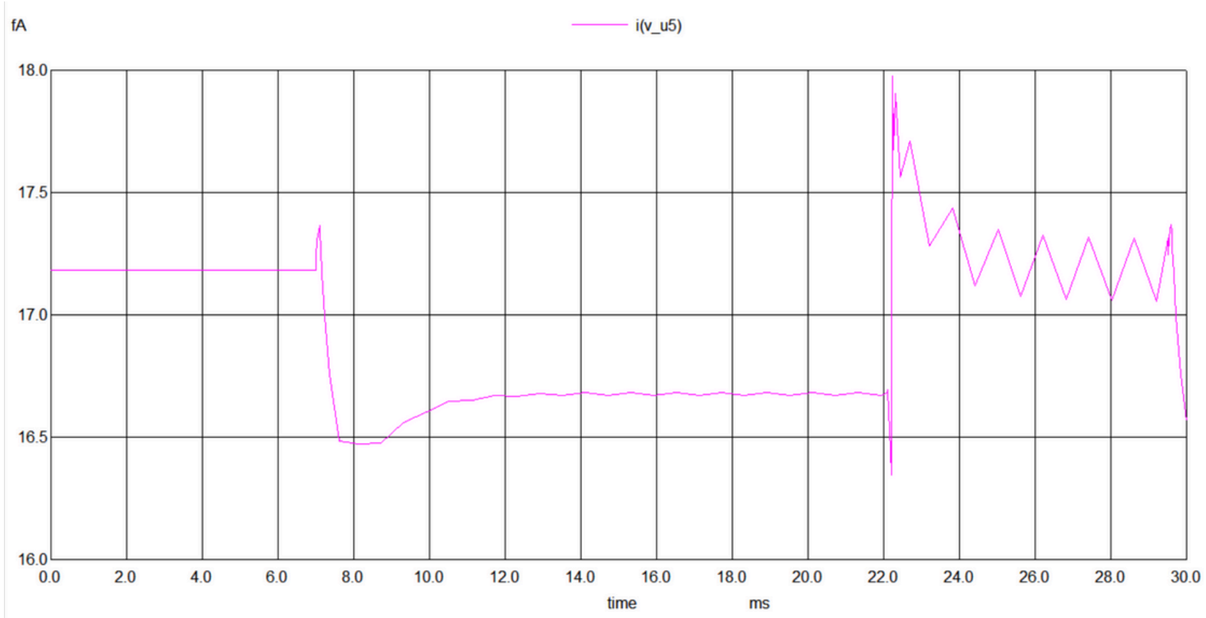


POR CIRCUIT DIAGRAM

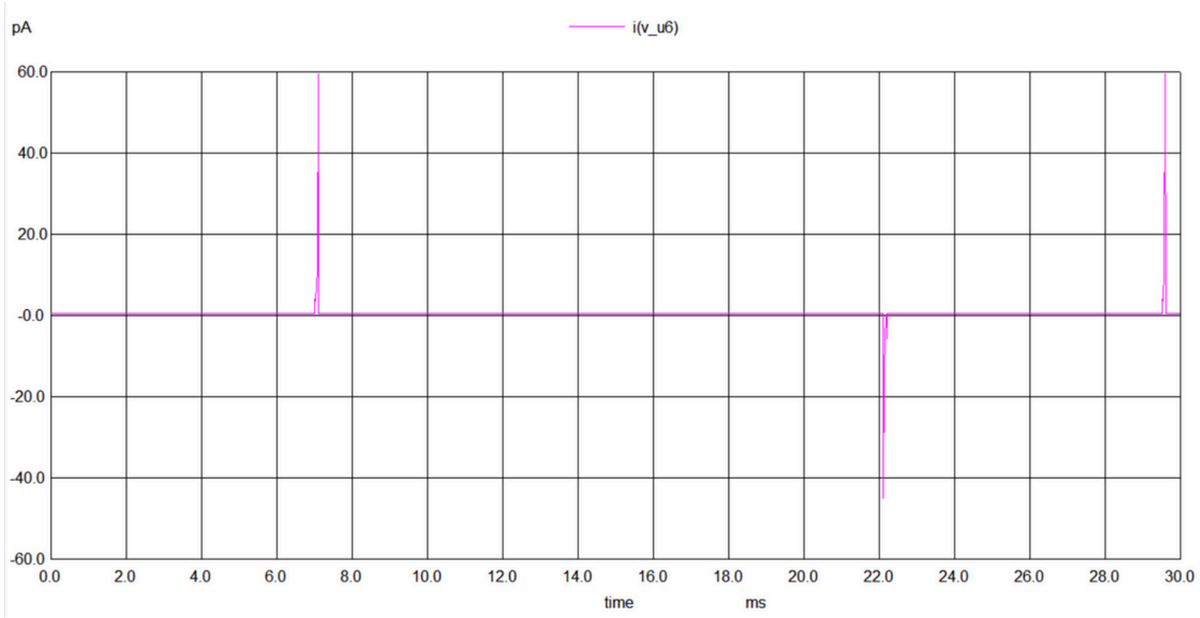


RESULTS

I(IREF) vs. Time [0 ms - 30 ms] @ V_{DD} = 0.5 V



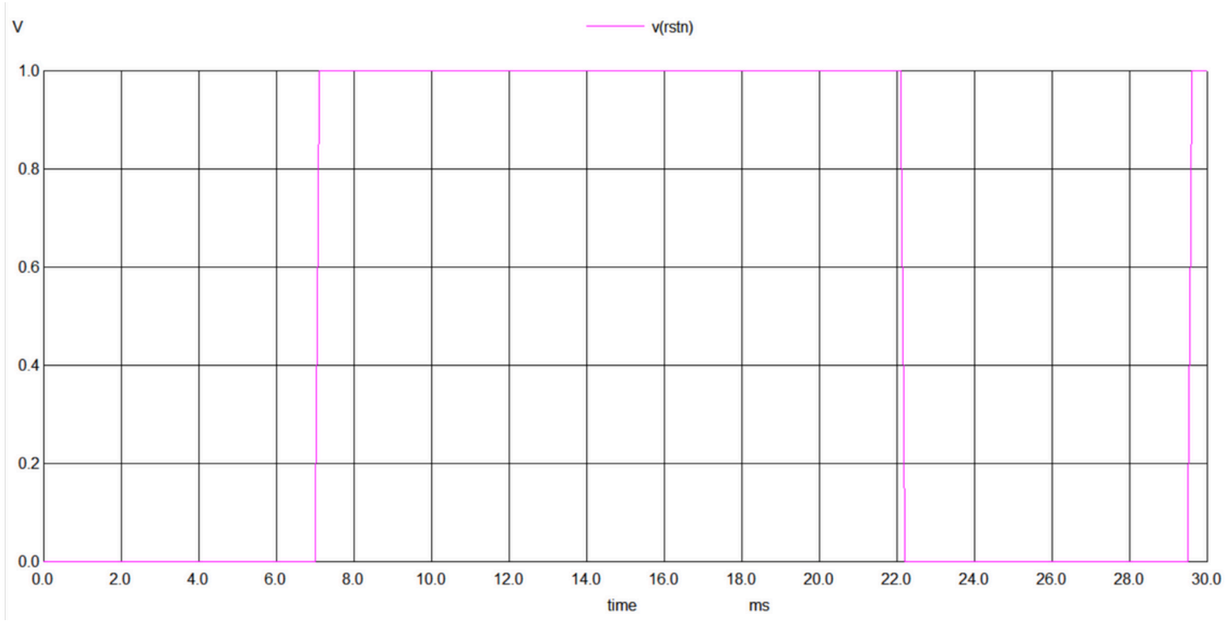
I(NM1) vs. Time [0 ms - 30 ms] @ V_{DD} = 0.5 V



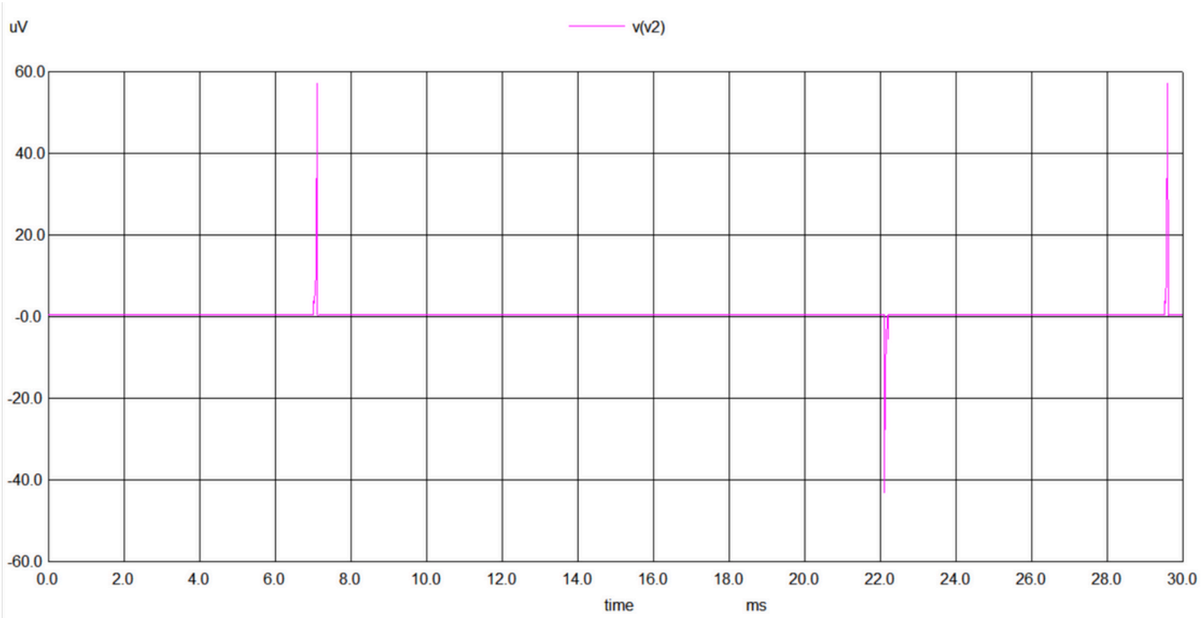
At first, the reference current is greater than the current of NM1, causing node V2 to charge high through PM1.

RESULTS

RSTN vs. Time [0 ms - 30 ms] @ V_{DD}= 0.5 V



V2 vs. Time [0 ms - 30 ms] @ V^{DD} = 0.5 V



When the NM1 current becomes greater than the reference current, node V2 discharges to low, and the reset signal (RSTN) transitions to high.

APPLICATIONS

01

Wearable Electronics

02

IOT Devices

03

Consumer Electronics

03

Medical Devices

FUTURE WORK

01 Investigate improvements in **brown-out detection** accuracy and **power consumption.**

02 Explore the performance of the proposed circuit in **smaller technology nodes** to evaluate its scalability and effectiveness at lower power levels.

03 Design a variant of the circuit with **more** transistors (e.g., 14 or more) to support **higher supply voltages**.

04 Study the circuit's behavior under **varying temperature conditions** to ensure reliable operation in diverse environmental settings.

REFERENCES

[1] H. You, J. Yuan, Z. Yu and S. Qiao, **"An Accurate Low-Power Power on-Reset Circuit in 55-nm CMOS Technology"**, in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 69, no. 8, pp. 3361 3365, Aug. 2022

[2] Xinxin Ren, xiaoyu hu, Shushan Qiao. **"An Ultra-Low-Power Reconfigurable Power-On Reset for Multi-Supply Voltages Applications"**, Authorea, Jan. 2023

[3] H. B. Le, X. D. Do, S. G. Lee and S. T. Ryu, **"A Long Reset-Time Power-On Reset Circuit With Brown-Out Detection Capability"**, in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 58, no. 11, pp. 778-782, Nov. 2011

THANK YOU