Performance Analysis of Low-Power Power-on-Reset Circuit using SKY130 PDK Technology

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***Abstract*—This paper presents an accurate low-power power-on-reset (POR) circuit utilizing SKY130 PDK technology, addressing the demand for efficient solutions in IoT applications. By implementing a current reference and comparator architecture, the design achieves configurable trip voltages with minimal power overhead, enhancing performance in low-voltage systems while effectively managing supply noise and brown-out events.**

Keywords— Power-on-reset, low-voltage, low-power, high accuracy, area efficient, Brown-out detection

I. INTRODUCTION

The increasing demand for low-power integrated circuits in Internet of Things (IoT) applications necessitates efficient power-on-reset (POR) circuits. These circuits are essential for ensuring that memory elements maintain a known state during power-up, thus preventing erratic behaviour in digital systems. Traditional POR designs often rely on bandgap references, which, while robust, can consume significant power. In contrast, this paper presents an accurate low-power POR circuit utilizing SKY130 PDK technology. By implementing a current reference and comparator architecture, our design achieves configurable trip voltages with minimal power overhead, enhancing performance in low-voltage applications while addressing challenges like supply noise and brown-out events.

II. PRINCIPLE OF GENERATION

The proposed power-on-reset (POR) circuit operates based on a current reference and comparator architecture. During power-up, a reference current is generated and compared against a Vdd-tracking current. This comparison determines when the supply voltage reaches the predefined trip voltage (VPOR). To ensure stability, hysteresis is implemented by defining a brown-out reset (BOR) threshold (VBOR) slightly below VPOR. This architecture allows for configurable trip voltages by adjusting the characteristics of the MOS transistors used, minimizing power consumption and area overhead while maintaining accuracy.

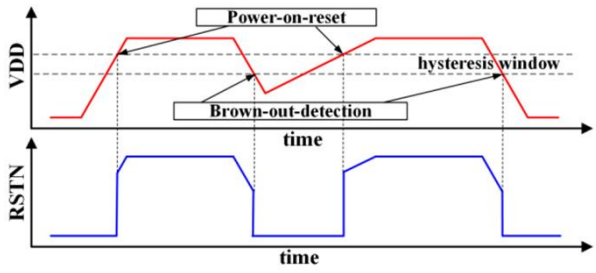

Fig. 1 Function of a power-on-reset circuit with brown out detection

III. IMPLEMENTATION

The proposed power-on-reset (POR) circuit schematic, illustrated in Fig. 2, employs a 10-transistor configuration to generate a stable reference current using the sub-threshold currents of NM2a and NM2b. Current mirrors formed by NM3, NM4, PM2, and PM1 replicate this reference current. NM1 directly connected to VDD serves as a measure of the power supply voltage. The voltage at node V2 fluctuates based on the comparison between the reference current and NM1's current. When the reference current exceeds NM1's current, V2 rises, charging through PM1. Conversely, if the reference current drops below NM1's, V2 discharges through NM1. PM4 and NM6 function as an inverter to generate the reset signal, RSTN, ensuring accurate reset operation during power fluctuations.

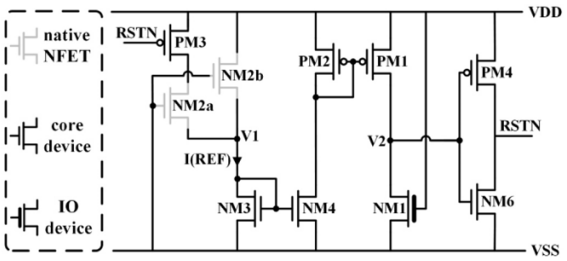

Fig. 2 Schematic of the proposed 10-transistor POR circuit

IV. ISSUES AND IMPROVEMENTS

The 10-transistor POR circuit is effective for low-voltage applications but lacks suitability for higher voltage systems. To address this limitation, we can design a 14-transistor variant capable of generating higher trip voltages. This enhancement improves the circuit's versatility, making it applicable across a broader range of power supply voltages while maintaining low power consumption and accuracy.

V. CONCLUSION

In conclusion, the proposed low-power power-on-reset circuit demonstrates significant advancements in reliability and efficiency for low-voltage applications. By employing a current reference and comparator architecture, the design ensures accurate trip voltage detection while minimizing power consumption.

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