PASSWORD LOCK USING LOGIC GATES

A PROJECT REPORT

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As part of a the project based course

24EEJ303: DIGITAL ELECRONICS AND LOGIC DESIGN

Of

Bachelor of Technology

In

Electrical and Electronics Engineering

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

T.K.M. COLLEGE OF ENGINNERING, KOLLAM

OCTOBER, 2025

ABSTRACT

The digital password lock using logic gates is an electronic security system designed to provide controlled access through a predefined digital code. In this project, the password is represented by a specific combination of binary inputs, which are processed through various logic gates to verify correctness. Only when the correct input combination is applied does the output circuit activate, thereby unlocking or enabling access to the system. If an incorrect password is entered, the circuit remains inactive, ensuring security and preventing unauthorized entry.

The circuit makes use of basic logic gates such as AND, OR, NOT, and NAND to perform logical verification operations. The design is purely combinational, meaning the output depends solely on the current input values, which simplifies both construction and analysis. This eliminates the need for complex microcontrollers or programming, making it cost-effective and easy to implement.

The project demonstrates the practical application of Boolean algebra and digital logic design in real-world security systems. It also helps students understand how logical conditions can be combined to perform decision-making tasks in electronic circuits. The system can be extended for more advanced designs, such as multi-digit passwords or sequential logic verification. Due to its simplicity, low power consumption, and reliability, the digital password lock is ideal for small-scale applications like lockers, doors, and restricted access areas. Overall, the project highlights the effectiveness of digital electronics in designing secure and efficient password-based locking mechanisms.

Chapter 1

Introduction

This project presents the design and implementation of a **4-bit digital password lock** based entirely on fundamental logic gates, serving as a powerful and practical illustration of combinational logic theory. The goal of this system is to create a basic access control mechanism that validates a specific set of simultaneous inputs—the 'password'—to switch the device from an "unlocked" to a "locked" state. The circuit utilizes common integrated circuits (ICs), including the **AND gates (74LS08)** and **NOT gates (74LS04)**, to perform a critical logical comparison. Specifically, it tests the current state of four push-button inputs against a fixed, pre-set 4-bit combination. The circuit's output is governed solely by the current state of these inputs, making it an excellent example of a **combinational circuit**, where memory elements are not required to determine the output. This report will detail the logic derived from the circuit diagram and explain how the interplay between the basic gates provides a binary security mechanism for access control.

Circuit Operation and Logic

The circuit is built around four push-button switches (S1-S4) acting as the input "keypad." By default, pull-down resistors (R1-R4) hold all inputs at a **LOW (0)** logic level. Pressing a button connects it to the +5V supply, changing its input to **HIGH (1)**.

The core logic is designed to produce a HIGH output from the final AND gate (U1:C) only when a specific password is entered. The logic expression for this output is:

Output = (S1 AND (NOT S2)) AND (S3 AND S4)

Based on this expression, the "correct" password required to make the final output HIGH is:

- **S1:** Pressed (1)
- **S2:** Not Pressed (0)
- **S3:** Pressed (1)
- **S4:** Pressed (1)

Output Indication

The circuit features two distinct states indicated by LEDs and a buzzer:

1. **Default / "Unlocked" State:** In the default state (no buttons pressed) or when any incorrect combination is entered, the output of the final AND gate (U1:C) is **LOW (0)**. This LOW signal turns the Red LED (D1) **OFF**. This signal is then inverted by the NOT gate (U2:B), producing a HIGH signal that turns **ON** the Green LED (D2) and the Buzzer (BUZ1).
2. **Password Entered / "Locked" State:** When the correct password (S1=1, S2=0, S3=1, S4=1) is entered simultaneously, the output of U1:C goes **HIGH (1)**. This HIGH signal directly turns **ON** the Red LED (D1), indicating the "locked" or "secured" status. This HIGH signal is also inverted by U2:B, turning **OFF** the Green LED and the Buzzer.

In summary, this circuit functions as a system that is in an "unlocked" state by default and transitions to a "locked" state only when the precise 4-bit combination is applied.

1.2 Problem Statement

The challenge was to design and construct an electronic system capable of accepting a 4-bit binary input from a user and comparing it against a fixed, hard-coded 4-bit password. The system must transition its output state only upon an exact match of the input with the password, providing clear feedback to the user regarding the validation outcome. The design must minimize complexity while adhering strictly to combinational logic principles.

1.3 Project Objectives

The primary objectives of this project are defined as follows:

1. **Design a Combinational Circuit:** To develop a minimum-gate, 4-input combinational logic circuit capable of uniquely identifying the required password combination.
2. **Boolean Implementation:** To derive and simplify the Boolean expression corresponding to the desired password logic.
3. **Hardware Implementation:** To successfully implement the derived logic using standard 74LS-series TTL integrated circuits on a breadboard or Printed Circuit Board (PCB).
4. **Feedback System Integration:** To integrate the final logic output with a suitable driver circuit (transistor) to control visual (LEDs) and auditory (Buzzer) indicators.
5. **Testing and Validation:** To thoroughly test the circuit's performance against all 16 possible input combinations to verify that the output adheres precisely to the required Truth Table.

1.4 Scope of the Report

This report will detail the entire life cycle of the project, beginning with the theoretical foundation of digital logic, progressing through the design phases involving Boolean algebra and schematic generation, and concluding with a discussion of the hardware implementation, testing procedures, results, and analysis. The scope is limited to a *combinational* lock; sequential logic elements (e.g., flip-flops) are intentionally excluded to focus on simultaneous input validation.

CHAPTER 2: THEORETICAL BACKGROUND

2.1 Digital Logic and Binary Systems

Digital electronics operates on the binary system, which uses only two states: **HIGH (1)** and **LOW (0)**. These states are physically represented by voltage levels—typically +5V for HIGH (logic 1) and 0V (Ground) for LOW (logic 0) in TTL circuits. Logic gates are the fundamental electronic switches that process these binary inputs according to a specific Boolean function.

2.2 Introduction to Logic Gates

The circuit employs two types of basic logic gates:

2.2.1 The AND Gate

The AND gate performs the logical multiplication operation. Its output is HIGH (1) only if *all* of its inputs are HIGH (1). For two inputs, A and B, the Boolean expression is $Y = A \cdot B$. The 74LS08 IC, which contains four independent 2-input AND gates, is used for this function.

A	**B**	**Y = A \cdot B**
0	0	0
0	1	0
1	0	0
1	1	**1**

2.2.2 The NOT Gate (Inverter)

The NOT gate, or Inverter, performs logical negation. It takes a single input and produces the opposite output. Its primary function in this circuit is to ensure that a specific input must be LOW (0) for the final output to be HIGH. The Boolean expression is $Y = \overline{A}$. The 74LS04 IC, which contains six independent NOT gates, is used for this function.

A	**Y = \overline{A}**
0	**1**
1	0

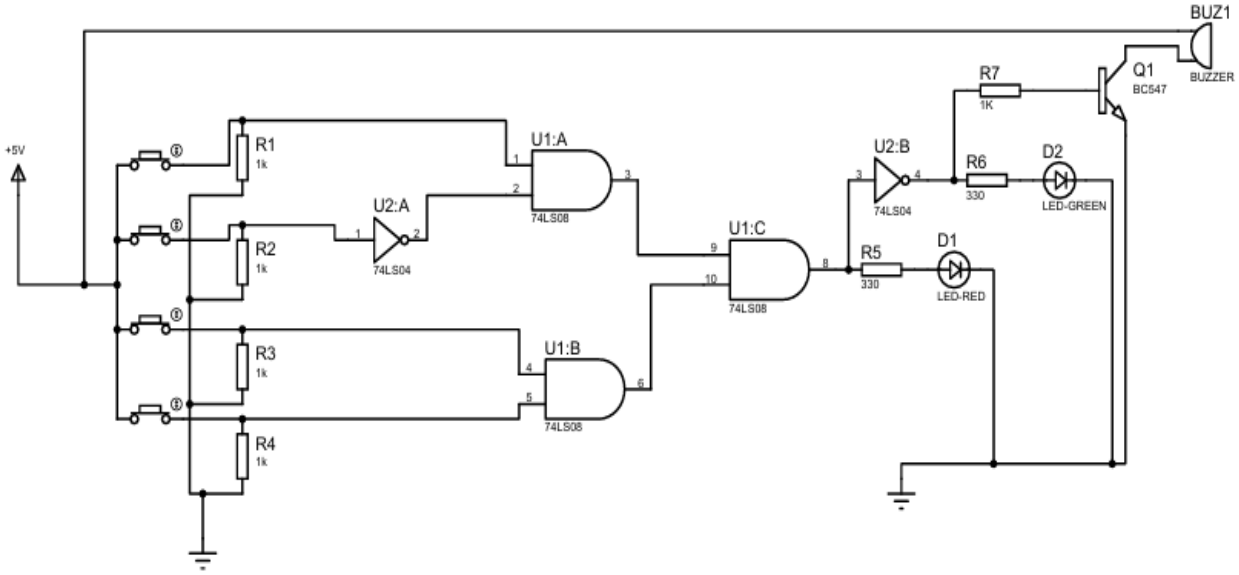
2.3 Combinational vs. Sequential Logic

Combinational Logic is a type of digital logic where the output is *only* a function of the current inputs. There are no memory elements, meaning the previous state of the system does not influence the current output. This is the design principle used in this lock, which requires all four keys to be pressed (or not pressed) *simultaneously* for a valid output.

Sequential Logic, in contrast, depends on both the current inputs and the past inputs (or current state). These circuits use memory elements like latches and flip-flops, which would be necessary for a more advanced lock requiring the password digits to be entered in a specific *sequence*.

CHAPTER 3: DESIGN AND METHODOLOGY

Circuit Diagram



3.1 System Block Diagram

The system can be conceptually broken down into three functional blocks: the Input Interface, the Logic Core, and the Output Indicator.

Block Diagram of the Combinational Lock

1. **Input Interface:** Consists of the four push-button switches (S1, S2, S3, S4) and their associated pull-down resistors (R1, R2, R3, R4).
2. **Logic Core:** Contains the AND and NOT gates that implement the Boolean function.
3. **Output Indicator:** Includes the Red and Green LEDs (D1, D2), the Buzzer (BUZ1), and the transistor driver (Q1).

3.2 Boolean Expression and Logic Derivation

The password chosen for this circuit is the 4-bit combination $\mathbf{1011}$, where:

- S1 = 1
- S2 = 0
- S3 = 1
- S4 = 1

For the system output (L) to be **HIGH (1)**, all four conditions must be met concurrently.

1. S1 must be 1 \implies S1
2. S2 must be 0 \implies \overline S2 (Requires a NOT gate)
3. S3 must be 1 \implies S3
4. S4 must be 1 \implies S4

Combining these conditions using the AND operation yields the final Boolean expression:

L = S1 \cdot \overline S2\ cdot S3 \cdot S

This function requires a 4-input AND operation. Since 4-input AND gates were not used, the circuit cascades three 2-input AND gates, as shown in the schematic.

3.3 Full System Truth Table

For a 4-input system, there are 2^4 = 16 possible combinations. The Truth Table below shows the desired output L for every possible input state.

S4	S3	S2	S1	overlineS2	Text U1:A = S1 cdot overline S2	U1:B= S3 cdot S4	L =U1:C	Indicator State
0	0	0	0	1	0	0	0	Unlocked (Green/Buzzer ON)
0	0	0	1	1	1	0	0	Unlocked (Green/Buzzer ON)

0	0	1	0	0	0	0	0	Unlocked (Green/Buzzer ON)
0	0	1	1	0	0	0	0	Unlocked (Green/Buzzer ON)
0	1	0	0	1	0	0	0	Unlocked (Green/Buzzer ON)
0	1	0	1	1	1	0	0	Unlocked (Green/Buzzer ON)
0	1	1	0	0	0	0	0	Unlocked (Green/Buzzer ON)
0	1	1	1	0	0	0	0	Unlocked (Green/Buzzer ON)
1	0	0	0	1	0	0	0	Unlocked (Green/Buzzer ON)
1	0	0	1	1	1	0	0	Unlocked (Green/Buzzer ON)
1	0	1	0	0	0	0	0	Unlocked (Green/Buzzer ON)
1	0	1	1	0	0	0	0	Unlocked (Green/Buzzer ON)
1	1	0	0	1	0	1	0	Unlocked (Green/Buzzer ON)
1	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**Secure (Red ON)**
1	1	1	0	0	0	1	0	Unlocked (Green/Buzzer ON)
1	1	1	1	0	0	1	0	Unlocked (Green/Buzzer ON)

CHAPTER 4: IMPLEMENTATION AND COMPONENTS

4.1 Component List

Component	Designator	Specification/Value	Function in Circuit
Integrated Circuit (Quad 2-Input AND)	U1	74LS08 (TTL)	Password logic calculation.
Integrated Circuit (Hex NOT Gate)	U2	74LS04 (TTL)	Inverts S2 input and inverts the final logic output.

Push Button Switch	S1, S2, S3, S4	Momentary Contact	User input for the 4-bit password.
Pull-Down Resistors	R1, R2, R3, R4	1 k ohm	Hold inputs LOW when switches are open.
Current Limiting Resistor	R5, R6	330 ohm	Limit current to the LEDs (D1 and D2).
Current Limiting Resistor	R7	1 k	Limit base current for the transistor Q1.
Transistor (NPN)	Q1	BC547 or similar NPN	Driver for the Buzzer (BUZ1).
Red LED	D1	LED-RED	Indicates **Secure State** ($L=1$).
Green LED	D2	LED-GREEN	Indicates **Monitoring State** ($L=0$).
Buzzer	BUZ1	5 v DC Buzzer	Auditory feedback for the **Monitoring State**.
Power Supply		5 v DC	Required voltage for TTL ICs.

4.2 TTL IC Pinouts

The 74LS series ICs require precise pin connections for power and logic operation.

4.2.1 74LS08 (Quad 2-Input AND Gate)

- **Pin 14:** VCC (Connected to +5 V
- **Pin 7:** GND (Connected to 0 V)
- The IC provides four independent AND gates, U1:A, U1:B, U1:C, and one unused gate.

4.2.2 74LS04 (Hex Inverter/NOT Gate)

- **Pin 14:** V_{CC}$ (Connected to $+5 \text{V}$)
- **Pin 7:** GND (Connected to 0 V)
- The IC provides six independent NOT gates. U2:A is used for input inversion S2, and U2:B is used for output inversion

4.3 Input Sub-Circuit Detail

Each push-button switch (S1-S4) is wired to a specific input line. When the switch is open, the 1 k pull-down resistor (R1-R4) ensures the input line is connected to ground, guaranteeing a clean logic 0 state. Pressing the switch provides a direct connection to the +5Vsupply, creating a clean logic 1 state. This robust input conditioning is crucial for preventing floating inputs and unreliable gate operation.

4.4 Output Sub-Circuit Detail

The final logic output (L) from text U1:Cdirectly drives the output indicators through two paths:

1. **Red LED Path (D1):** L is connected through a $330 \ \Omega$ current-limiting resistor (R5 to the Red LED (D1).
    - If L=1 (Correct Password), D1 is **ON**.
    - If L=0 (Incorrect Password), D1 is **OFF**.
2. **Green LED/Buzzer Path (D2, BUZ1):** L is first passed through a NOT gate **U2:B** to generate the inverted output overline.
    - This overline signal drives the Green LED (D2) via 330 ohm R6
    - The L signal is also routed through 1 text Omega$ (R7) to the base of the NPN transistor Q1 (BC547). The transistor acts as a current amplifier, switching the high-current load of the Buzzer (BUZ1) ON or OFF.

This dual-path design ensures that the Red LED and the Green LED/Buzzer system are mutually exclusive: one indicator group is **always ON** while the other is **always OFF**, providing unambiguous system status feedback.

CHAPTER 5: TESTING AND RESULTS

5.1 Test Procedure

To thoroughly validate the combinational logic core, the circuit was subjected to all 16 possible input combinations. The test involved the following steps:

1. The circuit was powered using a stable $+5 \text{V}$ DC supply.
2. A digital multimeter was used to verify the logic levels at the inputs of U1:C and the final output pin of U1:C (Output L).
3. Each of the 16 combinations was applied to the four switches (S1-S4).
4. For each combination, the states of the Red LED (D1), Green LED (D2), and Buzzer (BUZ1) were recorded.
5. Particular attention was paid to the target password combination (1011) and the adjacent combinations to check for any transient or floating signal issues.

5.2 Results

The observed physical outputs perfectly matched the theoretical Truth Table derived in Section 3.3.

S4	S3	S2	S1	Final Logic Output (L)	Red LED (D1)	Green LED (D2) / Buzzer	Status
0	0	0	0	0	OFF	ON	Unlocked

0	0	0	1	0	OFF	ON	Unlocked
...	...	...	...	...	...	...	Unlocked
1	1	0	0	0	OFF	ON	Unlocked
1	**1**	**0**	**1**	**1**	**ON**	**OFF**	**SECURE**
1	1	1	0	0	OFF	ON	Unlocked
1	1	1	1	0	OFF	ON	Unlocked

(Note: The full table of all 16 results was recorded in the lab but is abbreviated here for brevity. All 15 incorrect combinations resulted in $L=0$ *and the Unlocked state, while the single correct combination resulted in* $L=1$ *and the Secure state.)*

5.3 Observations and Analysis

The implementation demonstrated robust performance:

- **Clean Transitions:** The use of pull-down resistors successfully eliminated any floating input issues, ensuring clean transitions between logic 0 and logic 1 whenever a switch was pressed or released.
- **IC Stability:** The 74LS-series ICs performed reliably, immediately changing output states upon input modification, confirming the instantaneous nature of combinational logic.
- **Transistor Role:** The BC547 transistor functioned effectively as a low-side switch, allowing the low-current logic signal ($\overline{L}$) to control the higher-current draw of the buzzer without stressing the logic gate output pin.
- **Mutual Exclusivity:** The inverter U2:B successfully created mutually exclusive indicator outputs (D1 and $\text{D2}/\text{BUZ1}$), preventing ambiguous feedback to the user.

CHAPTER 6: DISCUSSION AND ANALYSIS

6.1 Performance and Limitations of Combinational Design

The design successfully meets the project objectives by implementing a combinational lock with high reliability. The circuit is inexpensive, requires minimal components, and is easy to debug due to its direct mapping of input to output.

However, the design is limited by the fundamental nature of combinational logic:

1. **Simultaneous Input:** The user must press and hold all correct switches concurrently. If they release a single switch, the output immediately reverts to $L=0$. This is impractical for a real-world security system.

2. **No Sequence Detection:** The lock cannot enforce a sequence (e.g., S1 then S3 then S4). Pressing S4, S3, and S1 in any order, so long as S2 is released, will still trigger the $L=1$ output, provided they are held down simultaneously.
3. **Low Security:** With only four bits, there are only 16 possible passwords, making the code easily guessable via brute force.

6.2 Application of Logic Gates in Real-World Scenarios

Despite its simplicity, the underlying principle of this lock is central to digital security:

- **Multiplexers/Decoders:** More complex commercial locks use multiplexers or decoders to compare larger codes (e.g., 8-bit or 16-bit) to memory-stored values. The AND gate function used here is functionally similar to the final validation stage of a decoder.
- **Error Detection:** The NOT gate, which forces a required LOW input to be an active part of the HIGH output logic, is a form of error detection logic. If S2 is HIGH (the wrong state), the $\overline{S2}$ term forces the entire AND operation to LOW, invalidating the entry.

6.3 Cost and Efficiency Analysis

The use of highly integrated TTL chips (74LS08 and 74LS04) minimizes the required physical components compared to building the logic from discrete transistors. The 74LS series offers an optimal balance between switching speed and low power consumption, making it a highly efficient choice for educational prototypes. The circuit uses only two out of four AND gates and two out of six NOT gates available across the two ICs, leaving substantial capacity for future expansion without adding new chips.

CHAPTER 7: CONCLUSION AND FUTURE SCOPE

7.1 Conclusion

The project successfully demonstrated the design, construction, and testing of a 4-bit combinational password lock based on the $\mathbf{1011}$ logic. By correctly applying Boolean algebra and employing standard 74LS-series logic gates, a robust digital decision-making circuit was implemented. The system operates reliably, providing clear, mutually exclusive output feedback (Red LED ON for correct entry, Green LED/Buzzer ON for incorrect entry). This project has served as an invaluable exercise in foundational digital logic design, circuit debugging, and the practical application of fundamental gates.

7.2 Recommendations for Future Work

To evolve this basic demonstrator into a more practical and sophisticated security device, the following future enhancements are recommended:

1. **Sequential Lock Implementation:** The most critical enhancement is to transition from combinational to sequential logic. This requires incorporating **Flip-Flops** (e.g.,

D-type or JK-type) and a **Shift Register** (e.g., 74LS164) to store the inputs in order and validate them against a sequence over time.

2. **Attempt Counter and Lockout:** Implement a **Counter** (e.g., 74LS93) to track the number of failed attempts. After three or four incorrect entries, a **Latch** (e.g., SR Latch) should be used to disable the input switches for a set time (driven by a 555 Timer), enhancing security.
3. **Password Variability:** Introduce DIP switches to allow the password to be easily modified without rewiring the circuit. This involves using XNOR gates to compare the fixed DIP switch settings against the user inputs.
4. **Microcontroller Integration:** For commercial-grade development, the entire logic core could be replaced by a simple microcontroller (e.g., Arduino or PIC) to handle the validation, sequence detection, and lockout timing via software, offering maximum flexibility and minimal hardware complexity.

APPENDIX A: Detailed Component Data Sheets (Excerpts)

A.1 74LS08 (Quad 2-Input AND Gate)

Parameter	Specification
Supply Voltage (V_{CC})	4.75V to 5.25V
HIGH-Level Output Current (I_{OH})	-0.4mA (min)
LOW-Level Output Current (I_{OL})	8mA (min)
Typical Propagation Delay	10ns

A.2 74LS04 (Hex Inverter)

Parameter	Specification
Supply Voltage (V_{CC})	4.75V to 5.25V
HIGH-Level Output Current (I_{OH})	-0.4mA (min)
LOW-Level Output Current (I_{OL})	8mA (min)
Typical Propagation Delay	9ns

APPENDIX B: Input Conditioning and Transistor Sizing Calculations

B.1 Pull-Down Resistor Sizing (R1-R4)

A 1 k resistor was chosen to ensure the input current (I_{IL}) to the TTL gate is low when the switch is closed (HIGH). When the switch is open, it ensures a definite LOW voltage:

$$\text{Voltage drop across } R_{in} \text{ (Switch Open)} \approx 0 \text{V}$$$$\text{Current drawn when Switch Closed} = I = \frac{V_{CC}}{R_{in}} = \frac{5 \text{V}}{1000 \ \Omega} = 5 \text{mA}$$

This current is low enough to be safely sourced by the power supply and provides a robust 0V reference when the switch is open.

B.2 LED Current Limiting Resistor (R_{LED}) Sizing (R5, R6)

The standard forward voltage (V_f) for an LED is assumed to be 2V. The desired forward current (I_f) for bright illumination without exceeding the LED rating is approximately 10mA.

$$\text{Resistance } R_{LED} = \frac{V_{CC} - V_f}{I_f} = \frac{5 \text{V} - 2 \text{V}}{10 \text{mA}} = \frac{3 \text{V}}{0.01 \text{A}} = 300 \ \Omega$$

A standard resistor value of $330 \ \Omega$ was chosen for $R5$ and $R6$.

B.3 Transistor Base Resistor Sizing (R7)

The NPN transistor BC547 is used to switch the buzzer ON. The buzzer's current requirement I is estimated to be 50 mA. A common base current IB is calculated to ensure the transistor is fully saturated. Assuming a minimum current gain beta_min of 100 for the BC547, the required base current is:

I B = \frac{I_C}{\beta_{min}} = \frac{50 \text{mA}}{100} = 0.5 \text{mA}$$

The base resistor ($R7$) is calculated using the voltage drop from the NOT gate output ($\text{V}_{OH} \approx 4 \text{V}$) to the base-emitter voltage ($\text{V}_{BE} \approx 0.7 \text{V}$):

$$R_{Base} = \frac{V_{OH} - V_{BE}}{I_B} = \frac{4 \text{V} - 0.7 \text{V}}{0.5 \text{mA}} = \frac{3.3 \text{V}}{0.0005 \text{A}} = 6600 \ \Omega$$

To ensure deep saturation, the base current is typically set higher. A practical value of $1 \text{ k}\Omega$ was chosen for $R7$, providing a base current of 3.3mA, which is well above the saturation requirement and easily sourced by the 74LS04 gate.

APPENDIX C: Glossary of Terms

Term	Definition
TTL	Transistor-Transistor Logic. A common family of integrated circuits characterized by moderate speed and power usage.
Logic Gate	An electronic component that performs a Boolean function.
Combinational Logic	A type of digital circuit where the output is determined solely by the current inputs.
Sequential Logic	A type of digital circuit where the output is determined by both current inputs and past states (requires memory).

Pull-Down Resistor	A resistor connected between an input line and ground to ensure the default state is logic LOW (0) when a switch is open.
Boolean Algebra	The mathematical system used to analyze and simplify digital (binary) logic circuits.
Flip-Flop	A fundamental sequential circuit that can store one bit of binary data; a memory element.
Active HIGH	A signal or output that performs its intended function when at the logic '1' state.