CST 203	Logic System Design	Category	L	T	P	Credit	Year of Introduction
		PCC	3	1	0	4	2019

Preamble: The objective of the course is to familiarize learners with the basic concepts of Boolean algebra and digital systems. This course covers the design of simple combinational and sequential logic circuits, representation and arithmetic algorithms for Binary, BCD (Binary Coded Decimal) and Floating point numbers which in turn are helpful in understanding organization & design of a computer system and understanding how patterns of ones and zeros can be used to store information on computers, including multimedia data.

Prerequisite: Nil

Course Outcomes: After the completion of the course the student will be able to

CO#	CO
CO1	Illustrate decimal, binary, octal, hexadecimal and BCD number systems, perform conversions among them and do the operations - complementation, addition, subtraction, multiplication and division on binary numbers (**Cognitive Knowledge level: Understand**)
CO2	Simplify a given Boolean Function and design a combinational circuit to implement the simplified function using Digital Logic Gates (**Cognitive Knowledge level: Apply**)
CO3	Design combinational circuits - Adders, Code Convertors, Decoders, Magnitude Comparators, Parity Generator/Checker and design the Programmable Logic Devices - ROM and PLA. **(Cognitive Knowledge level: Apply)**
CO4	Design sequential circuits - Registers, Counters and Shift Registers. **(Cognitive Knowledge level: Apply)**
CO5	Use algorithms to perform addition and subtraction on binary, BCD and floating point numbers **(Cognitive Knowledge level: Understand)**

Mapping of course outcomes with program outcomes

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓	✓										✓
CO2	✓	✓	✓	✓		✓						✓
CO3	✓	✓	✓	✓		✓						✓
CO4	✓	✓	✓	✓		✓						✓
CO5	✓	✓	✓									✓

Abstract POs defined by National Board of Accreditation			
PO#	**Broad PO**	**PO#**	**Broad PO**
PO1	Engineering Knowledge	**PO7**	Environment and Sustainability
PO2	Problem Analysis	**PO8**	Ethics
PO3	Design/Development of solutions	**PO9**	Individual and team work
PO4	Conduct investigations of complex problems	**PO10**	Communication
PO5	Modern tool usage	**PO11**	Project Management and Finance
PO6	The Engineer and Society	**PO12**	Life long learning

Assessment Pattern:

Bloom's Category	Test 1 (%)	Test 2 (%)	End Semester Examination Marks (%)
Remember	20	20	20
Understand	35	35	35
Apply	45	45	45
Analyse			
Evaluate			
Create			

Mark Distribution:

Total Marks	CIE Marks	ESE Marks	ESE Duration
150	50	100	3

Continuous Internal Evaluation Pattern:

Attendance : 10 marks
Continuous Assessment Test : 25 marks
Continuous Assessment Assignment : 15 marks

Internal Examination Pattern:

Each of the two internal examinations has to be conducted out of 50 marks. First series test shall be preferably conducted after completing the first half of the syllabus and the second series test shall be preferably conducted after completing remaining part of the syllabus. There will be two parts: Part A and Part B. Part A contains 5 questions (preferably, 2 questions each from the completed modules and 1 question from the partly completed module), having 3 marks for each question adding up to 15 marks for part A. Students should answer all questions from Part A. Part B contains 7 questions (preferably, 3 questions each from the completed modules and 1 question from the partly completed module), each with 7 marks. Out of the 7 questions, a student should answer any 5.

End Semester Examination Pattern:

There will be two parts; Part A and Part B. Part A contains 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which a student should answer any one. Each question can have maximum 2 sub-divisions and carries 14 marks.

SYLLABUS

Module I

Number systems, Operations & Codes

Decimal, Binary, Octal and Hexadecimal Number Systems- Number Base Conversions. Addition, Subtraction, Multiplication and Division of binary numbers. Representation of negative numbers- Complements, Subtraction with complements. Addition and subtraction of BCD, Octal and Hexadecimal numbers. Binary codes- Decimal codes, Error detection codes, Reflected code, Character coding schemes – ASCII, EBCDIC.

Module II

Boolean Algebra

Postulates of Boolean Algebra. Basic theorems and Properties of Boolean Algebra. Boolean Functions - Canonical and Standard forms. Simplification of Boolean Functions- Using Karnaugh- Map Method (upto five variables), Don’t care conditions, Product of sums

simplification, Tabulation Method. Digital Logic Gates- Implementation of Boolean functions using basic and universal gates.

Module III

Combinational Logic Circuits

Design Procedure & Implementation of combinational logic circuits- Binary adders and subtractors, Binary Parallel adder, Carry look ahead adder, BCD adder, Code converter, Magnitude comparator, Decoder, Demultiplexer, Encoder, Multiplexer, Parity generator/ Checker.

Module IV

Sequential logic circuits:

Flip-flops- SR, JK, T and D. Triggering of flip-flops- Master slave flip- flops, Edge- triggered flip- flops. Excitation table and characteristic equation. Registers- register with parallel load. Counter design: Asynchronous counters- Binary and BCD counters, timing sequences and state diagrams. Synchronous counters- Binary Up- down counter, BCD counter.

Module V

Shift registers

Shift registers – Serial In Serial Out, Serial In Parallel Out, Bidirectional Shift Register with Parallel load. Ring counter. Johnson counter- timing sequences and state diagrams.

Arithmetic algorithms

Algorithms for addition and subtraction of binary numbers in signed magnitude and 2's complement representations. Algorithm for addition and subtraction of BCD numbers. Representation of floating point numbers, Algorithm for addition and subtraction of floating point numbers.

Programmable Logic devices

ROM. Programmable Logic Array(PLA)- Implementation of simple circuits using PLA.

Text Books:

1. M. Morris Mano, Digital Logic & Computer Design, 4/e, Pearson Education, 2013
2. Thomas L Floyd, Digital Fundamentals, 10/e, Pearson Education, 2009.
3. M. Morris Mano, Computer System Architecture, 3/e, Pearson Education, 2007.

Reference Books:

1. M. Morris Mano, Michael D Ciletti , Digital Design With An Introduction to the Verilog HDL, 5/e, Pearson Education, 2013.
2. Donald D Givone, Digital Principles and Design, Tata McGraw Hill, 2003

Sample Course Level Assessment Questions

Course Outcome1(CO1): Perform the following number base conversions:

a) $(250.55)_{10}$ to Hexadecimal b) $(357)_8$ to Decimal

Course Outcome 2(CO2): Given a Boolean function F and don't care conditions D, using Karnaugh map obtain the simplified expression in (i) SOP and (ii) POS:

$$F(A, B, C, D) = A'B'D' + A'CD + A'BC$$
$$D(A, B, C, D) = A'BC'D + ACD + AB'D$$

Course Outcome 3(CO3): Design a BCD to Excess-3 Code Convertor.

Course Outcome 4(CO4): Design a 4- bit binary ripple counter.

Course Outcome 5(CO5): Demonstrate floating-point addition algorithm.

Model Question Paper

QP CODE: PAGES: 2

Reg No:_____
Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY THIRD SEMESTER B.TECH DEGREE EXAMINATION, MONTH & YEAR

Course Code: CST 203

Course name : LOGIC SYSTEM DESIGN

Max Marks: 100 **Duration: 3 Hours**

PART-A

(Answer All Questions. Each question carries 3 marks)

1. Represent the decimal numbers $(459)_{10}$ and $(859)_{10}$ in hexadecimal and perform addition of these hexadecimal numbers.
2. Subtract $(1101)_2$ from $(11010)_2$ using: i) $2's$ complement and ii) $1's$ complement arithmetic.
3. Find the dual and complement of the boolean function $F = AB' + B(A + B')$.
4. Using K-map, reduce the expression: $AB + ABC + ABC + BC$.
5. Design a half subtractor with NAND gates only.
6. Design a combinational circuit that multiplies an input decimal digit by 5 represented in BCD. The output is also in BCD. Show that the outputs can be obtained from the input lines without using any logic gates.
7. Differentiate between ripple counter and synchronous counter.
8. Construct D flip- flop using NAND gates. Also give its truth table.
9. Explain how a shift register is used for serial data transfer?
10. Write short notes on ROM.

PART-B

(Answer any one full question from each module) **(14X5=70)**

11. (a) Perform the following operations using 2's complement arithmetic: (8)

(i) $88_{10} + (-37)_{10}$ (ii) $(-20)_{10} + (-12)_{10}$

(b) Perform the following base conversions: (i) $(101011.11)_2$ to octal (6)
(ii) $(3F9B)_{16}$ to binary (iii) $(121)_{10}$ to binary (iv) $(3077)_8$ to binary

OR

12. (a) Find the 12 bit $2's$ complement representation of the following decimal numbers. (6)

(i) – 97 (ii) – 224 (iii) - 197.5

(b) Perform the following operations (8)

(i) $(520)_8 + (488)_8$ (ii) $(520)_{16} - (488)_{16}$

13. (a) Prove that (i) $AB + A(B + C) + B(B + C) = B + AC$ (4)
(ii) $AB + A(B + C) + B(B + D) = A$

(b) Using K-map, simplify the Boolean function F in sum of products form, using the don't care conditions d: (10

$F(w, x, y, z) = w'(x'y + x'y' + xyz) + x'z'(y + w)$
$d(w, x, y, z) = w'x(y'z + yz') + wyz$

OR

14. (a) Simplify the following expressions using Karnaugh- map method. (8)

(i) $F = \Sigma(0,2,4,6,9,11,13,15,17,21,25,27,29,31)$
(ii) $F = \Pi(0,2,5,7)$

(b) Convert the following to the other canonical form: (6)

(i) $F(x, y, z, a) = \sum (1,3,7)$

(ii) $F(x, y, z) = \Pi(0,3,6,7)$

(iii) $F(A, B, C, D) = \Pi(0,1,2,3,4,6,12)$

15. (a) Implement Full adder circuit using NAND gate only. (4)

(b) Design a code converter for converting BCD to Excess 3 code (10)

OR

16. (a) With a neat diagram explain 4-bit carry look-ahead adder. (6)

(b) Design a Gray to binary code converter using a 4x1 MUX. Draw the circuit diagram and explain. (8)

17. (a) Design a counter that count the states 0,3,5,6,0… using T flip- flops. (10)

(b) Write the characteristics equation, excitation table of JK, T and D flipflop. (4)

OR

18. (a) Explain race around condition and how it can be avoided. (6)

(b) Design a synchronous Binary Up-Down Counter. (8)

19. (a) With a neat diagram explain universal shift register. (8)

(b) Explain Johnson Counter with timing diagram. (6)

OR

20. (a) Write algorithm for floating point addition and subtraction. (8)

(b) Implement the functions $Y_1 = AB'C' + AB'C + ABC$ and $Y_2 = BC + AC$ using minimum gates Programmable Logic Array. (6)

Teaching Plan

Module 1: Number systems, Operations & Codes (No algorithms)		**(7 hours)**
1.1	**Number Systems**: Decimal, Binary, Octal and Hexadecimal number systems, Number Base Conversions.	**1 hour**
1.2	**Binary Arithmetic:** Addition, Subtraction, Multiplication & Division of Binary Numbers. (Lecture 1)	**1 hour**
1.3	Addition, Subtraction, Multiplication & Division of Binary Numbers. (Lecture 2)	**1 hour**
1.4	Representation of Negative Numbers- Complements, subtraction with complements.	**1 hour**
1.5	**BCD Arithmetic:** Addition and Subtraction of BCD Numbers	**1 hour**
1.6	**Octal and Hexadecimal Arithmetic**: Addition & Subtraction of Octal and Hexadecimal Numbers.	**1 hour**

1.7	**Binary Codes:** Decimal Codes, Error detection codes, Reflected code, Character Coding Schemes-ASCII, EBCDIC	**1 hour**
Module 2: Boolean Algebra		**(9 hours)**
2.1	**Introduction to Boolean Algebra:** Postulates of Boolean Algebra	**1 hour**
2.2	Basic theorems and Properties of Boolean Algebra	**1 hour**
2.3	**Boolean Functions:** Canonical and Standard Forms	**1 hour**
2.4	**Simplification of Boolean Functions**: Karnaugh -Map Method (upto five variables), Don't care conditions (Lecture 1)	**1 hour**
2.5	**Simplification of Boolean Functions**: Karnaugh -Map Method (upto five variables), Don't care conditions (Lecture 2)	**1 hour**
2.6	**Product of sums simplification**	**1 hour**
2.7	**Tabulation method**	**1 hour**
2.8	**Digital Logic Gates:** AND, OR, NOT, NAND, NOR, XOR, XNOR, Implementation of Boolean functions using basic and universal gates. (Lecture 1)	**1 hour**
2.9	**Digital Logic Gates:** AND, OR, NOT, NAND, NOR, XOR, XNOR, Implementation of Boolean functions using basic and universal gates. (Lecture 2)	**1 hour**
Module 3: Combinational Logic Circuits		**(9 hours)**
3.1	Design Procedure & Implementation of Combinational Circuits	**1 hour**
3.2	**Binary Adders:** Implementation of Half Adder, Full Adder	**1 hour**
3.3	**Binary Subtractors:** Implementation of Half Subtractor, Full Subtractor	**1 hour**
3.4	Implementation of Binary Parallel Adder ,Carry look ahead Adder, BCD Adder (Lecture 1)	**1 hour**
3.5	Implementation of Binary Parallel Adder ,Carry look ahead Adder, BCD Adder (Lecture 2)	**1 hour**

3.6	**Implementation of Various Combinational Circuits:** Code Converters, Magnitude Comparator	**1 hour**
3.7	Implementation of Decoder, Demultiplexer	**1 hour**
3.8	Implementation of Encoder, Multiplexer	**1 hour**
3.9	Implementation of Parity Generator/Checker	**1 hour**
Module 4: Sequential logic circuits:		**(9 hours)**
4.1	**Flip flops:** SR, JK, T and D flip- flops (Lecture 1)	**1 hour**
4.2	SR, JK, T and D flip- flops (Lecture 2)	**1 hour**
4.3	Triggering of flip-flops- Master slave flip- flop, Edge- triggered flip-flops (Lecture 1)	**1 hour**
4.4	Triggering of flip-flops- Master slave flip- flop, Edge- triggered flip-flops (Lecture 2)	**1 hour**
4.5	Excitation table and characteristic equations of flip- flops	**1 hour**
4.6	**Registers-** Register with parallel load	**1 hour**
4.7	**Counter Design:** Asynchronous counters- Binary and BCD counters- timing sequences and state diagrams. (Lecture 1)	**1 hour**
4.8	Asynchronous counters- Binary and BCD counters- timing sequences and state diagrams. (Lecture 2)	**1 hour**
4.9	Synchronous counters- Binary Up- down counter, BCD counter	**1 hour**
Module 5: Shift registers, Arithmetic algorithms & PLD's		**(11 hours)**
5.1	**Shift Registers** - Serial In Serial Out, Serial In Parallel Out.	**1 hour**
5.2	Bidirectional Shift Register with Parallel load	**1 hour**

5.3	**Shift register counters** - Ring Counter, Johnson Counter- timing sequences and state diagrams	**1 hour**
5.4	**Arithmetic Algorithms:** Algorithm for addition and subtraction of binary numbers in Signed magnitude and 2's complement representations (Lecture 1)	**1 hour**
5.5	Algorithm for addition and subtraction of binary numbers in Signed magnitude and 2's complement representations (Lecture 2)	**1 hour**
5.6	Algorithm for addition and subtraction of BCD numbers	**1 hour**
5.7	Representation of floating point numbers (IEEE Standard representations).	**1 hour**
5.8	Algorithms for floating point addition and subtraction	**1 hour**
5.9	**Programmable Logic devices** - ROM	**1 hour**
5.10	PLA, Implementation of simple circuits using PLA(Lecture 1)	**1 hour**
5.11	PLA, Implementation of simple circuits using PLA(Lecture 2)	**1 hour**