Designs of BCD Adder Based on Excess-3 Code in Quantum-Dot Cellular Automata

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Abstract:

Quantum-dot Cellular Automata (QCA), an innovative nano-electronic technology, has garnered attention for its minute feature sizes at the molecular or atomic level and its exceptionally low power consumption, positioning it as a prospective replacement for conventional complementary metal oxide semiconductor (CMOS) technology. Binary-Coded Decimal (BCD) adders, integral in industrial computing, are the focal point of this proposal, where we introduce two types of excess-3 code (XS-3) based BCD adders (XS-3DAs). Leveraging ripple-carry adders (RCA) and parallel binary adders (PBA) in the QCA Designer tool, we construct these XS-3DAs, with the PBA-based variant incorporating a novel correction logic.

Implementing these designs for 4-bit, 8-bit, and 16-bit configurations, comparative analyses reveal that, as the design scales, the PBA-based XS-3DAs exhibit substantial reductions in delay and area-delay product (ADP) compared to their RCA-based counterparts. Specifically, when contrasted with the 16-digit RCA-based XS-3DA, the proposed 16-digit PBA-based XS-3DA demonstrates noteworthy reductions of 37.88% in cell count, 25.99% in area, 37.68% in delay, and 53.88% in ADP. Key index terms encapsulating the essence of this study include QCA, excess-3 code, and BCD adder.

Introduction:

Data processing in computers is fundamentally binary-centric, but given people's inclination towards decimal numbers, there is a growing demand for computers to directly handle decimal data. Anticipating future challenges with CMOS technology, such as the short channel effect and high lithography cost, nanotechnologies, notably Quantum-dot Cellular Automata (QCA), emerge as promising alternatives with substantial potential for integrated circuit design and manufacturing. QCA technology, renowned for its high device density, rapid switching speeds, and ultra-low energy consumption, holds significant research opportunities and widespread application prospects.

The XS-3 concept, briefly introduced here, involves the addition of 8421 Binary-Coded Decimal (BCD) codes and $(0011)_2$, forming a self-complementary BCD code. This biased representation enables easy 9's complementation, simplifying calculations. For instance, the XS-3 of 2 is 0101, and reversing each digit yields 1010, precisely the XS-3 of 7. Researchers have explored QCA-based BCD converters, including 8421 BCD code to XS-3 and vice versa, harnessing the advantages of XS-3 for BCD adder designs. Various approaches to BCD adders have been studied in previous works, ranging from modular designs in 2008 to correction logic formulations for delay reduction and novel structures for compact layouts in subsequent years.

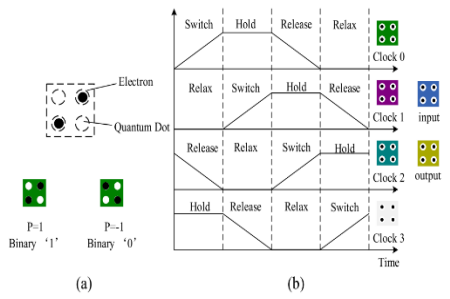


Fig. 1. QCA cells and QCA clock. (a) QCA cells and (b) QCA clock.

Notably, no QCA-based XS-3DAs have been reported in the literature. In this brief, we propose RCA-based and PBA-based XS-3DAs, with the PBA-based variant featuring a new correction logic. Utilizing the QCA Designer tool, we implement and analyze these XS-3DAs, demonstrating that, with increasing design scaling, the PBA-based XS-3DAs exhibit significantly reduced delay and area-delay product compared to their RCA-based counterparts.

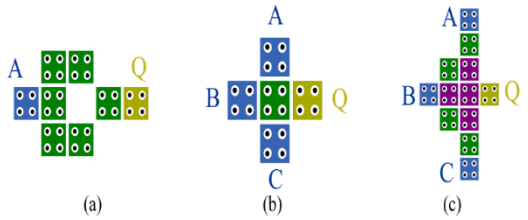


Fig. 2. QCA basic gates. (a) inverter, (b) 3-input majority gate and (c) 3-input XOR gate.

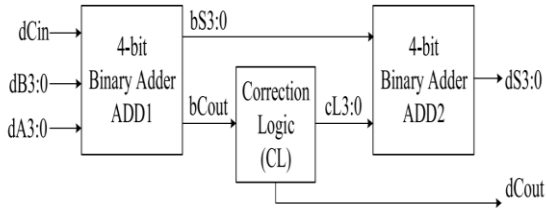


Fig. 3. Block diagram of 1-digit RCA-based XS-3DA.

The subsequent sections are organized as follows: Section II provides an introduction to the QCA technology, Section III outlines RCA-based and PBA-based XS-3DAs, Section IV presents simulation results and comparisons, and Section V concludes the brief.

Literature Review:

I. PRELIMINARIES OF QCA

Quantum-dot Cellular Automata (QCA) operates on QCA cells as its fundamental unit, each comprising two free electrons and four quantum dots. The electrostatic force effect allows the free electrons to settle into two stable states, representing binary values. QCA's distinct clock mechanism ensures signal stability, featuring four clock phases: switch, hold, release, and relax. During the switch phase, QCA cells enter the polarization state, reaching maximum polarity and remaining unchanged in the hold phase. The release phase sees a decrease in cell polarity, and in the relax phase, QCA cells lose polarization, reaching a non-polarized state. Figure 1 illustrates the QCA cells and clock mechanism.

Basic logic devices in QCA consist of 3-input majority gates and inverters, as depicted in Figure 2. Inverters reverse input signals, and 3-input majority gates adhere to the majority rule. The XOR function is achievable through a QCA-based gate, differing from the CMOS circuit's XOR gate construction. Figure 2 (c) showcases a 3-input XOR gate. These foundational elements lay the groundwork for understanding the unique characteristics and operations of QCA in subsequent sections.

II. PROPOSED RCA-BASED AND PBA-BASED XS-3Das:

A. RCA-Based XS-3Das:

The XS-3 code is generated by adding 8421 Binary-Coded Decimal (BCD) codes and $(0011)_2$. When adding two decimal numbers represented by XS-3S, the carry can be correctly generated, but the sum requires correction. The correction process involves adding $(0011)_2$to the sum if the carry is "1" and adding $(1101)_2$if the carry is "0." The correction logic circuit generates the two correction signals, $(0011)_2$ and $(1101)_2$.

The block diagram in Figure 3 illustrates the structure of the 1-digit RCA-based XS-3DA, comprising a 4-bit binary adder (ADD_1), correction logic (CL), and another 4-bit binary adder (ADD_2). Input signals $dA_{3:0}$ and $dB_{3:0}$ represent two decimal numbers in excess-3 codes, while dCout and $dS_{3:0}$ denote the carry and sum of the 1-digit XS-3DA. (ADD_1) computes binary $bS_{3:0}$ and carry bCout by adding $dA_{3:0}$, $dB_{3:0}$ and dCin. The CL circuit, composed of an inverter, generates the correction signal cL3:0. When bCout is 1, $cL_{3:0}$ becomes $(0011)_2$, and when bCout is 0, it becomes $(1101)_2$. (ADD_2) combines $cL_{3:0}$ and $bS_{3:0}$ to produce decimal $dS_{3:0}$. The delay expressions for the 1-digit RCA-based XS-3DA outputs (Cout and $dS_{3:0}$ are expressed by formulas (1)–(2).

$$D(1)_C = D_{ADD1} \quad (1)$$

$$D(1)_S = D_{ADD1} + D_{CL} + D_{ADD2} \quad (2)$$

D_{ADD1}, D_{CL} and D_{ADD2} represent the delay of ADD_1, CL and ADD_2, respectively. The delay of the outputs (Cout and $dS_{3:0}$) of the n-digit RCA-based XS-3DA can be expressed by formulas (3)–(4).

$$D(n)_C = nD_{ADD1} \quad (3)$$

$$D(n)_S = nD_{ADD1} + D_{CL} + D_{ADD2} \quad (4)$$

Previous studies have proved that the introduction of XOR logic to construct full adders can effectively reduce overhead of QCA circuits [8]. We use a 3-input XOR gate and a 3- input majority gate to propose a full adder (see Pro-FA in Fig. 4 and Table II) to reduce circuit overhead. Figure 4 shows the layout of the proposed 1-digit RCA-based XS-3DA in the QCA Designer tool. The cells marked with " " are on the second layer, and the cells marked with "×" are on the third layer. The dA3:0 and dB3:0 are two groups of input signals. The dCin represents the input carry signal, dCout represents the output carry signal, and dS3:0 represents the sum signal. The design consists of 539 cells, with an area of 0.60 um2, a delay of 2.25 clocks for signal dS3:0, and a delay of 1.25 clocks for the signal dCout. It is a 3-layer design. ADD1 and ADD2 of the proposed 1-digit RCA-based XS-3DAs are implemented using the proposed FAs. Because the signal cL0 is always "1", the rightmost FA of ADD2 can be replaced by an inverter. N-digit RCA-based XS-3DAs can be constructed using the proposed RCA-based XS-3DAs

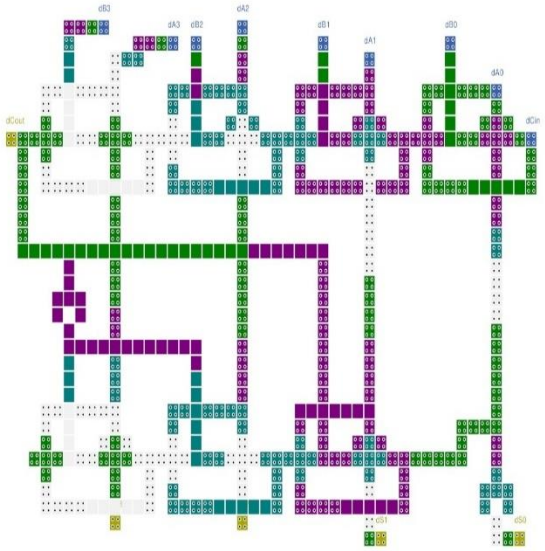


Fig. 4. Layout of the proposed 1-digit RCA-based XS-3DA.

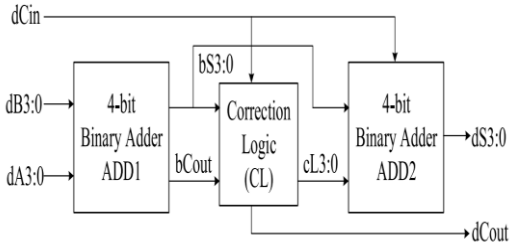


Fig. 5. Block diagram of 1-digit BCD adder [8].

B. PBA-Based XS-3Das:

Figure 5 shows a block diagram of BCD adders [6]. Ajitha et al. and Zhang et al. have applied the block diagram to design BCD adders based on 8421 BCD codes, respectively [5], [6]. We apply this method for the construction of XS-3DAs.

The following is the analysis of the proposed PBA-based XS-3DAs. The signals $dA_{3:0}$ and $dB_{3:0}$ are two decimal input numbers represented by excess-3 codes. It can be seen from Fig. 5 that, after adjusting the input of signal dCin, when the signal $bS_{3:0}$ is greater than or equal to "10", the carry signal bCout is correct no matter the value of dCin; when $bS_{3:0}$ is less than "9", the carry signal bC_{out} is correct no matter the value of dCin; when $bS_{3:0}$ is equal to "9" and dCin is equal to "0", the carry signal bCout is correct; when $bS_{3:0}$ is equal to "9" and dCin is equal to "1", the signal bCout is "0", which is wrong and needs to be corrected. The output carry dCout of the XS-3DAs can be rewritten as formula (5).

dCout = bCout + (bS3:0 == 9)dCin -----(5)

The excess-3 code of "9" is (1111) XS-3. Formula (5) can be rewritten as formula (6).

$$dC_{out} = bC_{out} + (bS_{3:0} == (1111)_{XS-3})dC_{in}$$
$$dC_{out} = bC_{out} + bS_3 \cdot bS_2 \cdot bS_1 \cdot bS_0 \cdot dC_{in}$$
$$dC_{out} = bC_{out} + (bS_3 \cdot bS_2) \cdot (bS_1 \cdot bS_0) \cdot dC_{in} \quad (6)$$

Figure 6 shows the proposed CL circuit of PBA-based XS3DAs. The CL circuit of the proposed PBA-based XS-3DAs can process signals $bS_{3:0}$, bCout and dCin to obtain signals dCout. Figure 7 shows the schematic diagram of the proposed PBA-based XS-3DAs. Compared with the CL circuit of the RCA-based XS-3DAs, although the proposed CL circuit of the PBA-based XS-3DAs has five more gates, the

signal dCin can flow directly into the CL circuit without flowing through ADD_1 and each ADD_1 of n-digit XS-3DA can be operated in parallel to reduce delay. Theoretically, when dCin is inputted, the carry signal dCout can be output after a delay of 0.5 clocks in QCA circuit, which can significantly reduce the delay of the n-digit XS-3DAs.

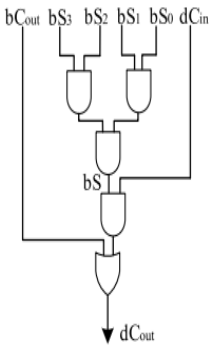
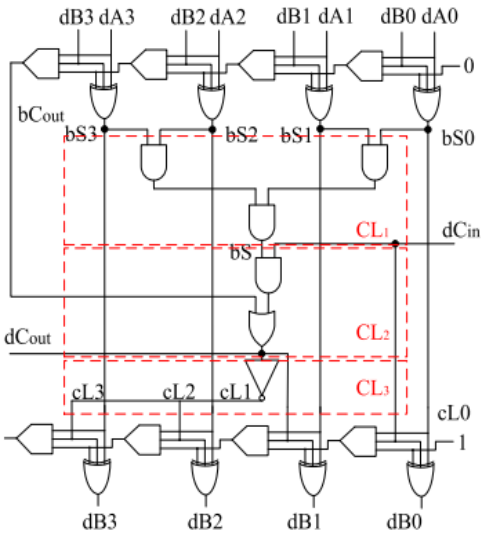


Fig. 6. The proposed CL circuit of PBA-based XS-3DAs.



. Circuit diagram of the proposed 1-digit PBA-based XS-3DA.

The delay of the outputs (Cout and $dS_{3:0}$) of the proposed 1-digit PBA-based XS-3DA can be expressed by formulas (7)–(8). For brevity, the CL circuit is divided into CL_1, CL_2 and CL_3 as shown in Fig. 7

$$D(1)_C = D_{ADD1} + D_{CL1} + D_{CL2} \quad (7)$$

$$D(1)_S = D_{ADD1} + D_{CL} + D_{ADD2} \quad (8)$$

The delay of the outputs (Cout and $dS_{3:0}$) of the proposed n-digit PBA-based XS-3DA can be expressed by formulas (9)–(10)

$$D(n)_C = D_{ADD1} + D_{CL1} + nD_{CL2} \quad (9)$$

$$D(n)_S = D_{ADD1} + D_{CL1} + nD_{CL2} + D_{CL3} + D_{ADD2} \quad (10)$$

Figure 8 depicts the layout of the proposed 1-digit Parallel Binary Adder (PBA)-based XS-3DA, implemented using the QCA Designer tool. Comprising 675 cells, the design occupies an area of 0.68um2, featuring a delay of 3.25 clocks for the signal dS3:0 and a delay of 2.25 clocks for the signal dCout. This 3-layer design incorporates a unique configuration where the low carry input of the leftmost Full Adder (FA) in ADD_1 is set to "−1," and the carry signal dCin is directly inputted into the Correction Logic (CL) circuit and ADD_2 for computation. The proposed design utilizes the USE mechanism, known for its flexibility in creating feedback paths of varying lengths and a well-defined clocking circuitry. The USE mechanism's clock circuitry is simple, ensuring high design flexibility in the implementation of the PBA-based XS-3DA.

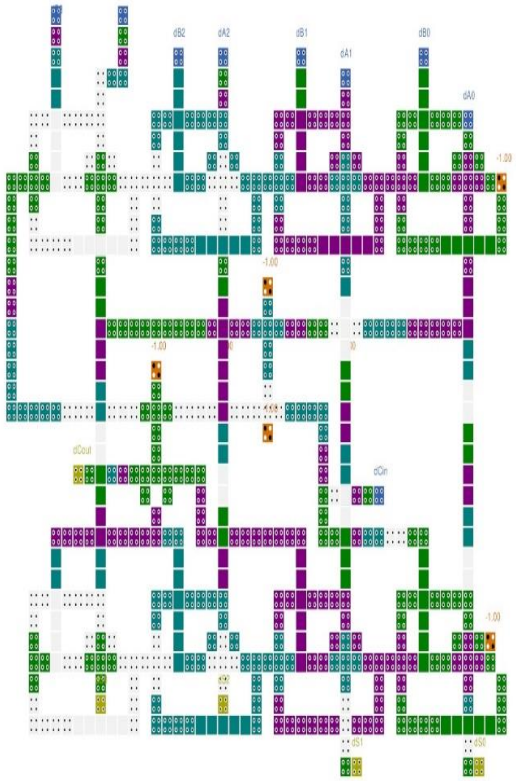


Fig. 8. Layout of the proposed 1-digit PBA-based XS-3DA.

IV. SIMULATION :

A.Simulation Results:

Figure 9 shows the simulation results of the proposed 1-digit PBA-based XS-3DA in the QCA Designer tool. The simulation engine of QCA Designer was set to the coherence vector engine [14], [15].

The other parameters of QCA Designer are set as default [16]. The delay of signal dCout is set to the same delay as signal $dS_{3:0}$ to synchronize outputs.

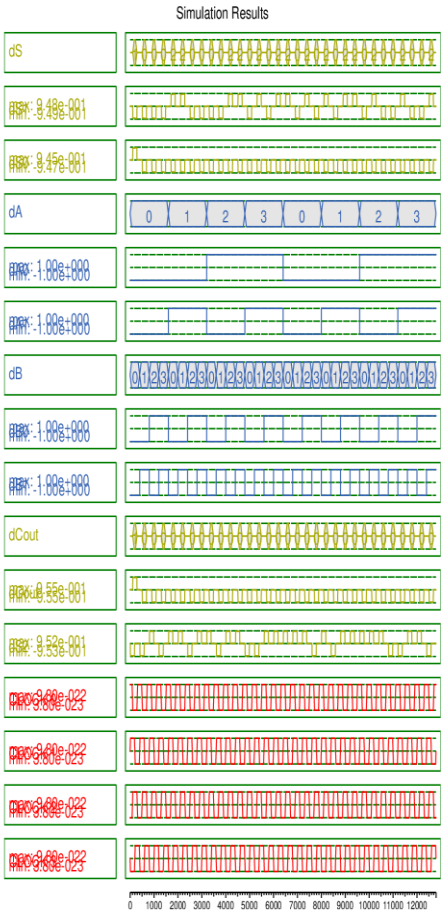


Fig. 9. Simulation results of the proposed 1-digit PBA-based XS-3DA.

B. Complexity Analysis:

We estimate area and delay based on the number of used QCA-based gates in the XS-3DAs. Ds presents the delay of the signal dSn−1:n−4 and Dc presents the delay of the signal dCout. Formula (11) presents the calculation of ADP [17].

ADP = Area × Ds ------(11)

The proposed 1-digit RCA-based XS-3DA consists of 16 QCA-based gates, including 7 majority gates, 2 inverters and 7 XOR gates. Thus, the area complexity of the n-digit RCA-based XS-3DA is 16n. The used QCA-based XOR gate requires a delay of a gate for calculation. The QCA-based ADD1 and ADD2 both requires a delay of 4 gates for calculation. The CL circuit of the proposed RCA-based XS-3DA composed of an inverter, which requires a delay of a gate. It can be seen from formulas (3)–(4) that, the input signals of the n-digit RCA-based adder flow through n ADD1s to get the signal dCout, and then flow through one CL circuit and one ADD2 to get the signal dSn-1:n-4. Therefore, the signals dCout and dSn−1:n−4 of the proposed n-digit RCA-based XS-3DA require a delay of 4n gates and 4n+5 gates, respectively. The proposed 1-digit PBA-based XS-3DA consists of 22 QCA-based gates, including 13 majority gates, 1 inverter and 8 XOR gates. Thus, the area complexity of the n-digit PBA-based XS-3DA is 22n. The CL1, CL2 and CL3 of the proposed PBA-based XS-3DA require a delay of two gates, two gates and one gate, respectively. It can be seen from formulas (9)–(10) that, the input signals of the n-digit PBA-based XS-3DA flow through one ADD1, one CL1 and n CL2s to get the signal dCout, then flow through one CL3 and one ADD2 to get the signal dSn-1:n-4. Therefore, the signals dCout and dSn−1:n−4 of the proposed n-digit PBA-based XS-3DA require a delay of 2n+6 gates and 2n+11 gates, respectively.

TABLE I
THEORETICAL COMPARISONS OF THE PROPOSED XS-3DAS

Design	MG	INV	XOR	Area	Delay		ADP
					D_S	D_C	
Pro-RCA1	7	2	7	16	9	4	144
Pro-RCAn	7n	2n	7n	16n	4n+5	4n	$64n^2$+80n
Pro-PBA1	13	1	8	22	13	8	286
Pro-PBAn	13n	n	8n	22n	2n+11	2n+6	$44n^2$+242n

TABLE II
COMPARISONS OF ALTERNATIVE FAS

Design	Cell Count	Area (um^2)	Delay (Clocks)	ADP	Layer type	Total energy dissipation
[10]	86	0.09	0.75	0.068	M	2.92e-002
[11]	58	0.03	0.75	0.023	M	2.59e-002
[12]	57	0.04	1.00	0.040	C	1.86e-002
Pro-FA	57	0.05	0.50	0.025	M	2.89e-002

Comparisions:

Table II shows the comparison of alternative adders. The proposed multilayer adder has a compact and regular layout, and the positions of the low carry terminal and the high output terminal are easy to access, which is very convenient for the construction of RCA. The proposed adder has a low delay and can be flexibly used in the design of decimal adders. Table III shows the comparisons of the decimal adders in terms of cell count, delay, area, ADP and layer type. Based on the proposed two XS-3DAs, 4-digit, 8-digit and 16-digit XS-3DAs are constructed, respectively. The decimal adders in [4], [5], [6], [7], [8] are based on 8421 BCD code. It can be seen from Table III that the proposed RCA-based XS-3DAs have the lowest area and delay overhead. The proposed PBA based XS-3DAs has the lowest area and ADP. Note that, the complexity analysis is based on the number of QCA gates, without considering the QCA wires for synchronous output. With the scale of the designs increases, the delay of the RCA based XS-3DA begins to be greater than that of the PBA-based XS-3DA, so that the RCA-based XS-3DA requires more QCA wires to synchronize outputs, resulting in the increase of its area. It can be calculated from Table III that, compared with the 16-digit RCA-based XS-3DAs, the cell count, area, delay and ADP of the 16-digit PBA-based XS-3DAs are reduced by 37.88%, 25.99%, 37.68% and 53.88%, respectively. Table IV shows the comparisons of energy dissipation of the proposed XS-3DAs. The energy dissipation of the proposed designs was estimated by QCA Designer-E tool. Because the CL circuit of the 1-digit PBA-based XS-3DA is more complex, its energy dissipation is greater than that of the 1-digit RCA based XS-3DA. However, with the design scale increases, the energy dissipation of PBA-based XS-3DA is gradually less than that of RCA-based XS-3DA (see Pro- RCA16 vs ProPBA16).

TABLE III
COMPARISONS OF THE DECIMAL ADDERS

Design	Digits	Cell Count	Area (um^2)	Delay (Clocks)	ADP	Layer type
RCA-based [4] (8421)	1	669	2.28	3.00	6.84	M
	4	3981	11.04	8.25	91.08	M
	8	11717	34.32	15.25	523.38	M
RCA-based [6] (8421)	1	918	3.03	4.00	12.12	M
	4	4226	17.04	7.00	119.28	M
	8	10091	48.27	11.00	530.97	M
PBA-based [6] (8421)	1	1294	2.64	3.75	9.90	M
	4	5500	11.46	5.25	60.17	M
	8	13456	35.13	7.25	254.69	M
RCA-based [7] (8421)	1	594	2.16	2.50	5.40	M
RCA-based [8] (8421)	1	476	0.64	2.25	1.44	C
	4	3075	5.37	8.25	44.30	C
	8	9265	18.15	16.25	294.94	C
RCA-based [8] (8421)	1	419	1.08	2.25	2.43	M
	4	2178	7.56	6.75	51.03	M
	8	5710	23.88	12.75	304.47	M
PBA-based [8] (8421)	1	733	1.01	3.50	3.54	C
	4	3494	4.98	6.50	32.37	C
	8	8572	12.73	10.50	133.67	C
PBA-based [8] (8421)	1	588	1.47	3.00	4.41	M
	4	2400	6.81	3.75	25.54	M
	8	5089	15.66	4.75	74.39	M
Pro-RCA (XS-3)	1	539	0.60	2.25	1.35	M
	4	2771	3.16	5.25	16.59	M
	8	7315	9.08	9.25	83.99	M
	16	28760	28.70	17.25	495.08	M
Pro-PBA (XS-3)	1	715	0.68	3.25	2.21	M
	4	3253	3.43	4.75	16.29	M
	8	7329	7.77	6.75	52.45	M
	16	17867	21.24	10.75	228.33	M

TABLE IV
COMPARISONS OF ENERGY DISSIPATION OF THE PROPOSED XS-3DAS

Design	Total energy dissipation (eV)	Average energy dissipation (eV)
Pro- RCA1	1.97e-001	1.79e-002
Pro- RCA4	8.70e-001	7.91e-002
Pro- RCA8	1.90e-000	1.72e-001
Pro- RCA16	4.50e-000	4.09e-001
Pro- PBA1	2.24e-001	2.04e-002
Pro- PBA4	9.94e-001	9.04e-002
Pro- PBA8	2.07e-000	1.88e-001
Pro- PBA16	4.45e-000	4.05e-001

Conclusion:

In this brief, we have proposed novel RCA-based and PBA based XS-3DAs in the QCA Designer tool. A new correction circuit is used to construct the PBA-based XS-3DAs. Our proposed RCA-based and PBA-based XS-3DAs show excel lent performance in terms of area and ADP. We have analyzed and compared the characteristics of the two types of XS-3DAs. The proposed CL circuit can significantly reduce the delay and ADP of the n-digit RCA-based XS-3DAs, thus saving the overall cost of QCA circuit designs.

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