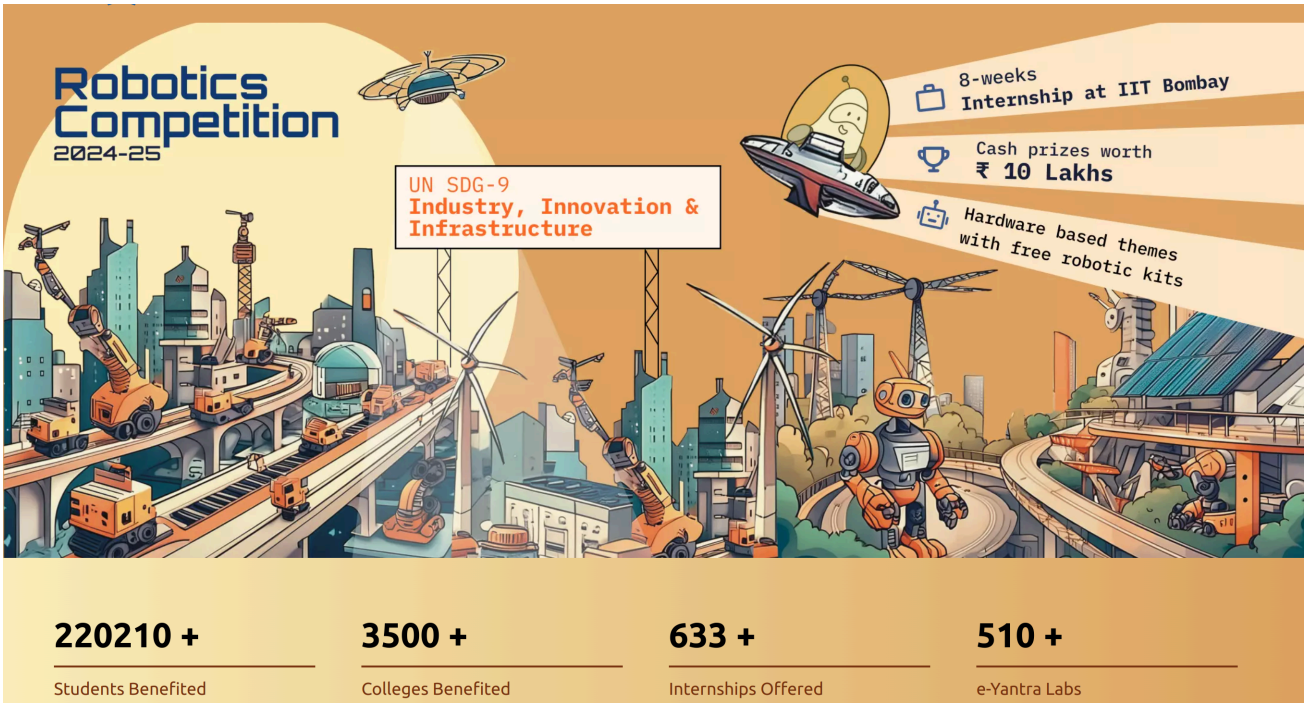
e-Yantra 2025, IIT Bombay

What is e-Yantra about?

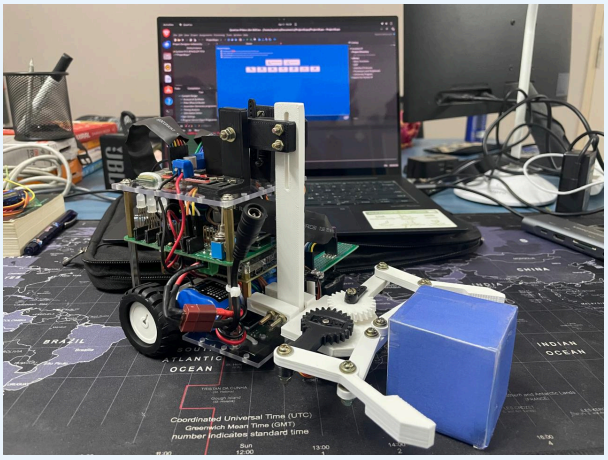
e-Yantra is a robotics competition like no other, a competition for everyone. It is hosted by the Department of Computer Science, IIT Bombay, headed by Dr. Kavi Arya, assistant professor, and sponsored by the Ministry of Education. It's a 7-8 months long competition open for undergraduate students across the world, all you need is the drive and the desire to continuously learn to perform well in this competition. e-Yantra is based on the UN SDG-9, Industry, Innovation and, Infrastructure, which has several **"gamified"** themes for participants to choose from. The 2024 - 25 edition saw 4 such themes, Logistic coBot (LB), Balancing Builder (BB), Ecomendor Bot (EB), and Warehouse Drone (WD), you can find about each of these problem statements at their main site.



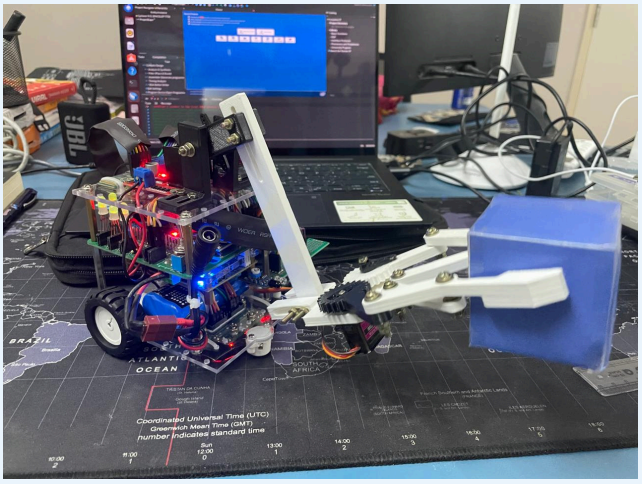
e-Yantra website homepage, season 2024-2025, visit site for more info.

Why should you participate?

Do you have interesting ideas but are unsure of how to get started? Or do you not have an idea but at least you would like to one day be able to identify real-world issues, build products to solve them, and scale them up? e-Yantra is a wonderful platform for exactly this, the mentorship and guidance are apt for you to learn and explore new domains while also keeping you not too dependent on the mentors themselves, they've got their balance right! External competition tends to keep you at the right learning pace with others.



Our bot final image.



Resource gripper arm in action.

Ecomendor Bot - Our Journey, Team EB#1039

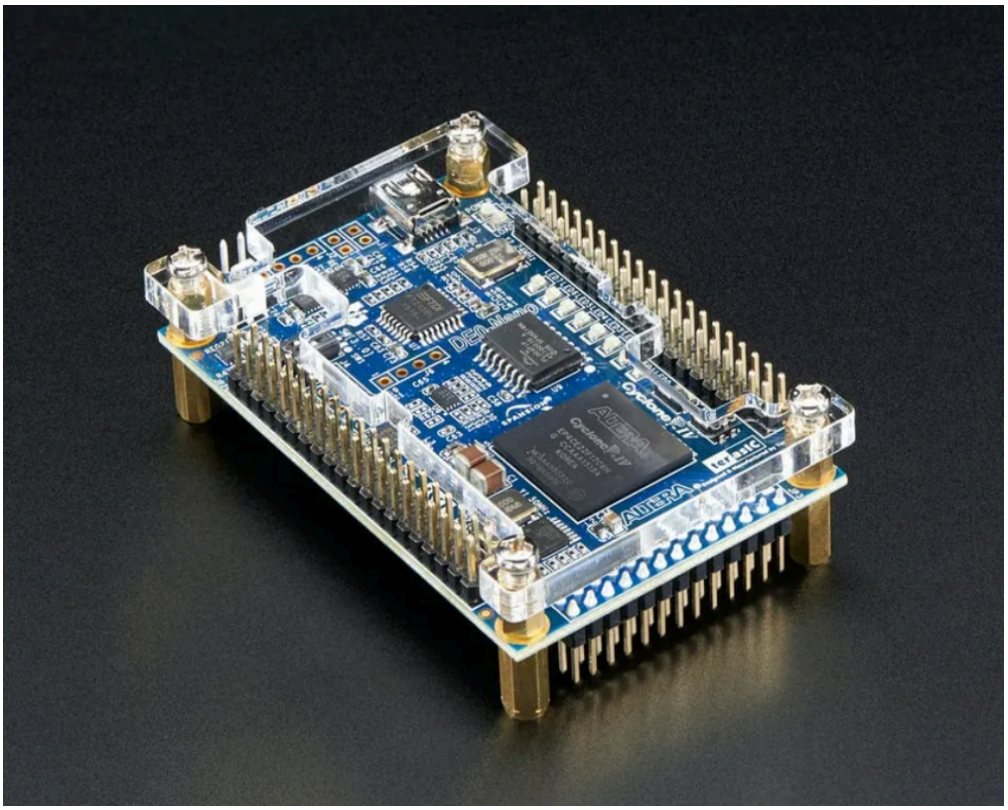
Problem Statement

The core challenge of this theme lies in constructing the EcoMender Bot from scratch, utilizing an FPGA (Field Programmable Gate Array) as its powerhouse. Through the FPGAs adept control over sensors and actuators, the robot adeptly traverses the arena, perceives its environment, and picks up essential components from the resource depot. Wireless communication serves as the primary means for exchanging vital information with the central hub. By participating in this theme, teams are presented with the opportunity to create a sophisticated CPU architecture using Verilog HDL, unveiling the remarkable parallel processing capabilities offered by FPGAs.

FPGAs - The Ditto of the Hardware World

In VLSI, IC design methodologies can be broadly classified into Full Custom and Semi Custom IC designs, Semi Custom IC designs are further divided into 4, Analog array, Gate array, Standard cell IC, and Programmable ICs, Programmable ICs are again sub-divided into 5 families under which we have the FPGAs. A special language called **"Hardware Descriptive Languages (HDLs)"** are used to design hardware for creating bitstreams are binary files that can be used to program FPGAs. **Verilog HDL**, most widely used HDLs in industry which is what we used in e-Yantra. FPGAs because of their ability to be programmed into any piece of hardware executing any communication protocols has found an important space for itself in R&D, product development, medical applications, space applications, robotics, developing hardware efficient coding algorithms, high-performance computing, digital-signal processing etc

apart from intended use of designing ICs. *FPGAs require a whole article for itself, do check them out yourselves to find out more.*

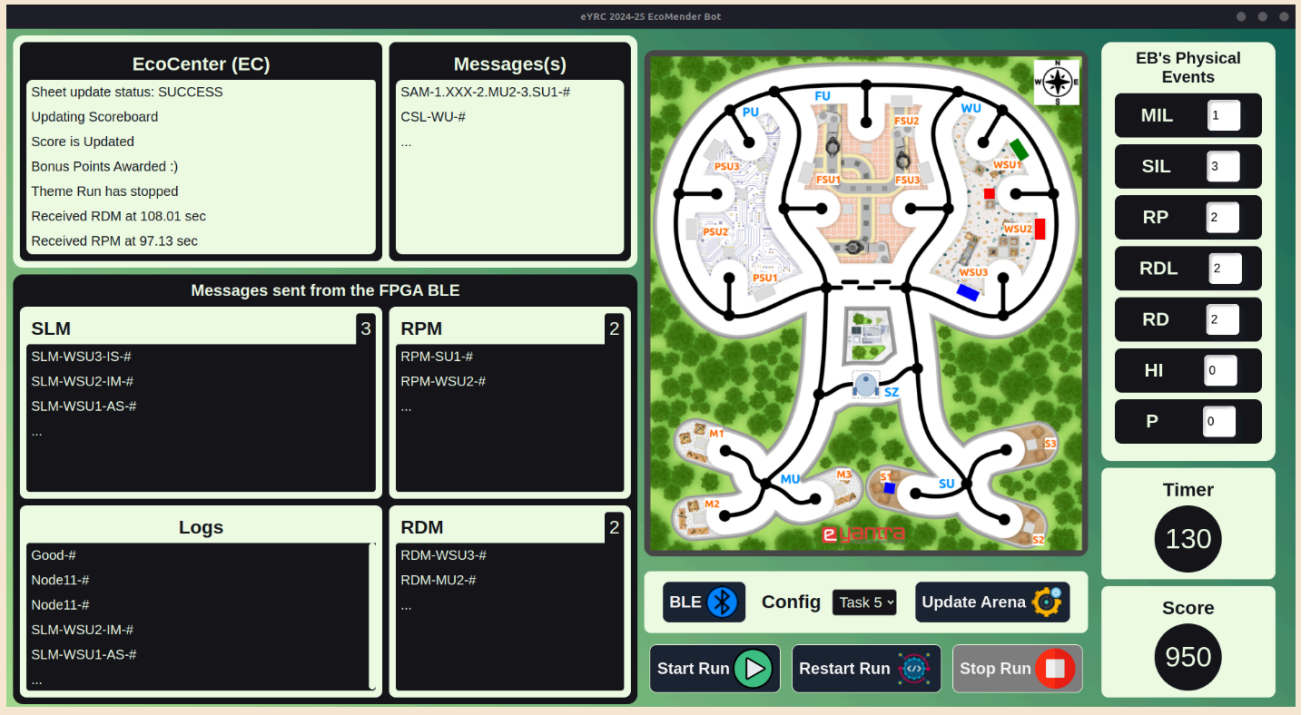


Altera Cyclone IV E EP4CE22F17C6 De0 Nano Development Board

The Gameplay

The whole arena is based on various units of a **chip design industry**, broadly **Storage Unit (SU)** and a **Maintenance Unit (MU)** with 3 core units - **the Prototyping Unit (PU)**, **Fabrication Unit (FU)** and **Waste Managament Unit (WU)**. The **Eco Center (EC)** is the control a software that is run on the laptop acting as the base control station which will be used to send important coded info for the bot to act accordingly and which is controlled by the jury themselves during the finale at IIT Bombay. There are various sub-units, **sustainability indicators (SI)** to be identified by the bot, efficiently communicated and indicate them using on-board RGB leds, move physical resources by choosing the best optimum path, avoiding obstacles on track, and communicating its status to the base control unit or the Eco center. There's a point system that'll be automatically updated on the base station software and a rule book was provided to have a good grasp on the theme run and the expectations.

Next 6-7 months was all about learning and understanding hardware design using Verilog HDL, CPU architectures, some basic C programming, developing C algorithms for path finding, efficiently managing the limited FPGA memory, designing and building our bot, 3D priniting, arena printing and building the external environmental parameters, etc. The whole work was divided into various tasks with deadlines and broadly two phases - **Stage I, the software phase** and **Stage II, the hardware phase**.



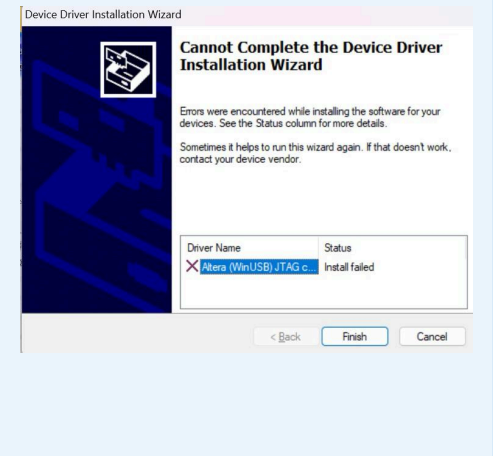
Base Station a.k.a. Eco Center

Stage I

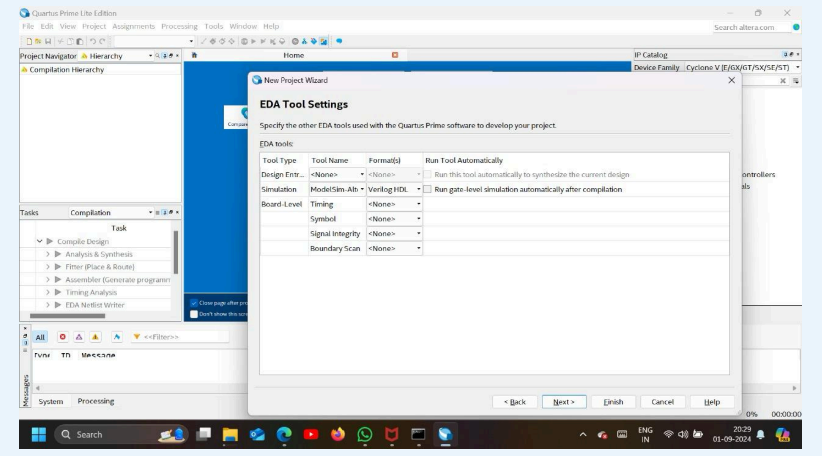
The initial tasks dealt more with helping us to understand how to use the resources and learn, how tasks are submitted and evaluated, running their evaluation scripts on local machine, generating the required files and making submissions through their online portal which evaluated and graded us based on the quality of work done. We were even presented with a live leader board to see where we stand.

TASK 0: Pre-requisites

In Task 0, we had to learn through the given resources and take a quiz on Computer Architecture and Digital Electronics, setting up our environment according to our OS, Windows 10+ or Jammy Linux. Build and configure RISCV toolchain, run some test scripts, upload the results to our portals.



Some issues faced by us.

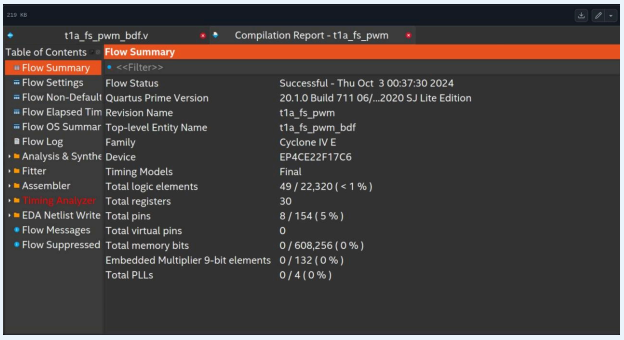


Working on Intel Quartus Prime Lite Installation.

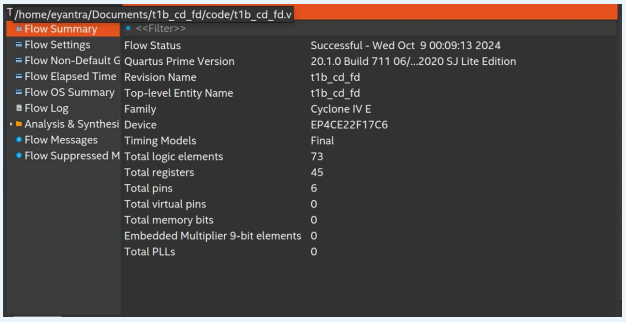
TASK 1: Building the CPU

Sub-tasks were present to work on various different peripherals for our CPU - A Single-cycle RV32I base instruction set, no extension, In-order processor which was later pipelined to a 5-stage processor, we couldn't completely get done with the design in pipelined as we had issues with branch instructions, the single-cycled cpu supports all 40 base instructions. There were enough resources and guidance to design them in few weeks time and find success in simulations.

Lots of notes made, brainstorming and ideation went through this.

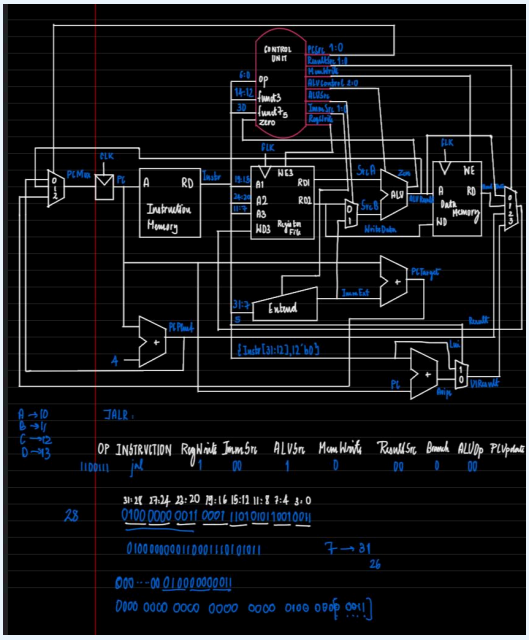


Resource util of our PWM block.

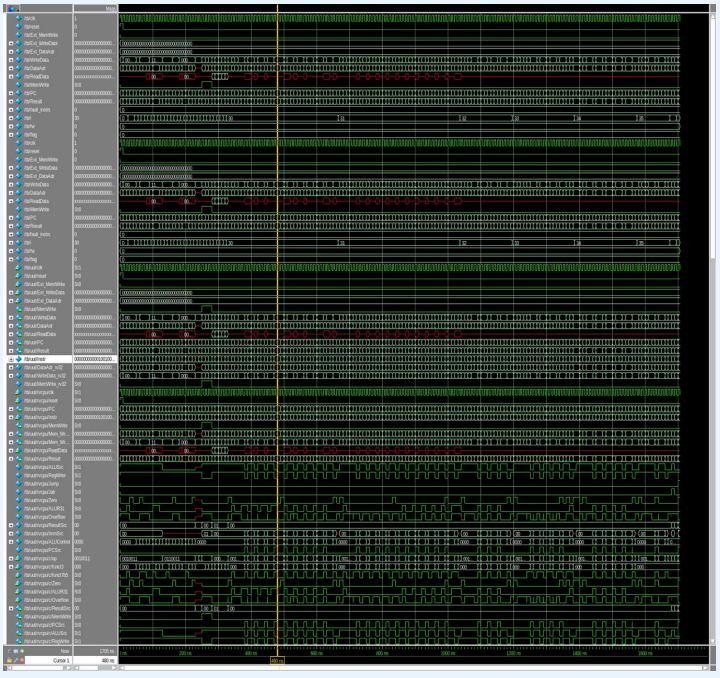


Resource util of our color detection block.

The above are some peripherals used in our CPU design.



Our CPU Datapath and Controller unit.



Our CPU signals running a program in C.

TASK 2: Path Finder Algorithm

We used a DPS and weights based pathfinder algorithm after mapping all the nodes in the arena to our FPGA memory. This was an important task for us as it was the last task of Stage 1, to qualify to stage 2 with hardware sponsorship from IIT Bombay we had to be in Top 50 teams all over the world, predominantly India from 500ish teams eligible for the task, we hadn't previously had a top 100 finish till then but we had the will to go to IIT Bombay for finals.

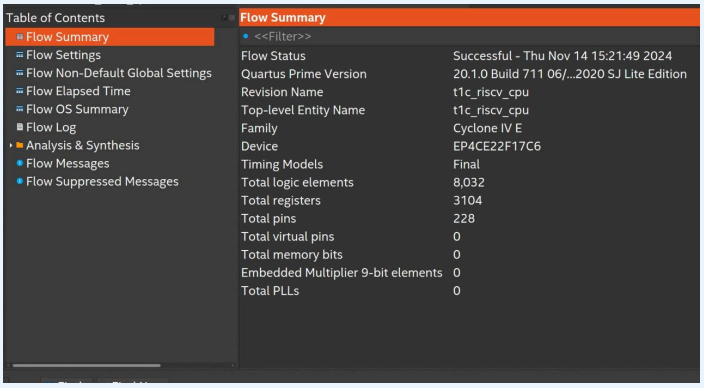
```
238: f85ff06f   jal     x0,1bc
1bc: 0d67c703   lbu     x14,214(x15)
1c0: 0ff77713   andi    x14,x14,255
1c4: 04e57063   bgeu    x10,x14,204
204: 0907a603   lw      x12,144(x15)
208: 0d67c703   lbu     x14,214(x15)
20c: 00e59733   sll     x14,x11,x14
210: 00c77733   and     x14,x14,x12
214: 00070a63   beq     x14,x0,228
228: 0d67c703   lbu     x14,214(x15)
22c: 00170713   addi    x14,x14,1
230: 0ff77713   andi    x14,x14,255
234: 0ce78b23   sb      x14,214(x15)
238: f85ff06f   jal     x0,1bc
```

Riscv 32 assembly instructions from our path finder algorithm written and compiled in C.

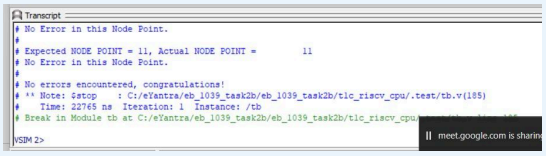
Memory Data - /tb/uut/instrmem/instr_ram - Default

```
00000000 02000117 04010113 02000197 7f818193
00000004 02000517 ff050513 39000593 00000613
00000008 330000ef 02000517 fdc50513 00000593
0000000c 00000613 340000ef 02000517 fc850513
00000010 308000ef 00000513 00000593 008000ef
00000014 0000006f fd010113 02112623 02812423
00000018 422007b7 02000437 00f42823 a01007b7
0000001c 00f42a23 5c0007b7 00f42c23 200007b7
00000020 00f42e23 02f42023 02f42223 81c007b7
00000024 02f42423 801007b7 0a078793 02f42c23
00000028 402817b7 02f42e23 001607b7 04f42023
0000002c 000807b7 04f42223 000987b7 04f42423
00000030 000207b7 04f42623 000267b7 04f42823
00000034 000087b7 04f42a23 000097b7 40078793
00000038 04f42c23 001037b7 80078793 04f42e23
0000003c 000017b7 06f42023 000027b7 30078793
00000040 06f42223 40000793 06f42423 48200793
00000044 06f42623 002007b7 14078713 01878793
00000048 06f42c23 02000793 06f42e23 02600793
0000004c 06e42823 08f42023 08000713 00800793
00000050 06e42a23 08f42223 02842623 02842823
00000054 02842a23 10900793 08f42423 00200793
00000058 08f42623 08042823 02000613 09440513
0000005c 0ff00593 200000ef 00044683 09042703
00000060 00100793 00d797b3 00e7e7b3 08f42823
00000064 00044783 00044703 02000613 0ff7f793
00000068 00f40433 020007b7 08e40a23 00100893
0000006c 01078e13 80000eb7 02000313 00000693
00000070 0907a583 00d89733 0ff6ff13 00b77733
00000074 02070463 00269513 01c50533 00000713
00000078 00052803 00eed5b3 0105f5b3 02059263
0000007c 00170713 fe6716e3 00168693 fc6692e3
00000080 fff60613 0ff67613 fa061ae3 0380006f
00000084 0907a803 00e895b3 00b87833 fc081ae3
00000088 0907a803 0105e5b3 08b7a823 00e785b3
0000008c 09e58a23 0047c583 0ff77813 0ff5f593
00000090 fb0598e3 02000737 09072683 00474603
00000094 00100793 00c797b3 00d7f7b3 08078063
00000098 0c070a23 00474703 020007b7 0ff77713
0000009c 0007c683 0ff6f693 06e69c63 0d47c703
000000a0 fff00593 02000537 0ff77713 00170693
000000a4 0ff6f693 0cd78a23 0007c683 00e78733
000000a8 0ad70a23 0d47c703 0ff77713 00070793
000000ac 40f706b3 fff78613 0ff6f693 04b61e63
000000b0 00000793 02000637 0ff7f693 06e6e463
000000b4 020007b7 00100713 00e78623 02c12083
000000b8 02812403 00000513 03010113 00008067
000000bc 0d47c683 0ff6f693 00168613 0ff67613
000000c0 0cc78a23 00d786b3 0ae68a23 00e78733
000000c4 09474703 f5dff06f 00f507b3 0b37c783
000000c8 02010813 00d806b3 fef68023 00060793
000000cc f81ff06f 00f106b3 0006c683 00178793
000000d0 00d60423 f85ff06f 00050213 00008067
000000d4 00050313 00060e63 00058383 00730023
000000d8 fff60613 00130313 00158593 fe0616e3
000000dc 00008067 00050313 00060a63 00b30023
000000e0 fff60613 00130313 fe061ae3 00008067
000000e4 00000000 00000000 00000000 00000000
```

Data memory of our algorithm with information on nodes and other program variables.



CPU resource util, yep pretty big.



Yay we got no errors finally after almost crying ourselves to bed thinking we lost the plot.

Stage II

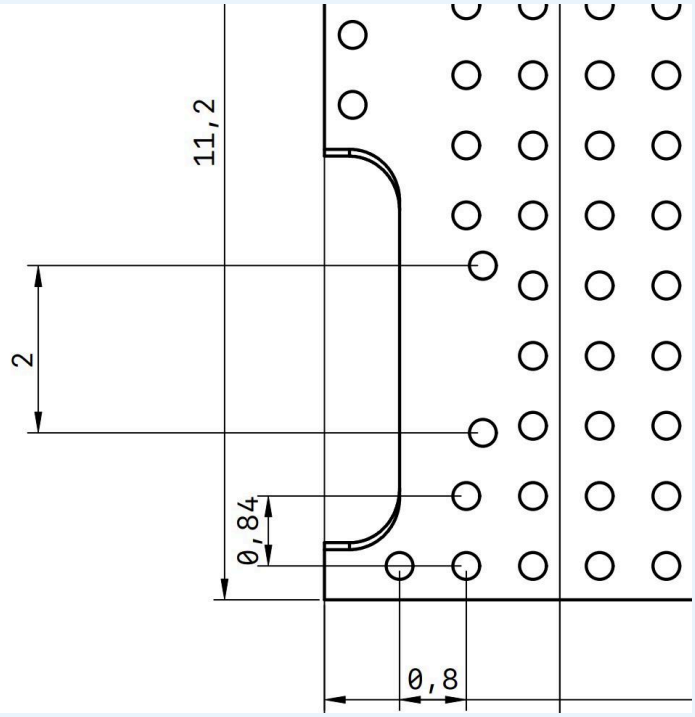
Then came the D-day, the day of result and guess what, we had a dream finish, 29th read the leader board against our team Id, this meant we are in game still and IIT Bombay will themselves provide us with all the components we require, except the chassis and the resource gripper arm which had to be designed and fabricated by us. The FPGA which costed about INR 15000.00 was given to us free of cost in a returnable basis.

RANK	TEAM	MARKS
#1	EB#1651	103.78
#2	EB#1706	103.75
#3	EB#4051	103.18
#4	EB#3699	102.62
#5	EB#1041	102.59
#6	EB#1274	102.54
#7	EB#2266	102.37
#8	EB#1739	102.37
#9	EB#1269	102.29
#10	EB#3149	102.26
#29	EB#1039	102.12

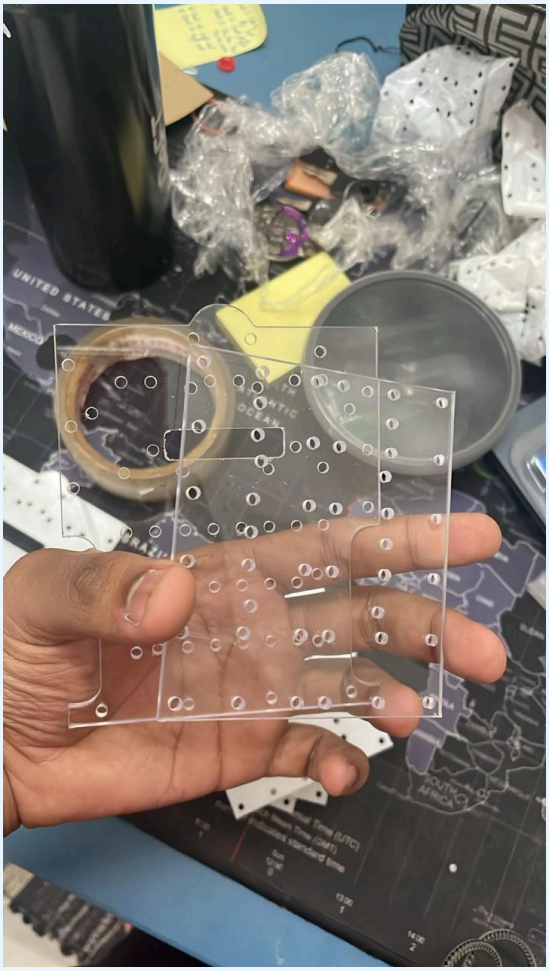
Our months of work from 500ish teams.

Package we finally received from IIT B

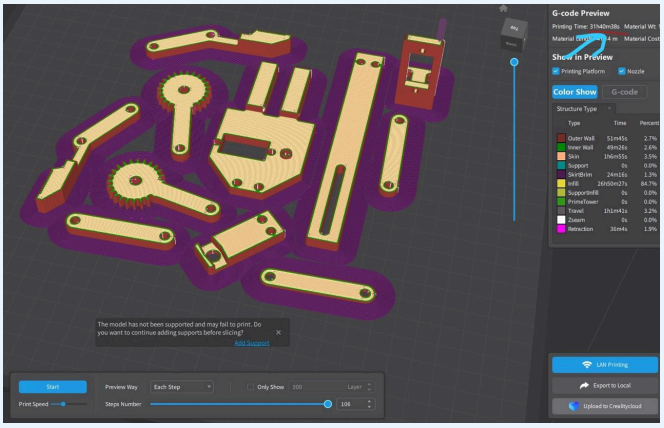
The next Tasks we tough not only because of the hardware nature but also because of the semesters and holiday season where we spent most of our times away from family even during our semester break, Christmas and New Year, To ideate and build this bad boy.



Chassis designed on a combo of Shapr3d and AutoCAD.

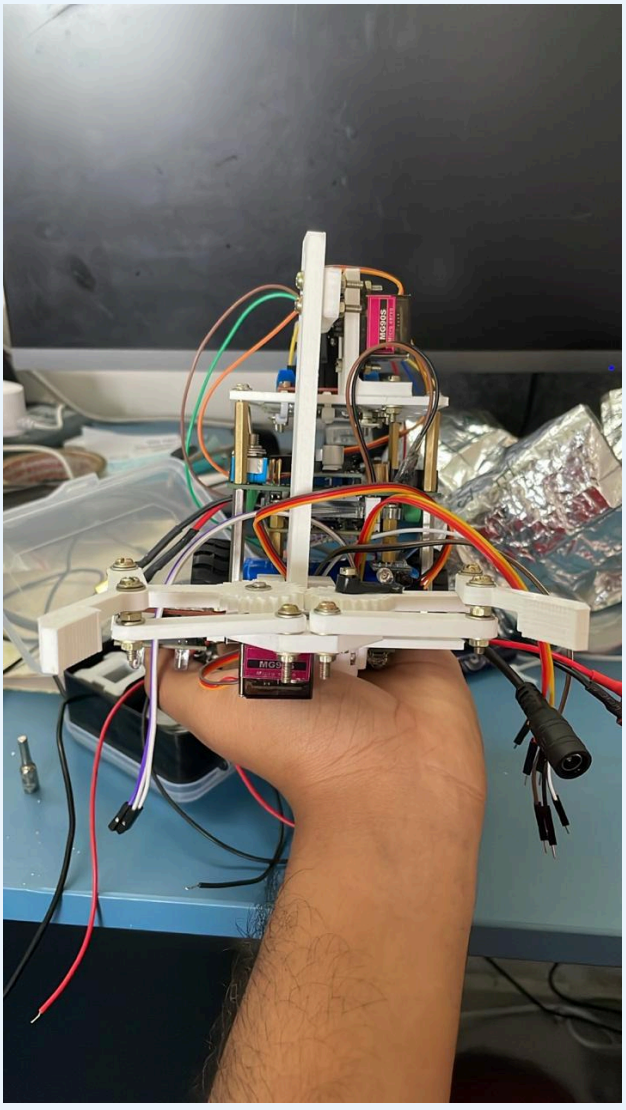


Chassis was made in 4 different materials with 2 copies of each design. The above is acrylic.

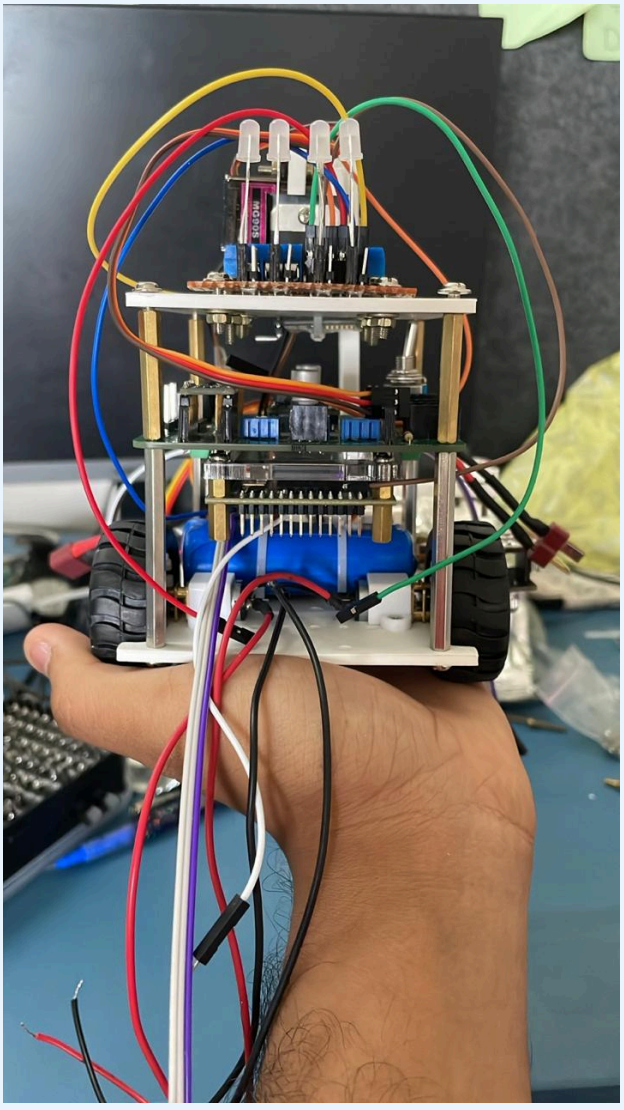


Custom designed gripper arm on Fusion 360 and printed using PLA plastic

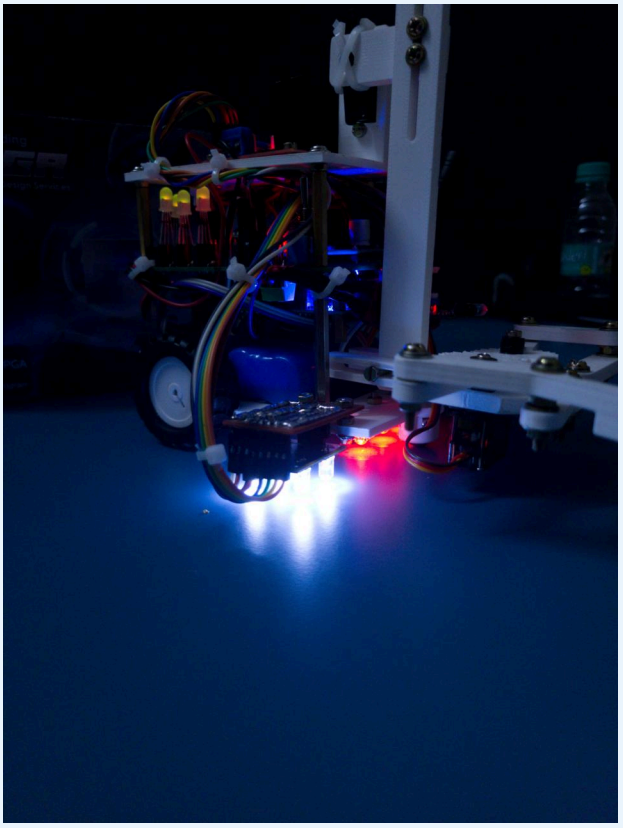
Gripper arm in action on target pick-up block.



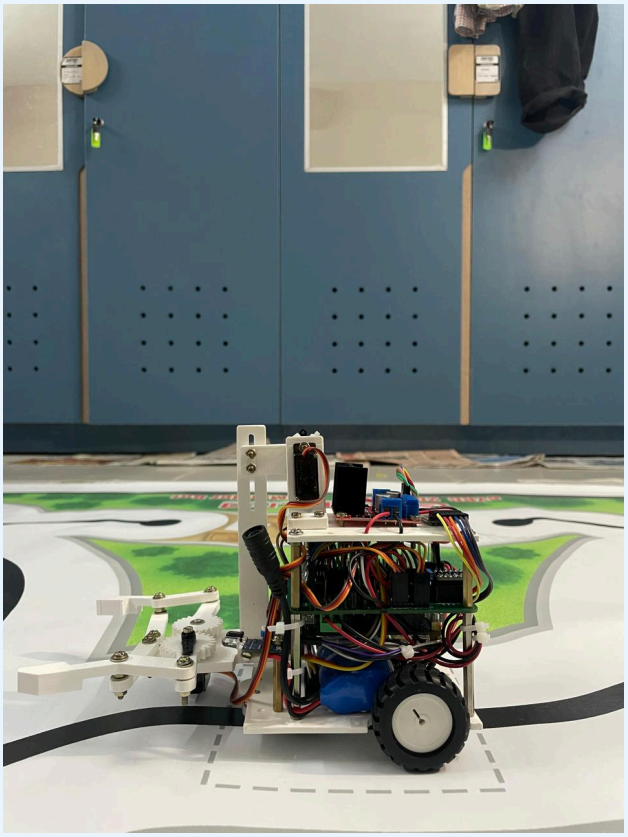
Front View of Bot during wiring phase.



Rear View of Bot during wiring phase.



Shared cuz sick lights.



Our bot going through a run on our arena.

We went through so much testing, designing and redesigning that it is not possible to contain everything or share everything in this article, so shared some completed results and test runs, we finished **TASK 3**, hardware bot design and flex sheet design with some of the best scores but met with severe challenges later with out UART protocol system failing after a brief period of it working and failing just before our **TASK 4** and **TASK 5** submission which saw a heart-breaking end to our 2025 theme campaign. We gave the bot all care and for several months it felt as a part of us, we had to later on pack him up to IIT B and claim our certificates for our run. * *In the End bgm intensifies*

THE END

It is truely one of a kind experience for all of us who took part, we learnt a ton in the journey, networked with others in discussion forums, saw other people innovating, took motivation and for 6 months everyday we worked to complete 29th on grid.
~Signing off TEAM EB#1039

Team EB#1039:

1. Ajitessh R - ECE Batch 2026
2. Sreeram R - ECE Batch 2026
3. Vineeth Roshan Premanand - ECE Batch 2026

4. G Kavin Rajan - CSE Batch 2026