Next Generation Computer Architecture

Assignment: ChampSim Simulator

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Traces used in this assignment:

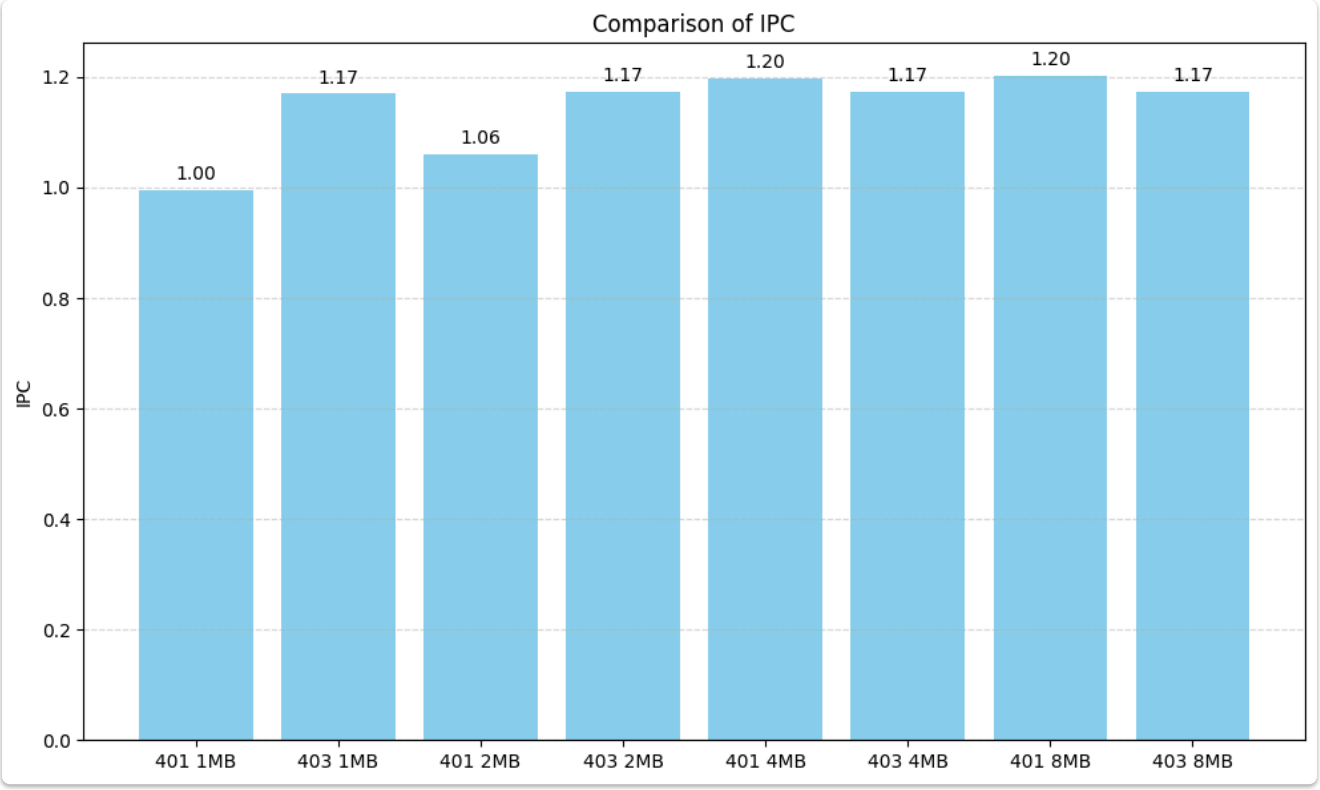
```
401.bzip2-277B.champsimtrace.xz
403.gcc-16B.champsimtrace.xz
434.zeusmp-10B.champsimtrace.xz
437.leslie3d-273B.champsimtrace.xz
450.soplex-92B.champsimtrace.xz
456.hmmer-327B.champsimtrace.xz
462.libquantum-1343B.champsimtrace.xz
482.sphinx3-1522B.champsimtrace.xz
605.mcf_s-665B.champsimtrace.xz
619.lbm_s-3766B.champsimtrace.xz
```

Simulator setup specifications:

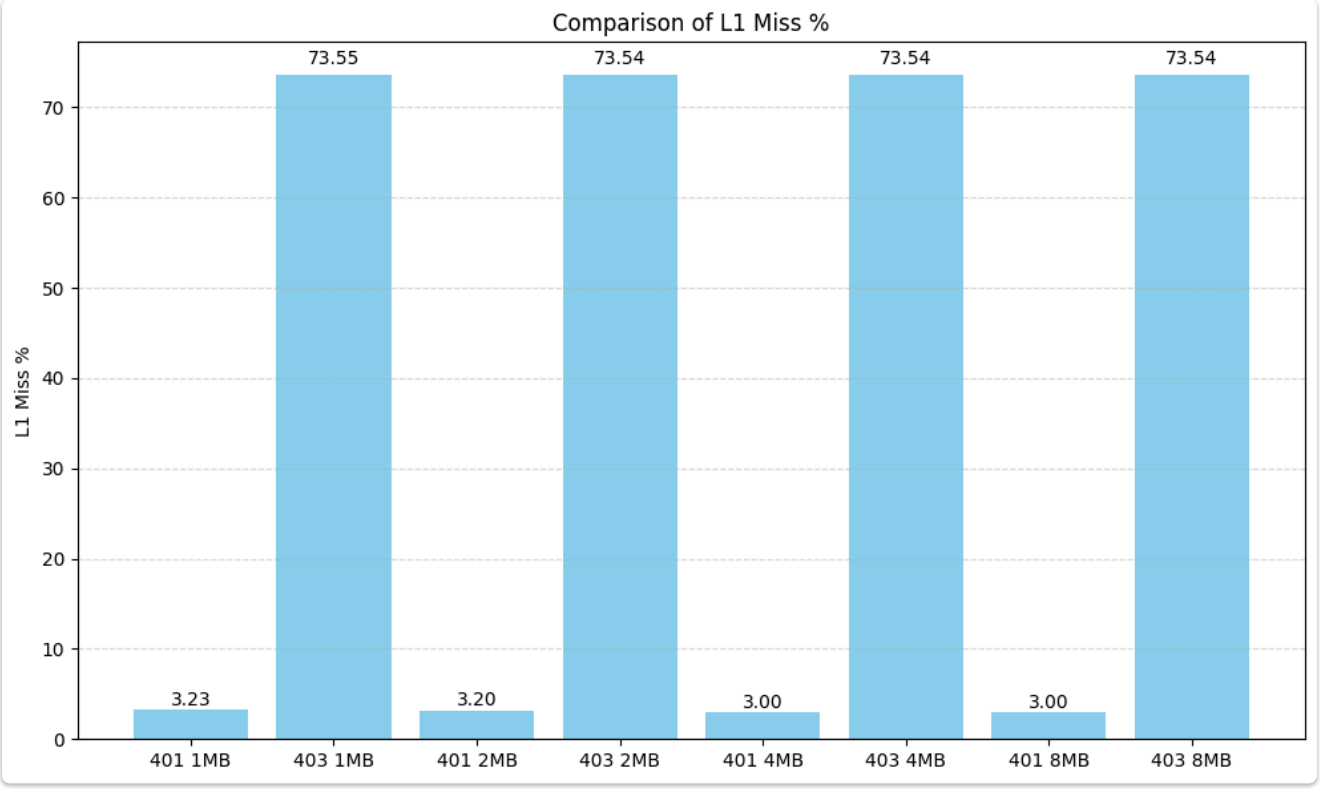
Single-core,
L1-I cache 32KB, L1-D Cache 32KB,
L2 cache 256KB,
L1 and L2 associativity 8-way
LLC associativity 16
L1 and L2 replacement policy: LRU
LLC Replacement policy: LRU (except for Task-3)
L3 cache (LLC) 4MB (except for task-1)
Block size for all levels of cache: 64B

Results to be collected: Cumulative IPC, miss% at L1, L2 and L3 caches, LLC hit rate, total writes at LLC and execution time

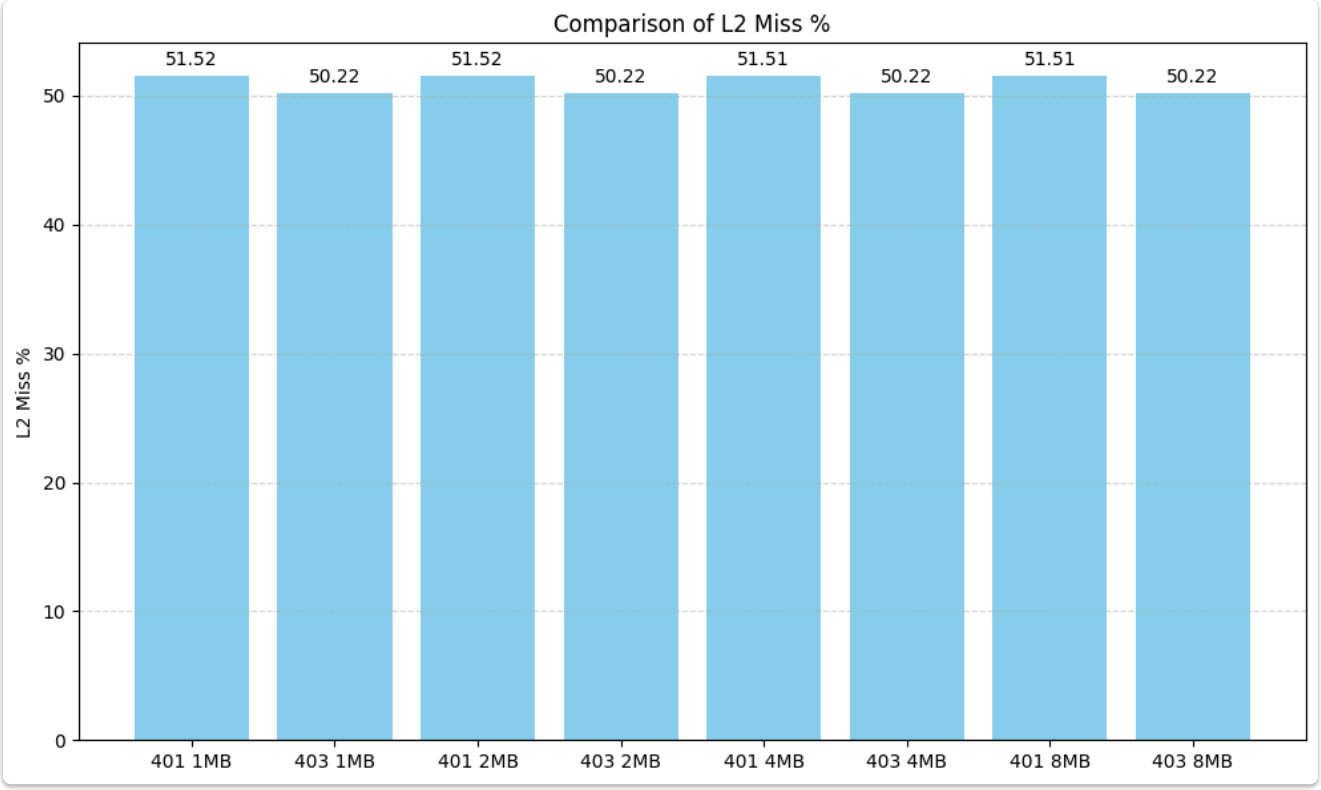
TASK 1: Size of last level cache (LLC): 1MB, 2MB, 4MB, 8MB.



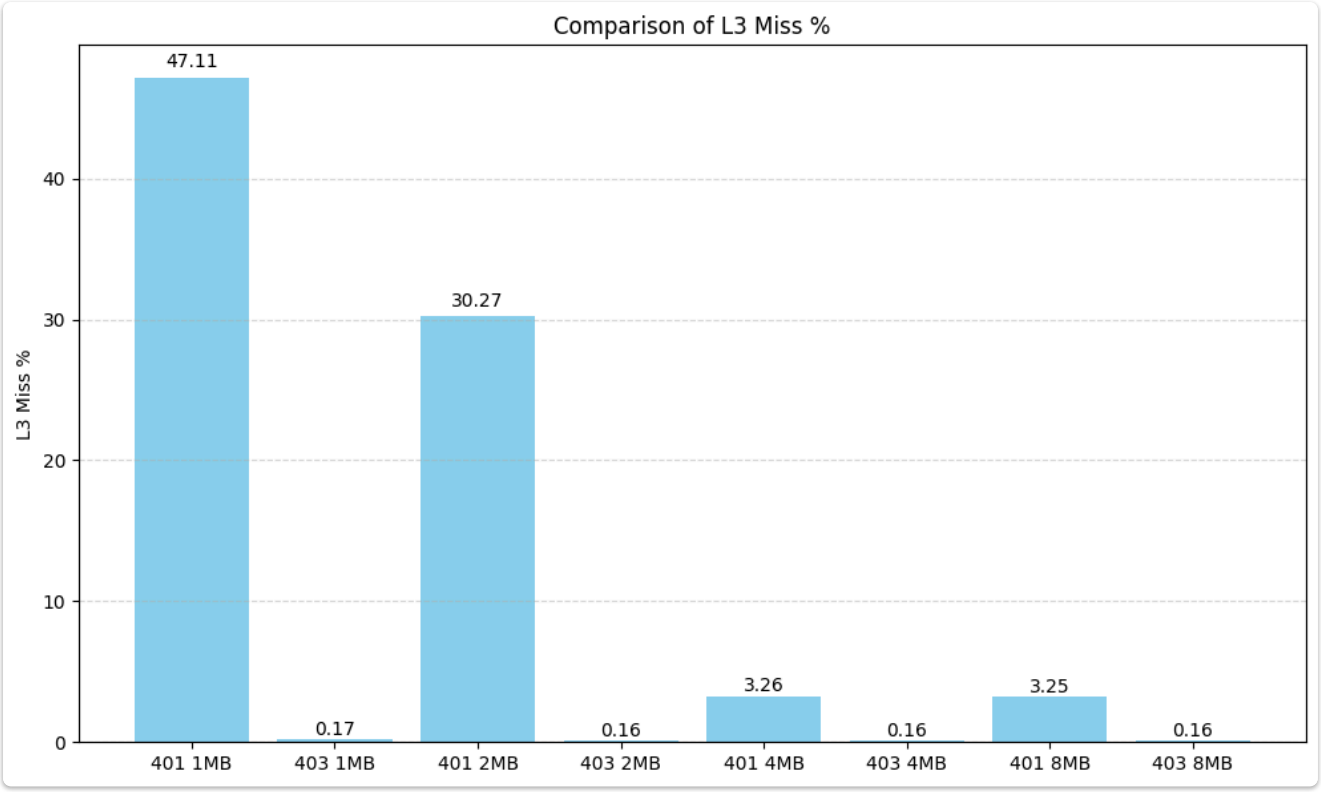
[Inference: IPC]
Best: 401 8MB (IPC = 1.20)
Worst: 401 1MB (IPC = 1.00)



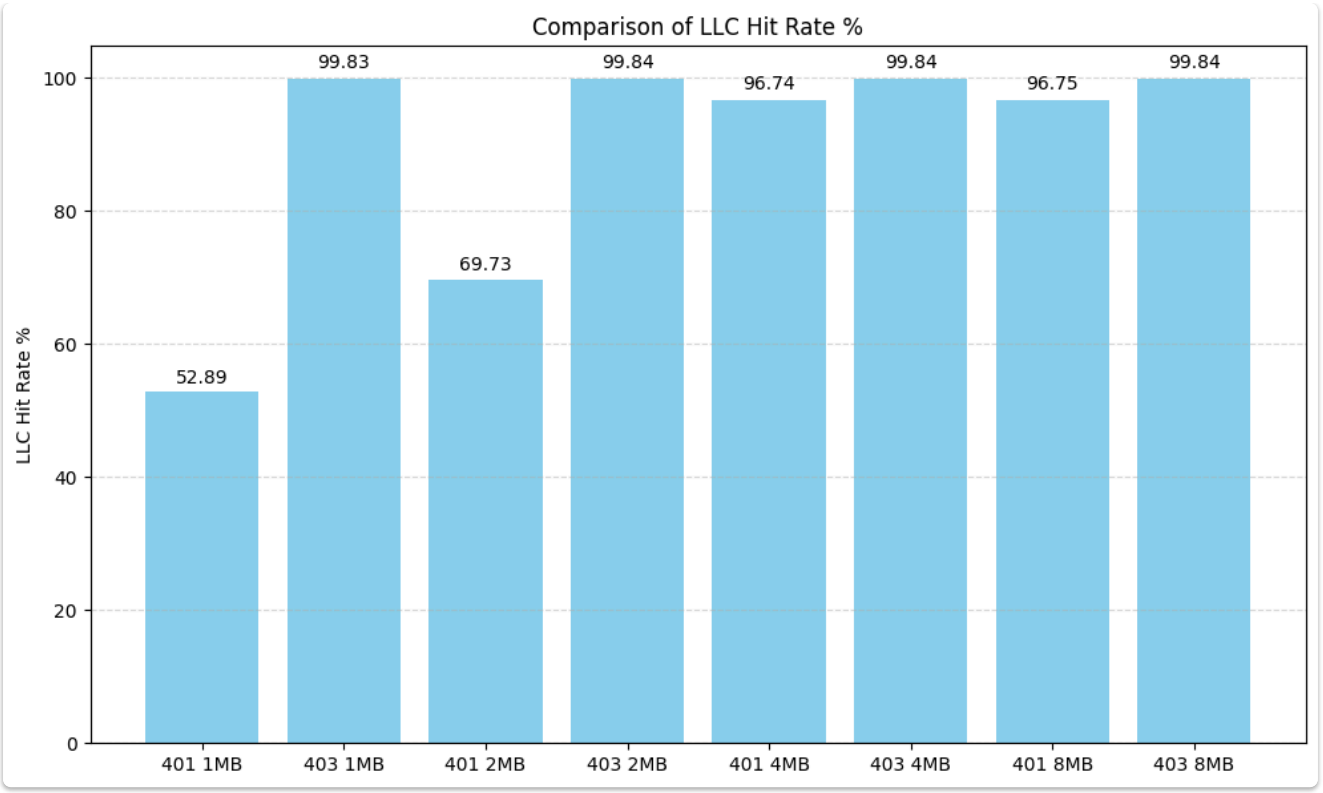
[Inference: L1 Miss %]
Best: 401 8MB (L1 Miss % = 3.00)
Worst: 403 1MB (L1 Miss % = 73.55)



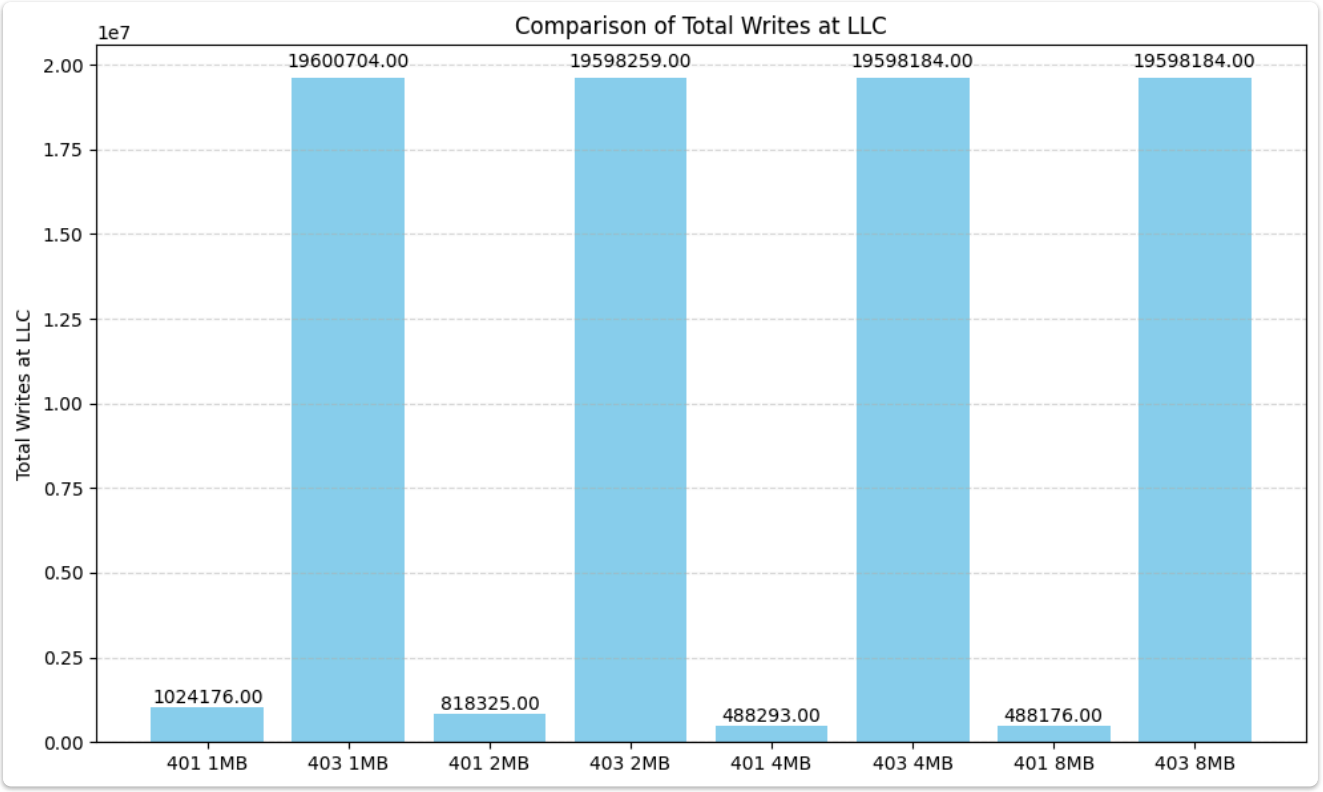
[Inference: L2 Miss %]
Best: 403 1MB (L2 Miss % = 50.22)
Worst: 401 1MB (L2 Miss % = 51.52)



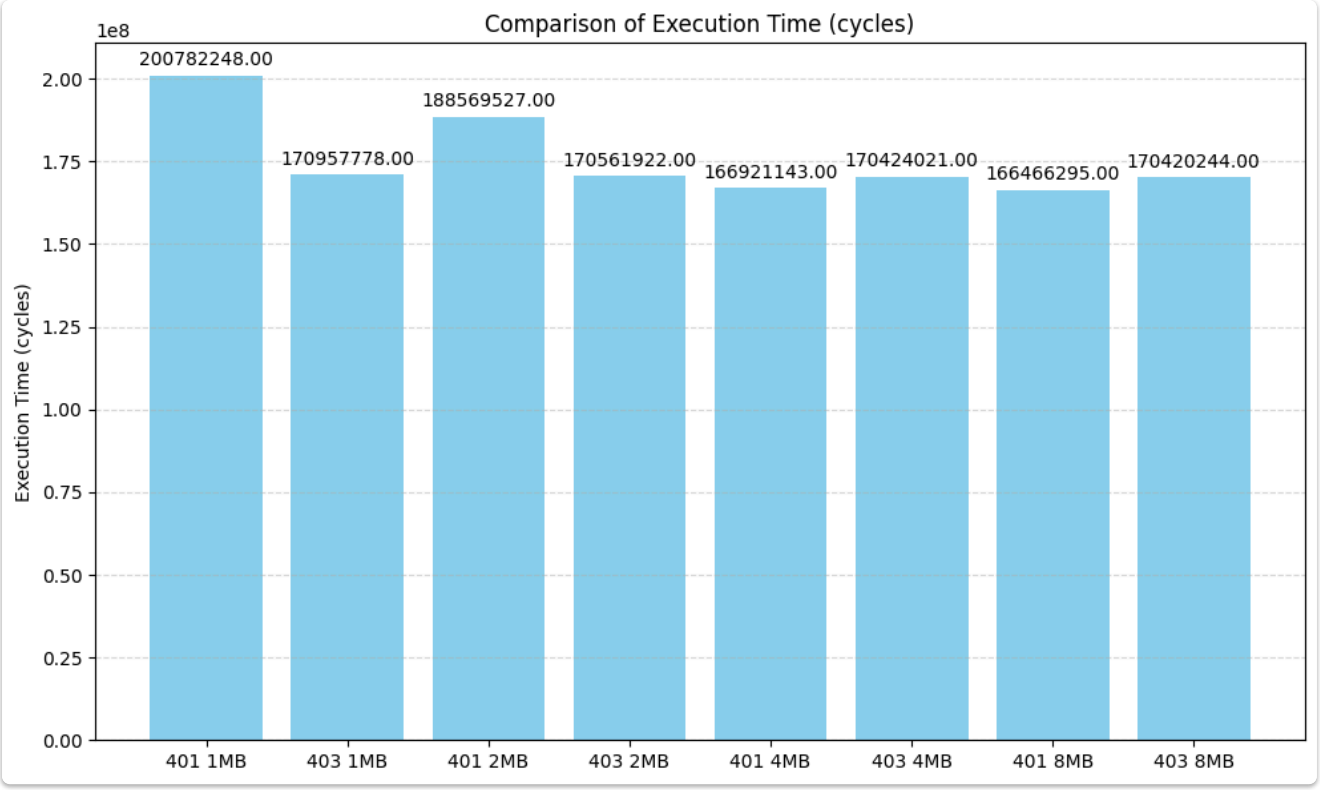
[Inference: L3 Miss %]
Best: 403 4MB (L3 Miss % = 0.16)
Worst: 401 1MB (L3 Miss % = 47.11)



[Inference: LLC Hit Rate %]
Best: 401 1MB (LLC Hit Rate % = 52.89)
Worst: 403 8MB (LLC Hit Rate % = 99.84)



[Inference: Total Writes at LLC]
Best: 401 8MB (Total Writes at LLC = 488176.00)
Worst: 403 1MB (Total Writes at LLC = 19600704.00)



[Inference: Execution Time (cycles)]
Best: 401 8MB (Execution Time (cycles) = 166466295.00)
Worst: 401 1MB (Execution Time (cycles) = 200782248.00)

Due to time constraints all my other simulation results are there in my github repo:

GitHub