VLSI ARCHITECTURE PROJECT

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Proposed paper: Improved Logarithmic Multipliers for Energy-Efficient Neural Networks

This paper presents an improved logarithmic multiplier (ILM) for energy-efficient neural networks (NNs). The ILM replaces multiplication with shift and addition operations, reducing energy usage while staying within NNs' error tolerance. A novel nearest-one detector (NOD) circuit and a compact adder enhance efficiency. Benchmark tests show the ILM achieves significant energy savings and improved classification accuracy compared to exact multipliers. The authors optimize the design based on synaptic weight characteristics and demonstrate the ILM's superiority over existing logarithmic multipliers in energy efficiency and accuracy.