GITAM Bengaluru Campus, NH 207, Nagadenahalli Doddaballapura

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"Ring Oscillator Using CMOS Inverter"

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MTech in VLSI Design

Technical Seminar

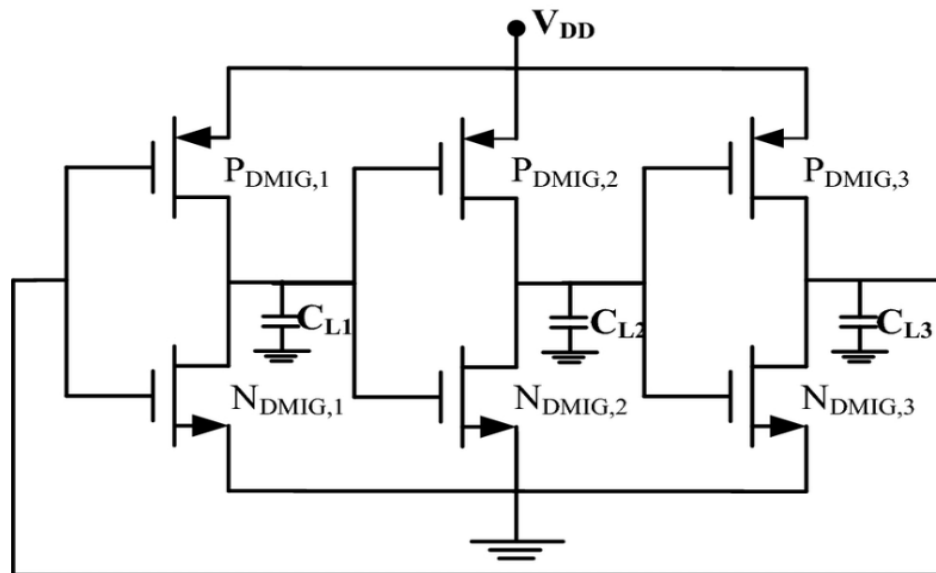# *Ring Oscillator using CMOS Inverter*

Figure 1 Ring Oscillator using CMOS Inverter Circuit Diagram

- ## What is Ring Oscillator?

  o A ring oscillator is a closed-loop circuit with an odd number of inverting stages that produces a continuous oscillating signal.

- ## What is the purpose of Ring Oscillator ?

  o Generate a periodic, oscillating signal.
  o Provide clock signals for digital circuits.
  o Enable frequency synthesis.
  o Facilitate built-in self-test (BIST) in ICs.
  o Function as voltage-controlled oscillators (VCOs).
  o Contribute to random number generation.

- ## Why it is used?

  o Ring oscillators are used because they provide a simple and efficient way to generate oscillating signals for various electronic applications.

- Simplicity:

  - Ring oscillators can be constructed with a minimal number of components, making them easy to design and implement, especially in integrated circuits.

- Integration:

  - They are highly suitable for on-chip integration, which is crucial in modern microelectronics.

- Versatility:

  - They can be adapted to serve a wide range of functions, from basic clock generation to more complex applications like frequency synthesis and random number generation.

- Cost-effectiveness:

  - Their simplicity translates to lower manufacturing costs compared to more complex oscillator designs.

- On chip clock generation:

  - They are very good at creating clock signals directly on integrated circuits.

- ## What are the applications of Ring Oscillator?

  - Clock generation
  - Frequency synthesis
  - Built-in self-test (BIST)
  - Voltage-controlled oscillators (VCOs)
  - Random number generation
  - Timing circuits

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1. Introduction:

- Ring oscillators are fundamental circuits used in various applications, including clock generation, frequency synthesis, and built-in self-test (BIST) circuits. This report focuses on the design and analysis of a Ring oscillator using CMOS Inverter, a basic yet important circuit for understanding oscillator behavior. The operation of a ring oscillator relies on the propagation delay of an odd number of inverting stages, creating a feedback loop that results in sustained oscillations. This case study aims to characterize the performance of a Ring oscillator using CMOS Inverter using Cadence Virtuoso in the gpdk090 technology.

2. Circuit Design:

2.1. Simulation and testing tool

This report presents the design, simulation, and analysis of a Ring oscillator using CMOS Inverter implemented in the gpdk090 technology. The circuit, consisting of three CMOS inverters, was designed using Cadence Virtuoso. Transient analysis was performed to characterize the oscillator's performance. The circuit utilizes PMOS and NMOS transistors with a width of 120nm and capacitors of 1uF. The simulation results demonstrate sustained oscillations with a frequency of approximately 10MHz. The design methodology, simulation setup, and key performance metrics, including oscillation frequency and waveform characteristics, are discussed.

2.1. Circuit Description:

o The ring oscillator consists of three cascaded CMOS inverters connected in a feedback loop. Each inverter is composed of a PMOS and NMOS transistor pair. The inherent propagation delay of the inverters introduces a phase shift, and with an odd number of stages, the signal fed back is inverted, leading to oscillation. The circuit is powered by a 1.8V DC supply. Capacitors (C0, C1, C2) are connected at the output of each inverter to ground. These capacitors are likely used as load capacitors to influence the oscillation frequency and waveform characteristics.
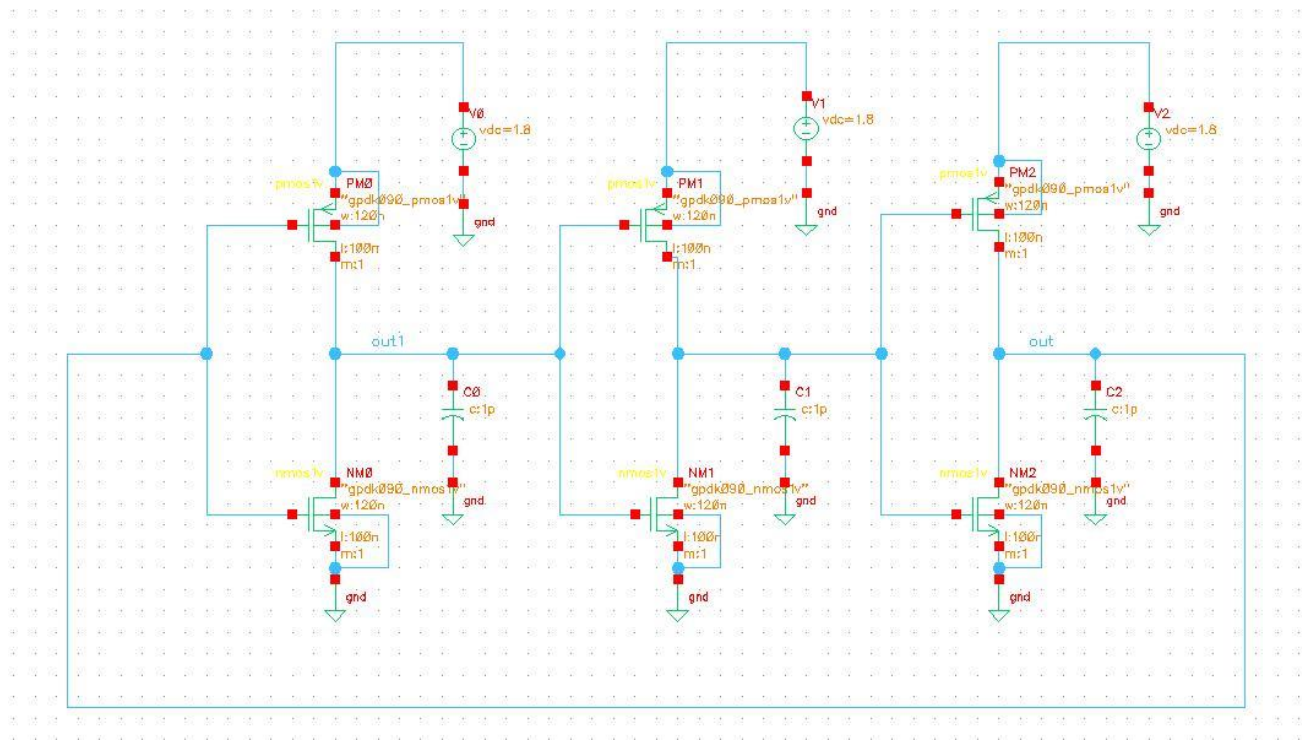
2.2. Schematic Diagram:

Figure 2 Schematic of Ring oscillator using CMOS Inverter

2.3. Component Selection:

o The PMOS transistors (pmos1v) and NMOS transistors (nmos1v) were selected from the gpdk090 technology library. Both the PMOS and NMOS transistors have a width (W) of 120nm and a multiplier (m) of 1. This transistor sizing was chosen to achieve a balance between drive strength and power consumption. The capacitors (C0, C1, C2) are all 1uF. These capacitors are used as load capacitors to affect the oscillator's frequency and the shape of the output waveform. The 1.8V supply voltage is a typical value used in the gpdk090 technology.

3. Simulation and Analysis:

3.1. Simulation Setup:

o   Transient analysis was performed using Cadence Virtuoso ADE L. The simulation parameters included a simulation time of 1us. The output to be plotted was selected from the schematic, specifically the 'out' node at the output of the last inverter stage. To aid in convergence and ensure the oscillator started correctly, the 'Convergence Aid' feature was used, and an initial condition of 0V was set at the 'out' node. This technique is often used in oscillator simulations to help the simulation reach a stable oscillating state.
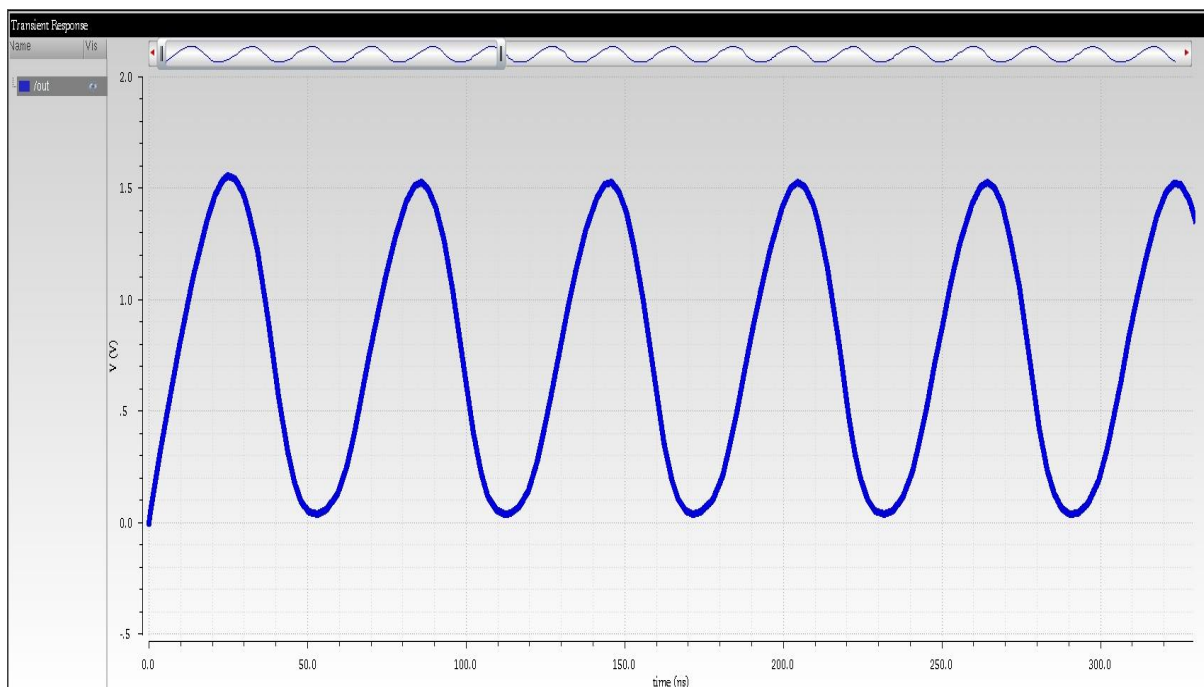
3.2. Transient Analysis Results:
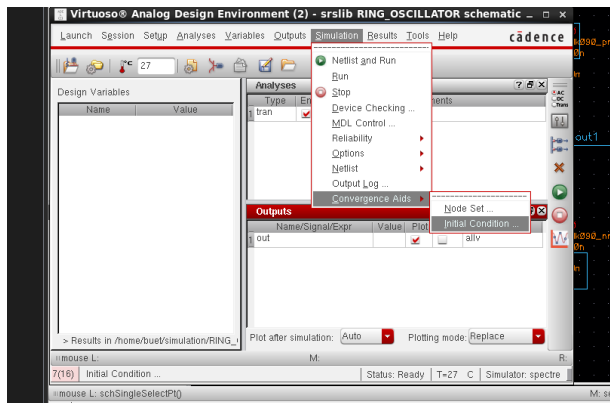

Figure 3 Output Waveform
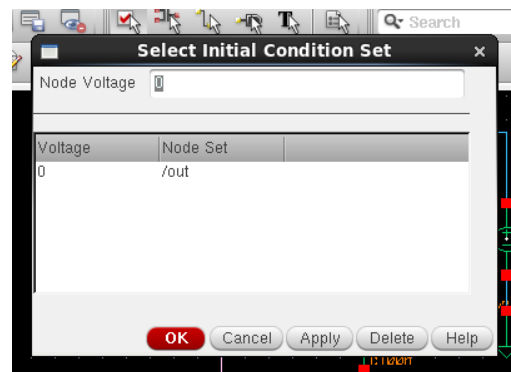
Figure 5 Simulation to be selected

Figure 4 Node Voltage value

o The transient analysis results, as shown in the waveform, demonstrate sustained oscillations, confirming the functionality of the designed ring oscillator. The waveform exhibits a somewhat rounded, triangular shape, indicating that the rise and fall times are not instantaneous. The amplitude of the oscillation ranges from approximately 0V to 1.8V, which corresponds to the supply voltage. The oscillation period is approximately 100ns, resulting in an oscillation frequency of approximately 10MHz. The rise time and fall time are estimated to be around 20ns and 20ns, respectively. This can be observed from the output waveform.

3.3. Performance Analysis:

o The oscillation frequency of 10MHz is influenced by several factors, including the transistor sizes (W/L ratios), the load capacitance (1uF capacitors), and the supply voltage (1.8V). Increasing the transistor sizes would generally increase the drive strength and potentially increase the oscillation frequency, while increasing the load capacitance would typically decrease the oscillation frequency. The rounded shape of the waveform suggests that the rise and fall times could be improved (i.e., made sharper) by optimizing the transistor sizing or reducing the load capacitance. However, these changes might affect other performance parameters like power consumption. The frequency of the oscillator can be modified by changing the W/L ratio of the transistors, the value of the capacitors C0, C1 and C2, and the value of the power supply.

4. State of Art

No.	Time Period	Technology and Key Features	Performance Metrics	Applications and Usage	Economic Considerations
1	1990-1995	CMOS technology, basic ring oscillator designs, larger feature sizes.	Lower frequency, higher power consumption, less stable output, larger device dimensions.	Early microprocessor clock generation, basic digital systems.	Moderate cost, higher than simpler oscillators due to integration.
2	1995-2000	Refined CMOS, BiCMOS introduction, emphasis on power reduction.	Improved frequency stability, lower power, BiCMOS for higher speed.	More complex digital systems, early communication devices.	CMOS cost reduction, BiCMOS more expensive.
3	2000-2005	Deep submicron CMOS, VCOs for frequency synthesis, ADPLL.	GHz frequencies, further power reduction, increased density.	Communication systems, high-performance processors.	CMOS scaling lowers cost, VCO/ADPLL adds complexity.
4	2005-2010	Nanometer CMOS (90nm, 65nm), low-power design, improved VCOs.	Higher frequencies, lower power, leakage current challenges, better VCO phase noise.	Multi-core processors, advanced communication, mobile.	Stable cost due to complexity, lower cost per function.
5	2010	Ring Oscillator using CMOS Inverter (Your Project): CMOS Inverters, 120nm transistors	Frequency: 10MHz	Basic oscillator circuit, educational demonstration	Part of academic exercise/simulation, specific cost not applicable
6	2010-2015	Continued scaling (32nm, 22nm),	Speed and power improvements, variability	High-speed data, advanced SoCs,	Higher design costs, lower manufacturing costs.

		variability and reliability focus, PLLs for high-speed.	concerns, complex designs for variability management.	specialized applications.	
7	2015-2020	FinFET technology, power management, energy efficiency, ring oscillators in IoT.	Improved energy efficiency, better leakage control, ultra-low power design.	IoT devices, wearable technology, energy-efficient systems.	FinFET initially higher, costs became competitive.
8	2020-2025	FinFET scaling, GAA FETs, specialized applications (AI, 5G), integration with sensors/RF.	Extremely high frequencies, ultra-low power, specialized performance.	AI hardware, 5G, advanced sensing, highly integrated SoCs.	GAA FETs are premium, higher costs, long-term reduction expected.

Table 1 Evolution of Oscillator Technologies

5. Conclusion:

- This report presented the design, simulation, and analysis of a Ring oscillator using CMOS Inverter in the gpdk090 technology. The transient analysis in Cadence Virtuoso confirmed the circuit's ability to generate sustained oscillations. The oscillator exhibited a frequency of approximately 10MHz. The waveform shape indicates that there is room for optimization in terms of rise and fall times. Further investigation could explore the impact of different transistor sizes, load capacitance values, and supply voltages on the oscillator's performance, with the goal of improving frequency stability, reducing power consumption, and achieving sharper rise and fall times.

6. References:

- [Improved Performance of Ring Oscillator Design](#)
- [https://www slideshare.net/slideshow/ring-oscillatorpptx/265759012](https://www.slideshare.net/slideshow/ring-oscillatorpptx/265759012).
- https://youtu.be/d2DAu4f-9-c?si=fifCAcWHEz8WYSLr
- https://github.com/SriSagarA/Ring-oscillator-using-CMOS-Inverter.git