Homework 1

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CS2323 Computer Architecture(CS16BTECH11044)

September 5, 2018

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1. Given No of accesses = 50000000 accesses/sec
   Leakage power = 0.07W
   Dynamic Energy =0.8nJ/access
   Execution time = 1sec
   leakage energy = 0.07 * 1 J = 0.07J
   Dynamic energy = 0.8nJ * 50000000 = 0.8*0.05 = 0.04J
   % of leak energy =(0.07)/(0.07+0.04) =63.63%.

2. TLB is amount of memory accessible from the TLB.
   TLB Reach=(TLB Size)*(Page Size)
   TLB1 Reach= (4kB)*(64) = 256kB
   TLB2 Reach= (2MB)*(32) = 64MB
   TLB3 Reach= (1GB)*(8) = 8GB
   TLB Reach = 256kB+64MB+8GB = 8.064256GB

3. Given block size =4
   offset = $log_2 4 = 2$ bits
   8 sets means set index is $log_2 8 = 3$ bits

	Tag	Set Index	Offset
0	000	000	00
63	001	111	11
1	000	000	01
62	001	111	10
2	000	000	10
61	001	111	01
3	000	000	11
60	001	111	00
4	000	001	00
59	001	110	11
5	000	001	01
58	001	110	10
6	000	001	10
57	001	110	01
7	000	001	11
56	001	110	00
8	000	010	00
55	001	101	11
9	000	010	01
54	001	101	10
10	000	010	10
53	001	101	01
11	000	010	11
52	001	101	00

cache-1
Tag is the first 3 bits and set index is the next 3 bits and the offset is in next 2 bits.

3bits	3 bits	2 bits
Tag	Setindex	offset

cache-2
Tag is the last 3 bits, and set index is the before 3 bits and the rest is offset.

2 bits	3 bits	3 bits
Offset	Setindex	Tag

a)For accessing the sequence by cache 1 After comparing set index and tag the hit miss sequence of these address access is:

0	63	1	62	2	61	3	60	4	59	5	58	6	57	7	56	8	55	9
M	M	H	H	H	H	H	H	M	M	H	H	H	H	H	H	M	M	H

54	10	53	11	52
H	H	H	H	H

ratio = $\frac{hits}{access} = \frac{18}{24} = \frac{3}{4}$

For accessing the sequence by cache 2 After comparing set index and tag the hit miss sequence of these address access is:

0	63	1	62	2	61	3	60	4	59	5	58	6	57	7	56	8	55	9
M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M

54	10	53	11	52
M	M	M	M	M

ratio = $\frac{hits}{access} = \frac{0}{24} = 0$

b)

	Tag	Setindex	offset
0	000	000	00
64	010	000	00
128	100	000	00
192	110	000	00
1	000	000	01
65	010	000	01
129	100	000	01
193	110	000	01
11	000	010	11
75	010	010	11
139	100	010	11
203	110	010	11
9	000	010	01
137	100	010	01
201	110	010	01
73	010	010	01

For accessing the sequence by cache 1 After comparing set index and tag the hit miss sequence of these address access is:

0	64	128	192	1	65	129	193	11	75	139	203	9	137	201	73
M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M

ratio = $\frac{hits}{access} = \frac{0}{16} = 0$
For accessing the sequence by cache 2 After comparing set index and tag the hit miss sequence of these address access is:

0	64	128	192	1	65	129	193	11	75	139	203	9	137	201	73
M	H	H	H	M	H	H	H	M	H	H	H	M	H	H	H

ratio = $\frac{hits}{access} = \frac{12}{16} = \frac{3}{4}$

4. Frequency of P1 = 2.2 GHz
Frequency of P2 = 1.6 GHz
No.of instruction in program = 10^6

No of instructions in A = $\frac{20}{100} * 10^6 = 2 * 10^5$

No of instructions in B = $\frac{25}{100} * 10^6 = 25 * 10^4$

No of instructions in C = $\frac{45}{100} * 10^6 = 45 * 10^4$

No of instructions in D = $\frac{10}{100} * 10^6 = 1 * 10^5$

CPI of P1 A=1,B=2,C=3,D=4
Total cycles for P1 to run a program = $\sum_{i=1}^{1=4} A_i$ * instructions in A_i
= 1*2 * 10^5 + 2 *25 * 10^4 + 3 *45 * 10^4 + 4 *1 * 10^5
=$24.5 * 10^5$
Time taken for P1 to run a program = $\frac{no.of.cycles}{frequency}$
= $\frac{24.5*10^5}{2.2GHz}$
CPI of P2 A=2,B=2,C=2,D=2
Total cycles for P2 to run a program = 2*2 * 10^5 + 2 *25 * 10^4 + 2 *45 * 10^4 + 2 *1 * 10^5
= 2 * 10^6
Time taken for P2 to run a program = $\frac{no.of.cycles}{frequency}$
= $\frac{2*10^6}{1.6GHz}$
As time taken for P1 is less than P2
So P1 is faster for this program.

5. After every write miss P+1 bit will be 1 and after every read miss P+1 bit will be 0

P0	P1	P2	P3	P+1
1	0	0	0	0

After P0 has read miss

P0	P1	P2	P3	P+1
0	1	0	0	1

After P1 has write miss

P0	P1	P2	P3	P+1
0	0	0	1	1

After P3 has write miss

P0	P1	P2	P3	P+1
0	0	1	1	0

After P2 has read miss

P0	P1	P2	P3	P+1
0	0	1	0	1

After P2 has write miss

P0	P1	P2	P3	P+1
1	0	1	0	0

After P0 has read miss

6. Two applictions are running on L2 cache Given that number of misses are scaled linearly
   So difference of misses between successive ways for application 1
   $=\frac{1000-400}{6-2} = 150$
   So difference of misses between successive ways for application 2
   $=\frac{2000-1800}{6-2} = 50$

way	2	3	4	5	6
application1	1000	850	700	550	400
application2	2000	1950	1900	1850	1800

   As the cache is given as 8 way,
   To improve the performance we must have less misses
   misses = ways in application1 * misses in application1 +ways in application2 *misses in application2

Application1(ways)	Application2(ways)	misses
2	6	2*1000+6*1800 =12800
3	5	3* 850+5*1850 =11800
4	4	4*700+4*1900 =10400
5	3	5*550+3*1950 =8600
6	2	6*400+2*2000 =6400

   So misses are minimum if 6 ways for application1 and 2 ways for application2

7. Given transaction rate of P=34/min
   transaction rate of Q=58/min
   transaction rate of R=81/min Given each of them make 500 transactions.
   Total no of transactions=500*3=1500

Time taken for running 1500 transactions=(500/34)+(500/58)+(500/81)
= 29.49min
Average transactions per minute =(1500/29.49)=50.86 transactions/min
We use harmonic mean here.

8. Assume 100s of time period. Time taken by the system0 is 100sec.(since it is single core).
   time taken by system1 for initialisation =25sec.
   time taken by system1 for vision-processing =37sec.
   time taken by system1 for signal-processing =38sec.
   Overall time for system1=25+(38/10)+(37/6).
   =34.96
   Speedup of system1 over system0 is (100/34.96) i.e 2.86

9. Given that running at 3GHz and 1Volt the program takes 30 sec to execute. Voltage is linearly dependent on the frequency. If voltage is 1.2V then frequency becomes 1.2 times.
   (i)Hence the smallest time it needs to execute a program is (30/1.2)sec=25sec.
   (ii)Dynamic power=V*V*f=V*V*V(since V and f are linearly related)
   Leakage power is also proportional to V
   Total power =(80*V*V*V)+30*V
   =64.96W.
   (iii)Energy = power*time
   =((80*V*V*V)+30*V)*(30/V)
   =((80*V*V*V)+30)*(30/V)
   =((80*V*V)+(30))*30
   =2436J

10. Given virtual address =48bit
    Physical memory =2GB=31 bits addressing
    Page size is given as 2kB means offset=11bits.
    The offset length remains same in virtual as well as the physical address.
    Number of bytes for storing one map in TLB = 48+31-11-11 =57bits
    Number of entries =32.
    The size of TLB =32*57 bits= 228Bytes.

11. In a given cycle, the addresses coming to the four ports of TLB are:
    0x4795BA21, 0x4795BB21, 0x5795BA21 and 0x4785BA21.
    Frame size is given as 1kB,offset=10
    Here the address 0x4795BA21,0x4795BB21 are same if we do not consider offset.That means both are same.
    So no of unique accesses =4-1=3.

12. (a)By following the LRU policy, we get the following hit(H)/miss(M) sequence:

A	B	C	D	A	B	C	D	A	B	C	D
M	M	M	M	M	M	M	M	M	M	M	M

(b)By following the MRU policy, we get the following hit(H)/miss(M) sequence:

A	B	C	D	A	B	C	D	A	B	C	D
M	M	M	M	H	M	M	H	M	M	H	M