Date: 15-02-2024   Marks: 60 Marks

Time: 3 hrs

Part A (Answer all Question: (10*2=20)

1. List the challenges in exposing instruction level parallelism.
2. Compare linear and non-linear pipeline.
3. When do we say that a cache block is exclusive?
4. What happens when a private and shared items are cached?
5. List the disadvantages of using symmetric shared memory.
6. What are the issues that occur with cache coherence?
7. In what way is multicore processor superior to single core processor?
8. Define the effectiveness of power utilization.
9. What is Kung's taxonomy?
10. Compare scalar and vector processors.

Part B (Answer any four: 4*10 = 40)

1. Explain in detail the Flynn's Classification.
2. Explain and illustrate with an example of Instruction Pipeline.
3. Evaluate the given matrix using a Systolic Array Processor. Draw a neat Systolic Array Matrix diagram and explain.
4. Assume that, a program has 100 lines of code (LOC) and each instruction takes 1 second to execute
   a) What is the total time taken to execute 100 LOC when we use a simple pipeline mechanism?
   b) Also calculate the total time to execute when we use super scalar pipelining technique.
5. Choose any four multicore architecture which you have studied analyze their advantages and disadvantages and present a summary of it.
6. Explain in detail the types of pipelining hazards and its dependencies.