PONDICHERRY UNIVERSITY – KARAIKAL CAMPUS
DEPARTMENT OF COMPUTER SCIENCE
END SEMESTER EXAMINATION MARCH 2022
ADVANCED COMPUTER ARCHITECTURE

Answer Any Four (4*10 = 40) Time: 10.30 A.M – 12.30 P.M

1. Assume that a simple addition of two elements requires a unit time. You are required to compute the execution time needed to perform the addition of a 40. 40 elements array using each of the following arrangements:
   (a) A SIMD system having 64 processing elements connected in nearest-neighbor fashion. Consider that each processor has only it's local memory.
   (b) A SIMD system having 64 processing elements connected to a shared memory through an interconnection network. Ignore the communication time.
   (c) A MIMD computer system having 64 independent elements accessing a shared memory through an interconnection network. Ignore the communication time.

2. Consider the two tasks T0 and T1 that are executed in parallel on processors P1 and P2, respectively, in a shared memory system. Assume that the print statement is uninterruptible, and A, B, C, D are initialized to 0.

T0	T1
A = 1;	C = 3;
B = 2;	D = 4;
Print A, D; Print B, C;	

3. Show four different possible outputs of the parallel execution of these two tasks. Consider a bus-based shared memory system consisting of three processors. The shared memory is divided into four blocks x, y, z, w. Each processor has a cache that can fit only one block at any given time. Each block can be in one of two states: valid (V) or invalid (I). Assume that caches are initially flushed (empty) and that the contents of the memory are as follows:

Memory block	x	y	z	w
Contents	10	30	80	20

4. Consider the following sequence of memory access events given in order:

   1) P1: Read(x)
   2) P2: Read(x)
   3) P3: Read(x),
   4) P1: x = x + 25
   5) P1: Read(z)
   6) P2: Read(x),
   7) P3: x = 15
   8) P1: z = z + 1

Show the contents of the caches and memory and the state of cache blocks after each of the above operations in the following cases: (1) write-through and write-invalidate and (2) write-back and write-invalidate.

5. Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Calculate-

    a. Pipeline cycle time
    b. Non-pipeline execution time
    c. Speed up ratio
    d. Pipeline time for 1000 tasks
    e. Sequential time for 1000 tasks
    f. Throughput

6. Explain in detail the working principle of PARAM machine. Illustrate with an example of 1000*1000 matrix