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Lab #5 Report

ECE 2031 L08

30 September 2018

APPENDIX A

THE IS THE VHDL (A HARDWARE DESCRIPTION LANGUAGE) IMPLEMENTATION OF A STATE MACHINE WHOSE LOGIC IS DESCRIBED BY THE BOOLEAN EXPRESSIONS: ($Q_1^+ = Q_1 \bullet X_0 \;\; OR \;\; X_1 \bullet X_0$ AND $Q_0^+ = Q_0 \bullet \overline{X_0} \;\; OR \;\; X_1 \bullet \overline{X_0}$).

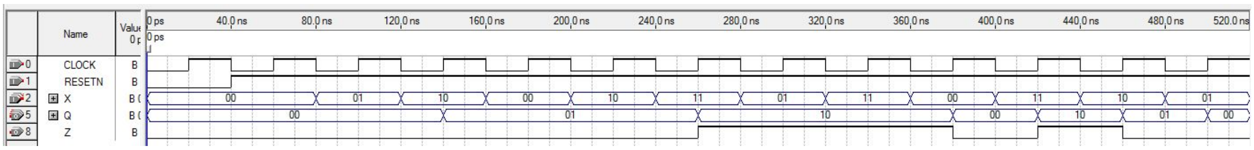

Figure 2. This is a functional simulation of the State Machine whose logic is described by the SM_VHDL.vhd and whose two Boolean Expressions were: ($Q_1^+ = Q_1 \bullet X_0 \;\; OR \;\; X_1 \bullet X_0$ and $Q_0^+ = Q_0 \bullet \overline{X_0} \;\; OR \;\; X_1 \bullet \overline{X_0}$) that used set inputs ($X_1 \; and \; X_0$) from the file: VECTORL08IN.tbl.

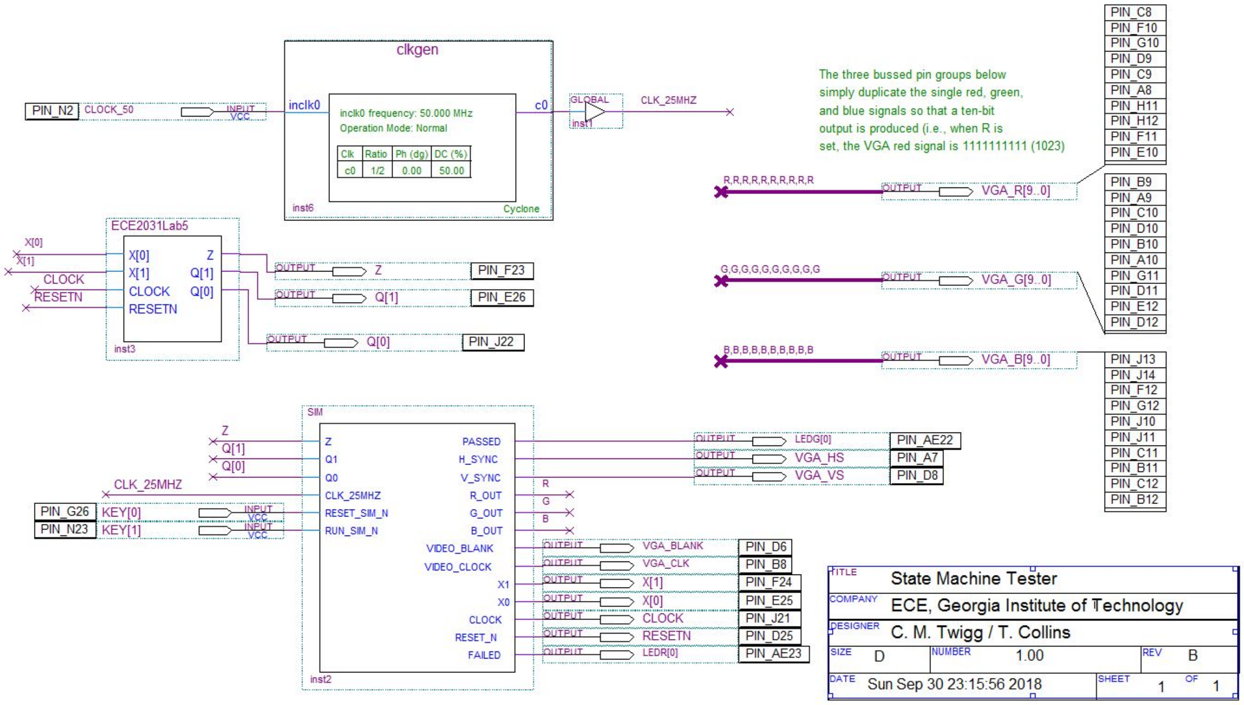

Figure 3. This is the schematic design for the State Machine whose logic is described by the two Boolean Expressions: ($Q_1^+ = Q_1 \bullet X_0 \;\; OR \;\; X_1 \bullet X_0$ and $Q_0^+ = Q_0 \bullet \overline{X_0} \;\; OR \;\; X_1 \bullet \overline{X_0}$) and the State Machine Tester which inputed different values and checked states to see whether the SM_SCHEMATIC (Renamed in diagram as ECE2031Lab5) worked properly.

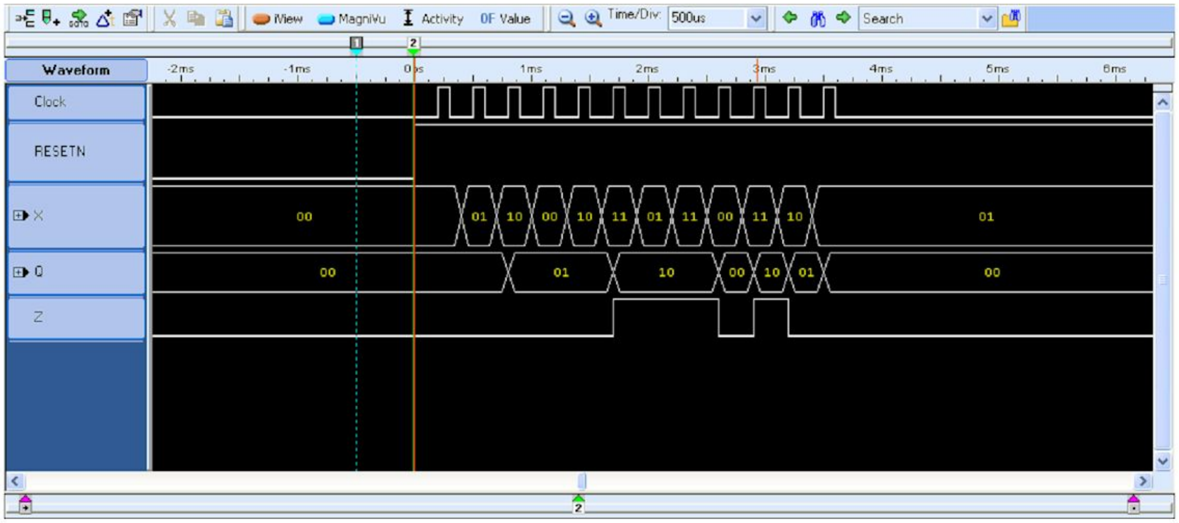

Figure 4. This is a waveform diagram of all the output and input values (1 or 0) for the State Machine whose logic is described by the Boolean Expressions: ($Q_1^+ = Q_1 \bullet X_0 \;\; OR \;\; X_1 \bullet X_0$ and $Q_0^+ = Q_0 \bullet \overline{X_0} \;\; OR \;\; X_1 \bullet \overline{X_0}$).

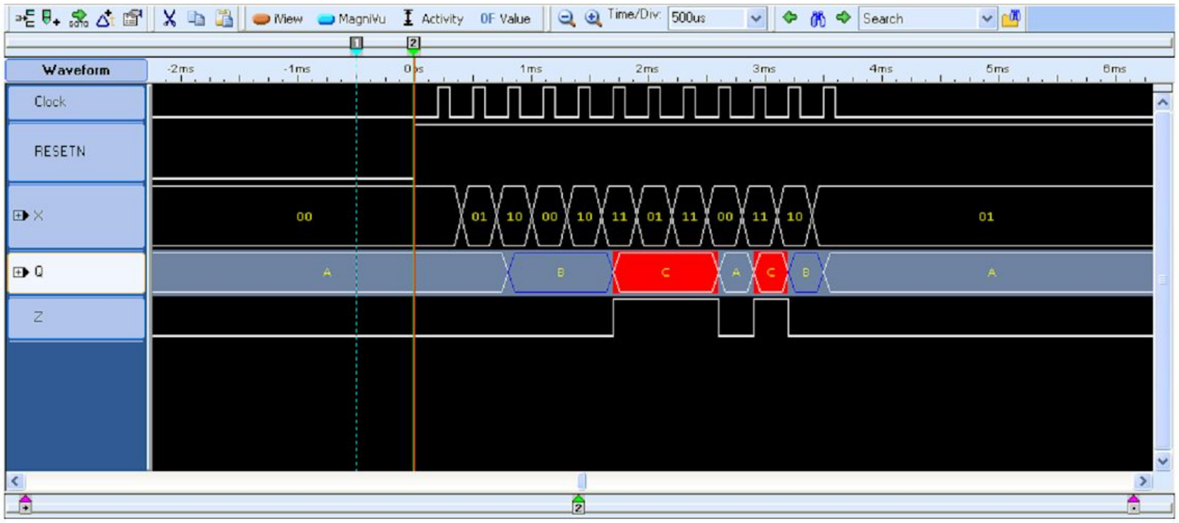

Figure 5. This is a customized waveform diagram of all the output and input values (1 or 0) for the State Machine whose logic is described by the Boolean Expressions: ($Q_1^+ = Q_1 \bullet X_0 \;\; OR \;\; X_1 \bullet X_0$ and $Q_0^+ = Q_0 \bullet \overline{X_0} \;\; OR \;\; X_1 \bullet \overline{X_0}$). It was specially made to show the State Names (A, B, C) and to highlight state "C" in red.

APPENDIX A

```
-- SM_VHDL.vhd
-- Basic State Machine Implementation (Boolean Expression: (Q1 = Q1
AND X0  OR  X1 AND X0  and Q0 = Q0 AND X0  OR  X1 AND X0))
-- Sriharsha Singam
-- ECE 2031 L08
-- October 2, 2018

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.All;

ENTITY SM_VHDL IS  -- Do not modify this entity statement!
  PORT(X       : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
       RESETN,
       CLOCK   : IN  STD_LOGIC;
       Z       : OUT STD_LOGIC;
       Q       : OUT STD_LOGIC_VECTOR(1 DOWNTO 0)  );
END SM_VHDL;       -- Do not modify this entity statement!


ARCHITECTURE behavior of SM_VHDL IS
  TYPE STATE_TYPE IS (A, B, C);
  SIGNAL state : STATE_TYPE;

  BEGIN
    PROCESS(CLOCK, RESETN)
      BEGIN
        IF RESETN = '0' THEN
          state <= A;
        ELSIF CLOCK'EVENT AND CLOCK = '1' THEN
          CASE state IS
            WHEN A =>
              CASE X IS
                WHEN "00"   =>
                           state <= A;
                     WHEN "01"   =>
                           state <= A;
                     WHEN "10"   =>
                           state <= B;
                     WHEN "11"   =>
                           state <= C;
              END CASE;
            WHEN B =>
                CASE X IS
                WHEN "00"   =>
                           state <= B;
                     WHEN "01"   =>
                           state <= A;
                     WHEN "10"   =>
                           state <= B;
                     WHEN "11"   =>
                           state <= C;
              END CASE;
            WHEN C =>
                CASE X IS
                WHEN "00"   =>
                           state <= A;
                     WHEN "01"   =>
                           state <= C;
                     WHEN "10"   =>
                           state <= B;
                     WHEN "11"   =>
                           state <= C;
              END CASE;
          END CASE;
        END IF;
      END PROCESS;
    Z  <= '1' WHEN state = C ELSE '0';
    Q  <= "00" WHEN state = A ELSE "01" WHEN state = B ELSE "10" WHEN
state = C;

  END behavior;
```