8 Bit Advanced RISC Processor

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Abstract

This project presents the design of an 8-bit RISC processor targeted for machine learning and deep learning AI applications in resource-constrained environments. Existing 2025-era processors optimized for AI workloads often exhibit high power consumption, architectural complexity, and limited flexibility for academic exploration.

Problem Statement

To address these limitations, a lightweight five-stage pipelined(Instruction Fetch, Instruction Decode, Execute, Memory Access, and Write Back) RISC architecture with Harvard memory organization is proposed. The processor supports a compact instruction set optimized for arithmetic, logical, shift, and data movement operations commonly used in ML computations. An 8-bit ALU, barrel shifter, and register-based datapath enable efficient low-precision processing.

Methodology

The design is implemented in Verilog HDL and synthesized for FPGA platforms. Emphasis is placed on low power consumption and reduced hardware overhead. The modular architecture supports scalability toward parallel and accelerator-based extensions.

Expected Outcome

Performance results show improved throughput over non-pipelined designs. The processor serves as a foundational compute engine for embedded AI, ML/DL research, and educational applications.