

Assignment-1

1. Simulate a CMOS inverter with following dimensions:

PMOS = 1 μ m/65nm

NMOS = 0.5 μ m/65nm, load capacitor = 5fF, Vdd = 1.2V

- a. Perform transient simulation with 1 GHz clock signal, plot the input and output voltages, PMOS and NMOS currents.
- b. Increase the clock frequency to 2GHz, 4GHz, 8GHz and plot the output waveform.
- c. Obtain DC transfer characteristics of the inverter, obtain the trip point of the inverter.
- d. Observe the effect of doubling PMOS and NMOS (one by one) , on the trip point in the transfer characteristics.
- e. For the original inverter in 1.a , increase the load capacitor to 100fF. Check the output waveform for 1GHz clock input signal.
- f. Insert two inverters of 3x and 9x widths, between the 1st inverter and load capacitor, check the output waveform.
- g. For the inverter in 1.a, check the gate leakage current and source to drain leakage current for $V_{in} = V_{dd}$ and $V_{in} = 0V$

Please include all snapshots in your google doc for this assignment. You can enter very brief discussions for each part, if needed