**Assignment-1**

1. Simulate a CMOS inverter with following dimensions:

PMOS = 1um/65nm

NMOS = 0.5um/65nm, load capacitor = 5fF, Vdd = 1.2V

1. Perform transient simulation with 1 GHz clock signal, plot the input and output

voltages, PMOS and NMOS currents.

b. Increase the clock frequency to 2GHz, 4GHz, 8GHz and plot the output waveform.

c. Obtain DC transfer characteristics of the inverter, obtain the trip point of the inverter.

d. Observe the effect of doubling PMOS and NMOS (one by one) , on the trip point in the transfer characteristics.

e. For the original inverter in 1.a , increase the load capacitor to 100fF. Check the output waveform for 1GHz clock input signal.

f. Insert two inverters of 3x and 9x widths, between the 1st inverter and load capacitor, check the output waveform.

g. For the inverter in 1.a, check the gate leakage current and source to drain leakage current for Vin = Vdd and Vin = 0V

Please include all snapshots in your google doc for this assignment. You can enter very brief discussions for each part, if needed

**2 Assignment :**

Simulate 4T Pixel with given sizes and circuit paramters, obtain Vout vs Id curve for Id varying from 100nA to 1uA

**3 Assignment:**

Simulate the single ended OTA with given device sizes, along with the current mirror based biasing circuit. Obtain AC, DC and Transient simulation results as discussed in class. Also try to increase the gain by 2X using appropriate design steps.

**4 Assignment:**

Simulate the CTIA APS pixel circuit with given design parameters. Obtain Vout vs Iin plot for Iin ranging from 50nA to 500nA. Check the effect of 25mV change in Vt of input device on the Vstart.