Week 0 Learnings

In this week we learnt the process of creating a chip from specifications to a manufacturing design. The key stages and concepts are as follows:

Stage 1: Chip Modelling & Specification (O1)

- The design process with the required specifications **is** represented as a C model.
- Also, a testbench has been written in C language to verify this model.

Stage 2: RTL Design (O2)

- Using Verilog, we have developed an RTL code to develop a “soft copy” of the hardware.
- This is a very crucial step in the System on Chip (SoC) design flow.

Stage 3: Synthesis & Integration (O3)

- **Synthesis:** The RTL code from the previous stage is converted into a Gate Level Netlist.
- **SoC Integration:** The netlist is then combined with other pre-designed blocks including processors, peripherals, analog **IPs** and GPIOs.

As a final step, this integrated design undergoes physical design, which includes floorplanning, placement, and routing to create the chip’s physical layout. This stage directly uses hardened libraries for macros and analog **IPs**.

The final output is a GDSII file, which is passed for DRC (Design Rule Check) and LVS (Layout Versus Schematic) checks, which **ensure** that the design is correct and manufacturable.

Once verified, the GDSII file is sent to the foundry for production.