EC804 - Digital VLSI Testing and Testability

Assignment - 3 Report

Submitted by

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VII SEM B.Tech (ECE)

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in partial fulfillment for the award of the degree

Bachelor of Technology

in

Electronics and Communication Engineering

At

Department of Electronics and Communication Engineering

National Institute of Technology Karnataka, Surathkal.

November 2021

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Problem Statement

Write a program to compute controllability and observability parameters of the circuit used for assignment 1 and 2.

Write a program for ATPG using D-Algorithm (your code should be able to take any netlist and fault as input and generate a test for that). Verify your code for the circuit used in assignment 1.

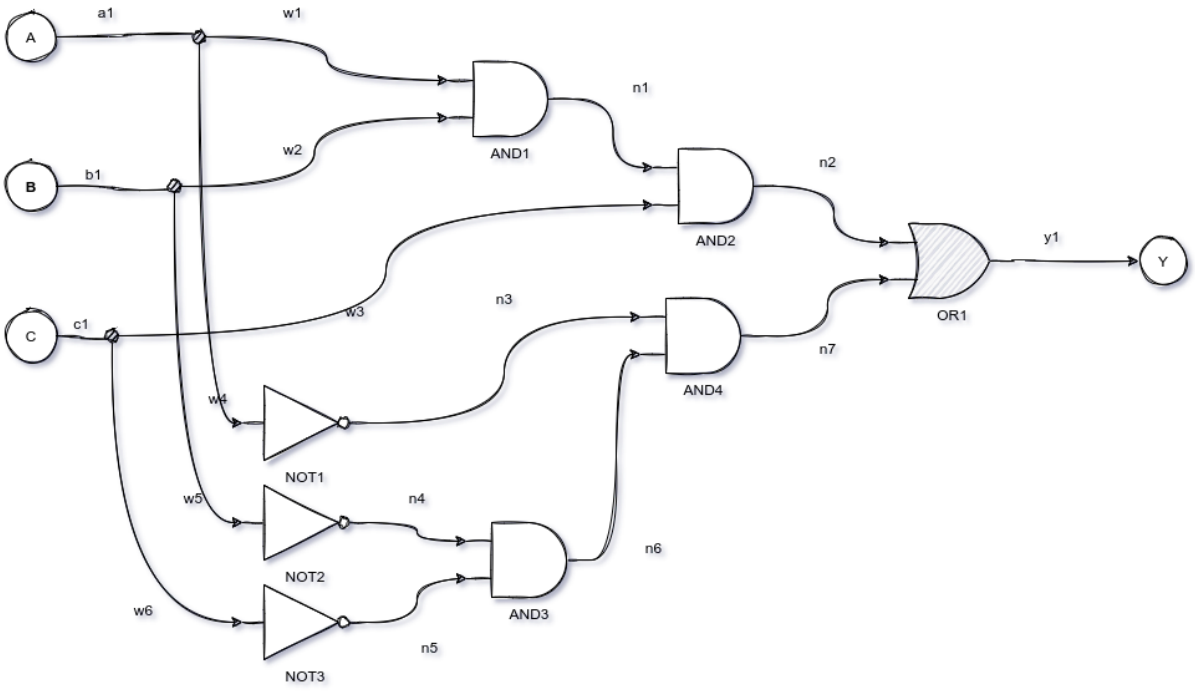
Circuit Description

Inputs : A, B, C

Outputs: Y

Expression: Y = ABC + A'B'C'

Number of gates : 8 (4 AND Gates, 3 NOT Gates, 1 OR Gate)



INPUT NETLIST

```
# 3 inputs
# 1 outputs
# 8 gates (4 ANDs + 3 NOTs + 1 OR)
# Y = ABC + A'B'C'
# assuming all gates have single output
INPUT A
INPUT B
INPUT C

OUTPUT Y
a1 = fanout A
b1 = fanout B
c1 = fanout C
w1 w4 = fanout a1
w2 w5 = fanout b1
w3 w6 = fanout c1
n1 = AND w1 w2
n2 = AND n1 w3
n3 = NOT w4
n4 = NOT w5
n5 = NOT w6
n6 = AND n4 n5
n7 = AND n6 n3
y1 = OR n2 n7
Y = fanout y1
```

SCOAP Parameters

```
srikarsiddarth@onetruth:~/7thSem/VLSI_Testing/assignment3$ python3 SCOAP.py
#       Wire    (CC0,CC1)       CO
15      a1      ( 1, 1)         8
16      b1      ( 1, 1)         8
17      c1      ( 1, 1)         8
18      w1      ( 1, 1)         8
19      w4      ( 1, 1)         10
20      w2      ( 1, 1)         8
21      w5      ( 1, 1)         10
22      w3      ( 1, 1)         8
23      w6      ( 1, 1)         10
24      n1      ( 2, 3)         6
25      n2      ( 2, 5)         4
26      n3      ( 2, 2)         9
27      n4      ( 2, 2)         9
28      n5      ( 2, 2)         9
29      n6      ( 3, 5)         6
30      n7      ( 3, 8)         3
31      y1      ( 6, 6)         0
srikarsiddarth@onetruth:~/7thSem/VLSI_Testing/assignment3$
```

D-Algorithm

```
srikarsiddarth@onetruth:~/7thSem/VLSI_Testing/assignment3$ python3 DAlgoFinal.py
ID      Name    Inputs  Outputs
0       fanout1 ['A']   [15]
1       fanout2 ['B']   [16]
2       fanout3 ['C']   [17]
3       fanout4 [15]    [18, 19]
4       fanout5 [16]    [20, 21]
5       fanout6 [17]    [22, 23]
6       AND1    [18, 20]        [24]
7       AND2    [24, 22]        [25]
8       NOT1    [19]    [26]
9       NOT2    [21]    [27]
10      NOT3    [23]    [28]
11      AND3    [27, 28]        [29]
12      AND4    [29, 26]        [30]
13      OR1     [25, 30]        [31]
14      fanout7 [31]    []
15      a1      0       [3]
16      b1      1       [4]
17      c1      2       [5]
18      w1      3       [6]
19      w4      3       [8]
20      w2      4       [6]
21      w5      4       [9]
22      w3      5       [7]
23      w6      5       [10]
24      n1      6       [7]
25      n2      7       [13]
26      n3      8       [12]
27      n4      9       [11]
28      n5      10      [11]
29      n6      11      [12]
30      n7      12      [13]
31      y1      13      [14]
Enter the Fault location from the list of wires: 22
Enter the type of fault (0 for sa0 and 1 for sa1): 0
Fault Testable?:  True
The test vector can be:  1 1 1
```