

VLSI DESIGN LAB JOURNAL

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Chapter 1

Introduction

Under the guidance of Prof. Ramesh Kini M. this journal focuses on the various lab experiments mentioned in the course EC302 - VLSI DESIGN LAB. The simulation codes used in this journal can be found here -

<https://www.github.com/SrikarSiddarth/VLSI-Design-Lab>

Various circuits were simulated in *ngspice* and layouts were made using *magic* softwares on an *Ubuntu - 16.04* operating system.

Chapter 2

VI Characteristics of NMOS Transistor

OBJECTIVE : Study the input and output characteristics of NMOS Transistor, effects of L, W , V_{to}, lambda, V_{sb}, and temperature on the behaviour of the transistor.

This experiment includes the simulation of a n-channel MOSFET and studying the input and output characteristics of the circuit. The variation patterns in the output voltage were studied by varying the length, width, threshold voltage, V_{sb} (voltage between source and body) and the temperature of the MOSFET within reasonable ranges. A high voltage of 3.3v is given to this circuit.

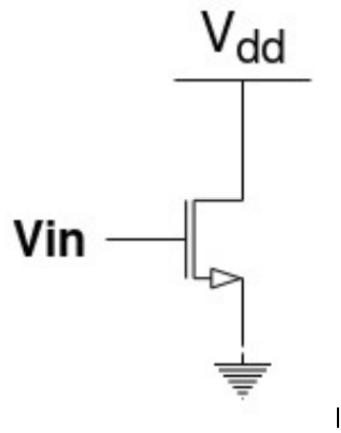


Figure 2.1: NMOS Transistor

The **V_{sb}** was varied from 0 to 1.5V. It was found that when the V_{sb} was less than 0.3V, the MOSFET current increased with increase in V_{gs}. When v_{sb} was equal to 0.3V, the MOSFET current changed order from hundred uA to a

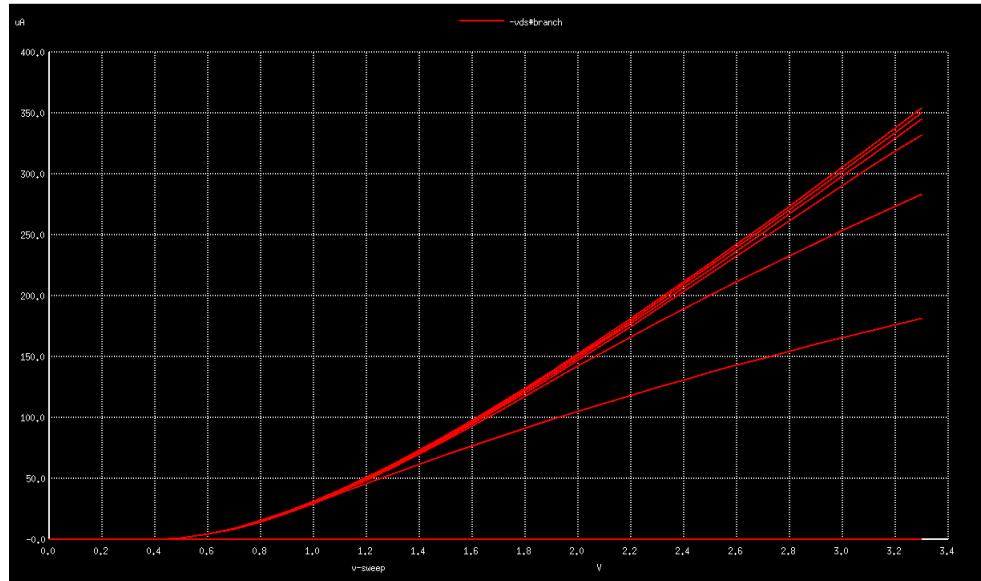


Figure 2.2: Input Characteristics with the V_{gs} on the x-axis and the MOSFET current on the y-axis. The curves with higher V_{ds} shows higher slopes

few fA(which is approximately zero). But a stranger event had occurred when the V_{sb} was increased beyond 0.3V, the current swapped its direction and now would increase in the negative direction with increase in V_{gs} . Refer Fig. 2.12

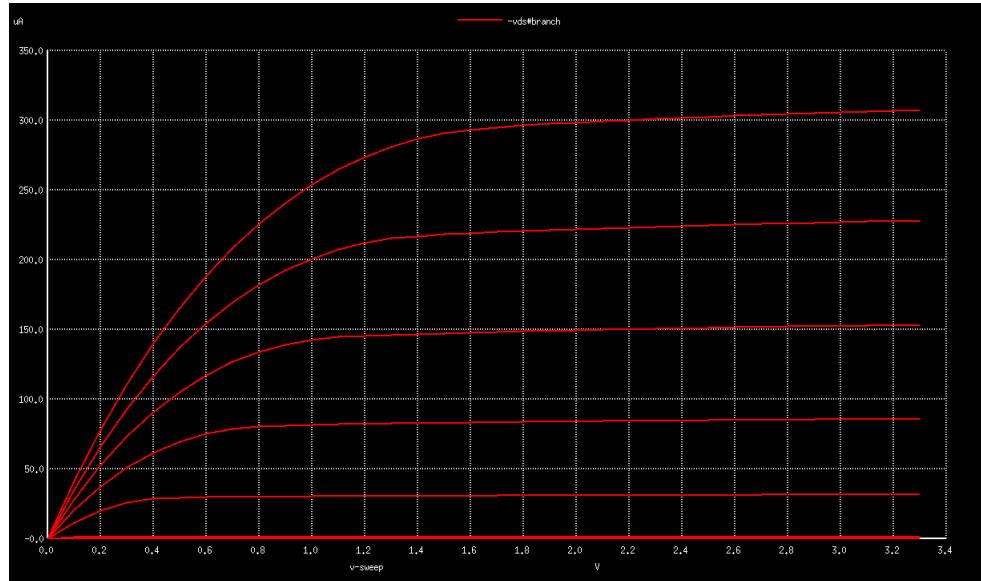


Figure 2.3: Output Characteristics. V_{ds} on the x-axis and the MOSFET current on the y-axis. The curves with higher saturation current corresponds to a greater V_{gs} value

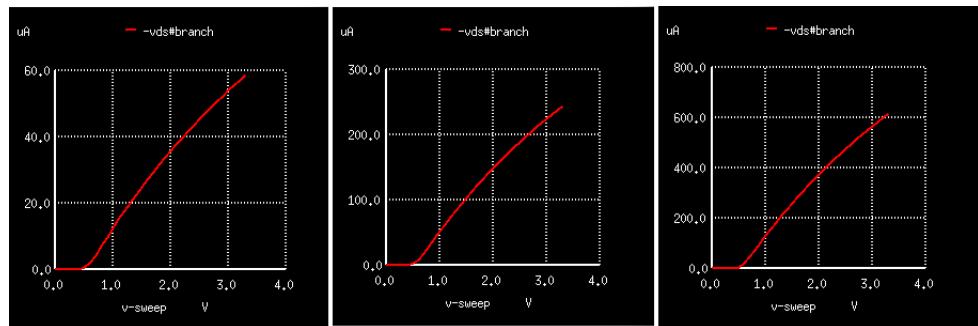


Figure 2.4: Variation of input characteristics with width equal to 0.5u, 2u, 5u respectively. As the **width** of the NMOS increases, the slope of the input characteristics curve also increases. That means that a MOSFET with higher width conducts more current for a given V_{ds} .

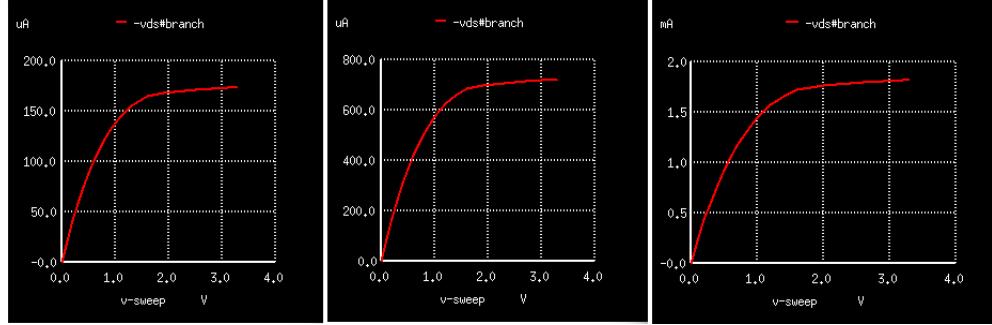


Figure 2.5: Variation of output characteristics with width 0.5u, 2u, 5u respectively. As the **width** of the NMOS increases, the saturation current MOSFET also increases. That means that a MOSFET with higher width conducts more current for a given V_{gs} .

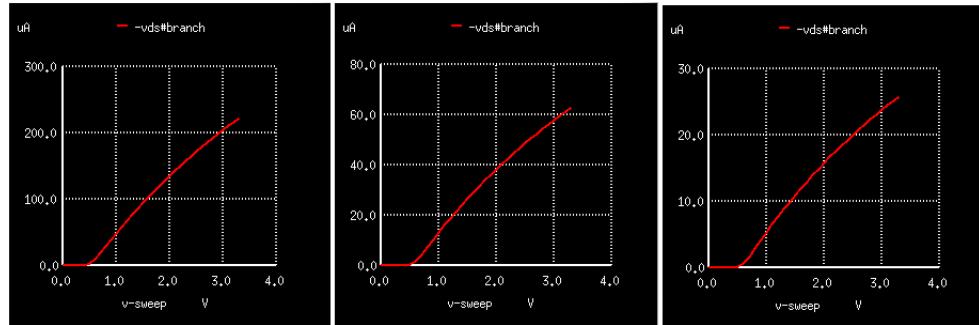


Figure 2.6: Variation of input characteristics with length 0.2u, 2u, 5u respectively. As the **length** of the NMOS increases, the slope of the input characteristics curve decreases. That means that a MOSFET with higher length conducts less current for a given V_{ds} .

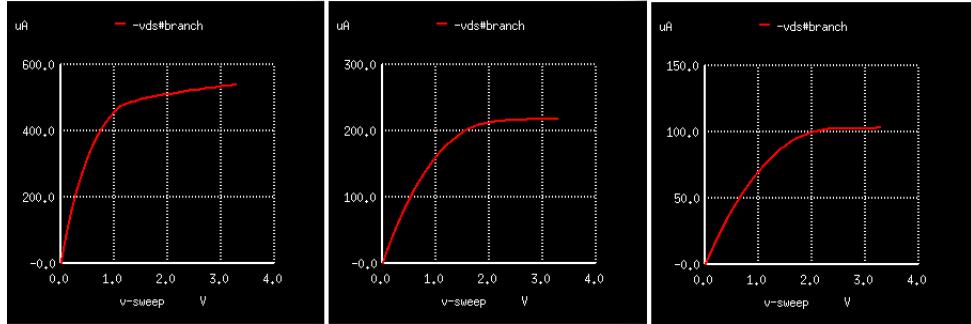


Figure 2.7: Variation of output characteristics with length 0.5u, 2u, 5u respectively. As the **length** of the NMOS increases, the saturation current of the MOSFET decreases. That means that a MOSFET with higher length conducts less current for a given V_{GS} .

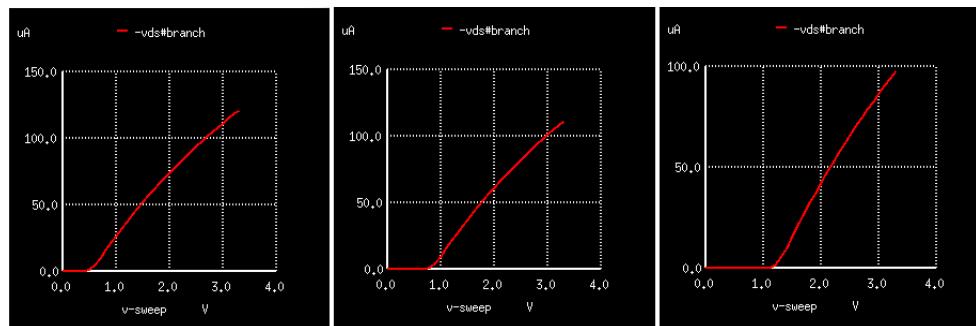


Figure 2.8: variation of input characteristics with threshold voltage 0.4V, 0.7V, 1.1V respectively. As the **threshold voltage**(V_t) of the NMOS increases, the slope of the input characteristics curve decreases. That means that a MOSFET with higher V_t conducts less current for a given V_{DS} .

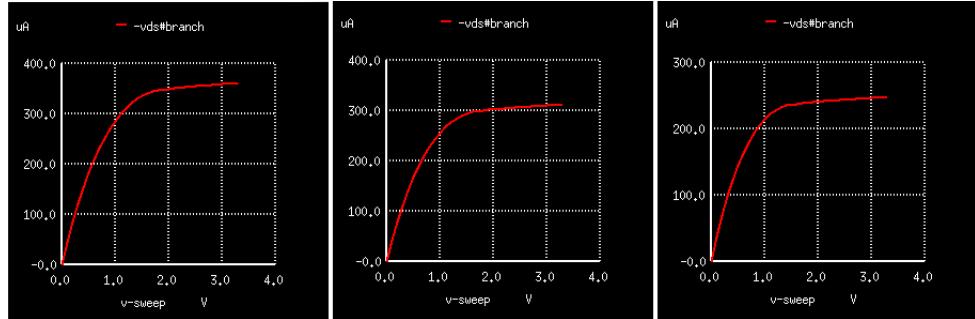


Figure 2.9: Variation of output characteristics with threshold voltage 0.4V, 0.7V, 1.1V respectively. As the **threshold voltage**(V_t) of the NMOS increases, the saturation current of the MOSFET decreases. That means that a MOSFET with higher V_t conducts less current for a given V_{gs} .

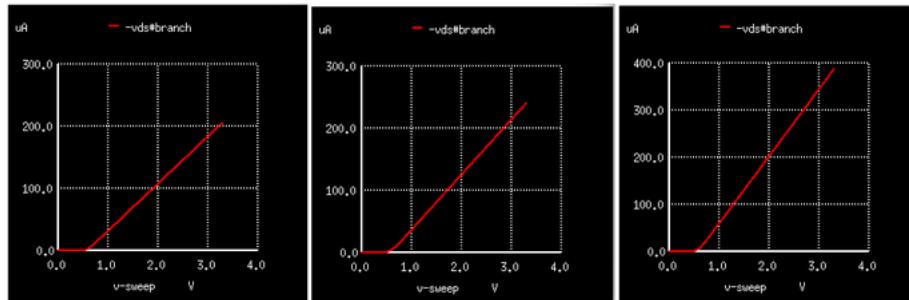


Figure 2.10: variation of input characteristics with lambda (channel length modulation factor) 0.04, 0.6, 3 respectively. As the **channel length modulation factor**(lambda) of the NMOS increases, the slope of the input characteristics curve also increases. That means that a MOSFET with higher lambda conducts more current for a given V_{ds} .

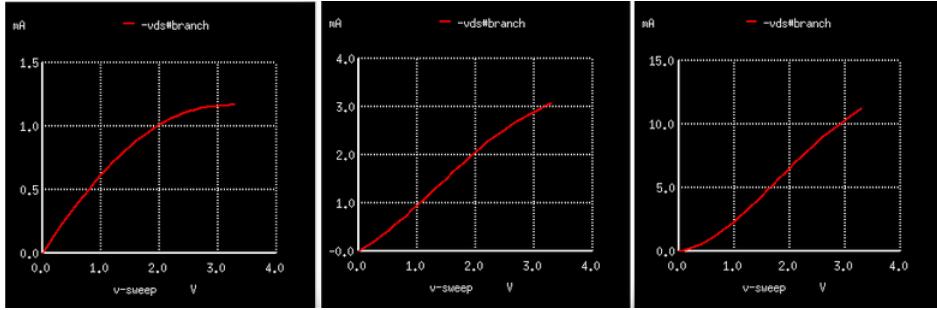


Figure 2.11: Variation of output characteristics with lambda (channel length modulation factor) 0.04, 0.6, 3 respectively. As the **channel length modulation factor**(lambda) of the NMOS increases, the saturation current MOSFET also increases. That means that a MOSFET with higher lambda conducts more current for a given V_{gs} .

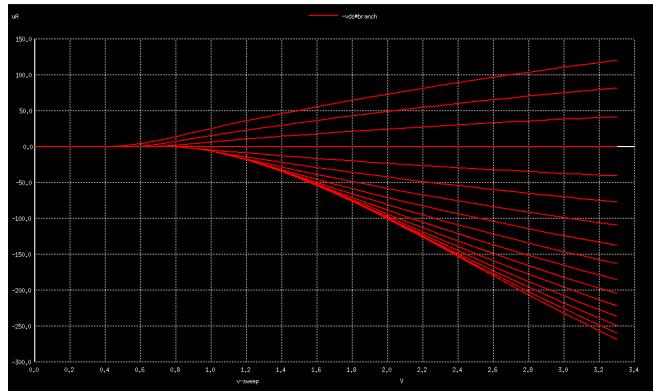


Figure 2.12: variation of input characteristics with V_{sb}

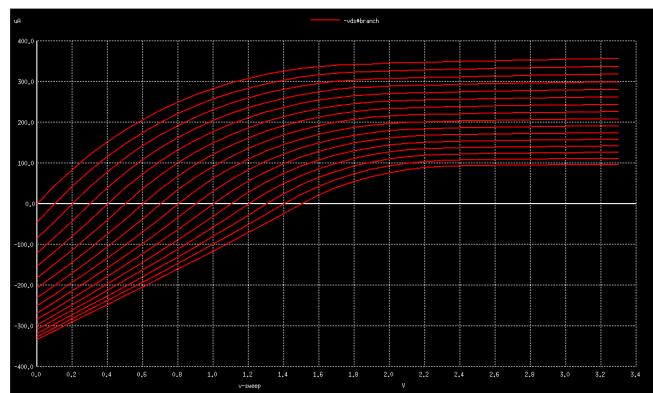


Figure 2.13: Variation of output characteristics with v_{sb} . As the V_{sb} increased, the Output characteristics shifted downwards for a given V_{gs}

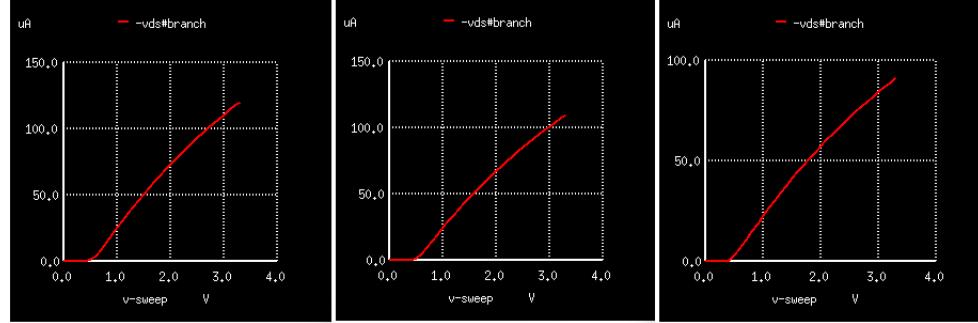


Figure 2.14: variation of input characteristics with temperature 27, 50 and 100 degrees Celsius respectively. With the increase in **temperature**, the MOSFET current decreases for a given V_{ds} and V_g .

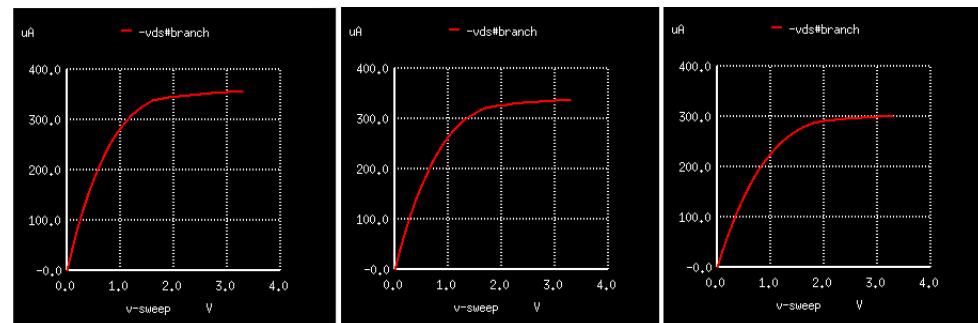


Figure 2.15: Variation of output characteristics with temperature 27, 50 and 100 degrees celcius respectively

Chapter 3

MOS Inverter with Passive Resistive Load

OBJECTIVE : STUDY THE TRANSFER FUNCTION, NOISE MARGIN, EFFECT ON RISE TIME, FALL TIME, PROPAGATION DELAY, POWER AND ENERGY CONSUMED OF A MOS INVERTER FOR VARIOUS L, W, LOAD CAPACITANCE, AND RISE/FALL TIME OF INPUT.

This experiment involves simulation of an inverter circuit with NMOS as the pulldown network and a resistor as the pullup network. The input is applied at the gate terminal of the MOSFET and the output is measured at the node in between the MOSFET and the pullup resistor.

Table 3.1: Varying Driver Resistance

Resistance-R	1k	5k	10k
vol	4.338	1.990	0.930
voh	4.995	4.975	4.950
trise	7.615e-11	1.559e-10	2.770e-10
tfall	6.841e-11	1.301e-10	1.275e-10
delay	1.598e-11	5.1e-11	8.348e-11
pavg	1.699e-3	1.555e-3	1.096e-3

The **noise margin** between Vil and Vol increased with increase in pullup resistance whereas the **noise margin** between Vih and Voh decreased.

The **rise time, propagation delay** increased with increase in pullup resistance whereas **fall time, power** consumed decreased.

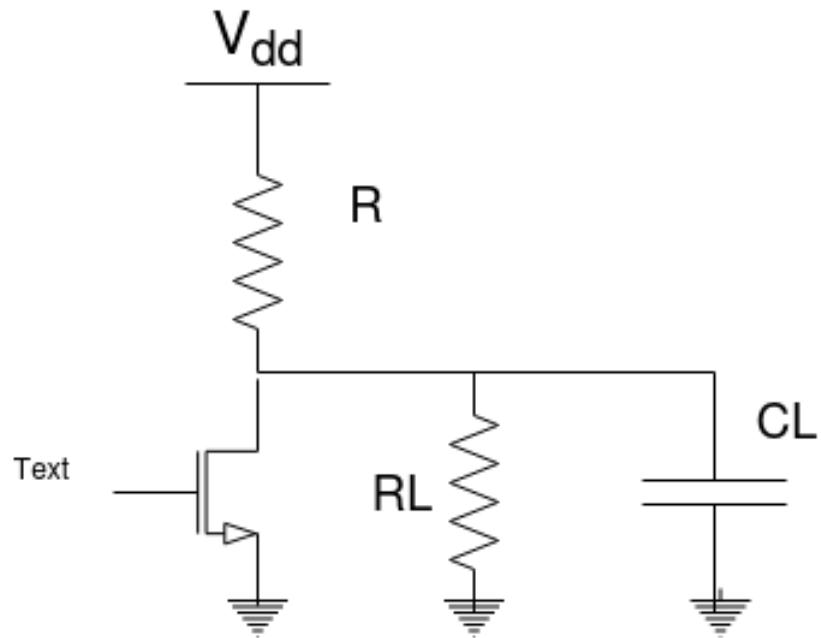


Figure 3.1: Circuit simulated

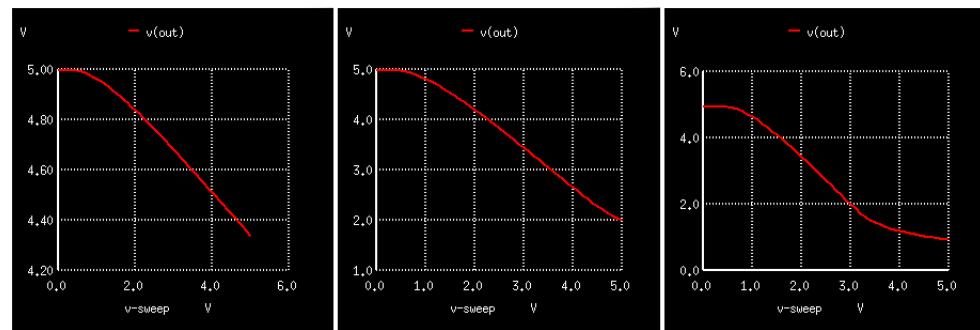
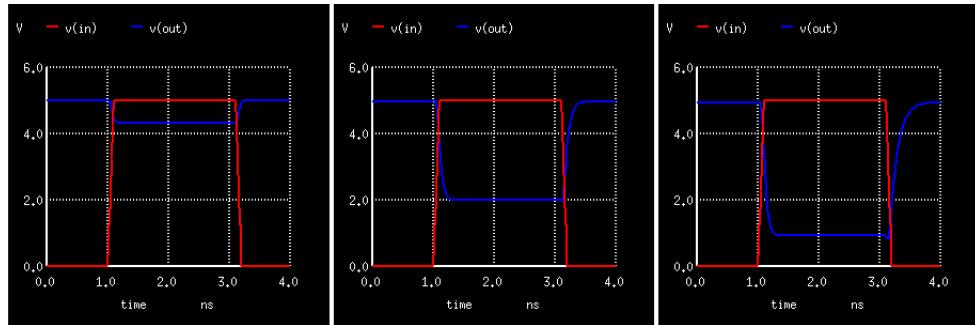
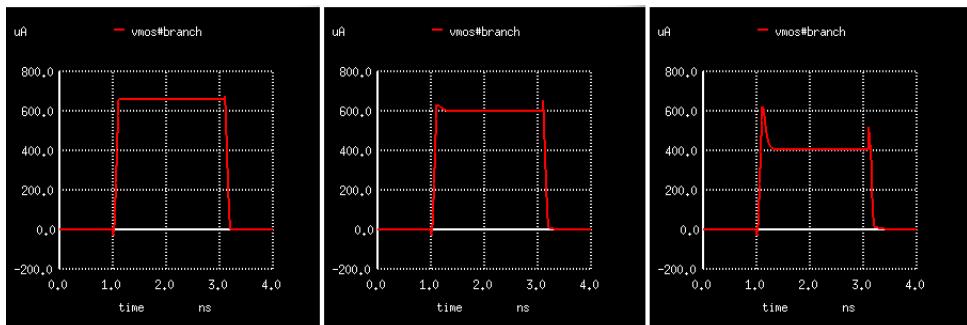
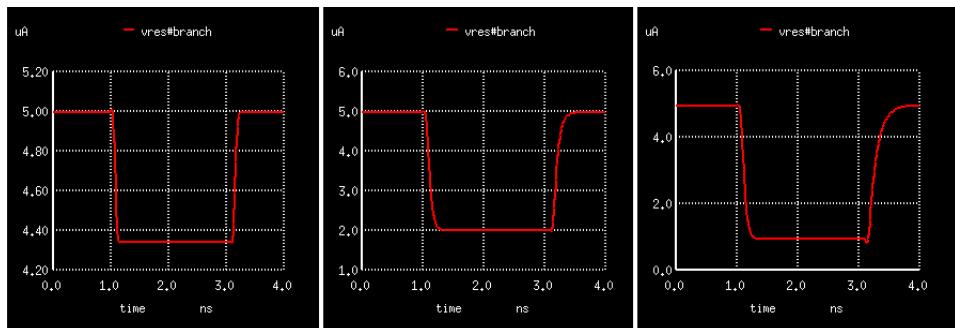


Figure 3.2: Transfer function with R as 1k, 5k and 10k

Figure 3.3: Transient Output Waveform with R as 1k, 5k and 10kFigure 3.4: Current through the NMOS with R as 1k, 5k and 10kFigure 3.5: Current through the load resistor RL with R as 1k, 5k and 10k

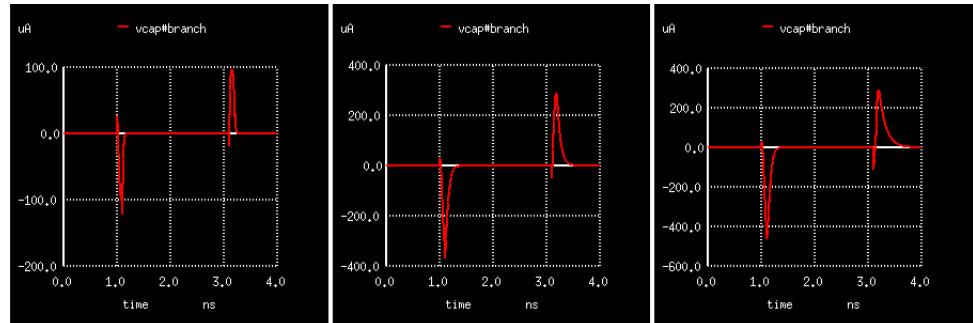


Figure 3.6: Current through the load capacitor with R as 1k, 5k and 10k

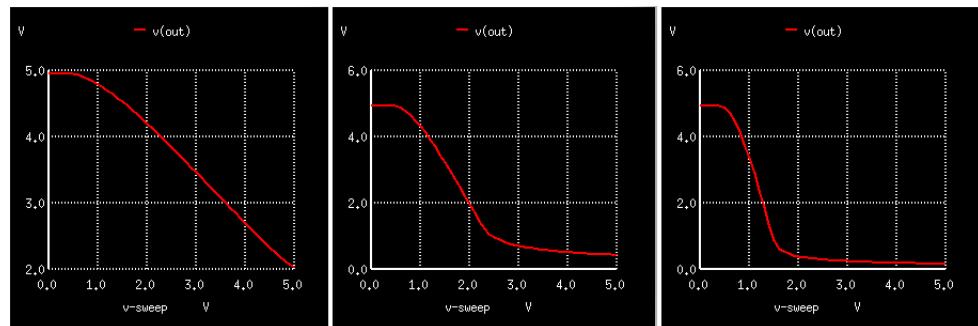


Figure 3.7: Transfer function with width as 0.5u, 2u and 5u respectively

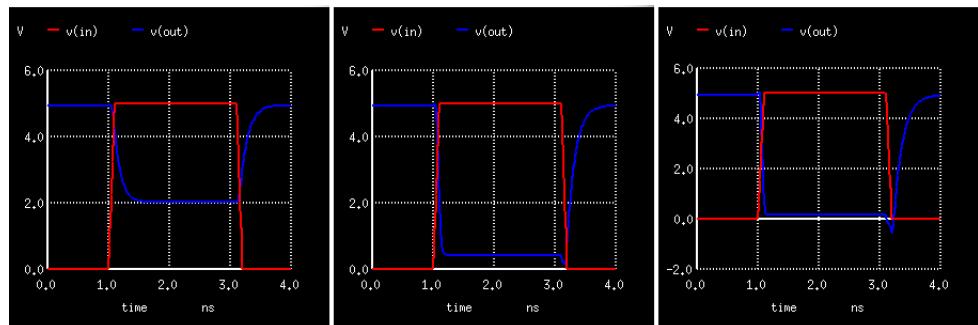


Figure 3.8: Transient Output Waveform with width as 0.5u, 2u and 5u respectively

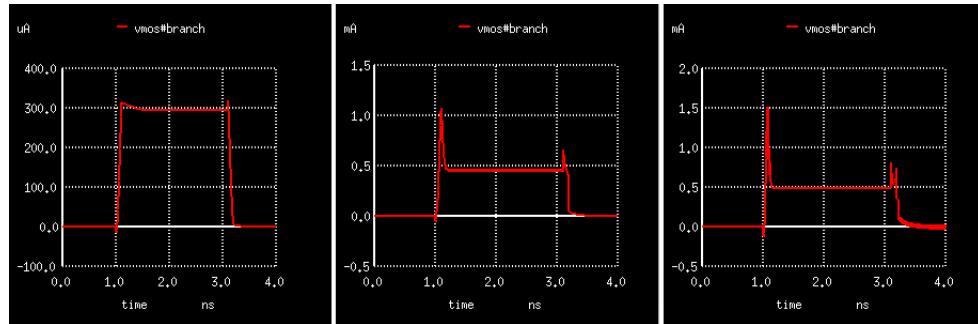


Figure 3.9: Current through the NMOS with width as 0.5u, 2u and 5u respectively

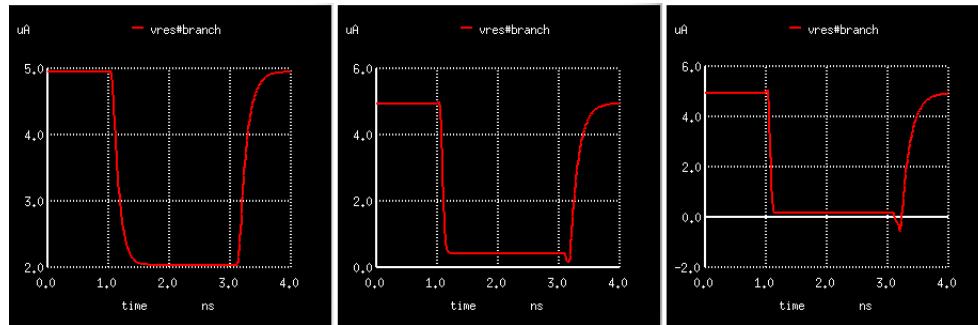


Figure 3.10: Current through the load resistor RL with width as 0.5u, 2u and 5u respectively

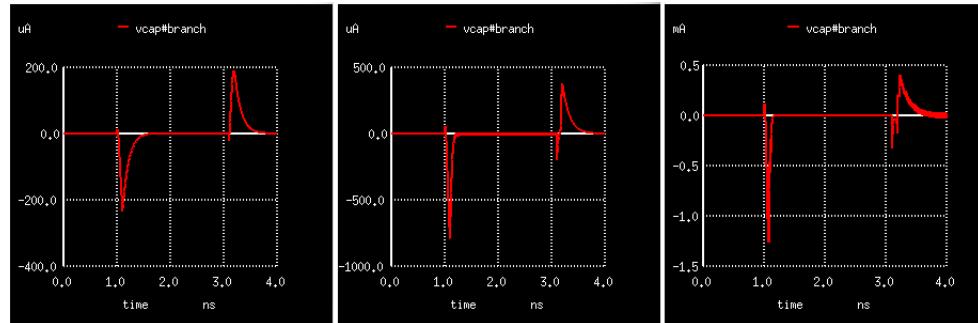


Figure 3.11: Current through the load capacitor with width as 0.5u, 2u and 5u respectively

Table 3.2: Varying NMOS width

Width	0.5u	2u	5u
vol	2.035	0.4291	0.1627
voh	4.95	4.95	4.95
trise	2.774e-10	2.876e-10	3.280e-10
tfall	2.325e-10	7.809e-11	5.9e-11
delay	8.786e-11	8.48e-11	1.038e-10
pavg	7.75e-4	1.269e-3	1.4e-3

The noise margin between Vil and Vol increased with increase in the MOSFET width, but the noise margin between Vih and Voh was not affected by the change. The **rise time, propagation delay** increased with increase in pullup resistance whereas **fall time, power** consumed decreased.

Chapter 4

MOS Inverter with Pseudo NMOS Load

OBJECTIVE : For a MOS Inverter with active load - NMOS and PMOS (pseudo NMOS load), study the transfer function, Noise margin, effect on rise time, fall time, propagation delay, power and energy consumed with variation in L and W of the pullup and pulldown transistors. Also power and energy consumed with non ideal step input.

Table 4.1: Varying Input Rise Time and Fall Time

Input Rise time	0.1n	0.2n	0.5n
Power	1.572e-3	1.605e-3	1.699e-3
Input Fall time	0.1n	0.2n	0.5n
Power	1.572e-3	1.596e-3	1.685e-3

Greater **power** was consumed with increase in rise time and fall time of the input signal.

Table 4.2: Non Ideal Step Input

Load Capacitance	1fF	10fF	20fF
Rise Time	8.547e-11	1.317e-10	1.871e-10
Fall Time	8.662e-11	1.312e-10	1.834e-10
Propagation delay	4.404e-11	6.587e-11	8.913e-11
Power Consumed	2.230e-3	2.267e-3	2.302e-3

The **rise time, fall time, propagation delay** has increased with increase in load capacitance while the power consumed was nearly the unaffected by change in load capacitance.

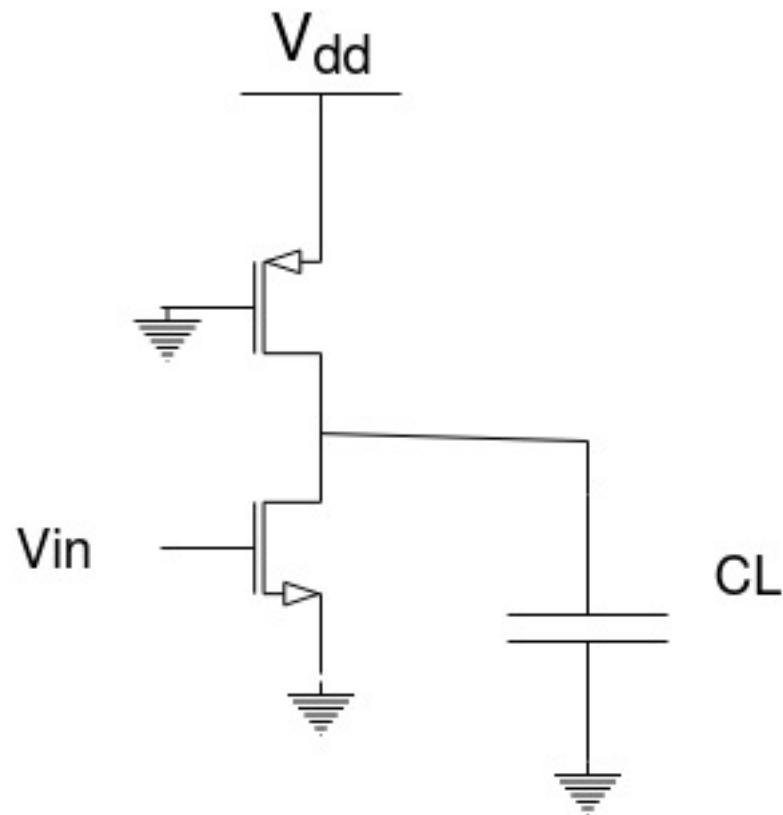


Figure 4.1: Circuit diagram for simulation

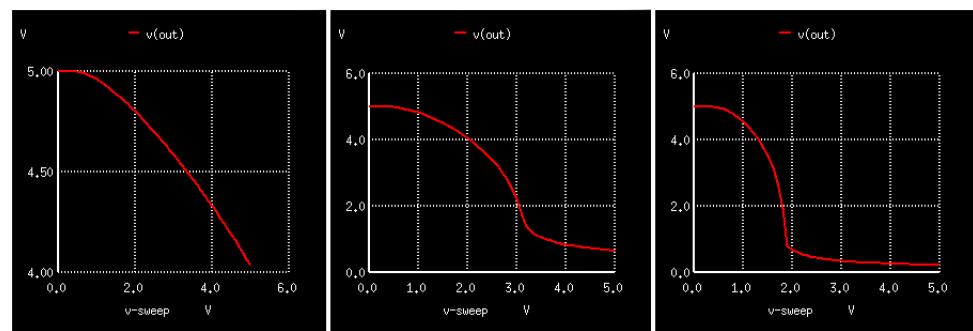


Figure 4.2: Transfer Curve Characteristics for Widths of NMOSFET at 0.5u, 2u and 5u respectively

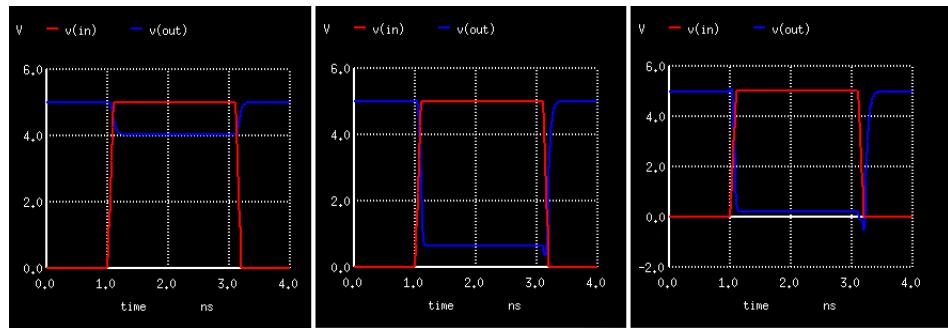


Figure 4.3: Transient Curve Characteristics for Widths of NMOSFET at 0.5u, 2u and 5u respectively

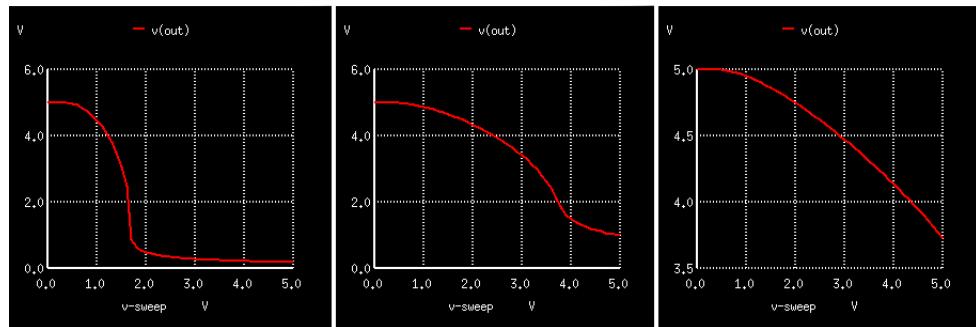


Figure 4.4: Transfer Curve Characteristics for Widths of PMOSFET at 0.5u, 2u and 5u respectively

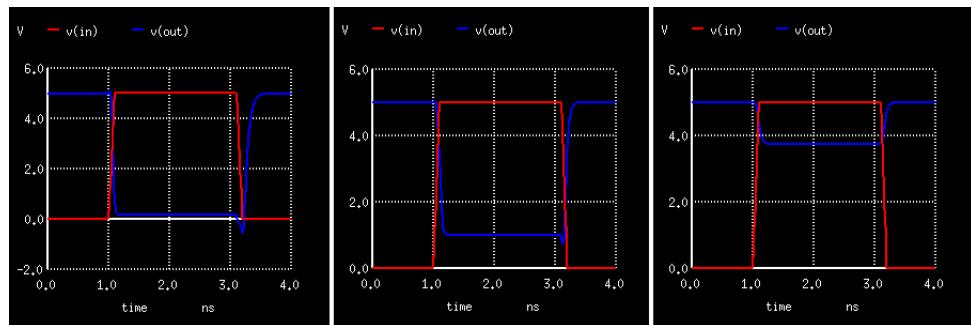


Figure 4.5: Transient Curve Characteristics for Widths of PMOSFET at 0.5u, 2u and 5u respectively

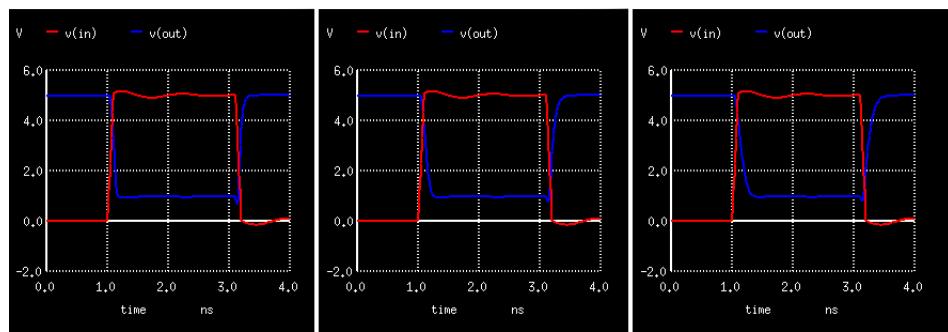


Figure 4.6: Transient Curve Characteristics for **Non ideal** Inputs with Load Capacitances of 1fF, 10fF and 20fF respectively

Chapter 5

CMOS Inverter

OBJECTIVE : For a CMOS Inverter study the transfer function, Noise margin, effect on risetime, falltime, propagation delay, power and energy consumed with variation in L and W of the pullup and pulldown transistors. Also power and energy consumed with non ideal step input.

Table 5.1: Varying Input Rise Time and Fall Time

Input Rise time	0.1n	0.2n	0.5n
Power	1.343e-4	1.386e-4	1.715e-4
Input Fall time	0.1n	0.2n	0.5n
Power	1.343e-4	1.168e-4	1.241e-4

Power consumption increased when the rise time was increased, but had decreased when the fall time was increased.

Table 5.2: Non Ideal Step Input

Load Capacitance	1fF	50fF	100fF
Rise Time	7.527e-11	3.184e-10	6.842e-10
Fall Time	2.626e-11	1.946e-10	3.701e-10
Propagation delay	6.248e-11	1.941e-10	3.135e-10
Power Consumed	1.301e-4	4.711e-4	7.108e-4

Rise time, fall time, delay and power consumption all increased with increase in load capacitance.

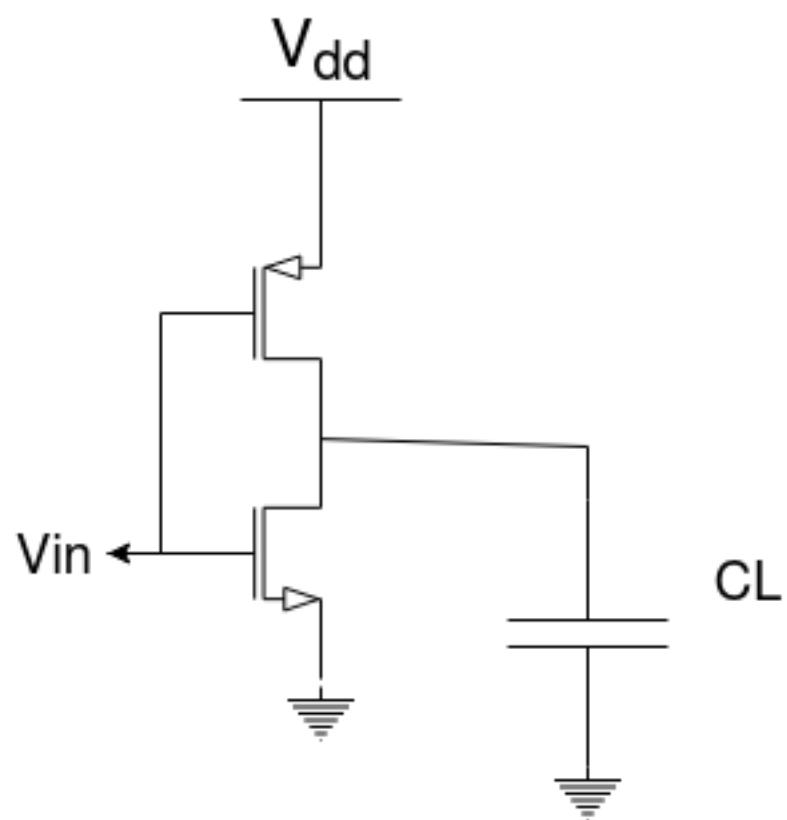


Figure 5.1: Circuit used for simulation

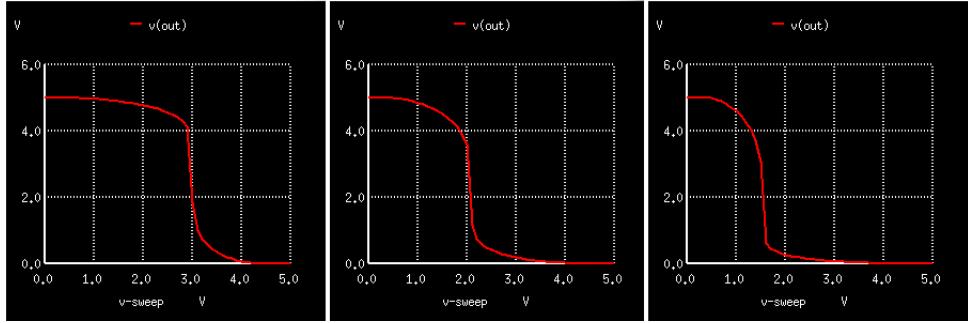


Figure 5.2: Transfer Curve Characteristics for Widths of NMOSFET at 0.5u, 2u and 5u respectively

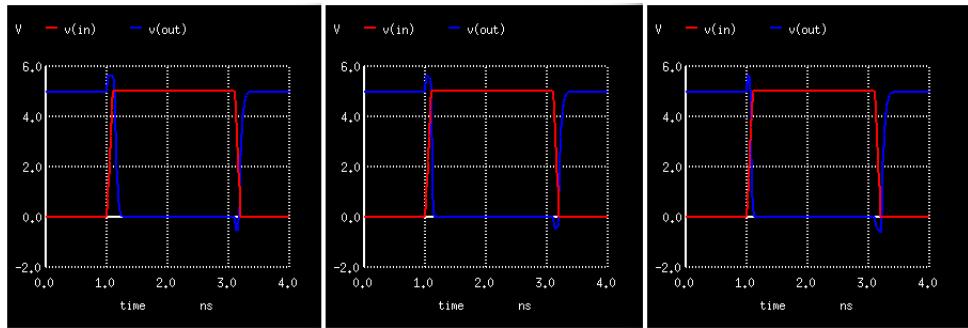


Figure 5.3: Transient Curve Characteristics for Widths of NMOSFET at 0.5u, 2u and 5u respectively

Table 5.3: Ideal Step Input

Load Capacitance	1fF	10fF	20fF
Rise Time	7.332e-11	3.824e-10	6.99e-10
Fall Time	2.664e-11	2.011e-10	3.809e-10
Propagation delay	2.216e-11	1.972e-10	3.221e-11
Power Consumed	1.343e-4	4.738e-4	7.162e-4

Rise time, fall time, delay and power consumption all increased with increase in load capacitance. But the increase was greater when an ideal step input was applied than when a non ideal input was applied.

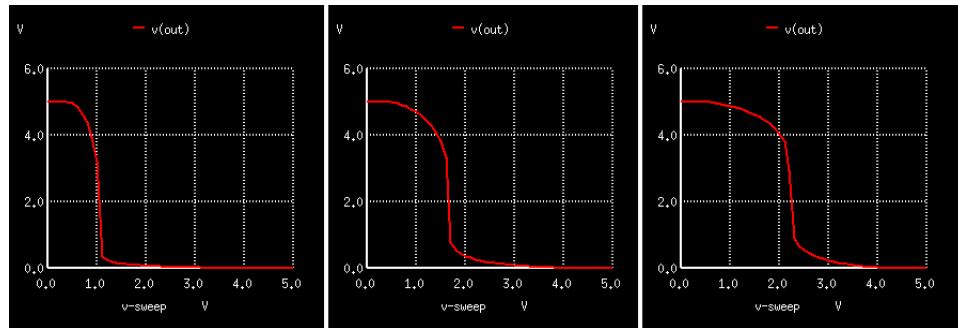


Figure 5.4: Transfer Curve Characteristics for Widths of PMOSFET at 0.5u, 2u and 5u respectively

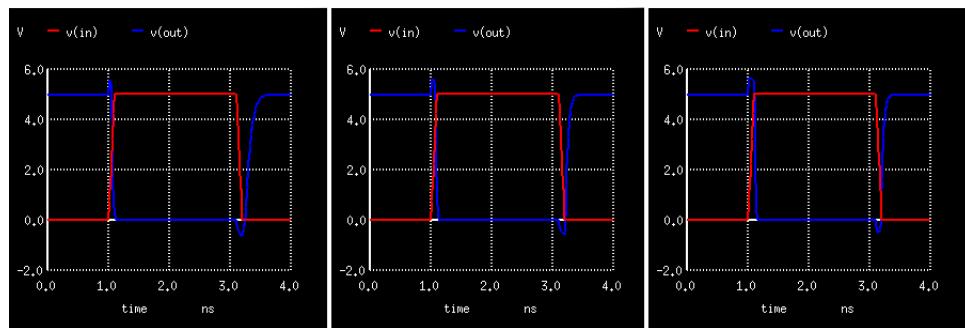


Figure 5.5: Transient Curve Characteristics for Widths of PMOSFET at 0.5u, 2u and 5u respectively

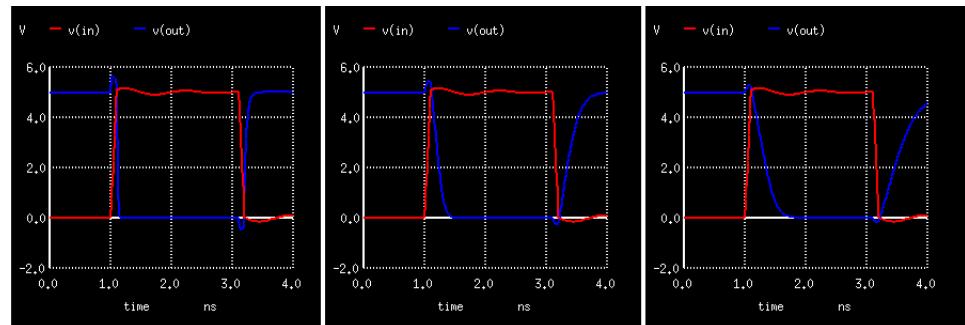


Figure 5.6: Transient Curve Characteristics for Non ideal Inputs with Load Capacitances of 1fF, 50fF and 100fF respectively

Chapter 6

CMOS Gates

OBJECTIVE : Study the behaviour transfer function, Noise margin, effect on rise time, fall time, propagation delay, power and energy consumed of a CMOS gates like NAND, NOR, functions like AOI (2 input AND gate, 2 input OR gate), and 2 input XOR gate with variation in L and W of the pullup and pulldown transistors.

The circuit is powered by a 5v source.

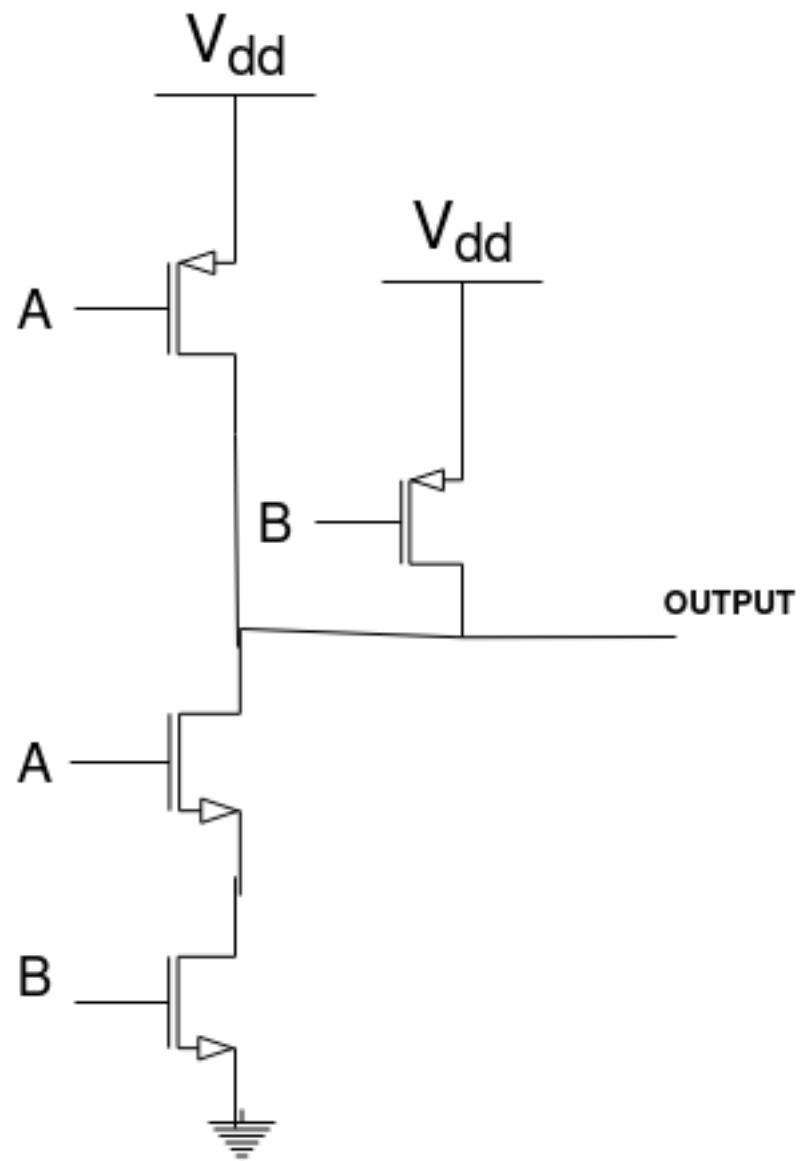


Figure 6.1: Nand gate with MOSFETS named mna, mnb, mpa and mpb corresponding to the pullup and pulldown networks respectively.

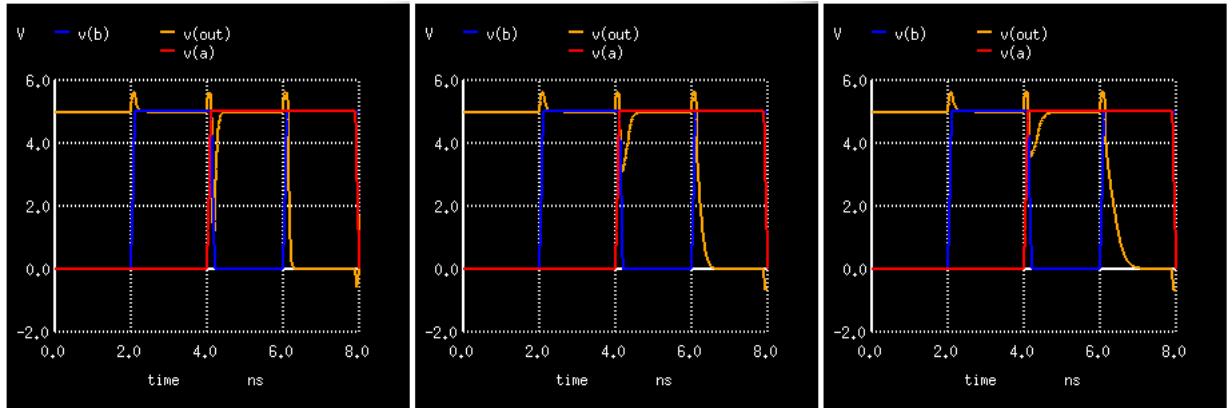


Figure 6.2: Transient characteristics with width of mna as 0.5u, 2u and 5u

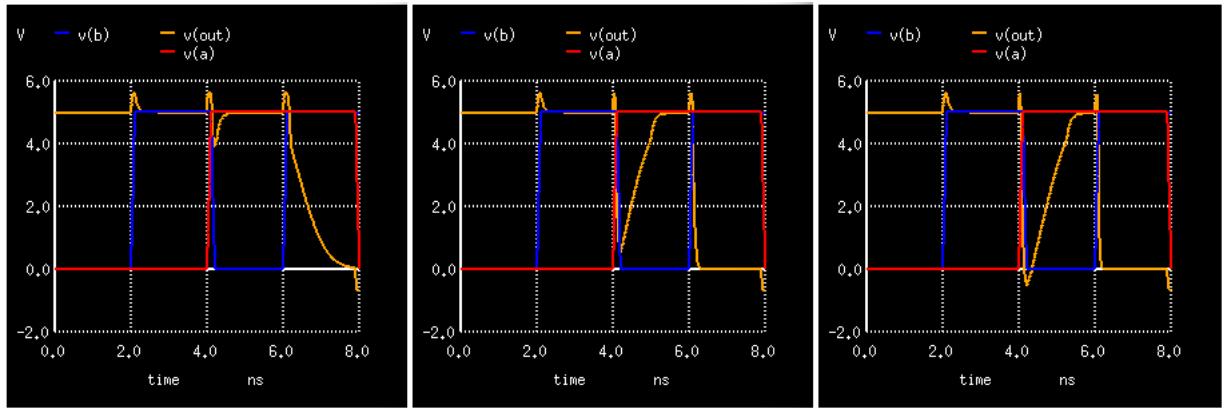


Figure 6.3: Transient characteristics with width of mnb as 0.5u, 2u and 5u

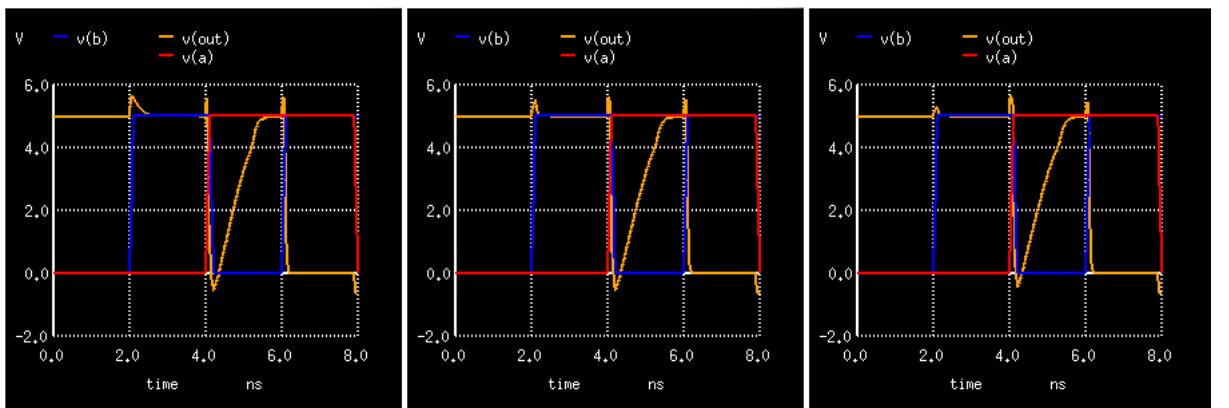


Figure 6.4: Transient characteristics with width of mpa as 0.5u, 2u and 5u

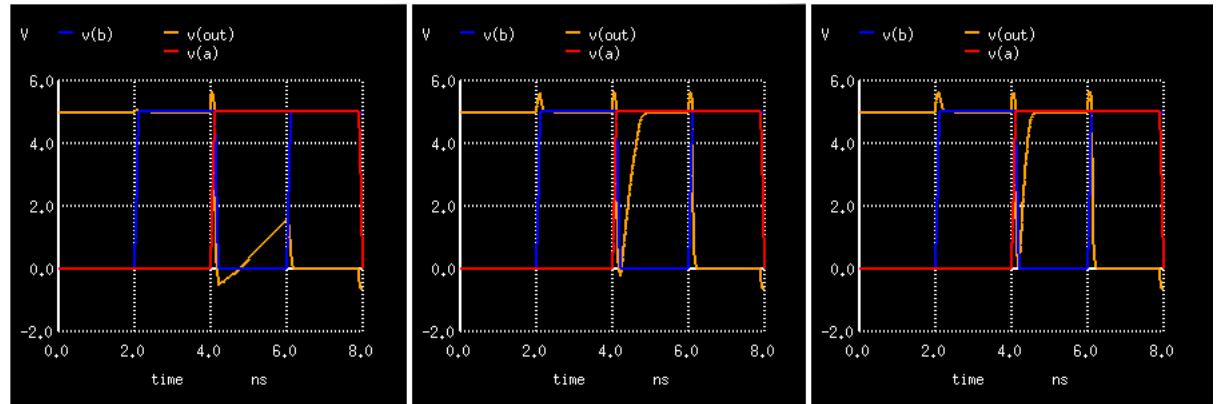


Figure 6.5: Transient characteristics with width of mpb as 0.5u, 2u and 5u

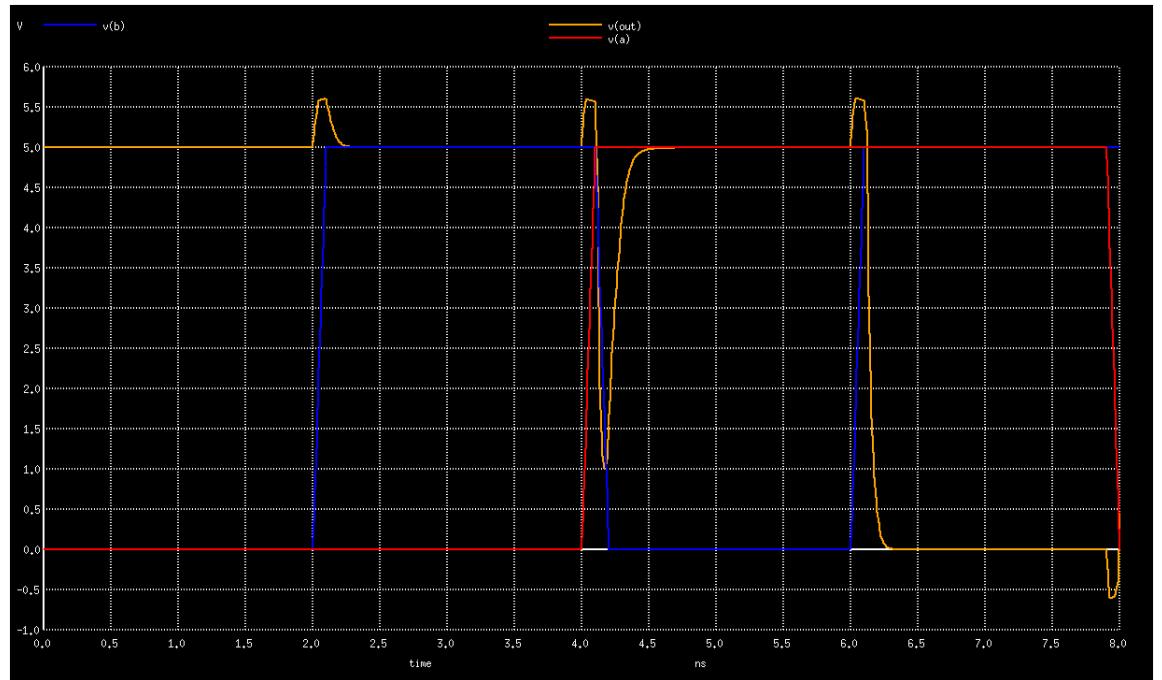


Figure 6.6: Power consumed by Nand circuit was 2.094393e-04 watts

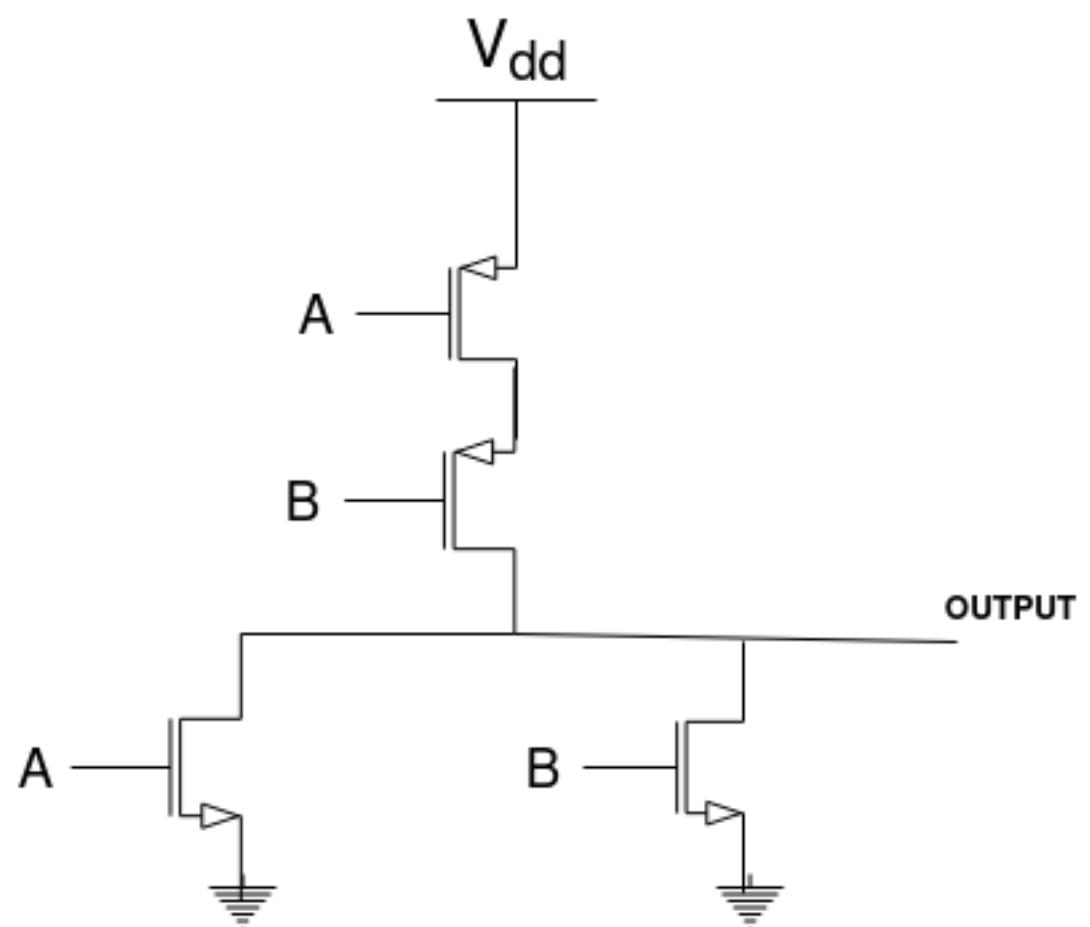


Figure 6.7: Nor Gate

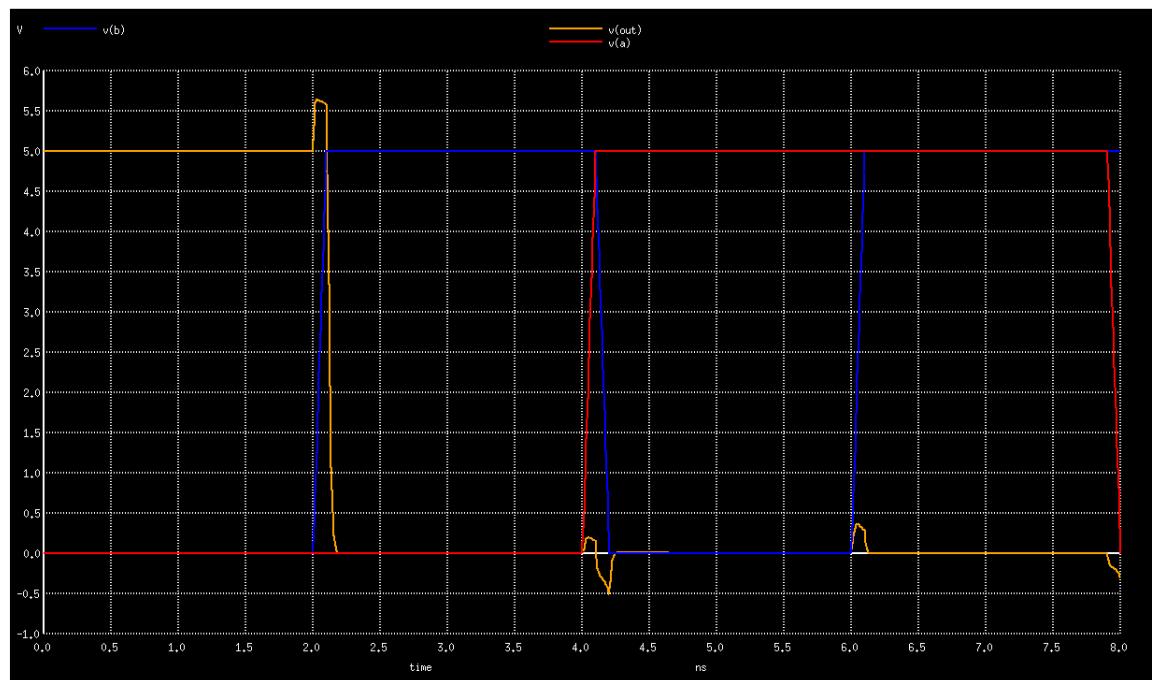


Figure 6.8: Power consumed by Nor gate was 1.586415e-04 Watt

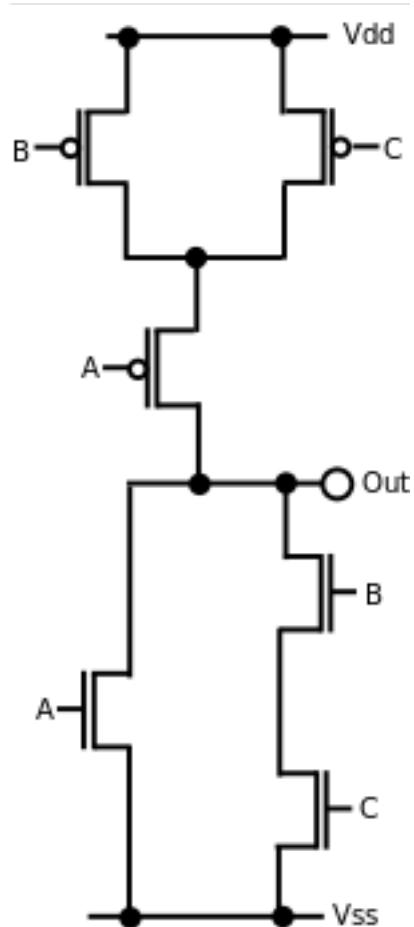


Figure 6.9: 3-Input And-Or-Invert Gate that performs $f=-(ab+c)$

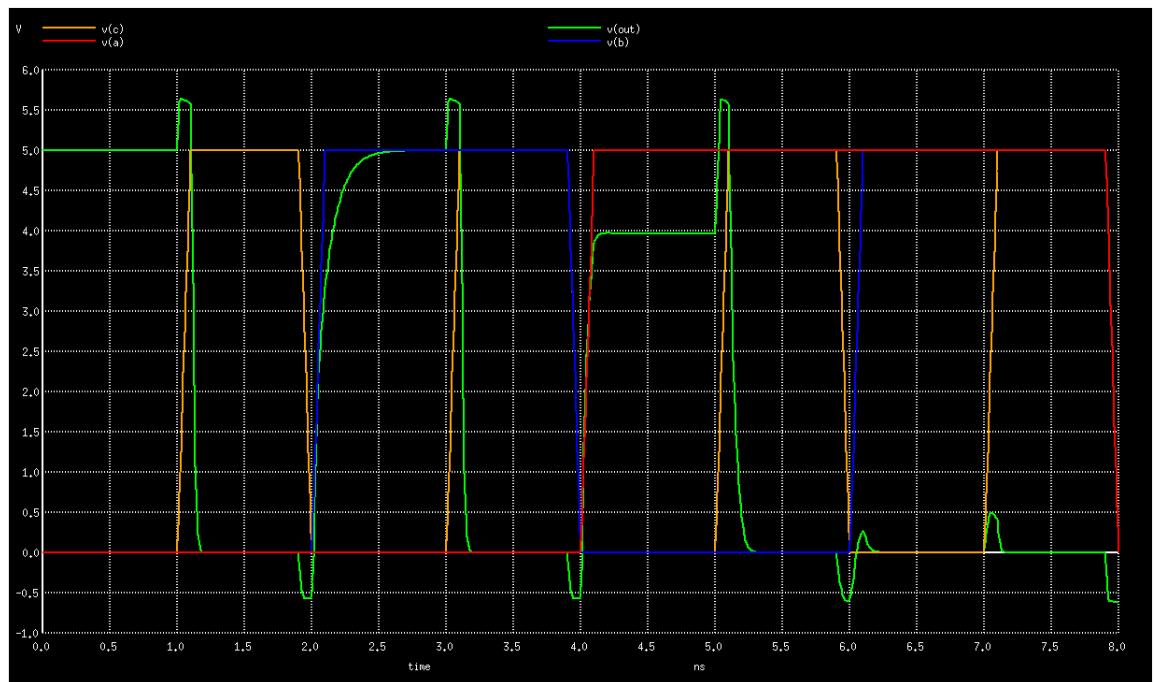
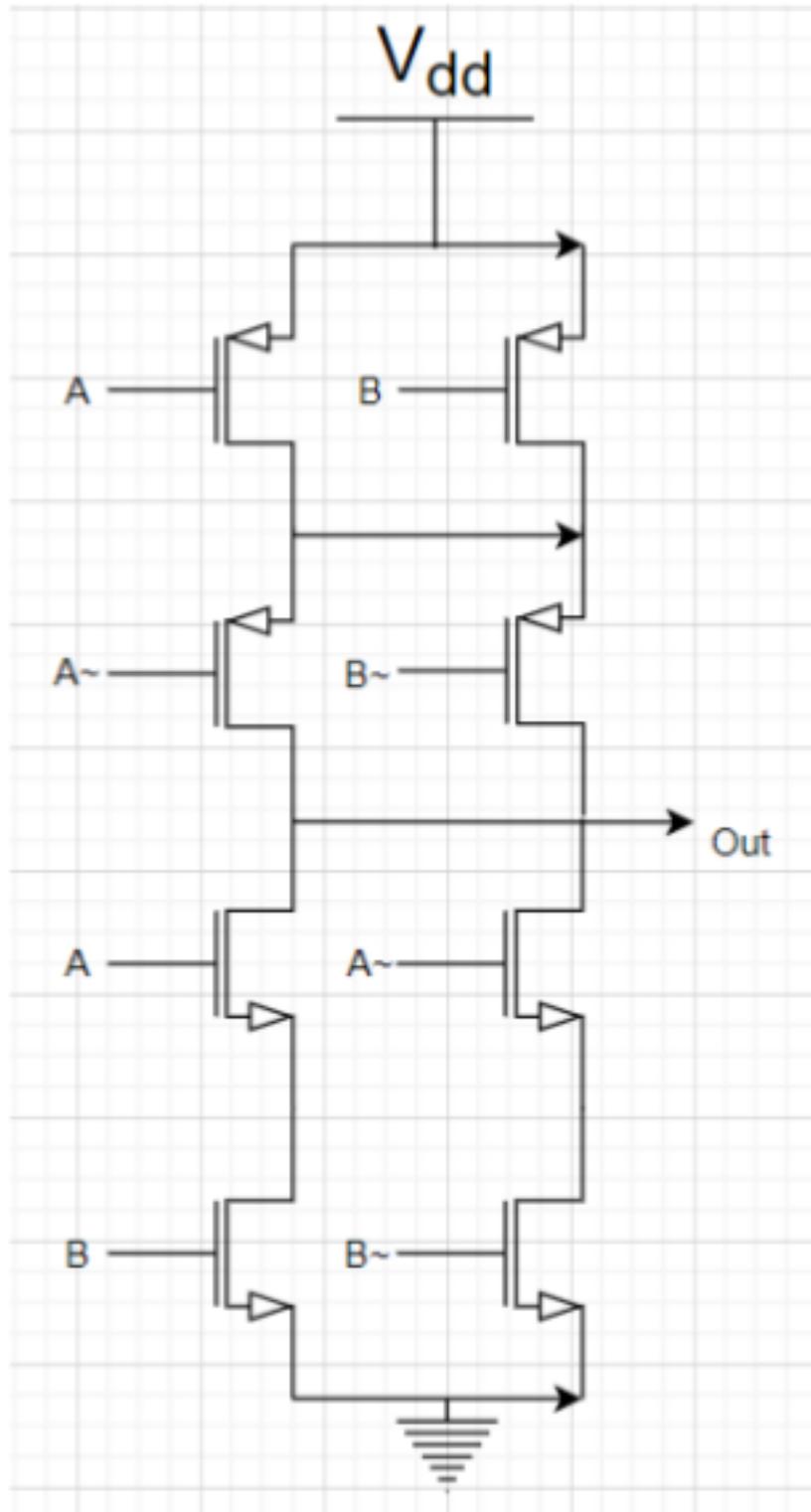


Figure 6.10: Power consumed in 3-input AOI gate is 3.173329e-05 watt

Figure 6.11: 2-Input Xor Gate that performs $f = a^*b + -a^*b$

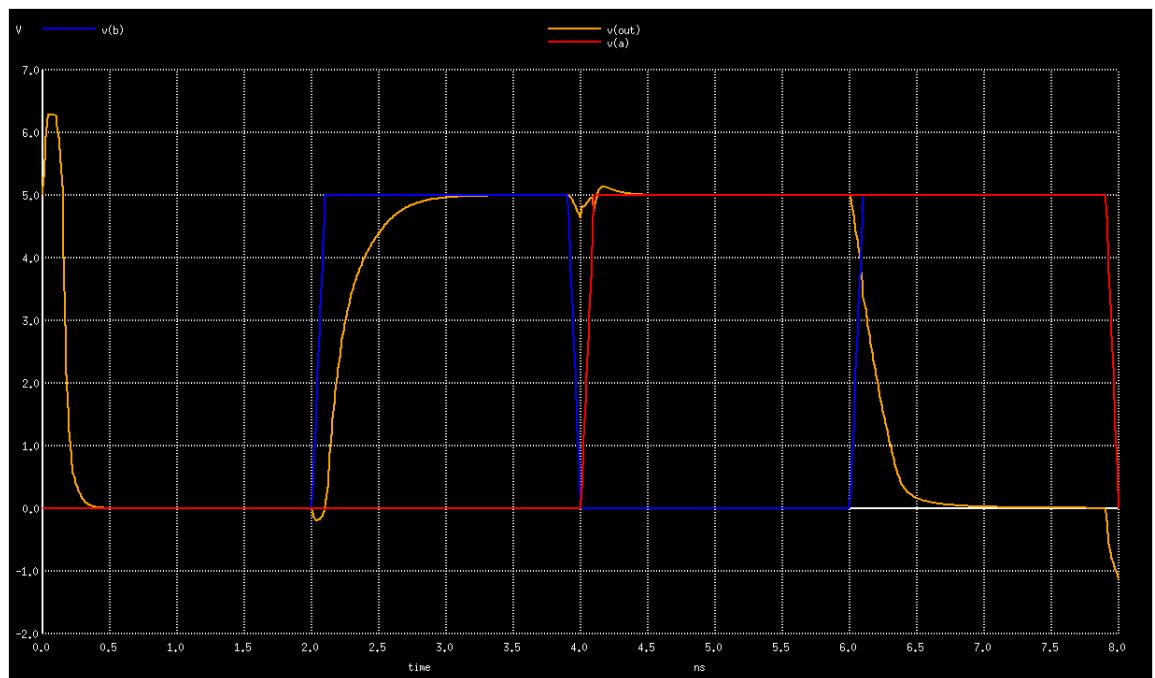


Figure 6.12: Power consumed by xor gate is $3.117662e-05$ watts

Chapter 7

CMOS Inverter Layout and Characterisation

OBJECTIVE : To learn layout, extract, LVS and Characterization process in the design flow with CMOS inverter as an example.

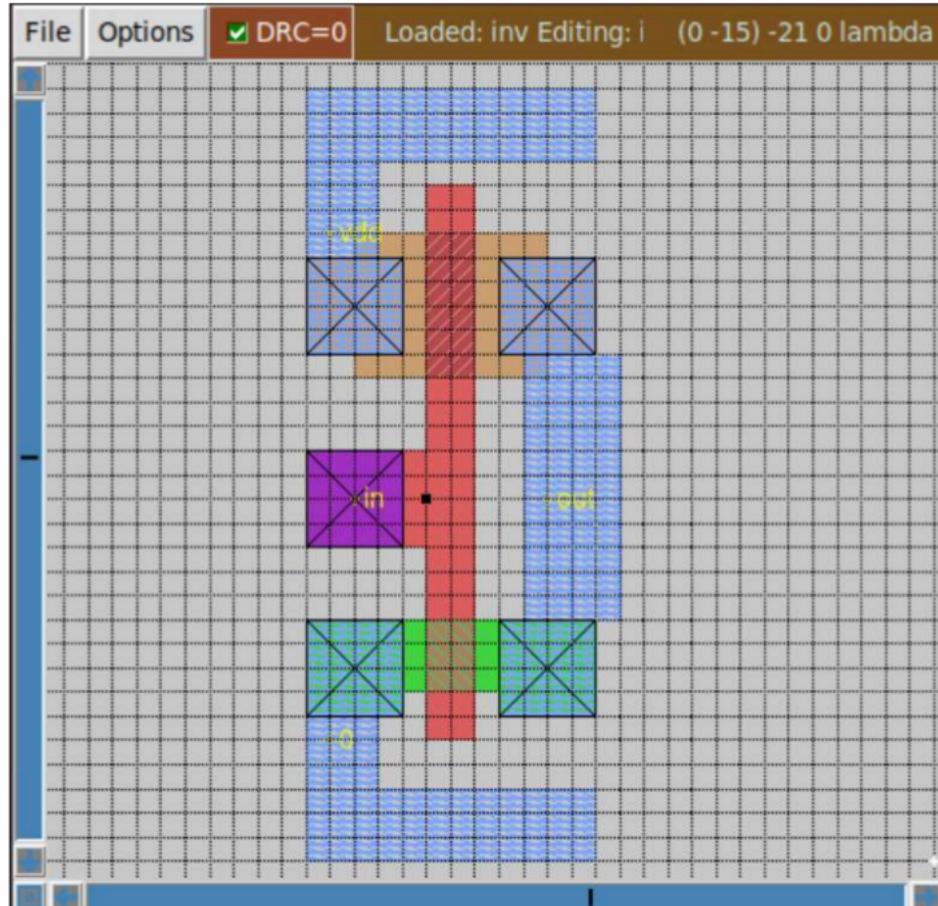


Figure 7.1: CMOS Layout

Load/Output cap	2.0fF	2.5fF	4.1fF	8.7fF
Area	416	448	544	832
Input capacitance	5.9fF	5.9fF	5.9fF	5.9fF
Rise time	7.028*e-10	7.066*e-10	7.186*e-10	7.529*e-10
Fall time	2.988*e-10	3.010*e-10	3.077*e-10	3.278*e-10
Average Power	6.247*e-04	6.383*e-04	6.520*e-04	6.724*e-04

Figure 7.2: Varying the area of CMOS inverter

Chapter 8

Generation of a Standard Library

OBJECTIVE : To create a standard cell library of CMOS gates - Two and Three input NAND, NOR, AND, OR, AOI, for TWO products of TWO variables, D-Latch, and a D-Flipflop.

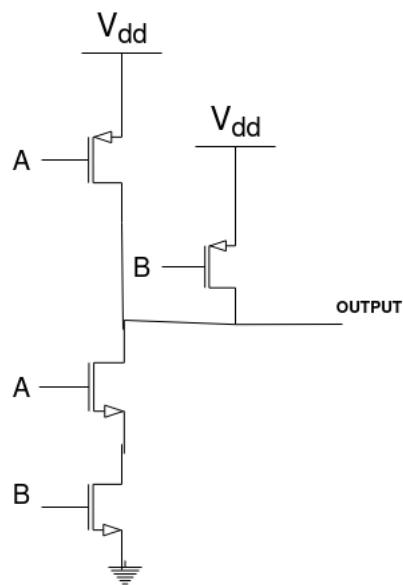


Figure 8.1: Circuit Diagram of a NAND Gate

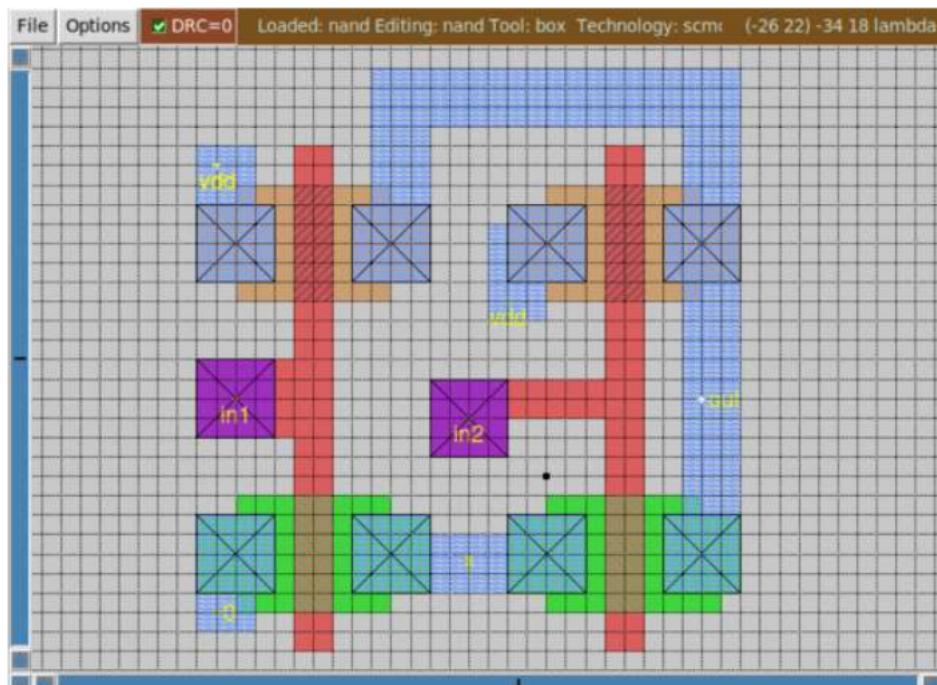


Figure 8.2: Layout of the NAND Gate

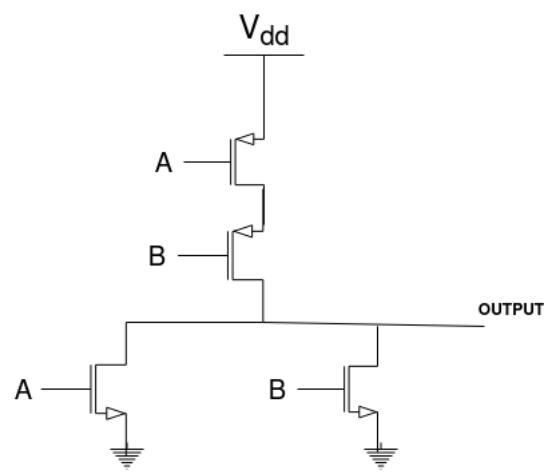


Figure 8.3: Circuit Diagram of a NOR Gate

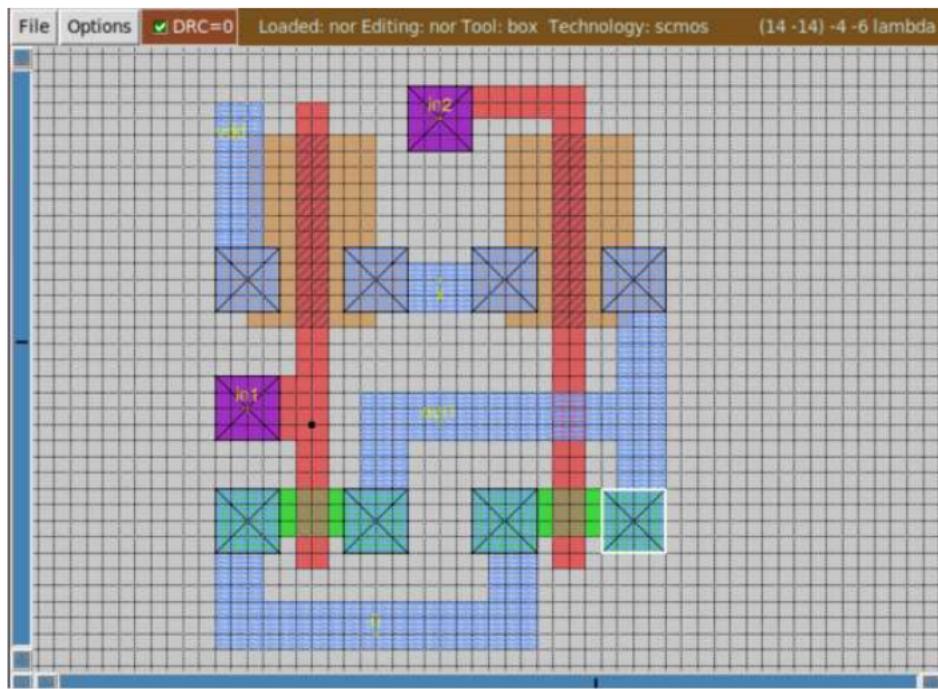


Figure 8.4: Layout of the NOR Gate

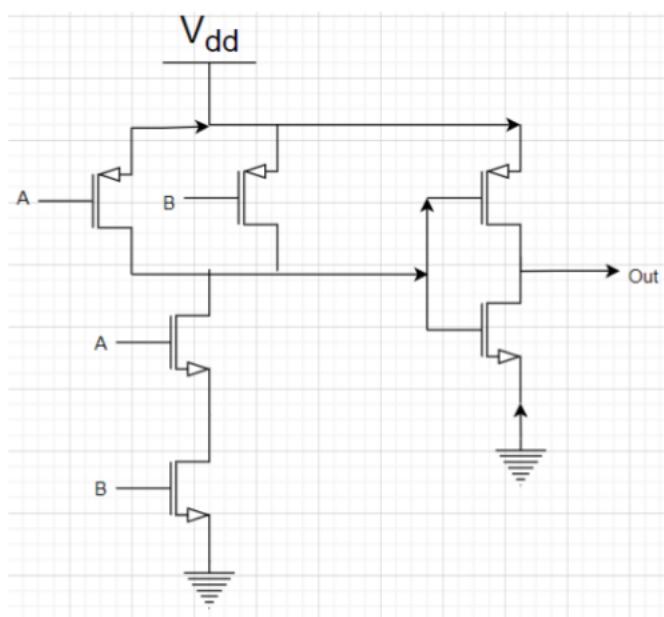


Figure 8.5: Circuit Diagram of an AND Gate

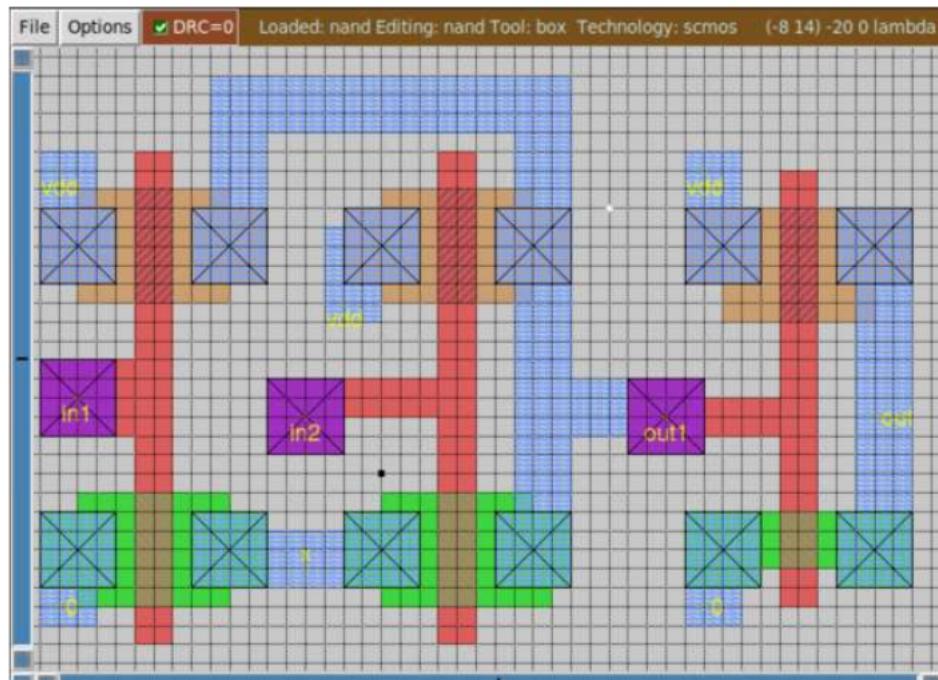


Figure 8.6: Layout of the AND Gate

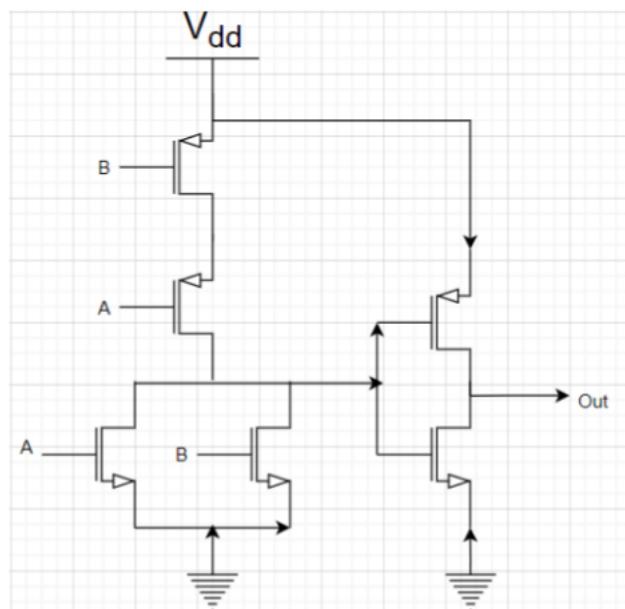


Figure 8.7: Circuit Diagram of an OR Gate

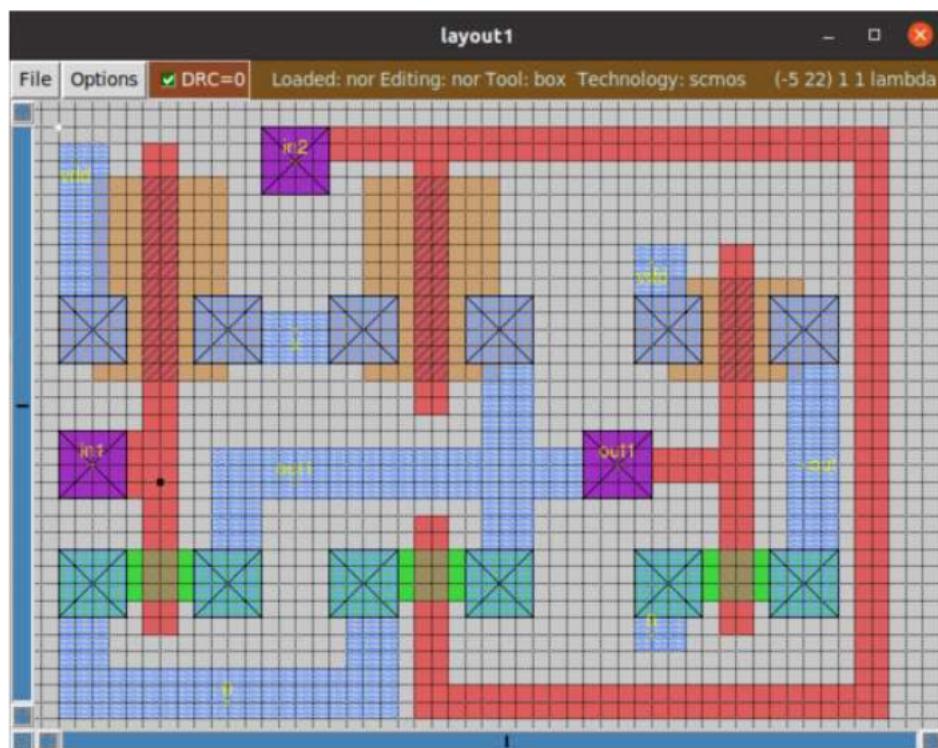


Figure 8.8: Layout of the OR Gate

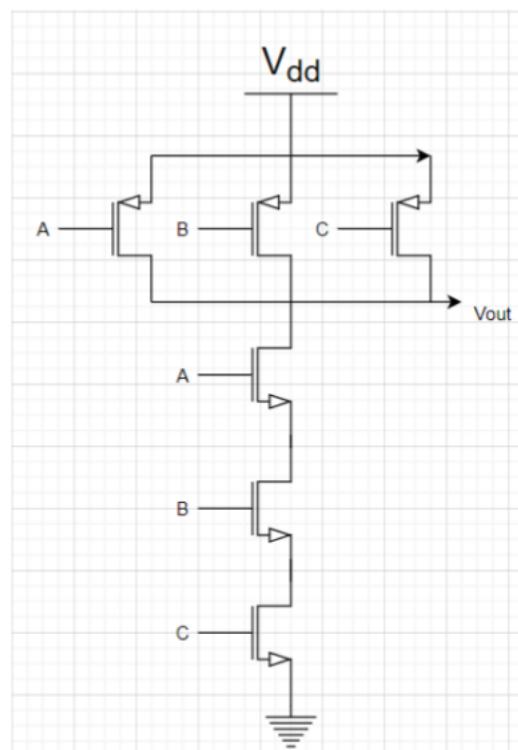


Figure 8.9: Circuit Diagram of a 3-input NAND Gate

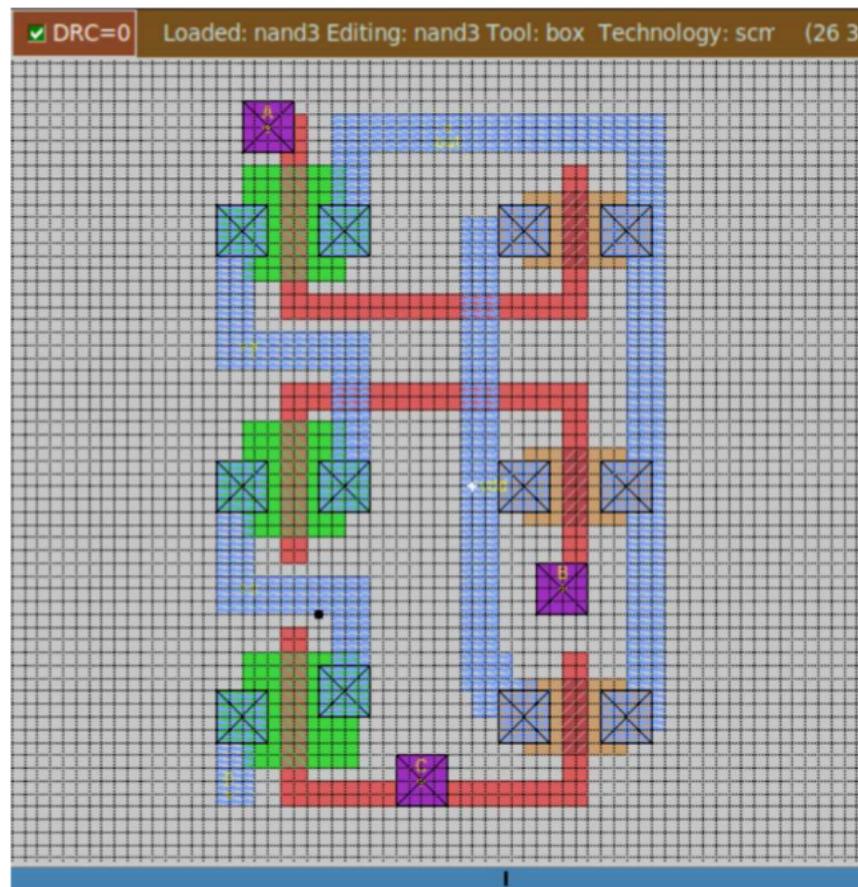


Figure 8.10: Layout of the 3-input NAND Gate

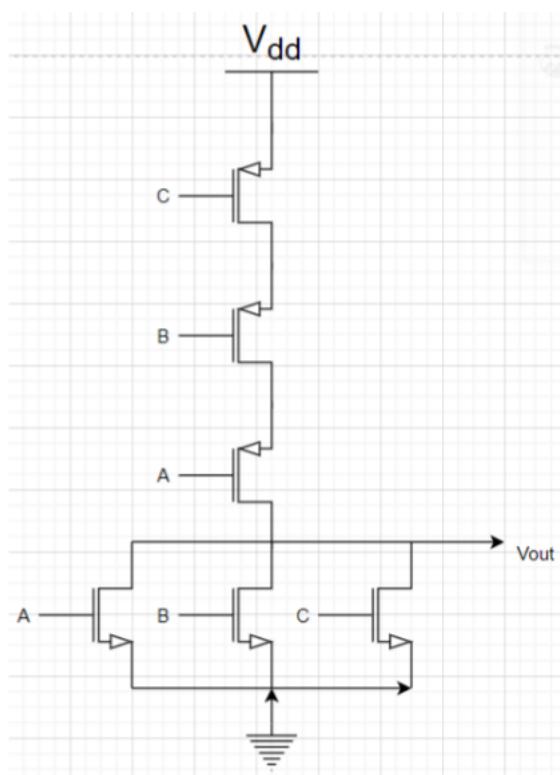


Figure 8.11: Circuit Diagram of a 3-input NOR Gate

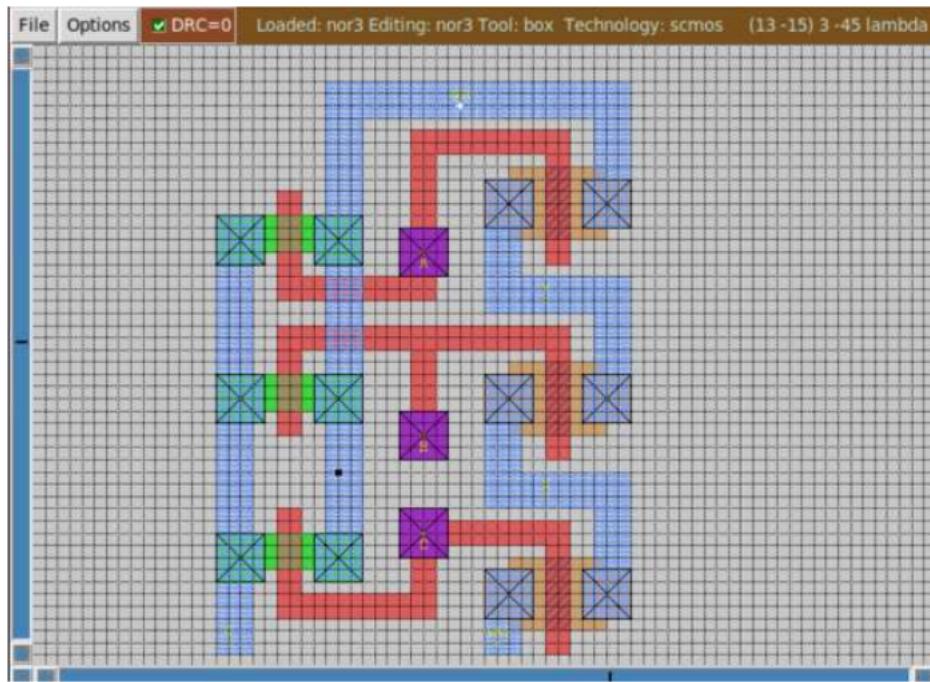


Figure 8.12: Layout of the 3-input NOR Gate

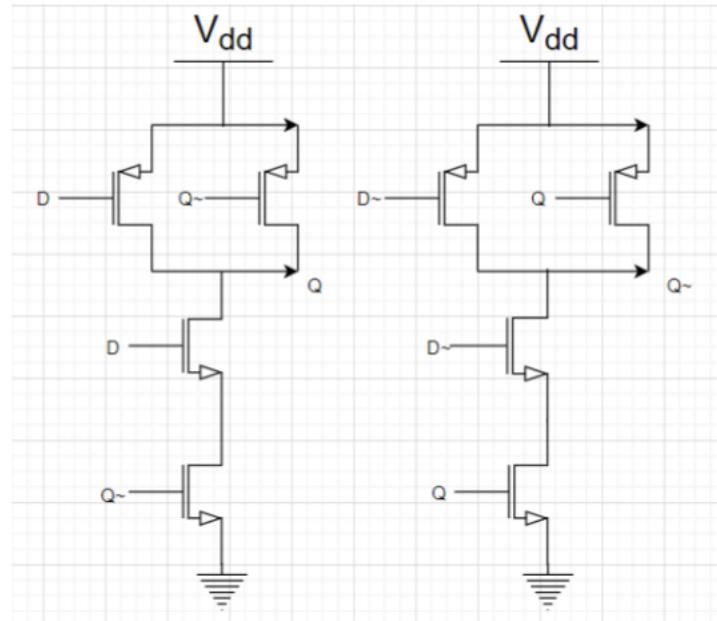


Figure 8.13: Circuit Diagram of a D-Latch

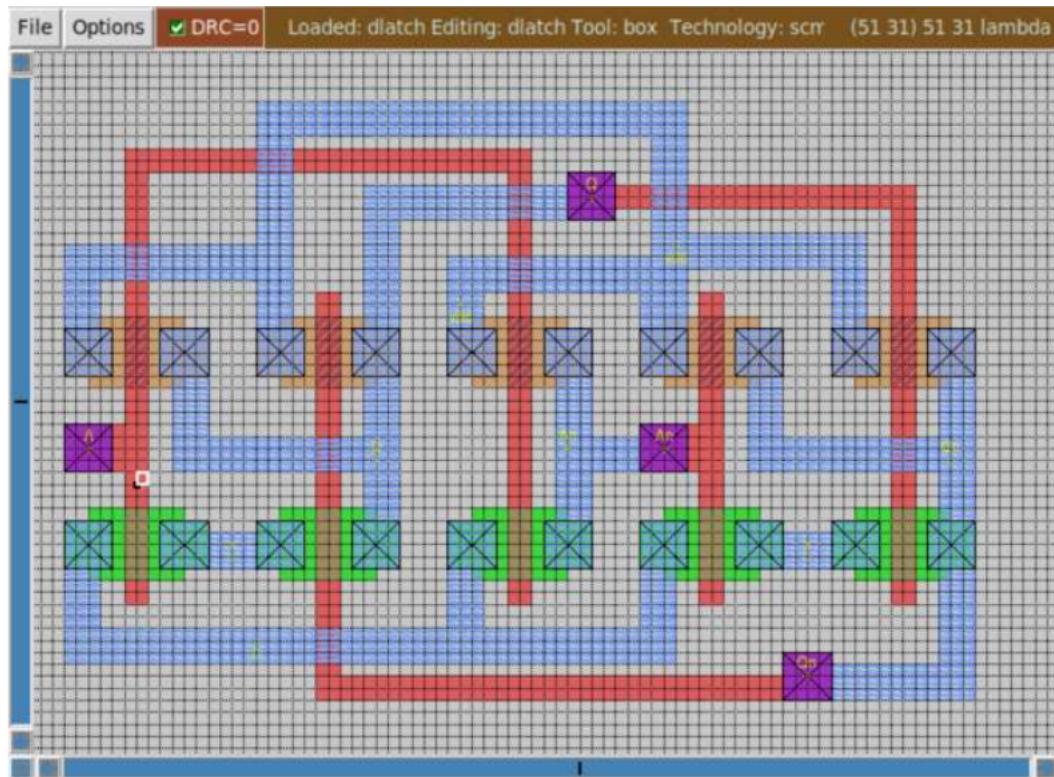


Figure 8.14: Layout of the D-Latch

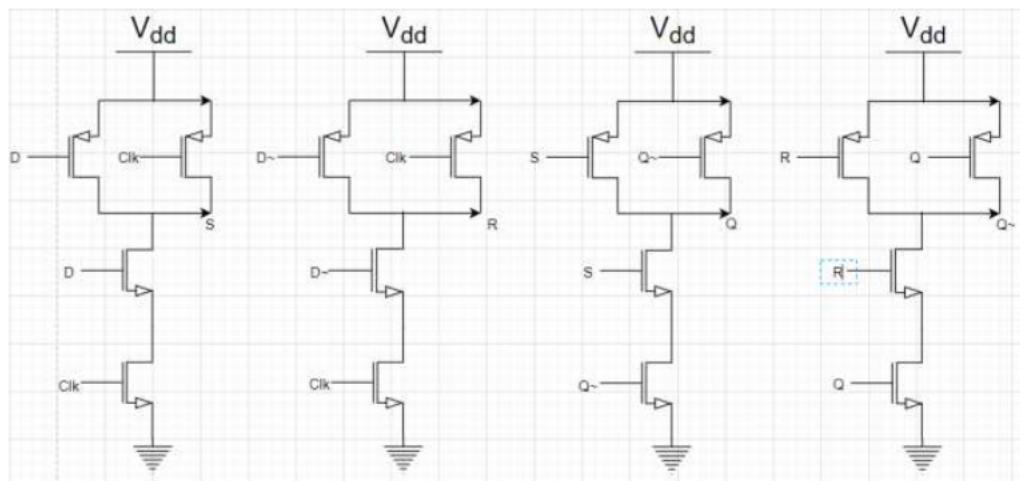


Figure 8.15: Circuit Diagram of a D-Flip-Flop

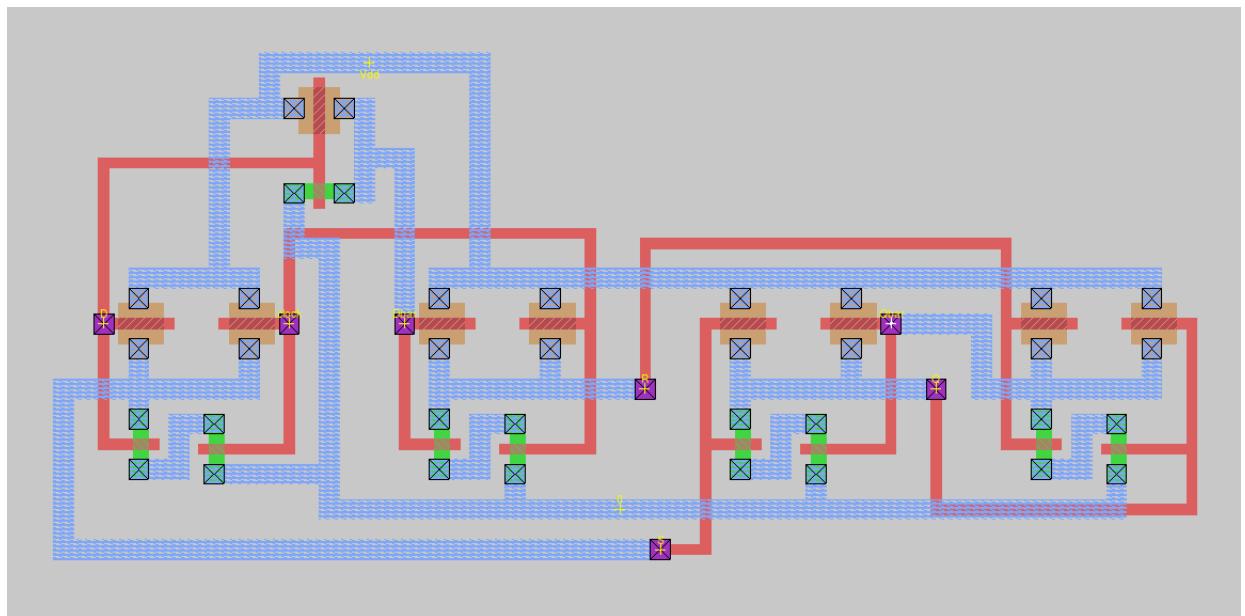


Figure 8.16: Layout of the D-Flip-Flop