EE-309: Microprocessor Project 1

Multi-cycle processor, IITB-RISC-22

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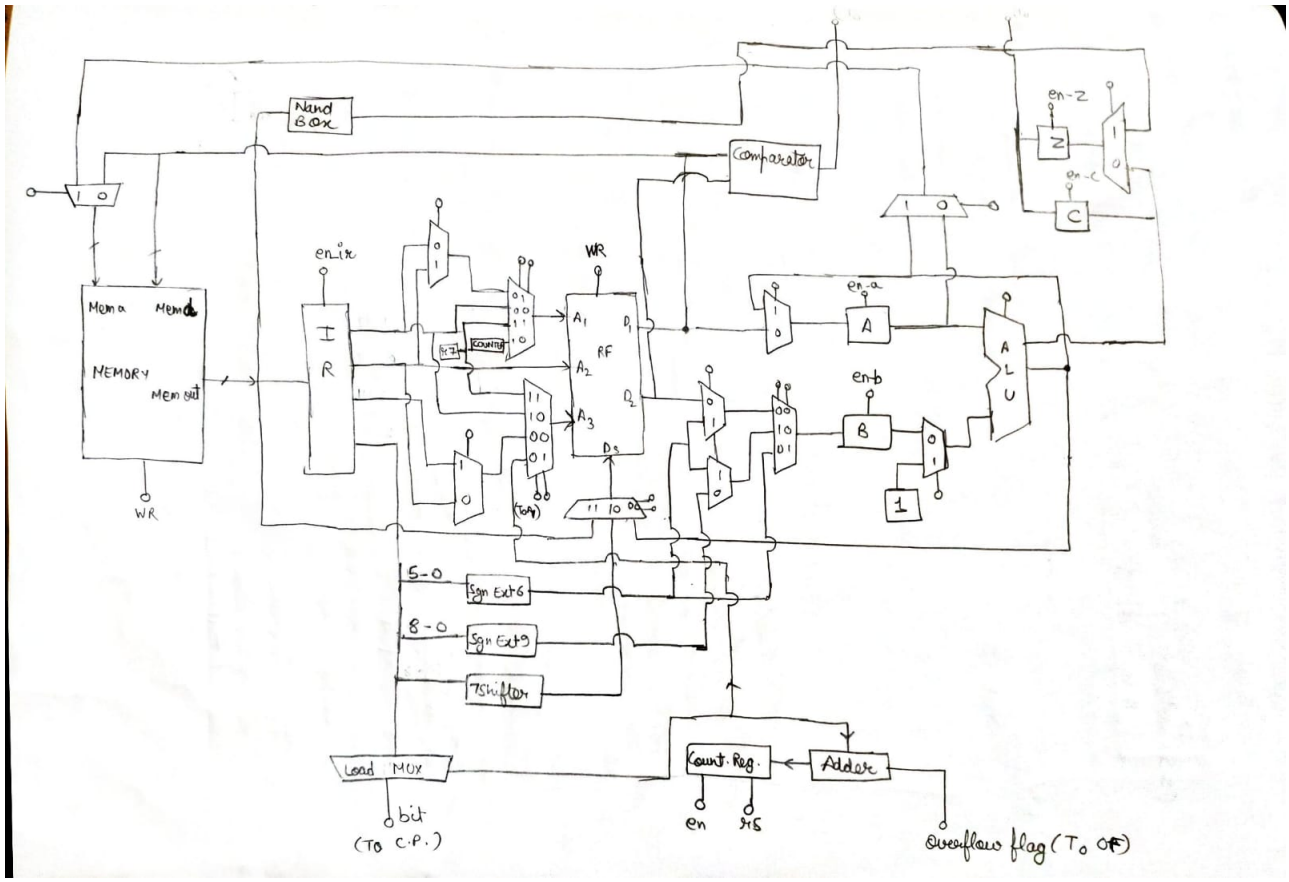
Design Document

Instructions Encoding

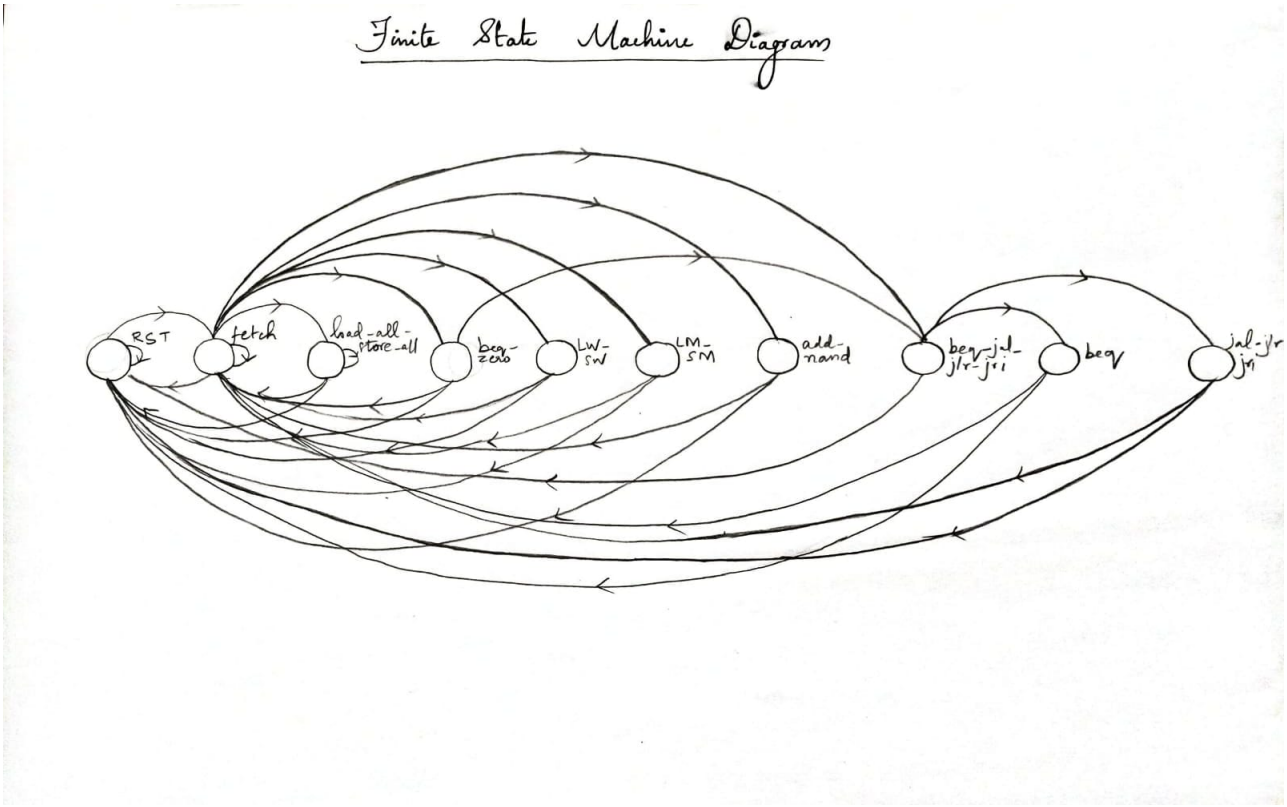
Instructions Encoding:

ADD:	00_01	RA	RB	RC	0	00
ADC:	00_01	RA	RB	RC	0	10
ADZ:	00_01	RA	RB	RC	0	01
ADL:	00_01	RA	RB	RC	0	11
ADI:	00_00	RA	RB	6 bit Immediate		
NDU:	00_10	RA	RB	RC	0	00
NDC:	00_10	RA	RB	RC	0	10
NDZ:	00_10	RA	RB	RC	0	01
LHI:	00_00	RA	9 bit Immediate			
LW:	01_11	RA	RB	6 bit Immediate		
SW:	01_01	RA	RB	6 bit Immediate		
LM:	11_00	RA	0 + 8 bits corresponding to Reg R0 to R7 (right to left)			
SM:	11_01	RA	0 + 8 bits corresponding to Reg R0 to R7 (right to left)			
BEQ:	10_00	RA	RB	6 bit Immediate		
JAL:	10_01	RA	9 bit Immediate offset			
JLR:	10_10	RA	RB	000_000		
JRI	10_11	RA	9 bit Immediate offset			

Datapath Component Design



FSM


Finite State Machine Diagram
RST
fetch
load_all_store_all
beq_zero
LW_SW
LM_SM
add_nand
beq_jal_jr_jri
beq
jal_jr_ji

Components (VHDL Code)

- ALU
- Datapath
- Multiplexers
- Register File
- Registers
- Sign Extenders
- LHI (Load higher immediate)
- Memory asyncread syncwrite
- Control Unit

Flowcharts from next page:

~~1) ADD, ADC, AD~~

1) ADD

OP	RA	RB	RC	Unused	Condition (CZ)
15-12	11-9	8-6	5-3	2	1-0

STATE 1:

$PC^{(R_7)} \longrightarrow$ Mem-a, ALU-A

$+1 \longrightarrow$ ALU-B

Mem-Out $\longrightarrow IR$

ALU-C $\longrightarrow PC(R_7)$

$IR_{11-9} \longrightarrow$ RF_A1

$IR_{8-6} \longrightarrow$ RF_A2

RF_D1 $\longrightarrow$ ALU-A

RF_D2 $\longrightarrow$ ALU-B

ALU-C $\longrightarrow$ RF_D3

$IR_{5-3} \longrightarrow$ RF_A3

2) ADI

State 1

$IR_{11-9} \longrightarrow$ RF_A1

$IR_{8-6} \longrightarrow$ RF_A3

$IR_{5-0} \longrightarrow$ SE9 $\longrightarrow$ ALU-B

RF_D1 $\longrightarrow$ ALU-A

ALU-C $\longrightarrow$ RF_D3

OP	RA	RB	6 bit immediate
15-12	11-9	8-6	5-0

3) LHI

State - I

OP	RA	9 bit immediate
15-12	11-9	8 - 0

$ir_{11-9} \longrightarrow RF\_A3$

$ir_{8-0} \longrightarrow$ 7 shifter $\longrightarrow RF\_D3$

4) LW

State - I

OP	RA	RB	6 bit immediate
15-12	11-9	8-6	5 - 0

$ir_{11-9} \longrightarrow RF\_A3$

$ir_{8-6} \longrightarrow RF\_A1$

$RF\_D1 \longrightarrow ALU\text{-}A$

$ir_{5-0} \rightarrow SE6 \rightarrow ALU\text{-}B$

Counter = "000"

State 4

$ALU\text{-}C \longrightarrow mem\ a$

$mem\text{-}out \longrightarrow RF\_D3$

$nandout \longrightarrow z$

$ir_{11-9} \rightarrow RF\_A3$

5) SW

State - I

OP	RA	RB	6 bit immediate
15-12	11-9	8-6	5 - 0

$ir_{11-9} \longrightarrow RF\_A1$

$ir_{8-6} \longrightarrow RF\_A2$

$RF\_D2 \longrightarrow ALU\text{-}A$

$ir_{5-0} \longrightarrow SE6 \longrightarrow ALUB$

Counter = "000"

$ALU\text{-}C \longrightarrow mem\text{-}a$

$RF\_D1 \longrightarrow mem\text{-}d$

6) JAL

State 1

OP	RA	9bit immediate
15-12	11-9	8 - 0

$IR_{11-9} \longrightarrow RF\_A3$

$R_7 \longrightarrow RF\_D3$

$IR_{8-0} \longrightarrow SE\ 9 \longrightarrow ALU\text{-}B$

$R_7 \longrightarrow ALU\text{-}A$

$ALU\text{-}C \longrightarrow R_7$

$R_7 \longrightarrow ALU\text{-}A$

$-1 \longrightarrow ALU\text{-}B$

$ALU\text{-}C \longrightarrow R_7$

7) JLR

State - 1

OP	RA	RB	6bit immediate (000000)
15-12	11-9	8-6	5 - 0

$IR_{11-9} \longrightarrow RF\_A3$

$R_7 \longrightarrow RF\_D3$

$IR_{5-0} \longrightarrow SE6 \longrightarrow ALU\text{-}B$

$IR_{6-8} \longrightarrow RF\_A2$

$RF\_D2 \longrightarrow R_7$

8) JRI

OP	RA	9bit immediate
15-12	11-9	8 - 0

State - 1

$IR_{11-9} \longrightarrow RF\_A1$

$RF\_D1 \longrightarrow ALU\text{-}A$

$IR_{8-0} \longrightarrow SE\ 9 \longrightarrow ALU\text{-}B$

$ALU\text{-}C \longrightarrow PC$

9) BEQ

OP	RA	RB	6 bit immediate
15-12	11-9	8-6	5-0

State 1

$ir_{11-9} \rightarrow RF\_A1$
$ir_{8-6} \rightarrow RF\_A2$
$RF\_D1 \rightarrow ALU\_A$
$ir_{5-0} \rightarrow SE6 \rightarrow ALU\_B$

COMPARATOR = 1

$ALU\_C \rightarrow RF\_D3$
$R7 \rightarrow RF\_A3$

COMPARATOR = 0 Next instruction

10) ADC | ADZ

OP	RA	RB	RC	0	Condition (CZ)
15-12	11-9	8-6	5-3	2	1-0

State 1

If C = 1 (Z = 1)

$ir_{11-9} \rightarrow RF\_A1$
$ir_{8-6} \rightarrow RF\_A2$
~~ir_{5-0}~~
$RF\_D1 \rightarrow ALU\_A$
$RF\_D2 \rightarrow ALU\_B$

$ALU\_C \rightarrow RF\_D3$
$ir_{5-3} \rightarrow RF\_A3$

If C = 0 (Z = 0)

Next instruction

11) NDU

OP	RA	RB	RC	0	Condition
15-12	11-9	8-6	5-3	2	1-0

State 1

$IR_{11-9} \rightarrow RF\_A1$

$IR_{8-6} \rightarrow RF\_A2$

$RF\_D1 \rightarrow ALU\text{-}A$

$RF\_D2 \rightarrow ALU\text{-}B$

S2

$ALU\text{-}C \rightarrow RF\_D3$

$IR_{5-3} \rightarrow RF\_A3$

S3

12) NDC / NDZ

OP	RA	RB	RC	0	10/01
15-12	11-9	8-6	5-3	2	1-0

State 1

If C = 1 (Z = 1)

↓

S2

↓

S3

If C = 0 (Z = 0)

Next instruction

13) ADL

OP	RA	RB	RC	0	11
15-12	11-9	8-6	5-3	2	1-0

State 1

$IR_{11-9} \rightarrow RF\_A1$

$IR_{8-6} \rightarrow RF\_A2$

$RF\_D1 \rightarrow ALU\text{-}A$

$RF\_D2 \rightarrow LS\text{hifter} \rightarrow ALU\ B$

$ALU\text{-}C \rightarrow RF\_D3$

$IR_{5-3} \rightarrow RF\_A3$

LM OP RA 0+8 bits corresponding to R0 to R7.

State 1 → State 4

If of = 0 , b = 1

Count → ALU A
+1 → ALU B
ALU C → Count

Count → RF-a3
Count → Load Mux
Mem out → RF-d3

If of = 0 , b = 0

Count → ALU A
+1 → ALU B
ALU C → Count

SM OP RA 0+8 bits corresponding to R0 to R7

State 1 → State 4

If of = 0, b = 1

Count → ALU A
+1 → ALU B
ALU C → Count

Count → RF A1, Load Mux
RF-d1 → Mem D

If of = 0, b = 0

Count → ALU A
+1 → ALU B
ALU C → Count