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RESEARCH ARTICLE

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A new structure of single-phase two-stage hybrid transformerless multilevel PV inverter

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Summary

Transformerless inverters are becoming popular for grid-connected photovoltaic applications due to their simplicity, reduced size, weight, cost, and higher efficiency. In this paper, a two-stage hybrid transformerless multilevel inverter (MLI) for single-phase grid-connected photovoltaic power generation system (PVPGS) is presented. The proposed topology comprises a multilevel boost converter (MLBC) and a symmetrical hybrid MLI. MLBC combines the boosting and switched capacitor voltage functions to produce self-balanced multiple voltage levels. The proposed MLI is derived from a combination of bidirectional switches, a half bridge, and a diode-clamped branch, which can produce only two variations in the total common mode voltage and is capable of suppressing leakage current as per DIN VDE 0126-1-1 grid standards. It offers the advantages of scalability, reactive power capability, reduced total harmonic distortion, and filter size. The proposed hybrid transformerless seven-level inverter is simulated in MATLAB, and experimental setup is built to validate the effectiveness of the proposed configuration. Finally, a comprehensive comparison is made with other seven-level inverter topologies.

KEYWORDS

bidirectional switch, leakage current, modular structure, multilevel inverter

1 | INTRODUCTION

Photovoltaic-based renewable energy sources (RES) have proved their potential, and so far, around 400-GW capacities of photovoltaic (PV) plants have been installed across the globe till 2017. This also effectively alleviates greenhouse gas emission and global warming associated with conventional fossil fuels.[1,2] The increased penetration of PV-based RES into the electric grid has drawn the attention of researchers, leading to the design of compact, highly reliable, low cost, and very efficient grid-connected photovoltaic power generation systems (PVPGS). Two-level single-stage grid-connected PV inverters are well commercialized in industries and residential applications due to the simple structure and higher efficiency.[3] RES like PV/fuel cell are usually connected in series to meet the grid peak voltage in two-level single-stage inverter structures. However, these inverters have the following drawbacks: poor maximum power point tracking (MPPT), imbalance in power sharing due to partial shading that result in overheating of the nonshaded PV panel, and lower safety of operation.[4] In addition, it requires high voltage–rated power semiconductor switches, and it has low quality of output power.[5]

Therefore, two-stage power conversion has become more popular and is capable of overcoming the shortcomings of single-stage inverters by employing a front-end DC-DC converter stage. It boosts the lower PV voltage to higher DC-link

voltage and then converts it to AC to meet the grid peak voltages.[6] Moreover, lower number of series-connected PV panels and better MPPT performance are achieved in two-stage inverters in comparison with single-stage inverters. In general, two-stage inverters are built with either a line frequency transformer (LFT) or a high frequency transformer (HFT) to boost the voltage and also to provide galvanic isolation for leakage current flow from the grid to PV source. However, the size, cost, and efficiency of the overall two stages degrade with the use of transformer.[7,8]

In view of the above, many industries are focusing on transformerless PVPGS[9]; however, the issue of leakage current due to parasitic capacitance formed between the PV source and ground due to the surface of cells, frame structure, dust covering, etc. The reasons for the leakage current are variations in common mode voltage (CMV), selection of modulation strategy, and the inverter topology. The injected leakage current finds the path via parasitic capacitance formed by PV panels. Moreover, it can be noticed that the leakage current flow affects power quality, introduces severe electromagnetic interference (EMI) and power losses, and affects the operator's safety. Hence, the control of leakage current within the standards DIN VDE 0126-1-1 is mandatory.[10,11]

Recently, multilevel inverters (MLIs) are emerging in the area of low-power grid-connected RES. MLIs are capable of synthesizing output waveform close to sinusoidal by connecting various DC sources in series. They are becoming popular due to the requirement of reduced device ratings, filter components, and good quality of output power from the perspective of harmonics. Hence, these are the better alternatives to limit the issues of two-level inverters. The popular MLIs in the literature are cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitor (FC). The limitations in these MLIs are more device count, DC voltage balancing issues, and control complexity for increased levels.[12-15]

Therefore, different asymmetrical two-stage MLI topologies have been proposed for seven-level operation with single PV source for grid-connected applications.[16,17] A PV module integrated with new asymmetrical cascaded H-bridge seven-level inverter with reduced device count is also presented in the previous study.[18] All these inverters are good at balancing the DC-link voltage and generating seven levels in the output voltage. But the topologies require a HFT only to boost the PV voltage to grid peak voltage, and there is no isolation between PV and grid. Therefore, an additional LFT or an EMI filter circuit is essential to limit the leakage current. Hence, it leads to an increase in overall system size; reduction in efficiency and also these inverters only support unity power factor conditions of the grid. It is essential to

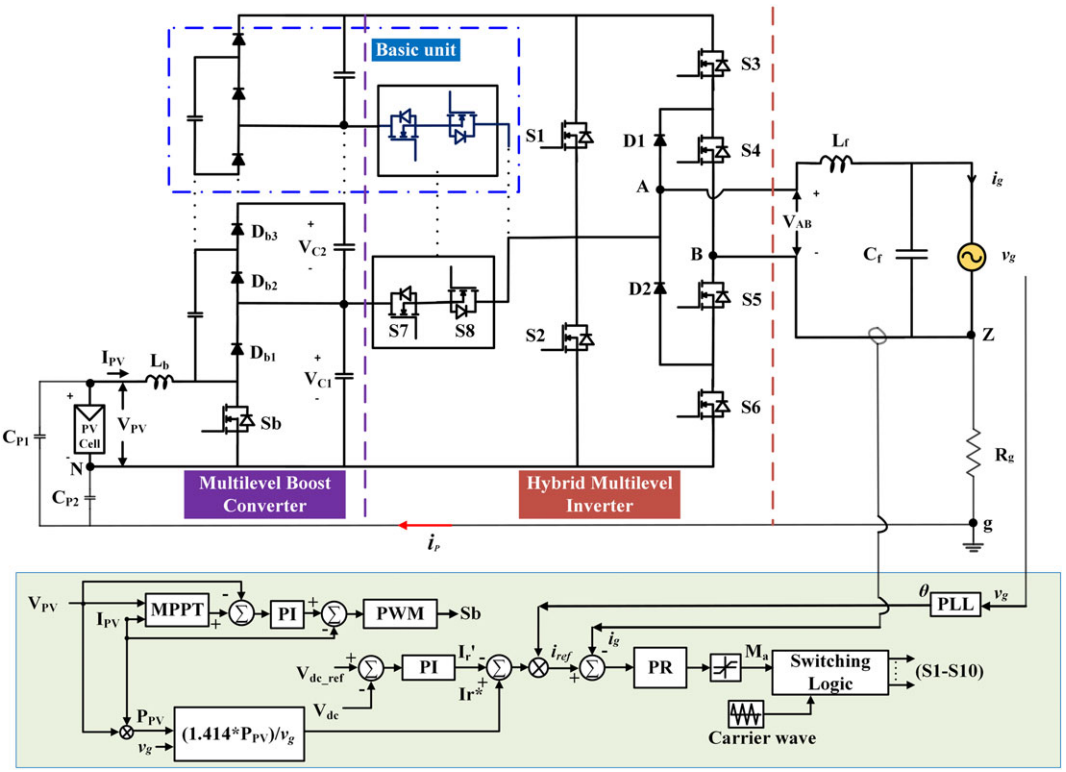

FIGURE 1 Proposed two-stage grid-connected photovoltaic (PV) inverter. MPPT, maximum power point tracking; PWM, pulse width modulation [Colour figure can be viewed at wileyonlinelibrary.com]

deal with high penetration of PV power into grid and reactive power capability in the future PV inverters.[19] This was the inspiration for the authors of the paper, to design a new two-stage configuration to address aforementioned problems.

In this paper, a two-stage module-type hybrid transformerless MLI for single-phase grid-connected PVPGS is presented. The significant advantages of the proposed transformerless two-stage PVPGS are as follows: (1) provides high DC-link voltage necessary to meet the grid peak voltage, (2) a modular structure capable of generating more output levels, (3) limits leakage current to lower than 300 mA as per DIN VDE 0126-1-1 grid standards, and (4) reactive power capability. The detailed working principle of the proposed two-stage configuration and control strategies are presented in Sections 3 and 4. The CMV analysis and design of passive components are discussed in Sections 5 and 6. The simulation and experimental results for unity and nonunity power factor loads are presented in Sections 7 and 8. Comparison of the proposed system with existing two-stage and single-stage MLIs is given in Section 9. Finally, loss calculation and concluding remarks are given in Sections 10 and 11.

2 | SYSTEM DESCRIPTION

The schematic arrangement of the proposed transformerless two-stage grid-connected PV inverter is shown in Figure 1. This two-stage configuration comprises multilevel boost converter (MLBC) and a symmetrical hybrid MLI. The MLBC produces *N* number of boosted voltage levels from the input PV source to meet the DC-link voltage requirement without using an HFT and extreme duty cycle ratio; also, each device blocks only (1/*N*) times DC-link voltage. It has significant advantages of (1) higher efficiency with reduced voltage stress across the devices and (2) guaranteed balancing of the DC-link capacitors by clamping the diodes based on the capacitor voltages.

The proposed hybrid MLI converts multilevel DC to AC. The gate pulses to the inverter switches are generated through modified sinusoidal level shifted pulse width modulation (SLS-PWM). It enables the inverter to operate under all types of loading conditions such as unity, lagging, and leading power factors without changing the CMV behavior. Moreover, the magnitude of root mean square (RMS) leakage current is well below the grid standards with simple asymmetrical filter inductor. Furthermore, the number of levels in the output voltage of MLBC and hybrid MLI can be increased by adding basic unit. The complete closed loop control diagram for MPPT and grid current injection of the two-stage system[16,20] is shown in Figure 1. The detailed operation of MLBC, hybrid MLI, control strategy, and CMV analysis is explained in the following sections.

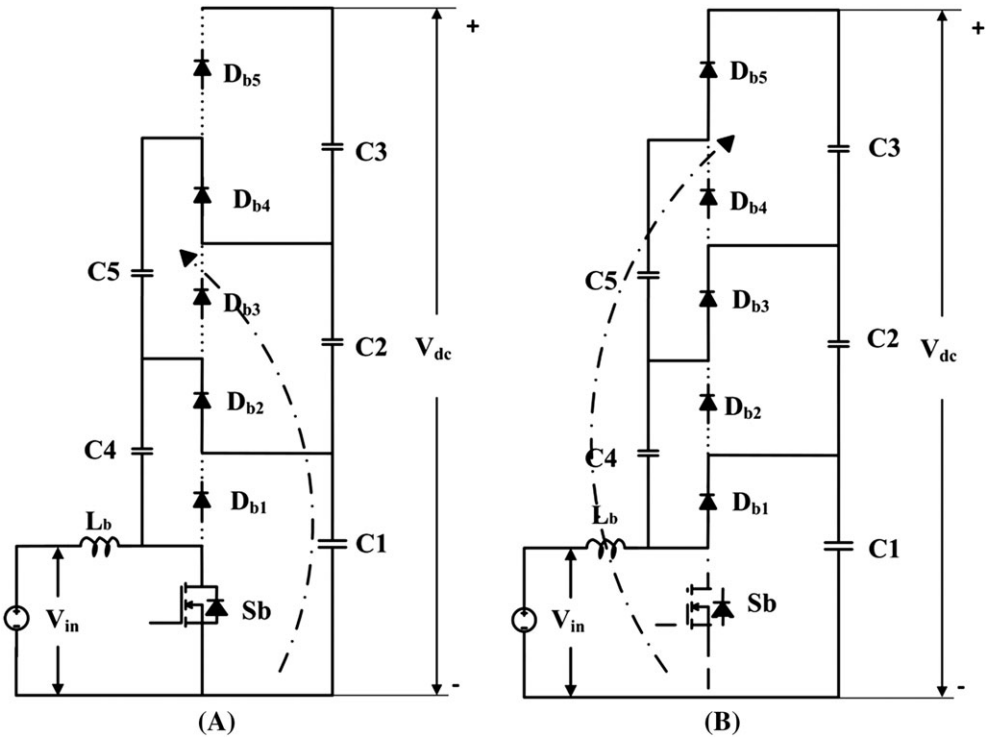

FIGURE 2 Operating condition of the switch: A, on state; B, off state

3 | MULTILEVEL BOOST CONVERTER

Figure 2 shows the three-level DC-DC converter which is derived from conventional boost converter using diodes and capacitors.[21] One of the main advantages of MLBC is its capability of balancing DC capacitors without adding additional circuits. The three-level boost converter acts as a front-end converter to boost the input DC voltage. The work of MLBC circuit is depicted in Figure 2A and 2B where different switching states of the power devices are described below. In Figure 2A, when the switch Sb is in ON state, inductor L_b is connected to the input DC source (V_{in}). Under this condition, if capacitor C4's voltage is less than C1's voltage, then C1 clamps C4's voltage through diode D_{b2} and switch Sb. Simultaneously, if the voltage across C4 + C5 is less than the voltage across C1 + C2, then C1 and C2 clamp the voltage across C4 and C5 through D_{b4} and Sb.

Similarly, in Figure 2B, when Sb is in OFF state, inductor current conducts D_{b1} and charges the capacitor C1. When D_{b1} conducts, C4 and the voltage V_{in} plus the inductor's voltage clamp the voltage across C1 and C2 through D_{b3}. Similarly, the voltage across the inductor plus V_{in}, C4, and C5 clamps the voltage across C1, C2, and C3 through D_{b5}. It is important to note that diodes D_{b1}, D_{b3}, and D_{b5} conduct synchronously in the circuit, and they are complement with the diodes D_{b4}, D_{b2}, and Sb. The total DC-link voltage (V_{dc}) and input inductor current (I_L) can be expressed in terms of the input voltage (V_{in}) and duty ratio as per Equations 1 and 2, respectively. R_o is the output resistance, and D is the duty ratio of MLBC. The total number of capacitors and diodes required for "N" level DC output is $(2N - 1)$. The voltage across the capacitors "V_c" and the blocking voltage "V_b" of switch and diode are expressed by Equation 3.

$$V_{dc} = \frac{N^* V_{in}}{(1-D)}, \tag{1}$$

$$I_L = \frac{N^2 V_c}{(1-D)R_o}, \tag{2}$$

$$V_b = V_c = \frac{V_o}{N}. \tag{3}$$

4 | PROPOSED TRANSFORMERLESS HYBRID MLI

The proposed MLI is derived by combining common emitter bidirectional MOSFET branches and a hybrid-bridge three-level inverter. The hybrid-bridge inverter consists of half-bridge leg with S1 and S2 and an NPC leg with S3, S4, S5, S6, D1, and D2; this enables the polarity generation for the three-level DC voltages.[22] The common emitter bidirectional

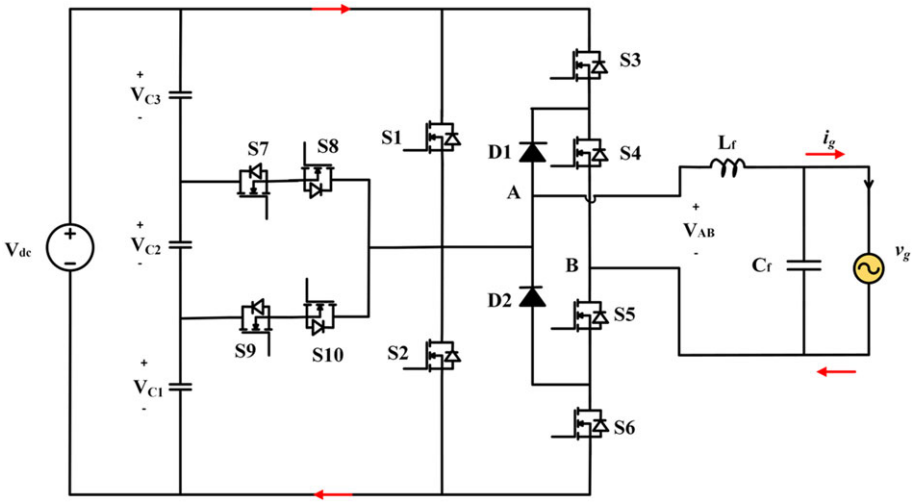

FIGURE 3 Proposed hybrid seven-level inverter topology [Colour figure can be viewed at wileyonlinelibrary.com]

branch can select capacitor voltages such as V_{C1}, $(V_{C1} + V_{C2})$, and $(V_{C1} + V_{C2} + V_{C3})$ based on the number of output voltage levels.

4.1 | Operating states of the inverter in different modes

In this section, the detailed switching configurations adopted for unity power factor of the grid (v_g and i_g positive, v_g and i_g negative) and nonunity power factor conditions of the grid (v_g positive, i_g negative and v_g negative, i_g positive) of seven-level inverter and the modified SLS-PWM are presented. Figure 3 shows the proposed seven-level inverter topology.

4.1.1 | Case I

Assume that both the grid voltage (v_g) and current (i_g) are positive, the voltage levels can be expressed as $(V_{C1} + V_{C2} + V_{C3}) = V_{dc}$, $(V_{C1} + V_{C2}) = (2/3)V_{dc}$, and $V_{C1} = (1/3)V_{dc}$. Figure 4A corresponds to state 1 in Table 1; switches S1, S5, S6, and S7 are turned ON while switches S2, S3, S4, S8, S9, and S10 are turned OFF which corresponds

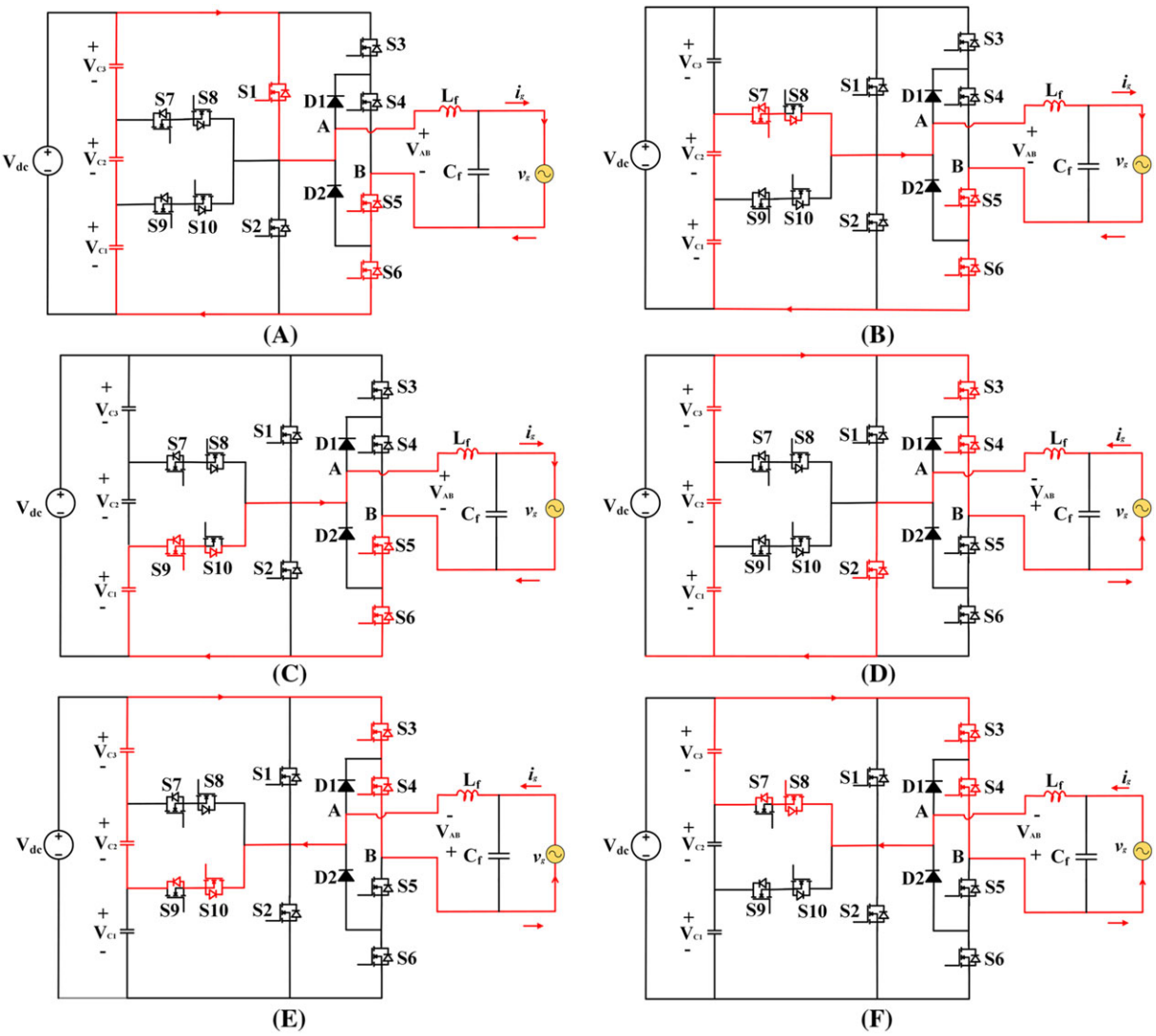

FIGURE 4 Operating modes of the proposed topology when v_g and i_g are positive and v_g and i_g are negative, respectively. A, $V_{AB} = (V_{C1} + V_{C2} + V_{C3})$ (state 1 in Table 1). B, $V_{AB} = (V_{C1} + V_{C2})$ (state 2 in Table 1). C, $V_{AB} = V_{C1}$ (state 3 in Table 1). D, $V_{AB} = -(V_{C1} + V_{C2} + V_{C3})$ (state 6 in Table 1). E, $V_{AB} = -(V_{C2} + V_{C3})$ (state 7 in Table 1). F, $V_{AB} = -V_{C3}$ (state 8 in Table 1) [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 1 Common mode voltage calculation

State	V_{AN}	V_{BN}	V_{CM}	V_{DM}	V_{S1}	$V_{tcm} = V_{BN}$
1	$3V$	0	$1.5V$	$3V$	$-1.5V$	0
2	$2V$	0	V	$2V$	$-V$	0
3	V	0	$0.5V$	V	$-0.5V$	0
4	0	0	0	0	0	0
5	$3V$	$3V$	$3V$	0	0	$3V$
6	0	$3V$	$1.5V$	$-3V$	$1.5V$	$3V$
7	V	$3V$	$2V$	$-2V$	V	$3V$
8	$2V$	$3V$	$2.5V$	$-V$	$0.5V$	$3V$

$V = (1/3)V_{dc}$.

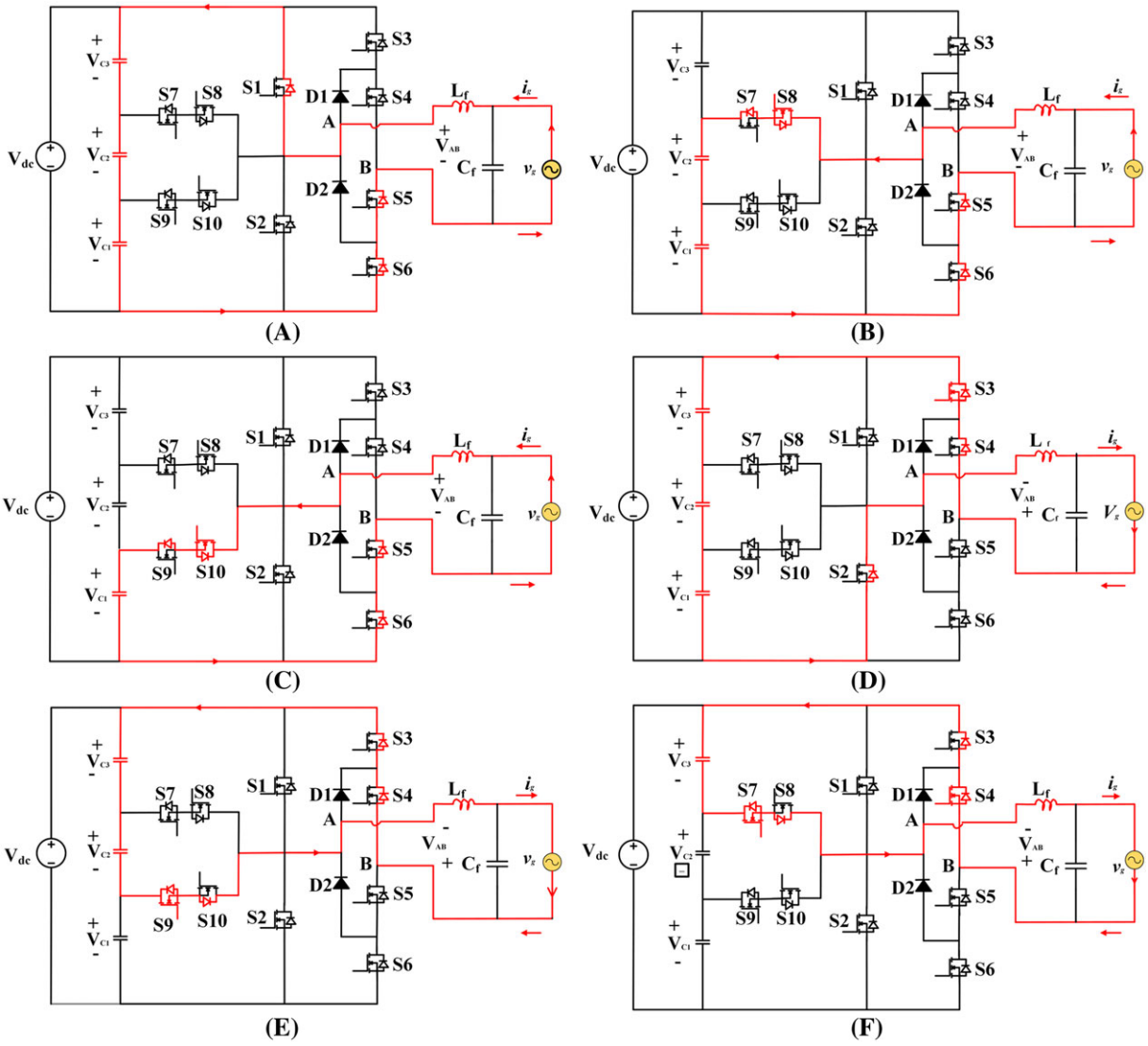

FIGURE 5 Operating modes of the proposed topology when v_g is positive and i_g is negative, and v_g is negative and i_g is positive, respectively. A, $V_{AB} = (V_{C1} + V_{C2} + V_{C3})$ (state 1 in Table 1). B, $V_{AB} = (V_{C1} + V_{C2})$ (state 2 in Table 1). C, $V_{AB} = V_{C1}$ (state 3 in Table 1). D, $V_{AB} = -(V_{C1} + V_{C2} + V_{C3})$ (state 6 in Table 1). E, $V_{AB} = -(V_{C2} + V_{C3})$ (state 7 in Table 1). F, $V_{AB} = -(V_{C3})$ (state 8 in Table 1) [Colour figure can be viewed at wileyonlinelibrary.com]

to the normal operation of a hybrid-bridge inverter. In this case, $V_{AB} = (V_{C1} + V_{C2} + V_{C3})$, and the output current flows from MLBC to load through S1 and returns through S5 and S6. Figure 4B corresponds to state 2 in Table 1; switch S1 is OFF, while S7 and the body diode of S8 are turned ON (S5 and S6 remain ON), and the switches S2, S3, S4, S9, and S10 are turned OFF. In this case, $V_{AB} = (V_{C1} + V_{C2})$, and the output current flows from the lower two capacitors to the load through switch S7 and the body diode of S8, S5, and S6. Figure 4C corresponds to state 3 in Table 1; switch S9 and the body diode of S10 are turned ON (S5 and S6 remain ON), and the switches S2, S3, S4, S7, and S8 are turned OFF. In this case, $V_{AB} = V_{C1}$, and the output current flows from the lower capacitor to the load through switch S9 and the body diode of S10, S5, and S6.

4.1.2 | Case II

When both the grid voltage (v_g) and currents (i_g) are negative, voltage levels $(V_{C1} + V_{C2} + V_{C3}) = -V_{dc}$, $(V_{C2} + V_{C3}) = -(2/3)V_{dc}$, and $V_{C3} = -(1/3)V_{dc}$ are produced as shown in Figure 4. Figure 4D corresponds to state 6 in Table 1; switches S2, S3, S4, and S10 are turned ON while the switches S1, S5, S6, S7, S8, and S9 are turned OFF, which corresponds to the normal operation of a hybrid-bridge inverter. In this case, $V_{AB} = -(V_{C1} + V_{C2} + V_{C3})$, and the output current flows from load to MLBC through S3 and S4 and returns through S2. Figure 4E corresponds to state 7 in Table 1; the body diode of S9 and S10 are turned ON (S3 and S4 remain ON), and the switches S1, S2, S5, S6, S7, and S8 are turned OFF. In this case, $V_{AB} = -(V_{C2} + V_{C3})$, and the output current flows from the load to upper two capacitors through switch S10 and body diode of S9, S3, and S4. Figure 4F corresponds to state 8 in Table 1; switch S8 and the body diode of S7 are turned ON (S3 and S4 remain ON), and the switches S1, S2, S5, S6, S9, and S10 are turned OFF. In this case, $V_{AB} = -V_{C3}$, and the output current flows from the load to top capacitor through switch S8 and the body diode of S7, S3, and S4.

4.1.3 | Case III

When the grid voltage (v_g) is positive and grid current (i_g) is negative, voltage levels $(V_{C1} + V_{C2} + V_{C3}) = V_{dc}$, $(V_{C1} + V_{C2}) = (2/3)V_{dc}$, and $V_{C1} = (1/3)V_{dc}$ are produced as shown in Figure 5 and the related states are given in Table 1. For all the states in this mode, current flows from the grid to MLBC; return path for currents is provided by the body diodes of S5 and S6. From Figure 5A, the output voltage $V_{AB} = (V_{C1} + V_{C2} + V_{C3})$ is produced and the current flows through the body diode of S1. In Figure 5B, S8 and body diode of S7 are conducting to complete the path for the current and the output voltage $V_{AB} = (V_{C1} + V_{C2})$. In state 3 (Figure 5C), S10 and body diode of S9 are conducting to complete the current path and the output voltage $V_{AB} = V_{C1}$.

4.1.4 | Case IV

When the grid voltage (v_g) is negative and current is positive (i_g), voltage levels $(V_{C1} + V_{C2} + V_{C3}) = -V_{dc}$, $(V_{C2} + V_{C3}) = -(2/3)V_{dc}$, and $V_{C3} = -(1/3)V_{dc}$ are produced as shown in Figure 5 and the related states are given

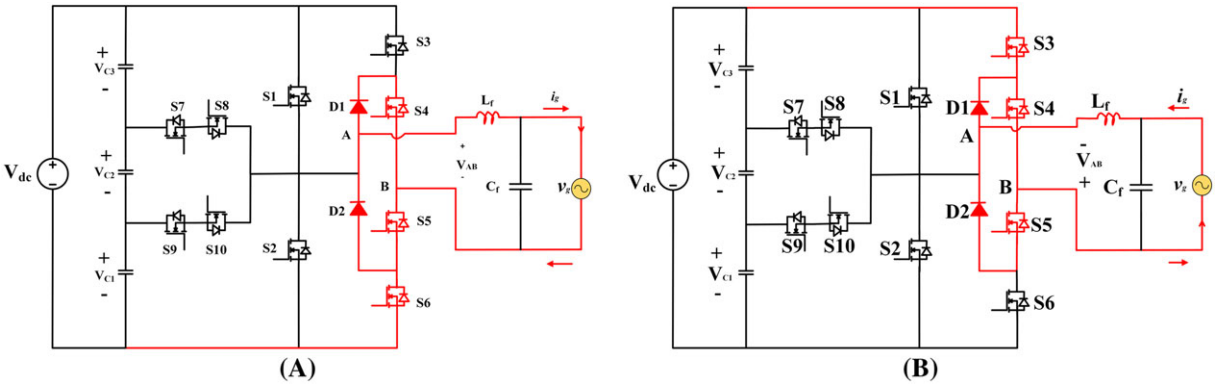

FIGURE 6 Operating modes of the proposed topology in zero states ($V_{AB} = 0$): A, state 4 in Table 1; B, state 5 in Table 1 [Colour figure can be viewed at wileyonlinelibrary.com]

Table 1. All the states in this mode, current flows from the MLBC to grid; return path for current is provided by the body diodes of S3 and S4. From Figure 5D, the body diode of S2 conducts to complete the current path and output voltage $V_{AB} = -(V_{C1} + V_{C2} + V_{C3})$. From Figure 5E, S9 and body diode of S10 are conducting to complete the current path and the output voltage $V_{AB} = -(V_{C2} + V_{C3})$. From Figure 5F, S7 and body diode of S8 are conducting to complete the current path and output voltage $V_{AB} = -V_{C3}$.

4.1.5 | Case V

Finally, freewheeling states can be produced in two different forms, as shown in Figure 6. In positive half cycle, switches S4, S5, and S6 are turned ON as shown in Figure 6A and state 4 in Table 1. In the negative half cycle, switches S3, S4, and S5 are turned ON as shown in Figure 6B, which corresponds to state 5 in Table 1. To clamp the voltages V_{AN} and V_{BN} to either zero or V_{dc} in the freewheeling period, switches S6 and S3 are turned ON, respectively. Therefore, the total common mode voltage (V_{tcm}) has only two voltage variations as shown in Table 1. It is evident that in both the cases, the current can flow in any direction through the diodes D1 and D2.

4.2 | Modified SLS-PWM modulation technique with reactive power capability

Several modulation schemes have been reported for MLI operation for better quality of supply and are mainly categorized as (1) sinusoidal PWM, (2) selective harmonic elimination, and (3) space vector PWM. Among these, the SLS-PWM technique is adapted for the output voltage generation. In this section, a detailed implementation of modified SLS-PWM is discussed. The seven-level output voltage waveform is synthesized using the states explained in Section 4.1, and they are split into four modes of operation. Figure 7 shows various operating modes of the grid and detailed switching pattern for the proposed inverter topology.[19,23]

For better visualization of the switching pattern, switching frequency (f_s) is selected as 2 kHz and demonstrated for 1 cycle of operation. It can be noticed that switches S1and S2 are conducting in the top level which corresponds to positive v_g and negative v_g, respectively. S3 and S6 operate at fundamental frequency of the grid and are complementary.

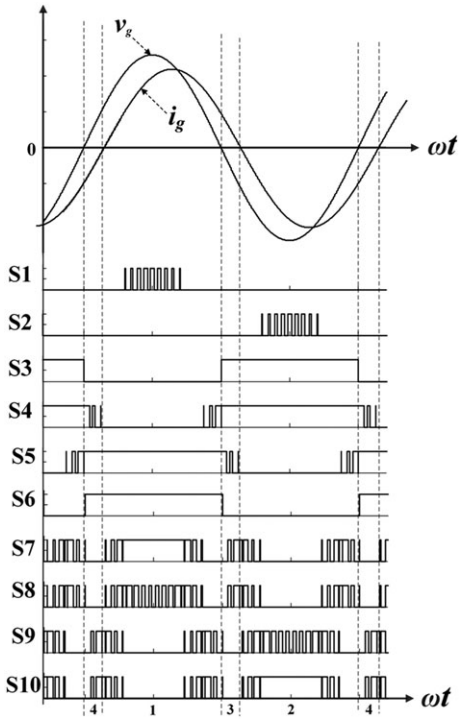

FIGURE 7 Switching patterns for the inverter switches with reactive power capability. Mode 1: The grid voltage and currents are positive. Mode 2: The grid voltage and currents are negative. Mode 3: The grid voltage is positive and current is negative. Mode 4: The grid voltage is negative and current is positive

Switch S4 conducts in positive half cycle, and S5 conducts in negative half cycle. Moreover, switches S4 and S5 also conduct in the freewheeling states, to provide current path under any current direction.

Switches S7, S8, S9, and S10 along with their body diodes conduct in $(2/3)V_{dc}$ and $(1/3)V_{dc}$ levels in any mode of operation as shown in Figures 4 and 5. To avoid the current dependent commutation of bidirectional MOSFET branch, gate pulses given to switches (S7, S8) and (S9, S10) are different. The detailed analysis is given in the previous study.[23] The modulation index M_a and the output voltage of the inverter are as follows:

$$M_a = \frac{V_{ref}}{3V_c}, \tag{4}$$

$$v_g = \frac{M_a{}^*V_{dc}}{\sqrt{2}}, \tag{5}$$

where V_{ref} is the peak value of reference sine wave and V_c is amplitude of carrier waveforms. Figure 8A illustrates SLS-PWM technique for the seven-level inverter with one sinusoidal reference wave and six triangular carrier waves (C1, C2, C3, C4, C5, and C6). Figure 8B shows the detailed implementation of the SLS-PWM technique. The Boolean logic functions derived for the control of switching devices are given in Equation 6.

$$\begin{gathered} S1 = C,\ S2 = F,\ S3 = \overline{G}, S4 = \overline{G} + \overline{A},\ S5 = G + \overline{D},\ S6 = G,\ S7 = B + E \oplus D,\ S8 = (E \oplus D) + (B \oplus C), \\ S9 = (A \oplus B) + (E \oplus F),\ S10 = (A \oplus B) + E \end{gathered} \tag{6}$$

5 | COMMON MODE VOLTAGE ANALYSIS

In this paper, the total common mode voltage analysis of the proposed inverter is carried out with reference to the guidelines addressed in the previous study.10 From Figure 1, the differential mode voltage (V_{DM}) and common mode voltage (V_{CM}) of the inverter are used to analyze the total common mode voltage (V_{tcm}) in each state of the inverter. In the proposed transformerless seven-level configuration, filter inductor is placed between the inverter phase and grid ($L_1 = L_f$ and $L_2 = 0$). Therefore, the voltage source (V_{S1}) is produced due to asymmetries in line impedances and also asymmetries in the parasitic capacitances between the switches and ground as expressed in Equation 9.

$$V_{DM} = V_{AB} = V_{AN} - V_{BN}, \tag{7}$$

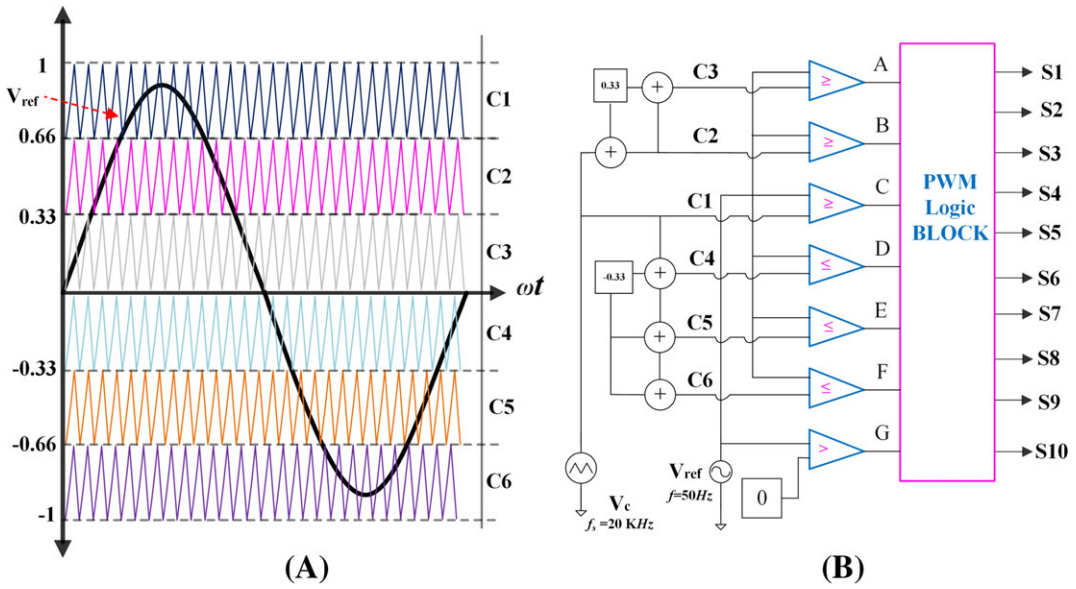

FIGURE 8 A, Seven-level SLS-PWM technique. B, Implementation of SLS-PWM. SLS-PWM, sinusoidal level shifted pulse width modulation [Colour figure can be viewed at wileyonlinelibrary.com]

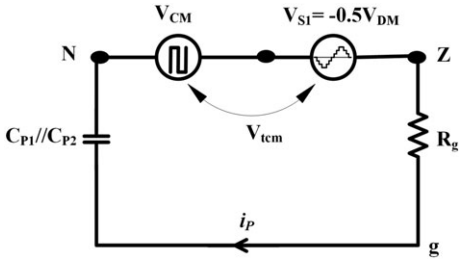

FIGURE 9 Equivalent common mode model for the proposed topology

$$V_{DM} = (V_{AN} + V_{BN})^{*}0.5, \tag{8}$$

$$V_{S1} = V_{DM}(L_2 - L_1)/(2^{*}(L_1 + L_2)) = -0.5V_{DM}. \tag{9}$$

Figure 9 illustrates the equivalent common mode model of the proposed configuration. From Figure 1, it can be noticed that the equivalent voltage between terminals N and Z are referred to V_{tcm} which directly feeds two impedances in the circuit path, such as equivalent parasitic capacitance C_P ($C_{P1}//C_{P2} = C_{P1} + C_{P2}$) of the PV source and the ground resistance R_g. From Equation 11, the magnitude of leakage current mainly depends on C_P and variations in the total CMV. From Table 1, it is observed that V_{tcm} has "0" during the positive half cycle, ie, states 1 to 4, and "V_{dc}" during the negative half cycle, ie, states 5 to 8. The transition between the two values is observed at zero states; hence, V_{tcm} commutates at the line frequency. Therefore, i_P is maintained almost close to zero most of the time, except at zero crossings, where it exhibits a large spike due to sudden variation in dV_{tcm}/dt during the transition. Table 1 shows the total common mode voltage calculation in different states, where it is assumed that all the DC-link capacitors are of equal magnitude, ie, $V_{C1} = V_{C2} = V_{C3} = (1/3)V_{dc}$.

$$V_{tcm} = V_{CM} + V_{S1} = V_{BN}, \tag{10}$$

$$i_P = C_P \frac{dV_{tcm}}{dt}. \tag{11}$$

6 | DESIGN OF PASSIVE COMPONENTS

This section presents the design of passive components which are used for boosting and filtering operation in the proposed two-stage system. The inductors and capacitors are selected based on the desired values of ripple content in the current and voltage, respectively. Moreover, the size of the passive components greatly depends on the selection of switching frequency (f_s). For residential PV applications, switching frequency is selected between 16 and 48 kHz with

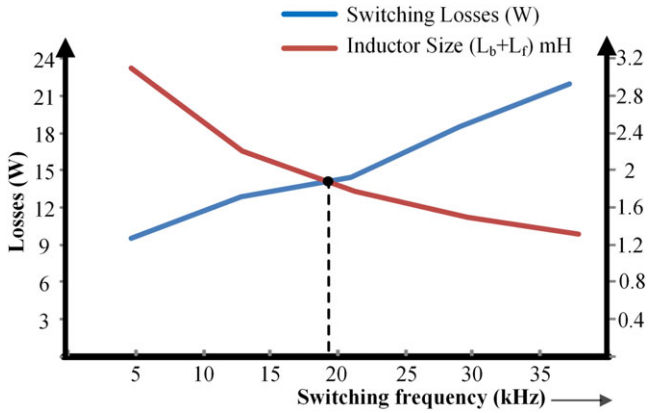

FIGURE 10 Selection of switching frequency [Colour figure can be viewed at wileyonlinelibrary.com]

around 20 kHz, a good compromise between filter size and switching losses.[24-26] Figure 10 shows the variation of switching losses and inductor size with respect to switching frequency by considering 20% of ripple. It is noticed that 20-kHz frequency will be the optimal value of "f_s" for the proposed two-stage system.

6.1 | Boost inductor

The expression used for the calculation of boost inductor (L_b) based on the ripple content in the input current (ΔI_{in}) and switching frequency (f_s) is as follows[27]:

$$L_b = \frac{V_{in} D}{\Delta I_{in} f_s}, \tag{12}$$

where V_{in} is the input voltage and D is the duty cycle of the boost converter.

6.2 | DC-link capacitors

The size of the DC-link capacitors[8,28] (C = C1 = C2 = C3 = C4 = C5) is determined by using Equation 13, which is derived based on the amplitude of ripple in DC-link voltage (ΔV_{dc}), where P_{rated} is the rated power and ω is the grid frequency in radian per second.

$$C = \frac{P_{rated}}{2\omega V_{dc} \Delta V_{dc}}. \tag{13}$$

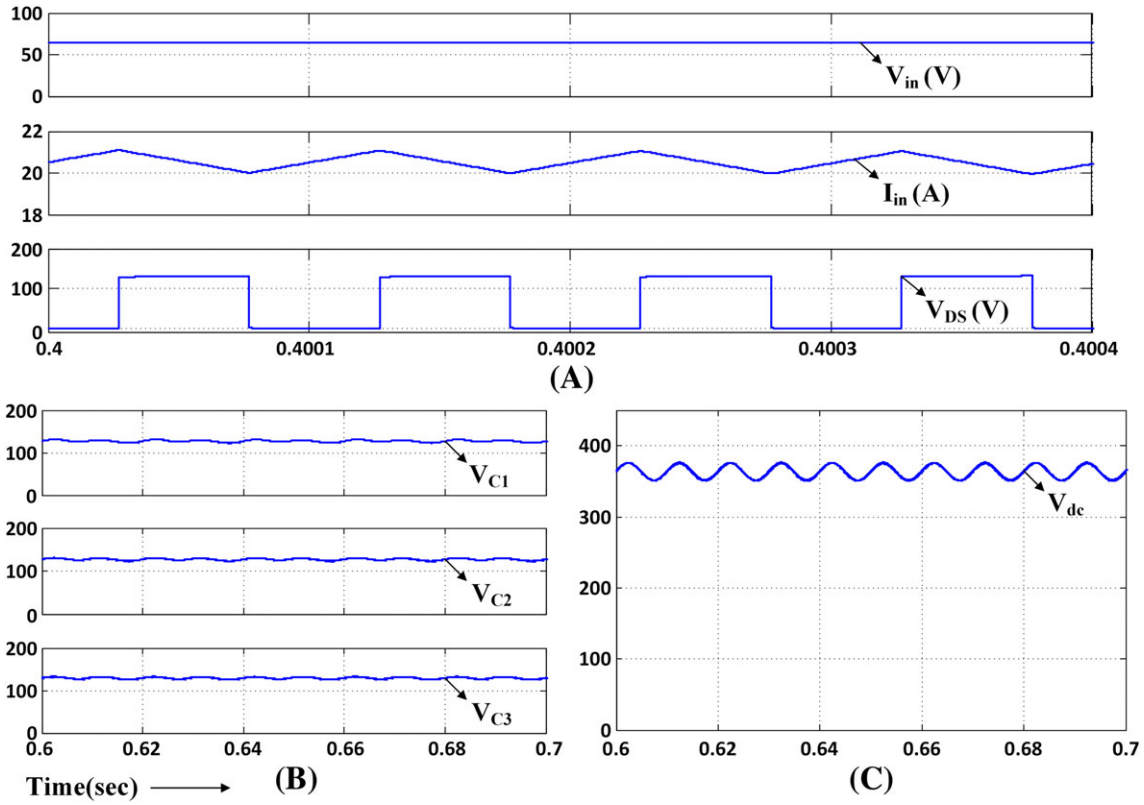

FIGURE 11 Simulation results of multilevel boost converter (MLBC). A, Input voltage, current, and drain source voltage of Sb. B, Balanced capacitor voltages. C, Total DC-link voltage [Colour figure can be viewed at wileyonlinelibrary.com]

6.3 | LC filter

A passive LC filter is employed to limit the harmonic content by DC-AC inverter at point of common coupling, and its detailed design procedure is given in the previous study.[29] In this paper, IEEE 1547 grid interconnection standards are considered to limit the harmonic content. The design of the filter inductor (L_f) depends on the desired peak-peak current ripple ($\Delta i_{LP\text{-}P}$), and it is given in Equation 14. The design of filter capacitor is based on the maximum power factor seen by the grid. The value of the filter capacitor (C_f) is calculated as per Equation 15, for 5% ripple, where P_{rated} is the rated power, v_g is the RMS value of the grid voltage, V_{dc} is the total DC-link voltage, and f and f_s are the grid frequency and switching frequency of VSI, respectively.

$$\frac{V_{dc}}{24 f_s L_f} = \Delta i_{LP\text{-}P} < 25\% \frac{P_{rated}}{v_g}, \tag{14}$$

$$C_f = 5\% \frac{P_{rated}}{2\pi f . v_g^2}. \tag{15}$$

7 | SIMULATION RESULTS

In order to verify the theoretical concept as aforementioned, the simulation work is carried out in MATLAB/SIMULINK software. The SLS-PWM technique is implemented to generate the control pulses for hybrid inverter using the switching logic given in Section 4. Various parameters selected for the simulation work are as follows: input DC voltage $V_{in} = 65$ V, $D = 0.5$, $P_{rated} = 1.2$ kW, for unity power factor operation, switching frequency $f_s = 20$ kHz, $M_a = 0.84$, passive elements $L_b = 0.5$ mH (20% of ΔI_{in}), C1 = C2 = C3 = C4 = C5 = 1300 μF (1% of ΔV_{dc}), $L_f = 1$ mH (20% of $\Delta i_{LP\text{-}P}$), $C_f = 4$ μF, $C_P = 20$ nF, and $R_g = 100$ Ω.

Figure 11A shows simulation results of input voltage, current, and drain source voltage (V_{DS}) of Sb. The voltages across the DC-link capacitors V_{C1}, V_{C2}, and V_{C3} and also total DC-link voltage are shown in Figure 11B and 11C, respectively. From Figure 11, it is noticed that the front-end MLBC is operating in continuous conduction mode (CCM) and

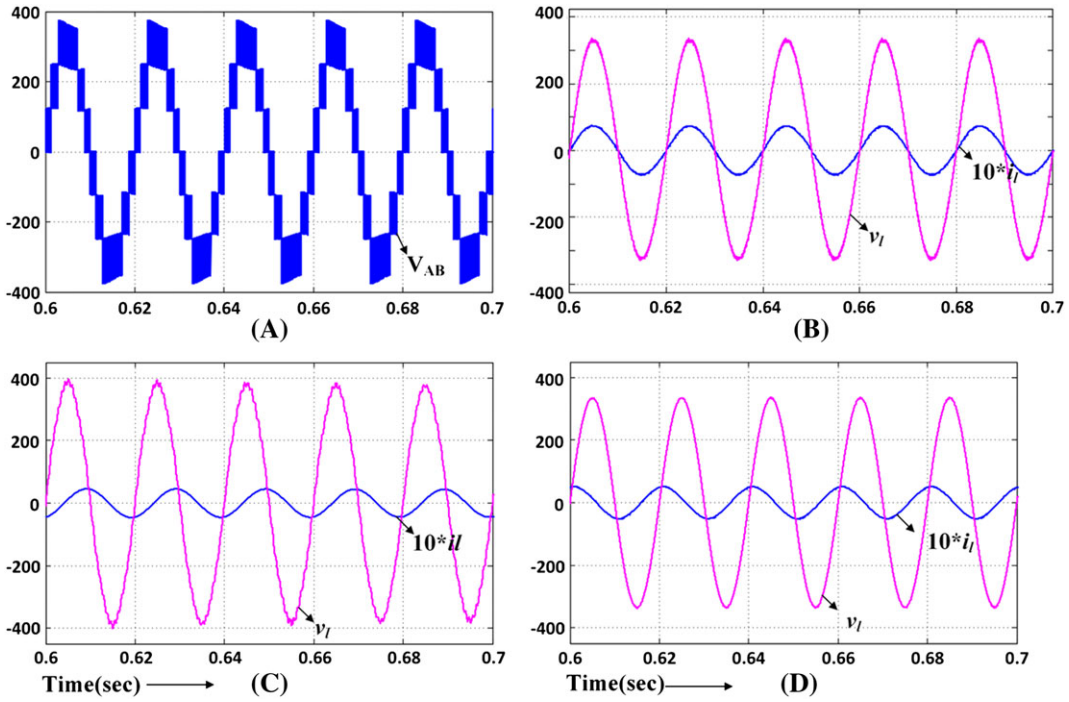

FIGURE 12 Simulation results for the proposed seven-level inverter: (A) seven-level output voltage; B-D, v_l and i_l at unity, lagging (0.58), and leading (0.58) power factor operations, respectively [Colour figure can be viewed at wileyonlinelibrary.com]

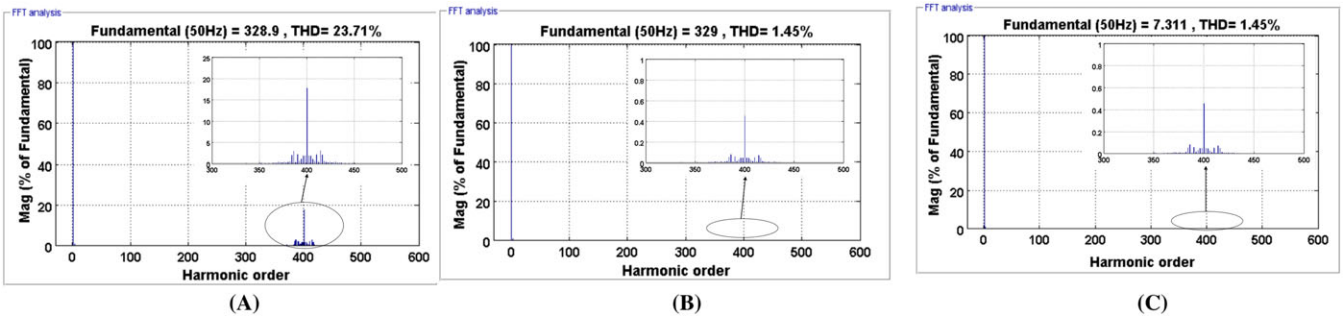

FIGURE 13 Total harmonic distortion (THD) spectrums of the seven-level multilevel inverter (MLI): A, terminal voltage V_{AB}; B, load voltage; C, load current with *R* load [Colour figure can be viewed at wileyonlinelibrary.com]

generating a three-level balanced DC-link voltages. The total DC output voltage of the MLBC is further fed to inverter stage to produce seven-level output voltage as shown in Figure 12A. The filtered output voltage and load current waveforms for unity, (0.58) lagging, and (0.58) leading power factors of the load are given in Figure 12B-D, respectively. It can be noticed that the proposed topology is capable of supplying reactive power as explained in Section 4.

The measured Fast Fourier Transform (FFT) spectrums for the seven-level MLI output waveforms are given in Figure 13. Figure 13A depicts the total harmonic distortion (THD) of seven-level voltage, and Figure 13B and 13C depicts the load voltage and current after the LC filter, respectively. It can be noticed that the measured THD of voltage reduced from 23.71% to 1.45% after filtering, and the current THD is 1.45%. Table 2 shows the comparison of %THD for different harmonic orders for various loading conditions. This confirms that the designed LC filter effectively attenuates the harmonic content, and it is within the limits of IEEE1547 grid standards.

Figure 14A-D illustrates the measured waveforms of terminal voltages V_{AN}, V_{BN}, V_{CM}, and i_P, respectively. It is to be noted that uncontrolled spikes in the leakage current appears with grid frequency variation due to changes in V_{tcm}. Moreover, the magnitude of the spikes depends on the V_{tcm} and parasitic capacitance (C_P) formed by the PV source. The transitions in V_{tcm}, at every zero crossing, generates a spike as shown in Figure 14D. Here, the RMS value of leakage current is 40 mA which is much below the DIN VDE 0126-1-1 grid standards. The ground resistance may help to suppress these peaks of the leakage current.[11] To prove the effectiveness of the proposed topology in limiting RMS leakage current, three different combinations of ground resistances and parasitic capacitances are considered to evolve at the leakage current magnitude. From Figure 15, it can be clearly noticed that in all three cases, the RMS leakage current does not exceed German DIN VDE 0126-1-1 grid standards. Hence, the proposed circuit configuration is effective in limiting the leakage current.

Figure 16 illustrates the performance of the proposed system with MPPT and grid-connected mode for changes in PV insolation from 1000 to 600 W/m^2. Two series (N_S) and three parallel (N_P) combinations of PV-MLU255HC panels were used as PV source. Specifications of the PV panel at standard test conditions are voltage at maximum power V_{MPP} = 31.2 V, current at maximum power I_{MPP} = 8.18 A, and maximum power P_{MPP} = 255 W. Simple perturb and observation algorithm is used for MPPT operation. It can be noticed that the DC-link voltage and grid voltage are well regulated, and the corresponding changes in the power levels were also observed at 0.6 second.

In order to show the modularity of the proposed two-stage system, five-level generation is presented through Figure 17 with reduction in one basic unit as compared to seven-level operation. Figure 18A and 18B shows the balanced DC-link voltages and the total DC output voltage of the two-stage MLBC which is fed to the inverter stage to

TABLE 2 Individual %THD comparison for different loading conditions

Harmonic Order, h		5	7	11	13	17	19	23	25	Overall THD, %
IEEE 1547 Harmonic voltage THD, %		4	4	2	2	1.5	1.5	0.6	0.3	<5
Harmonic voltage THD of the proposed system, %	R	0.08	0.02	0.05	0.08	0.05	0.06	0.07	0.01	1.45
	RL	0.12	0.03	0.05	0.08	0.04	0.06	0.07	0.00	2.26
	RC	0.08	0.01	0.05	0.08	0.04	0.06	0.07	0.00	1.19

Abbreviation: THD, total harmonic distortion.

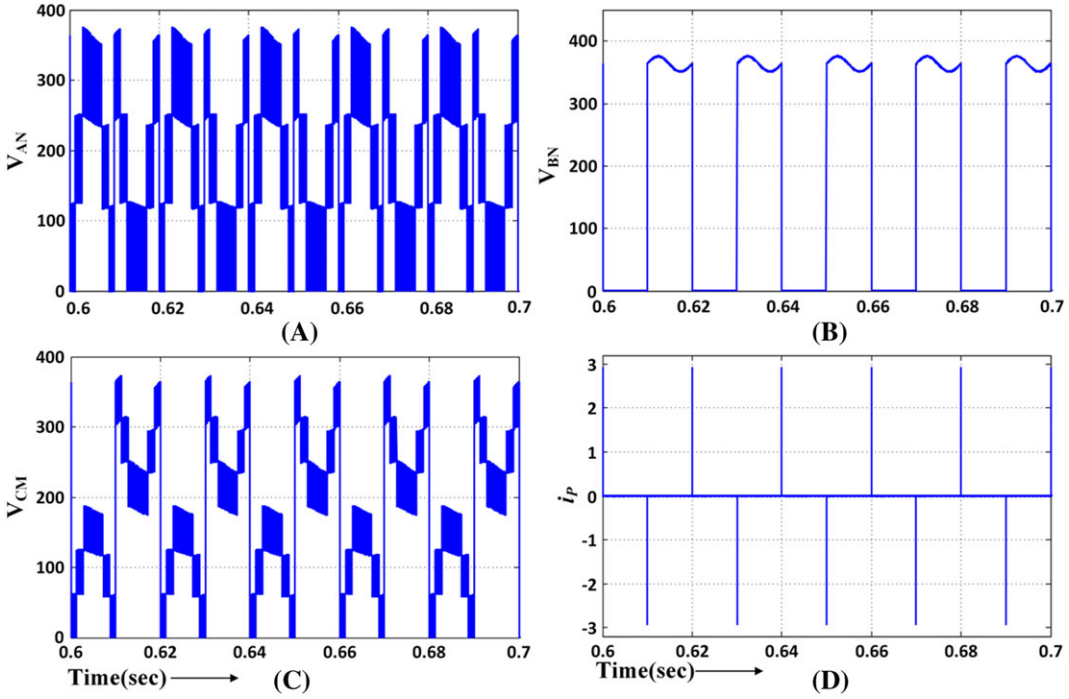

FIGURE 14 Simulation results of seven-level inverter: A, voltage V_{AN}; B, voltage V_{tcm} (=V_{BN}); C, common mode voltage (CMV); D, leakage current i_P [Colour figure can be viewed at wileyonlinelibrary.com]

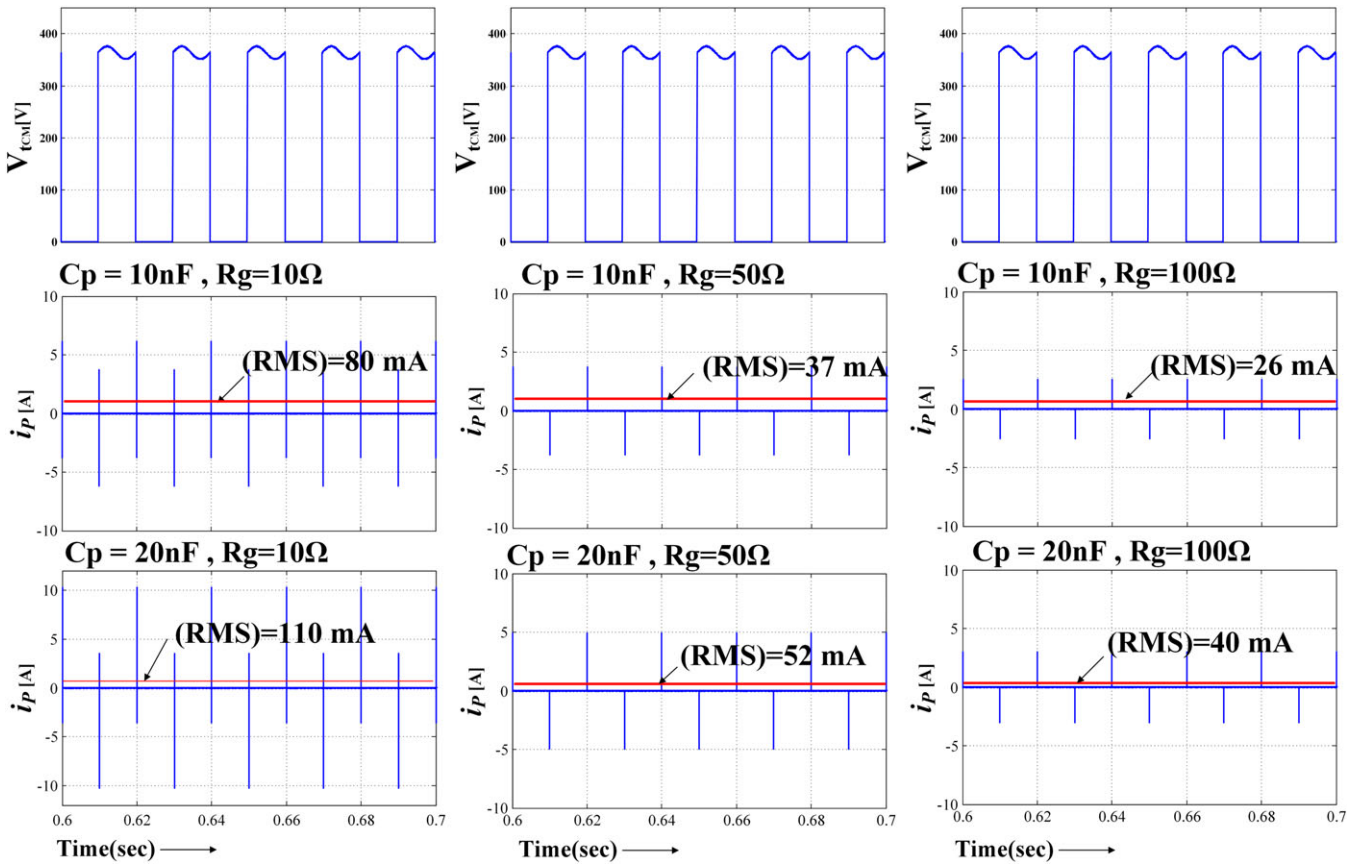

FIGURE 15 Total common mode voltage V_{tcm} (=V_{BN}) and leakage current i_P (ii) at three different parasitic capacitances and ground resistance conditions. RMS, root mean square [Colour figure can be viewed at wileyonlinelibrary.com]

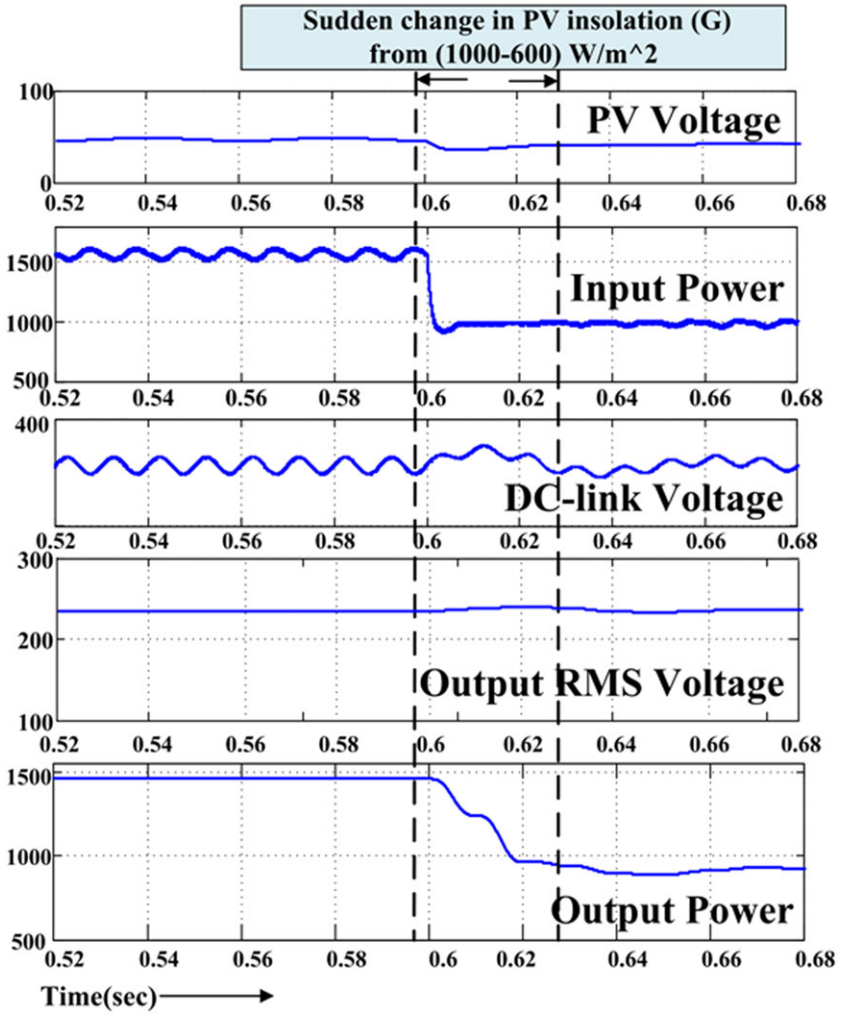

FIGURE 16 Voltage and power results of grid-connected two-stage inverter when insolation changes from 1000 to 600 W/m^2. PV, photovoltaic; RMS, root mean square [Colour figure can be viewed at wileyonlinelibrary.com]

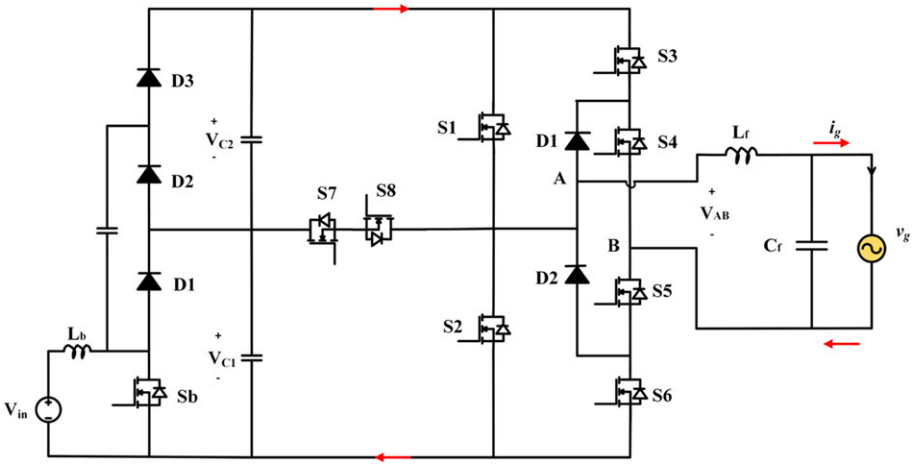

FIGURE 17 Proposed two-stage five-level inverter [Colour figure can be viewed at wileyonlinelibrary.com]

produce five-level output voltage as shown in Figure 18C. The filtered output voltage and their corresponding load current for unity power factor (UPF) operation are given in Figure 18D.

Further, to show the electromagnetic compatibility (EMC), the proposed two-stage system is tested using line impedance stabilization network (LISN) based on MIL-STD-461G standard.[30,31] Figure 19A and 19B depicts frequency versus conducted emission (CE) for both seven-level and five-level operations measured across the input of MLBC for same test

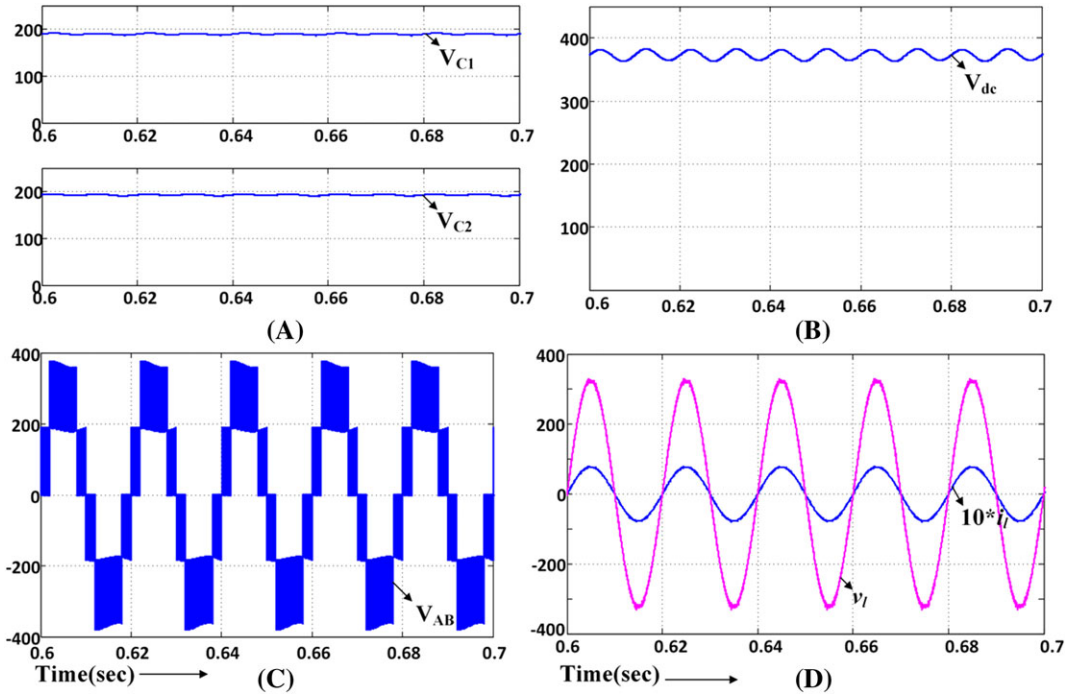

FIGURE 18 Simulation results of the proposed five-level inverter: A, DC capacitor voltages; B, DC-link voltage; C, five-level inverter voltage; D, output load voltage and current after the LC filter [Colour figure can be viewed at wileyonlinelibrary.com]

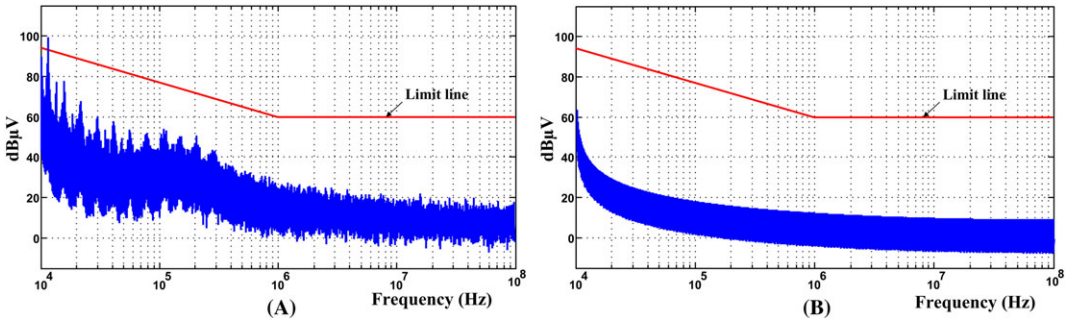

FIGURE 19 Conducted emission (CE) measurements at the input of multilevel boost converter (MLBC) for A, seven-level and B, five-level operations [Colour figure can be viewed at wileyonlinelibrary.com]

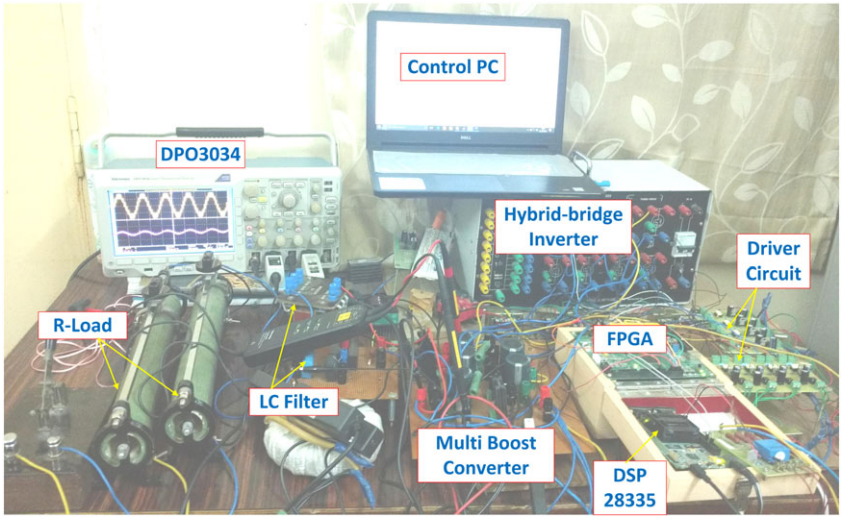

FIGURE 20 Experimental setup [Colour figure can be viewed at wileyonlinelibrary.com]

conditions. The measured CE is well below the limit line of MIL-STD-461G standard. Therefore, it is validated that CE of the proposed MLI is less than the standard of EMC.

8 | EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed two-stage system, a 200-W experimental prototype was built with available lab components as a proof of concept. Figure 20 shows the experimental prototype which consists of power circuits with switch IRF460, diode MUR1520, TLP250-based driver circuits, controllers, and loads. The PWM pulses to the MOSFET switches in the inverter are produced by DIGILENT ATLYS Spartan-6 FPGA board with $M_a = 0.84$. DSP TMS320F28335 is used for the generation of control pulse to the MOSFET used in MLBC.

The specifications of various components for the experiment are as follows: input DC voltage $V_{in} \approx 31$ V, switching frequency (f_s) as 20 kHz, duty ratio $D = 0.5$, boost inductor $L_b = 0.6$ mH (20% of ΔI_{in}), DC-link capacitors C1 = C2 = C3 = C4 = C5 ≈ 1000 μF (1% of ΔV_{dc}), $L_f = 1$ mH (20% of $\Delta i_{LP\text{-}P}$), $C_f = 3$ μF, $C_P = 20$ nF, and $R_g = 100$ Ω. The waveforms are captured using DPO 3034 with the help of differential voltage probe TMDP0200 and current probe TCP 0030. The experimental results for the proposed two-stage seven-level inverter are given in Figures 21–25. Figure 21 A depicts the input voltage, current, and drain-source voltage. It is observed that the input current is continuous in nature, which confirms that the MLBC is operating in CCM. The balanced DC-link voltages of the MLBC are depicted in Figure 21B.

The measured total DC-link voltage across the output of MLBC, seven-level output voltage, filtered output voltage, and load current are shown in Figure 22A and 22B, respectively. Figure 22C and 22D shows the waveforms of seven-level inverter under 0.58 lagging load and 0.58 leading load conditions. This shows that the proposed configuration is capable of controlling the reactive power without affecting the common mode voltage behavior and multilevel output quality. Further, the dynamic response of the proposed MLI is shown in Figure 23A-C. Here, the currents in Figure 23A and 23B are multiplied by a factor of three to better visualize the response.

Figure 23A and 23B shows the dynamic response of the proposed system under step change in load from 350 to 150 Ω and vice versa. Similarly, it can be noticed that from Figure 23C, the DC-link voltage is kept constant as the input DC voltage changes from 25 to 35 V and then to 30 V. It shows that the proposed two-stage system and its modulation scheme can effectively feed power into grid under temperature and insolation changes of the PV source.

Figure 24A shows the waveforms of the inverter terminal voltage V_{AN}, V_{BN}, and V_{CM}. Figure 24B shows the voltage waveform across the input DC source positive terminal to ground and corresponding leakage current flowing through the parasitic capacitor. It can be observed that the voltage across parasitic capacitor C_P varies at grid frequency. Consequently, the leakage current consists of sudden spikes when there is transition of voltage V_{Ng} from zero to V_{dc} as explained in Section 5. The RMS value of i_P reaches 7.146 mA, which is well below 300-mA limit imposed by German DIN VDE 0126-1-1 grid standards. The experimental performance of the proposed system shows the absence of high frequency transitions in the CMV. Therefore, the leakage current i_P is significantly reduced. In addition, the experimental THD of the proposed configuration is measured using DPO 3034 and YOKOGAWT310E digital power meter, shown in Figure 25A and 25B. It is observed that the filtered output voltage and their corresponding load current THD of 1.45% show good agreement with the simulation results and also meet IEEE1547 grid standards.

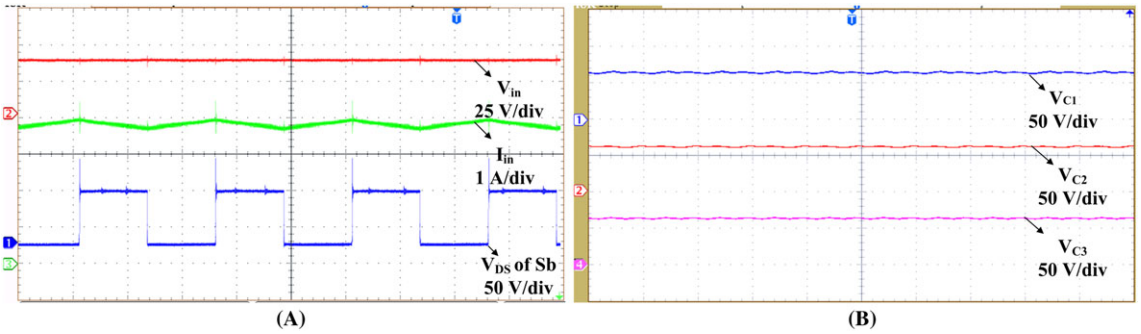

FIGURE 21 Experimental results of the multilevel boost converter (MLBC): A, input voltage, current, and drain source voltage of Sb; B, balanced DC-link voltages [Colour figure can be viewed at wileyonlinelibrary.com]

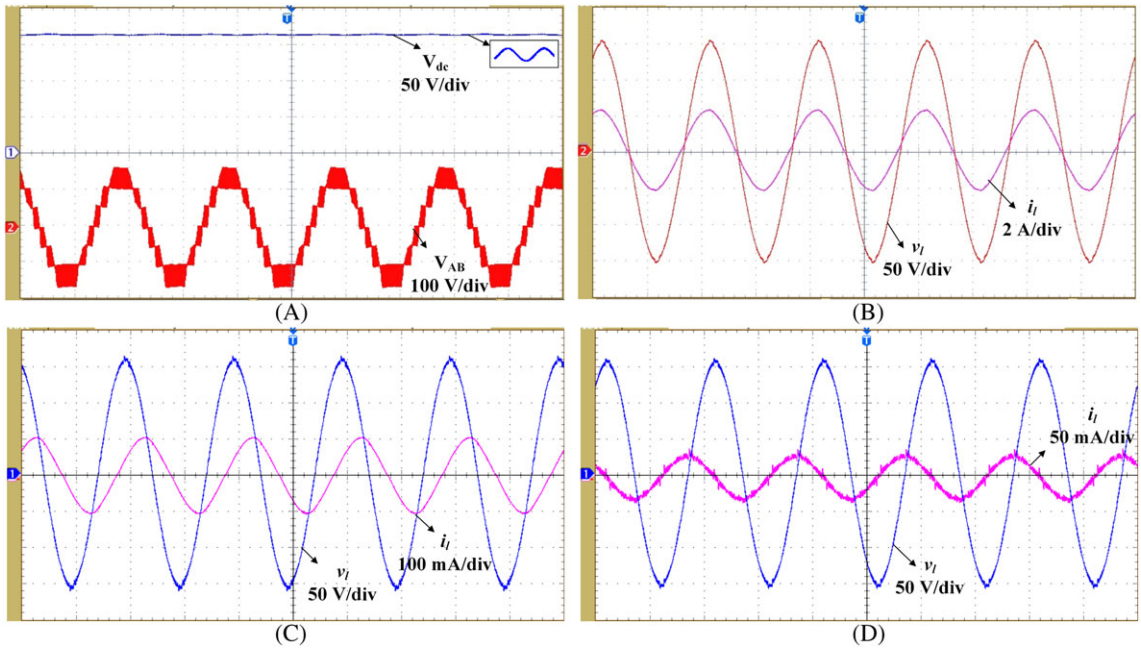

FIGURE 22 Experimental results of the proposed topology: A, total DC-link voltage and seven-level voltage; load voltage and current under B, UPF, C, 0.58 lagging, and D, 0.58 leading conditions, respectively [Colour figure can be viewed at wileyonlinelibrary.com]

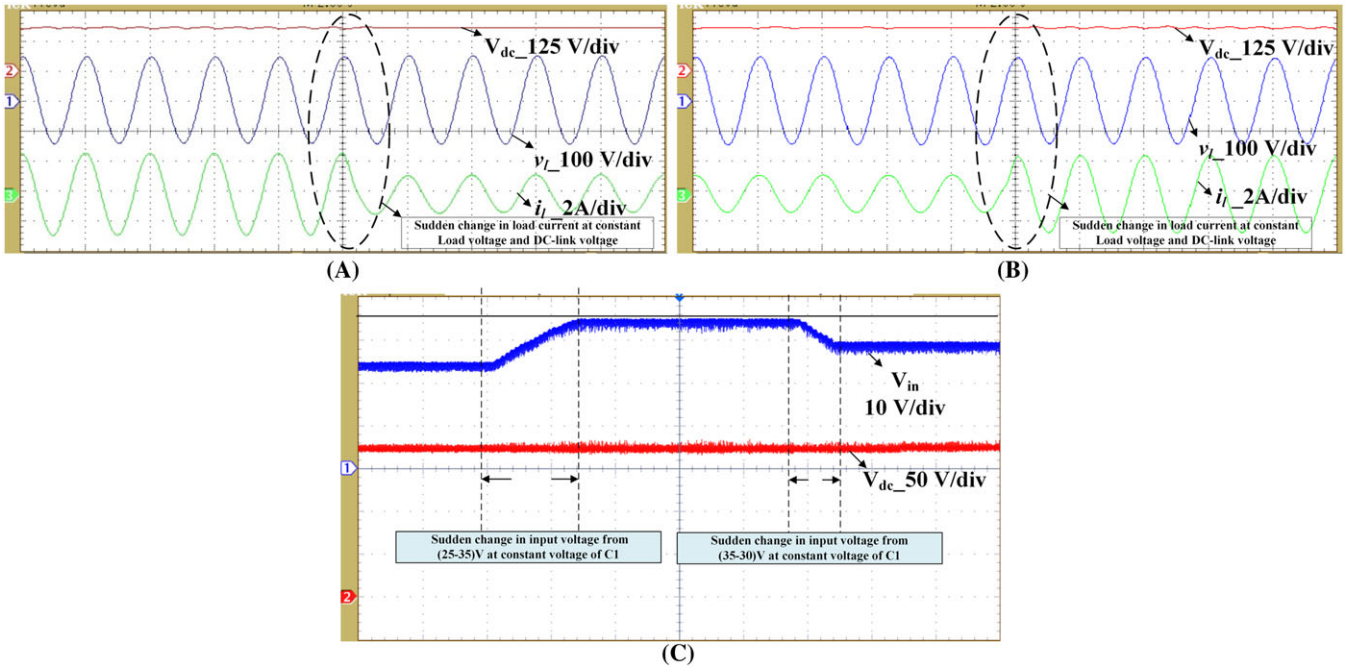

FIGURE 23 Experimental results of the proposed topology: A,B, step change in load current from high to low and low to high at constant output voltage; C, transient voltage variations in input voltage and their corresponding DC-link voltage [Colour figure can be viewed at wileyonlinelibrary.com]

To verify the modularity feature of proposed configuration, the experimental prototype is restructured for generation of five-level operation. Figure 26 shows the experimental results of the five-level inverter under UPF operation. The measured DC-link voltage across the output of MLBC, five-level inverter output voltage, and filtered output voltage and their corresponding load current, respectively, are shown in Figure 26A and 26B. From these, the experimental results are found to be in good agreement with the simulation results. The CMV and leakage current justify that the proposed transformerless hybrid PV inverter is well suited for grid-connected PV applications.

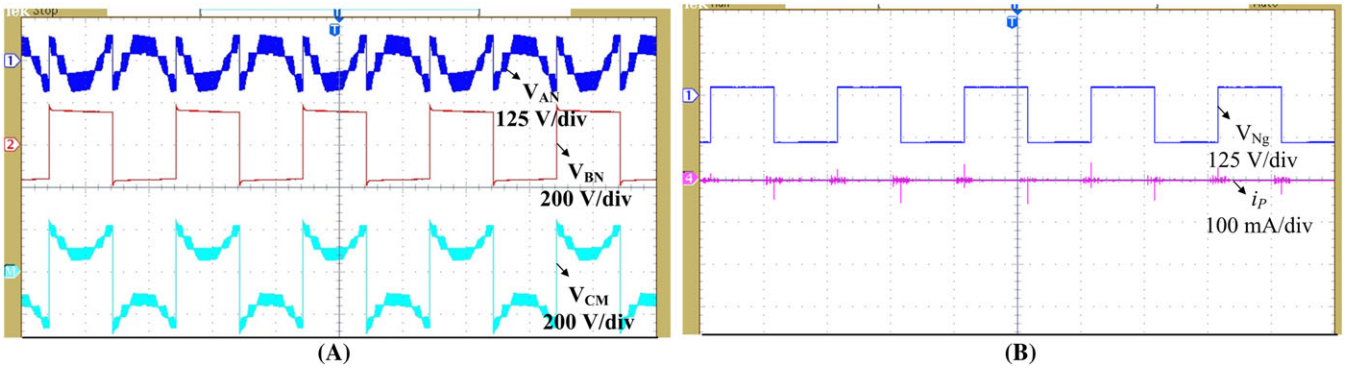

FIGURE 24 Experimental results of the proposed topology: A, terminal voltages of V_{AN}, V_{BN}, and V_{CM} and B, terminal voltage across DC source to ground V_{Ng} and corresponding leakage current [Colour figure can be viewed at wileyonlinelibrary.com]

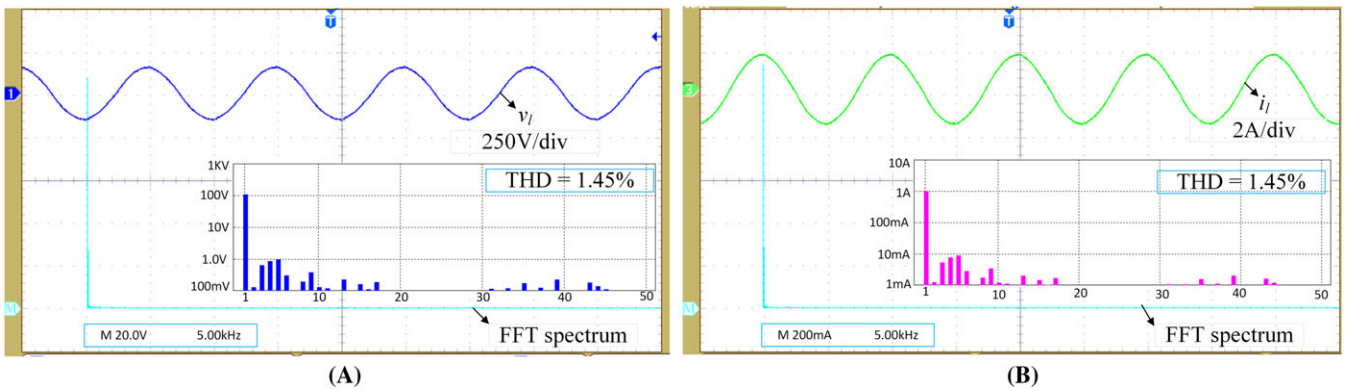

FIGURE 25 Experimental FFT spectrums for the proposed seven-level multilevel inverter (MLI). A, Load voltage. B, Load current. THD, total harmonic distortion [Colour figure can be viewed at wileyonlinelibrary.com]

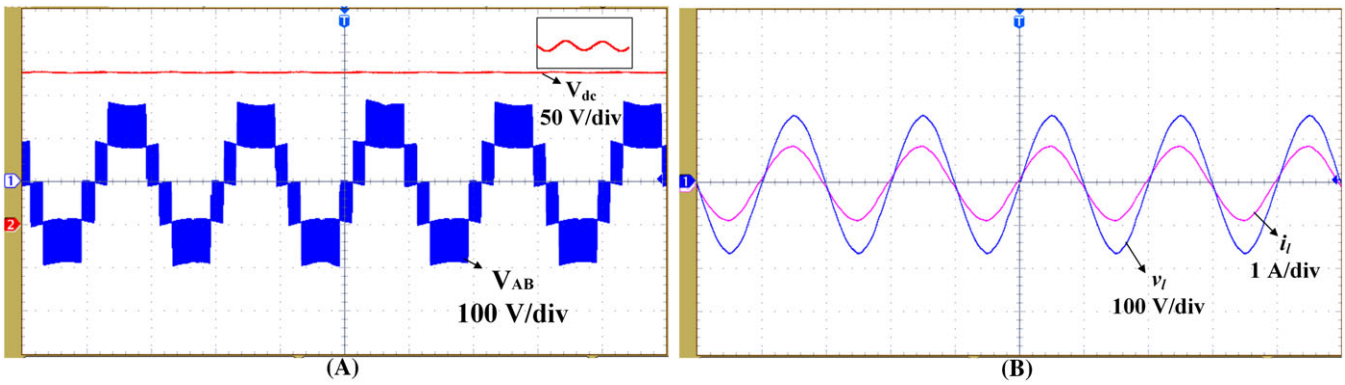

FIGURE 26 Experimental results of the proposed two-stage five-level inverter. A, DC-link and level voltage. B, Filtered output voltage and current waveforms under unity power factor (UPF) [Colour figure can be viewed at wileyonlinelibrary.com]

9 | COMPARISON WITH EXISTING TOPOLOGIES

In this section, a comparison of the two-stage topologies with the proposed system is given to highlight its merits. From Table 3, it can be noticed that the boosting factor of the proposed two-stage system is double without using HFT and extreme duty ratio. Hence, it requires fewer number of PV panels connected in series to maintain required DC-link voltage which improves the performance of MPPT and also efficiency. Moreover, the modular structure of the topology enables an increase in the number of levels in output voltage, which leads to an enhancement in the quality of output power with reduced filter size. Furthermore, the magnitude of leakage current is limited below the DIN VDE 0126-1-1

TABLE 3 Comparison of various two-stage configurations

Part Name	Wu and Chu16	Wu et al17	Manoharan et al18	Proposed
MOSFET	8	10	9	11
Diode	5	3	3	7
HFT	1	1	1	...
Capacitor	2	2	2	5
Boosting factor	$1.5kV_{in}$	$1.5kV_{in}$	$1.5kV_{in}$	$3kV_{in}$
Modularity	...	...	...	Yes
Leakage current	...	...	...	<300 mA
LFT or EMC filter	Yes	Yes	Yes	...
Voltage stress of MOSFET	$6V_{dc}$	$7V_{dc}$	$4.58V_{dc}$	$8.33V_{dc}$
Blocking voltage of diode	$2.33V_{dc}$	$2.33V_{dc}$	$1.08V_{dc}$	$3.33V_{dc}$
Reactive power possibility	No	Yes*	Yes*	Yes

Abbreviations: EMC, electromagnetic compatibility; HFT, high frequency transformer; LFT, line frequency transformer.

$k = 1/(1 - D)$. Yes*, possible with modified switching logic.

TABLE 4 Comparison of the proposed topology with conventional MLI topologies

Part Name		DC	FC	CHB	Proposed
MOSFET		12	12	12	10
Diodes		30	0	0	2
Capacitors	DC link	6	6	3	3
	Auxiliary	0	15	0	0
DC sources		1	1	3	1

Abbreviations: CHB, cascaded H-bridge; DC, diode clamped; FC, flying capacitor; MLI, multilevel inverter.

grid standard without employing LFT or EMC filter, which increases the efficiency and reduces the size of the overall two-stage system. Finally, reactive power capability is achieved with circuit structure and with modified SLS-PWM. But the limitation of the proposed system is an increase in the number of components used. However, the overall performance of the proposed two-stage system is better than the existing topologies in the previous studies.[16-18]

In Table 4, a comparison of conventional seven-level inverters with the proposed hybrid inverter is given in the previous studies.[12,13] The total number of active and passive components and DC sources required for the realization of seven-level output is fewer in comparison with conventional MLIs. Hence, the cost and size of the proposed inverter are lower.

10 | EFFICIENCY

Generally, losses in the semiconductor devices depend on the conduction period and the corresponding blocking voltage. Selection of switches is based on the blocking voltage with lower on-state resistance that enhances the overall

TABLE 5 Parameters and devices used for the calculation of efficiency

Parameter	v_O	f	f_s	L_b	D	M_a	L_f	C_f	C1-C5	C_P
Value	230 V	50 Hz	20 kHz	0.5 mH	0.5	0.84	1 mH	4 μF	1300 μF	20 nF
Device	S1 to S6		S8 and S9		S7, S10, and Sb			Diodes		
Part number	FCA76N60N		IRF300P227		IRFP4127PbF			RUR1S1560S		
Rating	400 V/76 A		300 V/50 A		250 V/75 A			600 V/15 A		

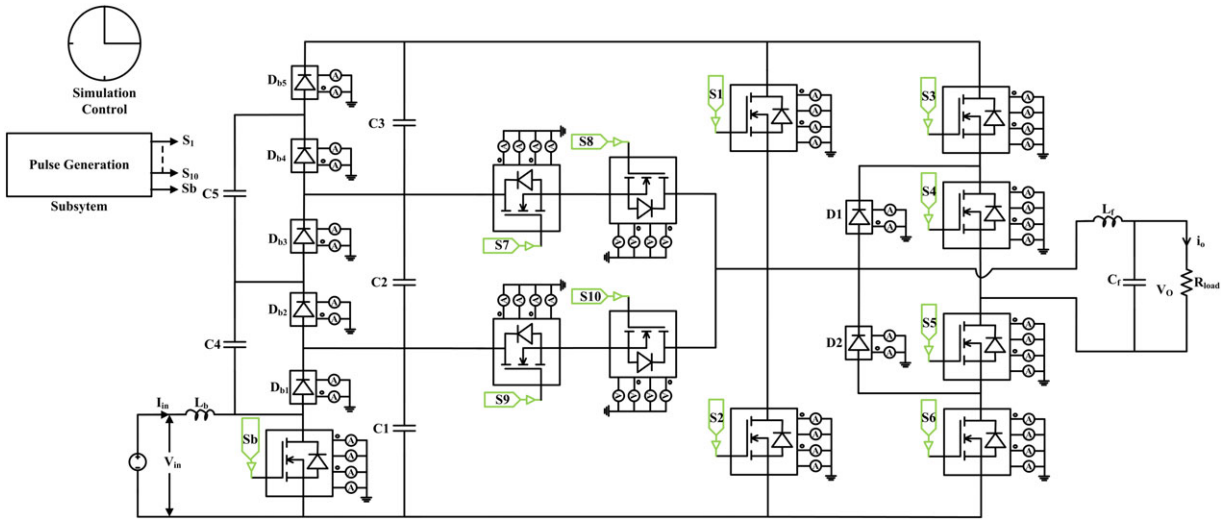

FIGURE 27 PSIM thermal module model for the proposed two-stage seven-level multilevel inverter (MLI) [Colour figure can be viewed at wileyonlinelibrary.com]

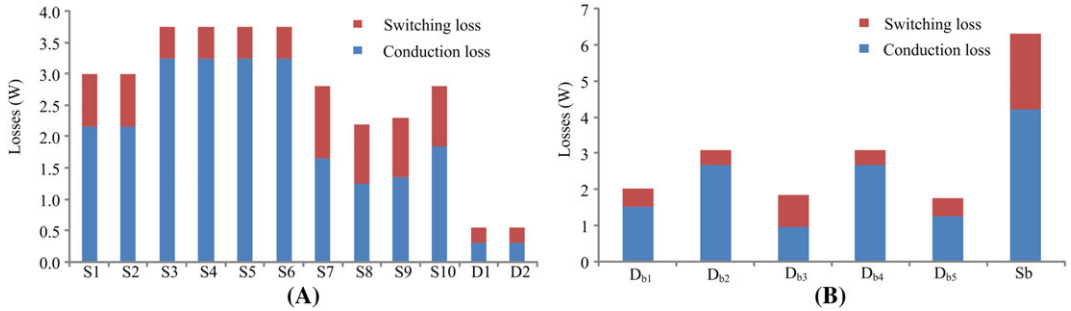

FIGURE 28 Distribution of power losses in the semiconductor switches of A, Hybrid seven-level inverter and B, multilevel boost converter [Colour figure can be viewed at wileyonlinelibrary.com]

efficiency of the system. Table 5 lists the various parameters, switches and diodes, and their corresponding part number used for the calculation of efficiency in both theoretical and PSIM studies. The theoretical evaluation of losses is carried out using the standard equations given in the previous studies.[32,33] In order to validate the losses, PSIM thermal module is implemented for the proposed configuration with the real parts as datasheets.[34,35]

Figure 27 illustrates the developed two-stage configuration of PSIM thermal module. Distribution of losses due to various switches and diode using PSIM is drawn in Figure 28. It is observed that the switching losses are reduced

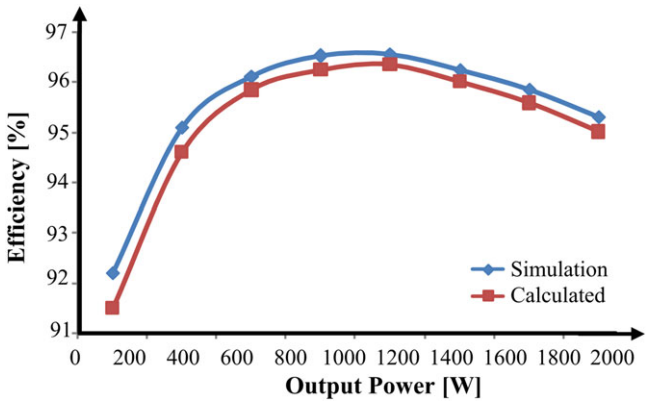

FIGURE 29 Efficiency curve [Colour figure can be viewed at wileyonlinelibrary.com]

considerably in comparison with conduction losses. Switches S3, S4, S5, and S6 operate almost close to grid frequency, and the blocking voltage is V_{dc}; thereby, the losses are equal. The clamping diodes used in the NPC leg conduct only in the freewheeling period; hence, the losses are very low. Losses across switches S1 and S2 are equal because the blocking voltage and operating frequency are same. The bidirectional switches S7 and S8 are operating at different frequencies and blocking voltages. For example, switch S7 blocks voltage of $(2/3)V_{dc}$ and switch S8 blocks voltage of $(1/3)V_{dc}$, and also, they are operating at different frequencies. Therefore, the losses in the bidirectional branch switches are different in the proposed inverter. The power loss in the boost converter switch Sb and diodes (D_{b1}-D_{b5}) is shown in Figure 28B. Finally, from Figure 29, it can be concluded that the efficiency of both the theoretical and the PSIM simulation matches so well that it validates the performance of the developed system.

11 | CONCLUSION

A single-phase two-stage hybrid MLI for grid-connected PV applications is presented. The self-balanced capacitor voltage capability of the MLBC enables low control complexity and modularity for any level output of DC and also provides high boosting gain. The proposed MLI structure and its modulation technique provide the bidirectional path to the current in all modes of operation. In addition, reactive power control is also possible without affecting common mode voltage behavior and the output levels in the MLI. The leakage current is within the limits of German DIN VDE 0126-1-1 grid standards due to grid frequency variations in total CMV. Thus, the proposed two-stage system provides high-quality output power and efficiency. The performance of the proposed two-stage system is validated by constructing a 200-W experimental prototype.

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