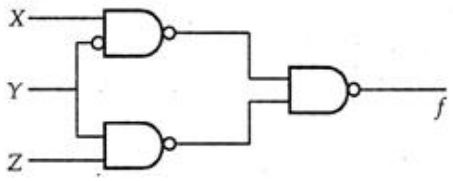
DIGITAL LOGIC

SOLUTIONS

1. Consider the following circuit:



Which one of the following is TRUE?

(a) f is independent of X
(b) f is independent of Y
(c) f is independent of Z
(d) None of X, Y, Z is redundant

Solution: Option (a)

2. Consider numbers represented in 4-bit gray code. Let $h_3h_2h_1h_0$ be the gray code representation of a number n and let $g_3g_2g_1g_0$ be the gray code of (n + 1) (modulo 16) value of the number. Which one of the following functions is correct?

(a) $g_0 (h_3,h_2, h_1, h_0) = \Sigma (1, 2, 3, 6, 10, 13, 14, 15)$
(b) $g_1 (h_3,h_2, h_1, h_0) = \Sigma (4, 9, 10, 11, 12, 13, 14, 15)$
(c) $g_2 (h_3,h_2, h_1, h_0) = \Sigma (2, 4, 5, 6, 7, 12, 13, 15)$
(d) $g_3 (h_3,h_2, h_1, h_0) = \Sigma (0, 1, 6, 7, 10, 11, 12, 13)$

Solution: Option (c)

3. We consider the addition of two 2's complement numbers $b_{n-1}b_{n-2}\ldots b_0$ and $a_{n-1}a_{n-2}\ldots a_0$. A binary adder for adding unsigned binary numbers is used to add the two numbers. The sum is denoted by $c_{n-1}c_{n-2}\ldots c_0$ and the carry-out by c_{out}. Which one of the following options correctly identifies the overflow condition?

(a) $c_{out}\overline{(a_{n-1} \oplus b_{n-1}}$
(b) $a_{n-1}b_{n-1}\overline{c_{n-1}} + \overline{a_{n-1}b_{n-1}c_{n-1}}$
(c) $\overline{c_{out} \oplus c_{n-1}}$
(d) $\overline{a_{n-1} \oplus b_{n-1} \oplus c_{n-1}}$

Solution: Option (b)

4. Consider a Boolean function f (w, x, y, z). suppose that exactly one of its inputs is allowed to change at a time. If the function happens to be true for two input vectors $i_1 = (w_1, x_1, y_1, z_1)$ and $i_2 = (w_2, x_2, y_2, z_2)$ we would like the function to remain true as the input changes from i_1 to i_2 (i_1 and i_2 differ in exactly one bit position), without becoming false momentarily.

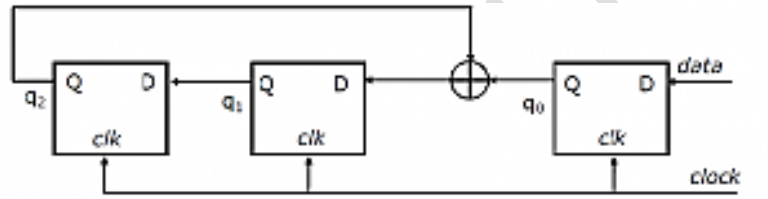
Let f (w, x, y, z) = ∑(5,7,11,12,13,15).

Which of the following cube covers of f will ensure that the required property is satisfied?

(a) w'xz, wxy', xy'z, xyz,wyz
(b) wxy,w'xz,wyz
(c) wx(yz)', xz, wx'yz
(d) wzy, wyz, wxz, w'xz, xy'z, xyz

Solution: Option (a)

5. Consider the circuit in the diagram. The ⊕ operator represents Ex-OR. The D flipflops are initialized to zeroes (cleared).



The following data: 100110000 is supplied to the "data" terminal in nine clock cycles. After that the values of $q_2q_1q_0$ are:

(a) 000
(b) 001
(c) 010
(d) 101

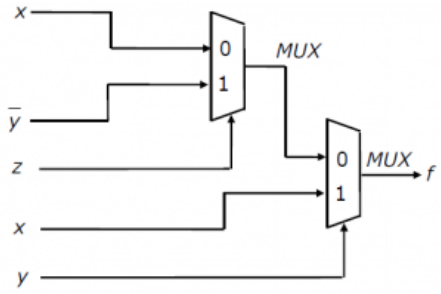
Solution: Option (c)

6. Given two three bit numbers $a_2a_1a_0$ and $b_2b_1b_0$ and c, the carry in, the function that represents the carry generate function when these two numbers are added is:

(a) $a_2b_2 + a_2a_1b_1 + a_2a_1a_0b_0 + a_2a_0b_1b_0 + a_1b_2b_1 + a_2a_0b_2b_0 + a_0b_2b_1b_0$
(b) $a_2b_2 + a_2b_1b_0 + a_2a_1b_1b_0 + a_1a_0b_2b_1 + a_1a_0b_2 + a_1a_0b_2b_0 + a_2a_0b_2b_0$
(c) $a_2 + b_2 + (a_2 \oplus b_2)\ (a_1 + b_1 + (a_1 \oplus b_1)(a_0 + b_0))$
(d) $a_2b_2 + \overline{a_2}a_1b_1 + \overline{a_2a_1}a_0b_0 + \overline{a_2}a_0\overline{b_1}b_0 + a_1\overline{b_2}b_1 + \overline{a_1}a_0\overline{b_2}b_0 + a_0\overline{b_2b_1}b_0$

Solution: Option (a)

7.



Consider the circuit above. Which one of the following options correctly represents f (x, y, z)?

(a) xz' + xy + y'z
(b) xz' + xy + (yz)'
(c) xz + xy + (yz)'
(d) xz + xy' + y'z

Solution: Option (a)

8. Let X denote the Exclusive OR (XOR) operation. Let '1' and '0' denote the binary constants. Consider the following Boolean expression for F over two variables P and Q:

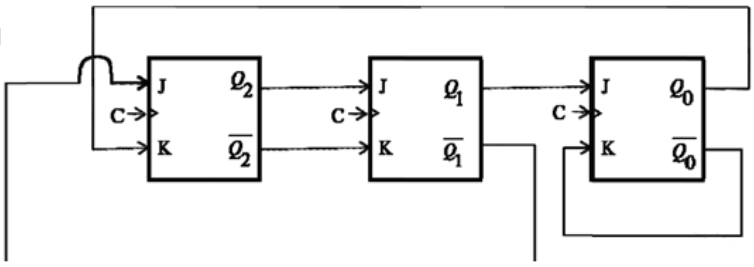
$$F(P, Q) = ((1 \times P) \times (P \times Q)) \times ((P \times Q) \times (Q \times 0))$$

The equivalent expression for F is

(a) P + Q
(b) (P + Q)'
(c) P × Q
(d) (P × Q)'

Solution: Option (d)

9.



The above sequential circuit is built using JK flip-flops is initialized with $Q_2Q_1Q_0 = 000$. The state sequence for this circuit for the next 3 clock cycle is

(a) 001, 010, 011
(b) 111, 110, 101
(c) 100, 110, 111
(d) 100, 011, 001

Solution: Option (c)

10. Consider the following combinational function block involving four Boolean variables x, y, a, b where x, a, b are inputs and y is the output.

```
f (x, y, a, b)
{
  if (x is 1) y = a;
  else y = b;
}
```

Which one of the following digital logic blocks is the most suitable for implementing this function?

(a) Full adder
(b) Priority encoder
(c) Multiplexor
(d) Flip-flop

Solution: Option (c)

11. Consider the following minterm expression for F:

$$F(P, Q, R, S) = \sum 0, 2, 5, 7, 8, 10, 13, 15$$

The minterms 2, 7, 8 and 13 are 'do not care' terms. The minimal sum-of-products form for F is

(a) $Q\overline{S} + \bar{Q}S$
(b) $\bar{Q}\bar{S} + QS$
(c) $\bar{Q}\bar{R}\bar{S} + \bar{Q}R\bar{S} + Q\bar{R}S + QRS$
(d) $\bar{P}\bar{Q}\bar{S} + \bar{P}QS + PQS + P\bar{Q}\bar{S}$

Solution: Option (b)

12. Consider the equation (123)5 = (x8)y with x and y as unknown. The number of possible solutions is _____.

(a) 1
(b) 2
(c) 3
(d) 4

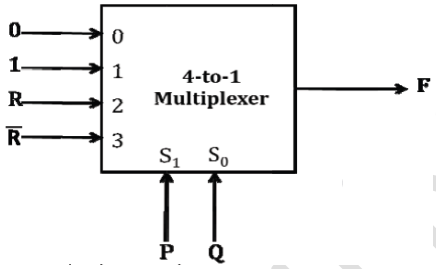
Solution: Option (c)

13. Let $k = 2^n$. A circuit is built by giving the output of an n-bit binary counter as input to an n-to-2^n bit decoder. This circuit is equivalent to a

(a) k-bit binary up counter.
(b) k-bit binary down counter.
(c) k-bit ring counter.
(d) k-bit Johnson counter.

Solution: Option (c)

14. Consider a 4-to-1 multiplexer with two select lines S_1 and S_0, given below



The minimal sum-of-products form of the Boolean expression for the output F of the multiplexer is

(a) P'Q + QR' + PQ'R
(b) P'Q + P'QR' + PQR' + PQ'R
(c) P'QR + P'QR' + QR' + PQ'R
(d) PQR'

Solution: Option (a)

15. Consider the following Boolean expression for F:

$$F(P, Q, R, S) = PQ + \bar{P}QR + \bar{P}Q\bar{R}S$$

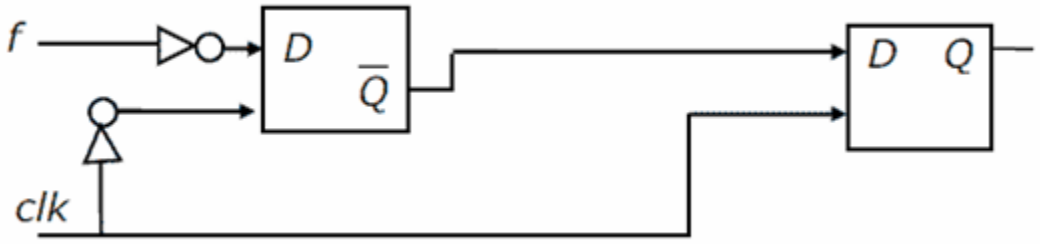
The minimal sum-of-products form of F is

(a) PQ + QR + QS
(b) P + Q + R + S
(c) $\bar{P} + \bar{Q} + \bar{R} + \bar{S}$
(d) $\bar{P}R + \bar{P}\bar{R}S + P$

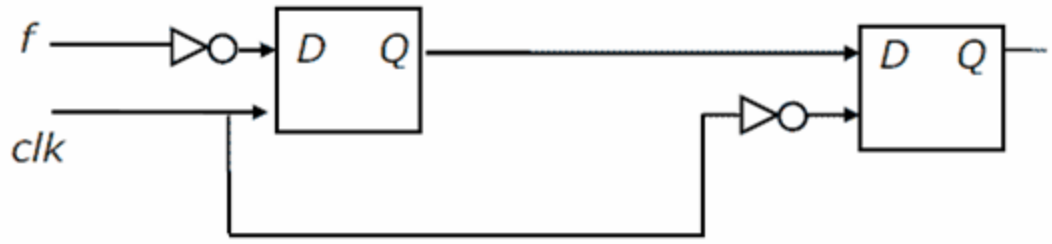
Solution: Option (a)

16. You are given a free running clock with a duty cycle of 50% and a digital waveform f which changes only at the negative edge of the clock. Which one of the following circuits (using clocked D flip-flops) will delay the phase of f by 180°?

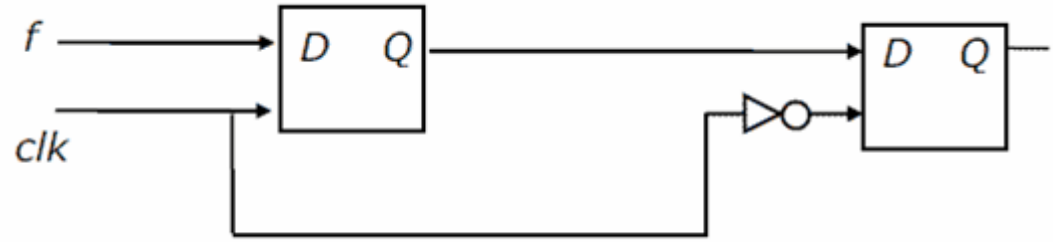
(a)



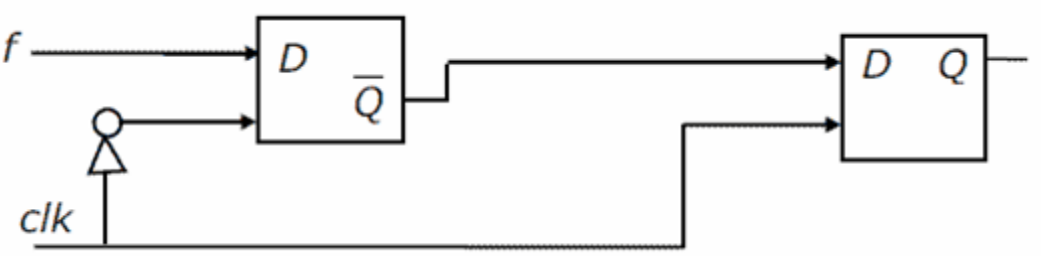
(b)



(c)



(d)



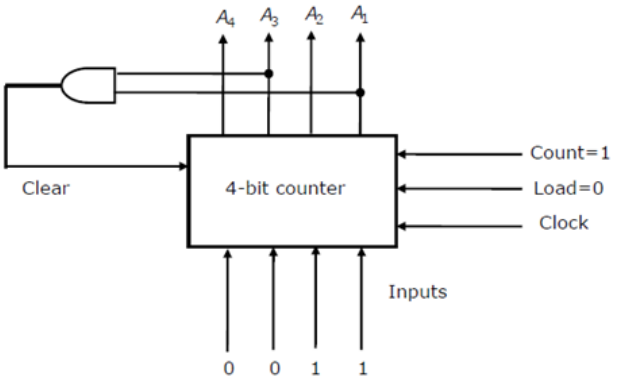
Solution: Option (c)

17. The control signal functions of a 4-bit binary counter are given below (where X is "don't care")

The counter is connected as follows:

Clear	Clock	Load	Count	Function
1	X	X	X	Clear to 0
0	X	0	0	No change
0	↑	1	X	Load input
0	↑	0	1	Count next

The counter is connected as follows:



Assume that the counter and gate delays are negligible. If the counter starts at 0, then it cycles through the following sequence:

(a) 0, 3, 4
(b) 0, 3, 4, 5
(c) 0, 1, 2, 3, 4
(d) 0, 1, 2, 3, 4, 5

Solution: Option (c)

18. In a look-ahead carry generator, the carry generate function G_i and the carry propagate function P_i for inputs A_i and B_i are given by:

$$P_i = A_i \oplus B_i \text{ and } G_i = A_i B_i$$

The expressions for the sum bit S_i and the carry bit C_{i+1} of the look-ahead carry adder are given by:

$$S_i = P_i \oplus C_i \text{ and } C_{i+1} = G_i + P_i C_i \text{ , where } C_0 \text{ is the input carry.}$$

Consider a two-level logic implementation of the look-ahead carry generator. Assume that all P_i and G_i are available for the carry generator circuit and that the AND and OR gates can have any number of inputs. The number of AND gates and OR gates needed to implement the look-ahead carry generator for a 4-bit adder with S_3, S_2, S_1, S_0 and C_4 as its outputs are respectively:

(a) 6, 3
(b) 10, 4
(c) 6, 4
(d) 10, 5

Solution: Option (b)

19. Suppose only one multiplexer and one inverter are allowed to be used to implement any Boolean function of n variables. What is the minimum size of the multiplexer needed?

(a) 2^n line to 1 line
(b) 2^{n+1} line to 1 line
(c) 2^{n-1} line to 1 line
(d) 2^{n-2} line to 1 line

Solution: Option (c)

20. Define the connective * for the Boolean variables X and Y as:

X * Y = XY + X' Y'. Let Z = X * Y.

Consider the following expressions P, Q and R:

P: X = Y*Z
Q: Y = X*Z
R: X*Y*Z=1

Which of the following is TRUE?

(a) Only P and Q are valid.
(b) Only Q and R are valid.
(c) Only P and R are valid.
(d) All P, Q, R are valid.

Solution: Option (d)