COMPUTER ORGANIZATION

(CPU Control Design, Memory Interface, I/O Interface)

SOLUTIONS

1. Consider a logical address space of 8 pages of 512 words each mapped onto a physical memory of 64 frames. How many bits are there in physical address?

Solution: From 15.45 To 14.55

2. How many cycles are required for a 100 MHz processor to execute a program which requires 5 seconds of CPU time?

(a) 10^9 cycles
(b) 50×10^7 cycles
(c) 10^8 cycles
(d) 50 cycles

Solution: Option (b)

Explanation:

$$\text{Cycle time} = \frac{10^9}{100 \times 10^6} = 10 \text{ ns;} \quad \text{Number of cycles} = \frac{5 \times 10^9}{10} = 50 \times 10^7 \text{cycles}$$

3. Arrange the following configurations for CPU in decreasing order of operating speeds.

1. Hard wired control
2. Vertical microprogramming
3. Horizontal microprogramming

(a) 1 > 2 > 3
(b) 1 > 3 > 2
(c) 2 > 3 > 1
(d) 3 > 2 > 1

Solution: Option (b)

Explanation:

Micro programmed control unit uses microinstructions, for generating control signals.

4. A = 1111 1010, B = 0000 1010 be two 8-bit 2's complement numbers. Their product in 2's complement is

(a) 1100 0100
(b) 1001 1100
(c) 1010 0101
(d) 1101 0101

Solution: Option (a)

Explanation:

$-6 \times 10 = -60$
It can be represented in 2's complement as 11000100

5. Main difference between CISC and RISC is

(a) RISC has few instructions
(b) RISC has few addressing modes
(c) CISC is having fewer registers
(d) Both (a) & (b)

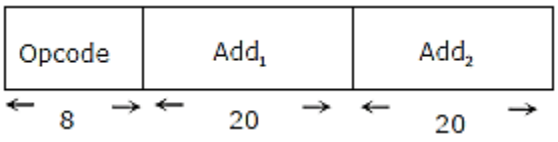
Solution: Option (d)

6. A computer supports one address and two address instructions. All the Addresses are the memory addresses. Memory size is 1Mbyte. How many one address instructions are possible if it has 240 two addresses instructions? (Assume binary instructions code has 48 bits)

(a) $\frac{2^{20}}{16}$
(b) 16×2^{20}
(c) $2^{28} - 256$
(d) None of these

Solution: Option (b)

Explanation:



$2^8 = 256$; One Address = $(256 - 240) \times 2^{20} = 16 \times 2^{20}$

7. An interrupt program takes one cycle for every instruction. A DMA takes 15 cycles for initialization and 2 cycles for each Byte to transfer; what is the speed up of DMA over interrupt

program of 5 instructions for the transfer of 100 Bytes? (Interrupt program must be executed for every byte)

Solution: From 2.369 To 2.231

Explanation:

$\text{DMA} = 15 + 100 \times 2 = 215$

$\text{Intrpt} = (1 \times 5) \times 100 = 500; \quad \text{Speed up} = \frac{500}{215} \approx 2.3$

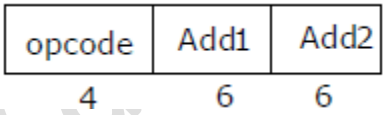
8. How many separate address and data lines are needed for a memory of 8K × 16?

(a) 13 address, 3 data lines
(b) 13 address, 16 data lines
(c) 12 address, 4 data lines
(d) 13 address, 4 data lines

Solution: Option (b)

Explanation:

$\text{Memory size} = 8\text{K} \times 16 = 2^{13} \times 16. \quad \text{So, address line} = 13, \text{data line} = 16$



$(2^4 - 4) \times 2^6 = 12 \times 64 = 768$

9. A system supports 1-address and 2-address instructions. If the instruction length is 16-bits and memory is having 64 words, how many 1-address instructions exists if there are '8' 2-address instructions?

Solution: From 527.36 To 496.64

Explanation:

Total number of 1-address instructions is $(2^4 - 8) * 2^6 = 512$

10. What is the average memory access time for a 3 level memory system where $T_2 = 2T_1$ and $T_3 = 3T_1$ and hit ratios $h_1 = h_2 = 0.9$. [T_i is effective access time]

(a) $1.11T_1$ (b) $1.22T_1$
(c) $1.09T_1$ (d) $1.01T_1$

Solution: Option (a)

Explanation:

$$0.9[T_1] + 0.1\left[0.9[2T_1] + 0.1[3T_1]\right] = 1.11T_1$$