COMPUTER ORGANIZATION AND ARCHITECTURE

SOLUTIONS

1. Consider the following statements.

S1: The RISC processor has CPI always 1.
S2: In horizontal instruction control signals are always in encoded form.
S3: In vertical instruction control signals are always in encoded form.
S4: In terms of speed vertical instruction is slower than horizontal instruction.

Which of the above statements are true?

(a) Only S1 and S2
(b) Only S2 and S3
(c) Only S1, S3 and S4
(d) None of the above

Solution: Option (c)

Explanation:

(c)

S1 is true property of RISC architecture.
S2 is false, horizontal instruction control signals are always in decoded form.
S3 is true, vertical instruction control signals are always in encoded form.
S4 speed of vertical instruction is less than horizontal instruction.
[Encoded control signals need to be decoded first and then they are interpreted]

2. Computer uses addressing mode technique for _____.

(a) giving program versatility to user by providing facilities as a pointer to memory counters for loop control
(b) reducing number of bits in the field of instruction
(c) specifying rules for modifying or interpreting address field of the instruction
(d) All of the above

Solution: Option (d)

Explanation:

(d)

Computer uses addressing mode technique for giving program versatility to user by providing facilities as a pointer to memory counters for loop control and to reduce number of bits in the field of instruction. Addressing modes are used in specifying rules for modifying or interpreting address field of the instruction.

So, all options are correct.

3. Which of the following is added to the page table in order to track whether a page of cache has been modified since it was read from the memory?

(a) Reference bit
(b) Dirty bit
(c) Tag bit
(d) Valid bit

Solution: Option (b)

Explanation:

(b)

Dirty bit is used to represent the status of cache whether it has been defined after copying from main memory to cache. Dirty bit = 0 shows no modification and dirty bit = 1 shows modification.

4. Match List-I with List-II and select the correct answer using the codes given below the lists:

List-I	**List-II**
A. Pointer	1. Indirect addressing mode
B. Position independent code	2. Immediate addressing mode
C. Constant operand	3. Relative addressing mode

Codes:

	A	**B**	**C**
(a)	1	2	3
(b)	3	2	1
(c)	1	3	2
(d)	2	3	1

Solution: Option (c)

Explanation:

(c)

For making use of pointer in programs, indirect addressing mode is used.

Pointer stores the address of a variable and indirect addressing mode stores address of effective address in instruction.

Position independent code makes use of relocation concept which is implemented by the use of relative addressing mode which uses relocation register to set the difference of logical and physical address.

Immediate addressing mode provides the value directly in the instruction which is suitable to be used for constant operands of the program.

5. A 50 kbps device is connected to the processor. The interrupt overhead is 50 μsec. The minimum performance achieved when interrupt initiated and data transferred is used instead of programmed I/O is _____.

(a) 2.4 (b) 0.4
(c) 3 (d) 3.5

Solution: Option (b)

Explanation:

(b)

1 sec → 50 kbyte

1 byte → $\frac{1}{50k} = 20 \times 10^{-6} sec = 20\ \mu sec$

For interrupt driven mode it takes 50 μsec
So performance achieved when interrupt driven used over programmed I/O

$$S = \frac{ET_{prog-IO}}{ET_{INT-IO}}$$

$$S = \frac{20}{50} = 0.4$$

6. Consider the following sequence of micro-operations.

MBR ‹ PC
MAR ‹ SP

M[MAR] ‹ MBR
PC ‹ Vector address.

Which of the following operation performed by this sequence?

(a) Instruction fetch
(b) Operand fetch
(c) Interrupt subprogram initialization
(d) Conditional branch

Solution: Option (c)

Explanation:

(c)

PC holds the value of next instruction to be executed. We store the value of PC to MBR and value of stack pointer to MAR. Then store the value of PC which is available in MBR to location addressed by MAR.

Atleast vector address return to the PC. This can be done in interrupt subprogram initialization.

7. We have two designs P_1 and P_2 for a synchronous pipeline processor. P_1 has 8 pipeline stages with execution time of 3 nsec, 2 nsec, 4 nsec, 8 nsec, 2 nsec, 5 nsec, 4 nsec and 1 nsec while design P_2 has 5 stages each with 5 nsec each with 5 nsec execution time. How much time (in μsec) can be saved using design P_2 over design P_1 for executing 500 instructions? (upto 3 digit).

(a) 2.536
(b) 1.365
(c) 1.536
(d) 1.653

Solution: Option (c)

Explanation:

(c)

Execution time for pipeline = $(k + n - 1) \times tp$
where k = Number of stages
n = Number of instruction
tp = Execution time = Max (all stages)

$P_1 = [8 + 500 - 1] \times 8 = 4056$
$P_2 = [5 + 500 - 1] \times 5 = 2520$

Time saved using P_2 = 4056 – 2520 = 1536 nsec = 1.536 μsec

8. In which of the following addressing mode, the content of the program counter is added to the address part of the instruction to get the effective address?

(a) Indexed addressing mode
(b) Implied addressing mode
(c) Relative addressing mode
(d) Register addressing mode

Solution: Option (c)

Explanation:

(c)

In relative addressing mode content of the program counter is added to the address part of the instruction to get the effective address.

9. Suppose that a cache is 20 times faster than main memory and cache memory can be used 80% of the time. The speed-up factor that can be achieved by using the cache is _____.

(a) 2.16
(b) 3.16
(c) 4.20
(d) 4.16

Solution: Option (d)

Explanation:

(d)

Apply Amdhal's law

$$\text{F = 80\%, S = 20, overall speed-up} = \left[(1-F)+\frac{F}{S}\right]^{-1}$$
$$= \left[(1-0.8)+\frac{0.8}{20}\right]^{-1}$$
$$= 4.16$$

10. If the last operation performed on a computer with an 8-bit word has an addition in which the two operands were 00000010 and 00000011, what would be the value of the Overflow, Sign and Half-Carry flags respectively?

(a) 0, 0, 0
(b) 0, 1, 0
(c) 1, 0, 1
(d) 0, 1, 1

Solution: Option (a)

Explanation:

(a)

```
 0 0 0 0 0 0 1 0
 0 0 0 0 0 0 1 1
----------------------
 0 0 0 0 0 1 0 1
----------------------
```

Overflow = 0, sign = 0, Half carry = 0

Half carry indicate addition of packed decimal numbers. When carry takes out of the lower digit order, this flag is set. Auxiliary carry is also known as half carry.

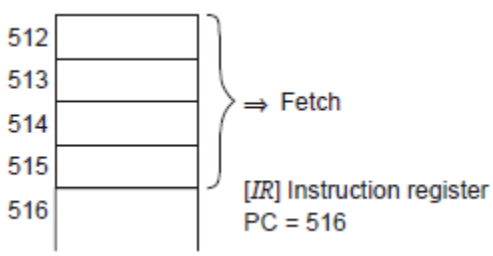
11. A 4 byte long PC-relative branch instruction is fetched from memory address 512_{10} and while its execution, the branch is made to location 885_{10}. What is the unsigned displacement present in the instruction? (relative value)

Solution: 369

Explanation:

(369)

4 byte instruction storage



Effective address = PC + Relative value
Relative value = EA – PC
= 885 – 516 = $(369)_{10}$

12. Consider the following program segment:

	Instruction	**Meaning**	**Size (words)**
I_1	LOAD r_0, 500	$r_0 \leftarrow [500]$	2
I_2	MOV r_1, r_0	$r_1 \leftarrow [r_0]$	1

I_3	ADD r_o, r_1	$r_0 \leftarrow r_0 + r_1$	1
I_4	INC r_0	$r_0 \leftarrow r_0 + 1$	1
I_5	INC r_1	$r_1 \leftarrow r_1 + 1$	1
I_6	ADD r_0, r_1	$r_0 \leftarrow r_0 + r_1$	1
I_7	Store r_1, r_0	$M[(r_1)] \leftarrow r_0$	2
I_8	Halt	Stop	1

Assume that memory is word addressable with word size 32 bits. Program is loaded into memory location $(3000)_{10}$ onwards. The value of PC at the end of execution of above program is _____.

Solution: 3009

Explanation:

(3009)

Word addressable storage
3000 – 3001
3002
3003
3004
3005
3006
3007 – 3008
3009

Valid program counter value after program is 3009.

13. A branch mark program is running on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count.

Instruction Type	**Instruction Count**	**Cycles per Instruction**
Integer arithmetic	45000	1
Date transfer	32000	2
Floating point	15000	2
Control transfer	8000	2

The execution time in msec is _____.

Solution: 3.87 (3.86-3.88)

Explanation:

3.87 (3.86-3.88)

$$CPI = \frac{\sum(J_i \times CP_i)}{I_C} = \frac{[45000\times1+32000\times2+15000\times2+8000\times2]}{10^5}$$

$$= \frac{155000}{10^5} = \frac{155}{10^2} = 1.55$$

Execution time = $\frac{I_C \times CPI}{f} = \frac{10^5 \times 1.55}{40\times10^6} = 3.87\ msec.$

14. A hypothetical control unit supports 5 groups of mutually exclusive control signals. The number of bits that can be saved using vertical approach compared to horizontal are _____.

Groups	G_1	G_2	G_3	G_4	G_5
# control signals	1	5	7	15	8

Solution: 22

Explanation:

(22)

In horizontal: 1 + 5 + 7 + 15 + 8 = 36
In vertical: log 1 + log 5 + log 7 + log 15 + log 8 = 1 + 3 + 3 + 4 + 3 = 14
Total saved bits = 36 – 14 = 22

15. Consider the micro-programmed control unit which support 256 instructions, each of which on an average takes 16 micro operations. The system support 16 flag conditions and 52 control signals. If vertical microprogramming control is used in the system then total length of control word is _____ (bits/word).

Solution: 22

Explanation:

(22)

Number of words in control memory = 256 × 16 = 4096 words
⇒ Address field = 12 bits

16 = 24 and 52 < 26

The length of control word = 

= 4 bit + 6 bit + 12 bit = 22 bits/ word

16. Consider a non-pipeline processor has clock rate of 25 MHz and CPI of 6, another processor designed with same clock rate and 8 stage instruction pipeline. If program containing 500 instructions is executed on both processors, then the speedup factor is _____.

Solution: 5.91 (5.90-5.92)

Explanation:

5.91 (5.90-5.92)

$$Speed - up(S) = \frac{Non - pipe}{Pipeline} = \frac{nt_n}{k + n - 1}$$

n = 500
t_n = 6 (for non-pipeline)
K = 8 (for pipeline)

$$S = \frac{500 \times 6}{500 + 8 - 1} = \frac{3000}{507} = 5.91$$

17. Consider the following statements:

S1: Compulsory miss can be reduced.
S2: Conflict miss can be reduced.
S3: Capacity miss can be reduced.

Which of the above statements are True?

(a) Only S1
(b) Only S1 and S2
(c) Only S2 and S3
(d) S1, S2 and S3

Solution: Option (d)

Explanation:

(d)

S2: Conflict miss are occur when too many blocks are mapped into same line or set. So by increasing the associativity i.e. increases the size of set and increases the number of sets.

S2: Compulsory miss can be reduced by increasing the line size i.e., reduce number of lines.
S3: Capacity miss can be reduced by increasing the cache memory size.

All of the three statements are true.

18. Consider the hypothetical processor which support 512 k words memory. It uses the memory mapped IO configuration. In which when 2 MSB bits of address are 1 then assigned to IO port.

How many numbers of I/O port address and memory addresses are possible in the processor respectively?

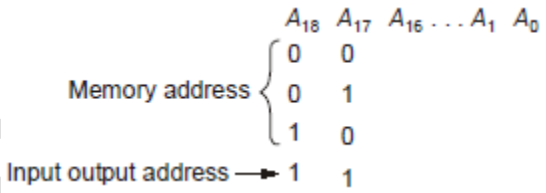
(a) 1×2^{17}, 3×2^{17}
(b) 3×2^{17}, 1×2^{17}
(c) 2×2^{17}, 1×2^{17}
(d) None of these

Solution: Option (a)

Explanation:

(a)

512 kW = 219 words = 19 bit address



So number of input output addresses = 1×2^{17}
Number of memory addresses = 3×2^{17}

19. Which of the following statements are True?

S1: Reference bit in page table entry used for page replacement.
S2: In hierarchical memory access organization, CPU perform read and write operation on only level 1 memory.
S3: In simultaneous memory access organization, CPU perform read and write operation on any level of memory.

(a) S1 and S2 only
(b) S1 and S3 only
(c) S2 and S3 only
(d) S1, S2 and S3

Solution: Option (d)

Explanation:

(d)

All the above statements are correct.

S1: Reference bit sometimes called access bit used in page table entry to show if page is replaced or not.
S2: In hierarchical memory access, CPU perform read and write operation only on level 1 memory. If miss occur then data is first transferred to level 1 then CPU access data.
S3: In simultaneous memory access, CPU perform read and write operation on any level of memory i.e. not necessary to take data first into level 1 memory than access it.

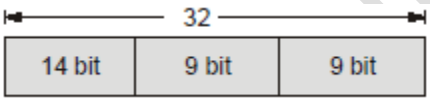
20. A computer has 32-bit instruction and 9-bit address. If there are 400 two address instructions then how many one address instructions can be formulated?

(a) 2^{14}
(b) $2^{32} - 200$
(c) $2^{14} - 400$
(d) $(2^{14} - 400) \times 2^9$

Solution: Option (d)

Explanation:

(d)



2^{14} two address instructions are possible.
Here 400 two addresses are needed so $(2^{14} - 400)$ op-codes are free.
We can store $(2^{14} - 400) \times 2^9$ one address instructions.

21. Which of the following is true?

(a) In write through protocol, cache location and main memory location are updated simultaneously.
(b) In write back protocol, cache location and main memory location are updated simultaneously.
(c) Modified or dirty bits are used by write through protocol.
(d) None of these.

Solution: Option (a)

Explanation:

(a)

Write through protocol update cache and main memory simultaneously where write back first cache is updated and marked by dirty bit then main memory is updated.

Dirty bits are used by only write back protocol to know which cache block is updated.

22. A 16KB 4-way set associative write-back cache is organized as multiple blocks, each of size 64-bytes.

The processor generates 32-bit addresses. The cache controller maintains the tag information for each cache block comprising with 1 valid bit and 1 Modified bit.

As many bits as the minimum needed to identify the memory block mapped in the cache. What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache?

(a) 5362 bytes
(b) 5361 bytes
(c) 704 bytes
(d) 176 bytes

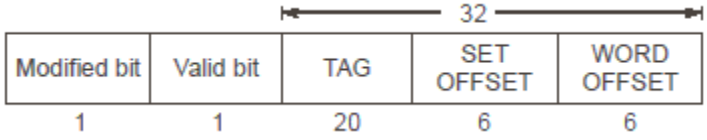
Solution: Option (c)

Explanation:

(c)

$$Total\ number\ of\ blocks = \frac{16 \times 2^{10}B}{2^{6}B} = 2^{8}$$

$$Total\ number\ of\ sets = \frac{256}{4} = 64$$



Total TAG size will be 22 bits

Total size of meta data will be $\frac{22 \times 256}{8} bytes = 704\ bytes$

23. Consider a system with the main memory access time as 200 ns and cache access time as 10 ns. Hit ratio for read request is 0.8 and 80% of the memory requests are for read. If write through policy is used, then the average time considering both read and write requests is _____.

(a) 169.6 ns
(b) 192.4 ns
(c) 78.4 ns
(d) None of these

Solution: Option (c)

Explanation:

(c)

T_{memory} = 200 ns
T_{cache} = 10 ns
f_{read} = 80%
H_{read} = 0.8
H_{write} = 1 (by default for write through)
f_{write} = 20%

$$T_{avg\ read} = (0.8 \times 10) + (0.2 \times 200)$$
$$= 8 + 40 = 48\ ns$$

$$T_{avg\ write} = 1 \times 200 = 200\ ns$$

$$T_{avg} = f_{read} \times T_{avg\ read} + f_{write} \times T_{avg\ write}$$
$$= 0.8 \times 48 + 0.2 \times 200 = 78.4\ ns$$

24. Consider the following instructions.

$I_1 : R_1 = 100$
$I_2 : R_1 = R_2 + R_4$
$I_3 : R_2 = R_4 + 25$
$I_4 : R_4 = R_1 + R_3$
$I_5 : R_1 = R_1 + 30$

Calculate sum of (WAR, RAW and WAW) dependencies the above instructions.

(a) 10
(b) 12
(c) 6
(d) 8

Solution: Option (c)

Explanation:

(c)

RAW	WAR	WAW
In-Out	Out-In $I_3 \rightarrow I_2$ $I_4 \rightarrow I_3$ $I_5 \rightarrow I_4$	Out-Out $I_2 \rightarrow I_1$ $I_5 \rightarrow I_1$ $I_5 \rightarrow I_2$
= 0	= 3	= 3

Sum = (0 + 3 + 3) = 6

25. A 4-way set associative cache memory consists of 128 blocks. The main memory consists of 32768 memory blocks and each block contains 512 eight bit words. Find how many bits are needed to represent TAG, SET and WORD field respectively?

(a) 5, 9, 10
(b) 10, 6, 8
(c) 10, 9, 5
(d) 10, 5, 9

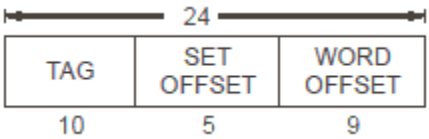
Solution: Option (d)

Explanation:

(d)

Main memory size = 32768 blocks
1 block = 512 words
= 32768 × 512 words
= $2^{15} \times 2^9$ = 224 words

Main memory takes 24 bits.
Block size = 512 words = 2^9 words
Number of bits for block size = 9 bits.
Number of blocks in set associative = 128
Number of blocks in one set = 4
Number of sets in cache = 128/ 4 = 32 = 2^5
Number of bits in set offset = 5 bits



Number of TAG bits = 24 – (9+5) = 10 bits.

26. Suppose directed mapped cache with 2^m lines 2^p bytes per cache lines. Memory is byte addressable of 2n bytes. Compute the space required for storing tags (in bits)?

(a) $2^{n-(m+p)}$
(b) $2^m \times (n-(m+p))$
(c) 2^{n+m}
(d) $(m+n) \times 2^m$

Solution: Option (b)

Explanation:

(b)

Line offset = $\log_2(2^m)$ = m bits
Word offset = $\log_2(2^p)$ = p bits
Address field size = $\log_2(2_n)$ = n bits
Tag bits per line = n – (m+p)
Tag size = Number of cache lines = Number of tag bits per line
= $2^m \times (n-(m+p))$

27. Consider a small two-way set-associative cache memory, consisting of 4 blocks. For choosing the block to be replaced, use the least recently used (LRU) scheme. The number of cache misses for the sequence of block addresses 18, 22, 10, 22, 18 is _____.

(a) 2
(b) 3
(c) 4
(d) 5

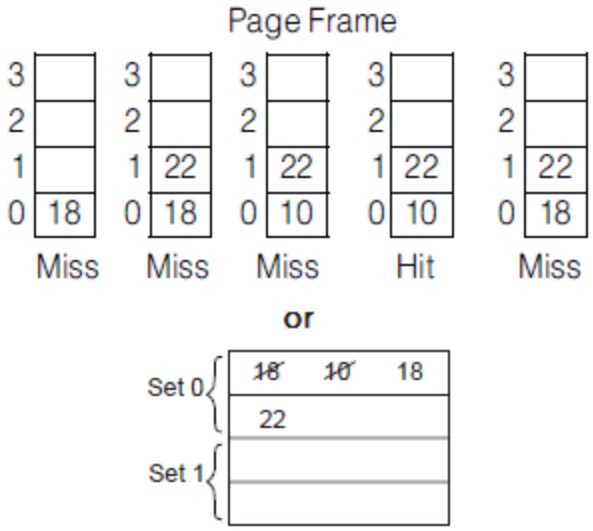
Solution: Option (c)

Explanation:

(c)

Sequence: 18, 22, 10, 22, 18.

Apply the LRU as follows:



Total number of misses = 4.

28. Consider a pipelined system with four stages: IF, ID, EX, WB. Following chart shows the clock cycles required by each instruction to compete each stage

Instructions	Instruction Fetch(IF)	Instruction Decode(ID)	Instruction Execute(EX)	Write back(WB)
I_0	1	1	2	1
I_1	2	2	3	1
I_2	2	2	2	2
I_3	2	1	1	1
I_4	3	2	1	2

How many clock cycles are required to complete the above instructions?

(a) 15
(b) 9
(c) 14
(d) 13

Solution: Option (a)

Explanation:

(a)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
I_0	IF	ID	EX	EX	WB										
I_1		IF	IF	ID	ID	EX	EX	EX	WB						
I_2				IF	IF	ID	ID		EX	EX	WB	WB			
I_3						IF	IF	ID			EX		WB		
I_4								IF	IF	IF	ID	ID	EX	WB	WB

It requires 15 clock cycles.

29. A computer has a cache, main memory and a hard disk used for virtual memory. If referenced word is in cache, 20 ns are required to access it. If it is in main memory but not in cache 60 ns are needed to load it into cache and then reference is started again. If word is not in main memory, 12 ms are required to fetch the word from disk followed by 60 ns to copy into cache, the reference is started again. The cache hit ratio is 0.9 and main memory hit ratio is 0.6.

The average time in nano seconds required to access a referenced word on this system is _____.

Solution: 480026

Explanation:

(480026)

There are 3 cases to consider

Location of referenced word	Probability	Total time for access in ns
In cache	0.9	20
In main memory but not in cache	(0.1)(0.6) = 0.06	60 + 20 = 82
Not in main memory	(0.1)(0.4) = 0.04	12ms + 60 + 20 = 12000080

So average access time should be

$$= 0.9(20) + (0.06)(80) + (0.04)(12000080) = 480026 \text{ nsec}$$

30. In an enhancement of a design of a CPU, the speed of a floating point unit has been increased by 30% and the speed of a fixed point unit has been increased by 20%. The overall speedup achieved if the ratio of the number of fixed point operation to floating point operations is 4 : 6 and the floating point operation used to take twice the time taken by fixed point operation in the original design (upto 2 decimal places) is _____.

Solution: 1.27 (1.26-1.28)

Explanation:

(1.27)

Let total operation be 100 and total time taken is t = 100 sec.

Floating point operations are $= \frac{6}{10} \times 100 = 60$

Fixed point operations are $= \frac{4}{10} \times 100 = 40$

Let time taken by floating point is t_1 and time taken by fixed point is t_2. So $t_1+t_2=100$ … (1)

Time taken by 60 floating point operation = t_1

1 floating operation = $\frac{t_1}{60}$

Similarly 1 fixed point operation takes $\frac{t_2}{40}$

$\because \frac{t_1}{60} = 2\frac{t_2}{40}$

$2t_1 = 6t_2$

From equation 1 and 2

$$t_1 = \frac{600}{8} \; and \; t_2 = \frac{200}{8}$$

After speed-up $t_1' = \frac{t_1}{1.3} = \frac{600}{1.3\times8} = \frac{6000}{104}$

$$t_2' = \frac{t_2}{1.2} = \frac{100}{1.2\times8} = \frac{2000}{96}$$

$$t_1' = t_1' + t_2' = \frac{6000}{104} + \frac{2000}{96}$$

$$S_2 = \frac{t_t}{t'} \times S_1$$

$$S_2 = \frac{100}{\left[\frac{6000}{104}+\frac{2000}{96}\right]} \times S_1 = \frac{100}{57.69+20.83} \times S_1$$

$$S_2 = \frac{100}{78.52} \times S_1 = 1.27\, S_1$$

31. Suppose that in 1000 memory references there are 150 misses in first level and 100 miss in second level cache. Assume that miss penalty from L_2 cache to memory is 120 cycles. The hit time of L_2 cache is 50 cycles.

If there are 4 memory references per instruction, the average stall per instruction is _____.

Solution: 78

Explanation:

(78)

4 memory references → 1 instruction
1000 memory references → ? instructions.

Number of instructions = $\frac{1000}{4} = 250$

$$\left[\frac{\#\ memory\ stalls}{\#\ Instructions}\right] = \left[\frac{\#\ misses\ L_1}{\#\ Instructions} \times hit\ L_2\right] + \left[\frac{\#\ misses\ L_2}{\#\ Instructions} \times miss\ penalty\ L_2\right]$$

$$= \left[\frac{150}{250} \times 50\right] + \left[\frac{100}{250} \times 120\right]$$

$$= [30 + 48] = 78\ cycles$$

32. Consider the machine with a byte addressable main memory of 2^{16} byte, block size of 16 byte and a 2 way set associative mapped cache having 2^{10} lines. Suppose there are two bytes in main memory i.e. first byte $[E\ 01\ F]_{16}$ and second byte $[E\ 208]_{16}$ respectively then the difference of the set value (in decimal) between given two bytes i.e. (SET value of second byte – SET value of 1st byte) is _____.

Solution: 31

Explanation:

(31)

Block size = 2^{16} byte = 4 bits
Blocks in main memory = 2^{10}
So number of sets = $\frac{2^{10}}{2^1} = 2^9 \Rightarrow 9\ bits$
# of bits in physical address= $2^{16} \Rightarrow$ 16 bits

SET value$_1$ = 000000001 = Decimal value = $(1)_{10}$
SET value$_2$ = 000100000 = Decimal value = $(32)_{10}$
Difference = $SET_2 - SET_1$
= 32 – 1 = $(31)_{10}$

33. Consider two cache organizations. The first one if 64 KB way associative with 64 byte block size. The second one is of the 64 KB direct mapped cache. The size of an address is 32 bits in both organizations. A 4 to 1 multiplexer has latency of 0.8 ns which k bit comparator has latency of k/5 nsec. The difference between the hit latencies of both cache organizations (i.e. associative hit latency – direct mapped hit latency) (in nsec) is _____.

Solution: 1.2

Explanation:

(1.2)

Number of cache lines = $\frac{64\ kB}{64\ B} = 1\ k = 2^{10}$

Number of sets = $\frac{2^{10}}{2^2} = 2^8$

Tag	Set	Block
18	8	6

H_1 = 18/5 + 0.8 ns

= 3.6 + 0.8 ns = 4.4 ns

Direct mapped cache:

Tag	Set	Block
16	10	6

This is no need of multiplexer in direct mapped cache.

So H_2 = 16/ 5 nsec

= 3.2 nsec

Difference = $H_1 - H_2$

= 4.4 – 3.2 = 1.2 nsec