COMPUTER ORGANIZATION

(Instruction Pipelining, Cache & Main memory, Secondary Storage)

SOLUTIONS

1. More than one word is put in one cache block to

(a) Exploit temporal locality references in a program
(b) Exploit spatial locality references in a program
(c) Reduce miss penalty
(d) All of these

Solution: Option (b)

2. A pipeline P is found to provide a speedup of 6.16 when operating at 100 MHz and an efficiency of 88 percent. How many stages does P have?

Solution: From 7.21 To 6.79

Explanation:

$\text{Clock Time} = 10\text{ns},$

$$\frac{88}{100}\left[\frac{p \times 10}{10}\right] = 6.16,$$

$p = 7$

3. How big is a four way set associative cache memory with a block size of 64 Bytes and containing 1024 sets?

Solution: From 263.68 To 248.32

Explanation:

$1024 \times 4 \times 64$ Bytes $= 2^{18} = 256$ Kbytes

4. A five stage pipeline has a clock cycle time of 5ns. If the non-pipeline clock is also of the same duration than what is the speed up for 75% of pipeline efficiency?

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Solution: From 3.863 To 3.638

Explanation:

Non-pipeline: 5 × 5 = 25
Pipeline – 5

For $100\% - \frac{25}{5} = 5$

For $75\% - \frac{75}{100} \times 5 = 3.75$

5. A tiny bootstrap loader program is situated in

(a) Hard disk
(b) ROM
(c) BIOS
(d) None of these

Solution: Option (b)

6. If a cache access requires one clock cycle and handling cache misses stalls the processor for an additional five cycles, which of the following cache hit rates comes closest to achieving an average memory access of 2 cycles (in %)?

Solution: From 82.4 To 77.6

Explanation:

2 cycle average access = (1 cycle for cache) + (1 – hit rate) (5 cycles stall) ⇒ hit rate = 80%

7. Cache and word addressable main memory system has the following specification

Cache block size = 16 words
Set size = 2 blocks
Number of sets = 128
Number of bits in a word = 32 bits
Cache access time (Tc) = 20ns
Memory access (Tm) = 120ns
Hit (H) = 0.8
Size of main memory address = 21bits

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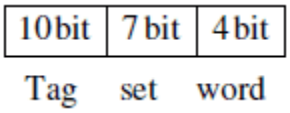
What is the total cache size needed?

(a) (16k + 140) bytes
(b) (16k + 320) bytes
(c) (256k + 180) bytes
(d) (60k + 300) bytes

Solution: Option (b)

Explanation:



$$\text{Total size of cache} = \underbrace{\frac{128 \times 2 \times 16 \times 32}{8}}_{\substack{128 \text{ set, each set 2 block} \\ \text{each block 16 word,} \\ \text{each word 32 bit}}} + \underbrace{\frac{128 \times 2 \times 10}{8}}_{\substack{128 \text{ set, each set 2 block} \\ \text{each block 16 word,} \\ \text{each word 32 bit}}}$$

$\frac{2^7 \times 2 \times 2^4 \times 2^5}{2^3} + 16 \times 2 \times 10 = (16\text{K} + 320)\text{byte}$

8. Consider a machine with 10ns clock and it takes 4 clock cycle per ALU instruction, 5 clock cycle per branch instruction, 6 clock cycle memory instruction. There exists 40% ALU instruction, 20% branch instruction and 40% memory instruction.

What is throughput of pipeline system if overhead is 2ns?

(a) 83MIPS
(b) 84MIPS
(c) 85MIPS
(d) 86MIPS

Solution: Option (a)

Explanation:

Average access time for non-pipeline system

$$[4 \times .40 + 5 \times .20 + .40 \times 6] \times 10\text{ns} = [1.6 + 1 + 2.4] \times 10\text{ns} = 5 \times 10\text{ns} = 50\text{ns}$$

For pipeline system in every clock cycle one instruction will get executed and overhead of 2 nano sec.

So, average time = (10 + 2) ns = 12 ns,

throughput of system $\frac{1}{12\text{ns}} = 83$ MIPS

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9. A 5 stage pipeline has the stages IF, ID, OF, PO, WB (Assume that there are no separate data and instruction caches). For the program below, what is/are the hazard(s) possible?

$\text{MOV } R_1, A;\ R_1 \leftarrow \mu[A]$
$\text{MOV } R_2, A;\ R_2 \leftarrow \mu[B]$
$\text{ADD } R_1, R_2;\ R_1 \leftarrow R_1 + R_2$
$\text{MOV } X, R_1;\ \mu[x] \leftarrow R_1$

(a) Data Hazard
(b) Structural Hazard
(c) Control Hazard
(d) Both (a) & (b)

Solution: Option (b)

10. An instruction pipeline consists of 4 stages fetch(F), decode(D), execute(E) and write(W). Different instruction spent different number of clock cycles.

Stage / Instruction	F	D	E	W
I_1	1	2	2	1
I_2	2	3	3	2
I_3	3	1	1	1
I_4	1	1	1	1

The value in the box represents clock cycles taken by instructions in different states.

At what clock cycle, instruction I_3, will complete its decoding?

(a) 6^{th} clock cycle
(b) 7^{th} clock cycle
(c) 12^{th} clock cycle
(d) 13^{th} clock cycle

Solution: Option (b)

Explanation:

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	1	2	3	4	5	6	7	8	9	10	11	12	13
I_1	F	D	D	E	E	W							
I_2		F	F	D	D	D	E	E	E	W	W		
I_3				F	F	F	D			E		W	
I_4							F	D			E		w

At 7^{th} clock cycle I_3 will complete its decoding.

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