COMPUTER ORGANIZATION & ARCHITECTURE

SOLUTIONS

1. A program consists of four major types of instructions. The instruction mix and the CPI for each instruction type are given in the following table.

Instruction Type	CPI	Instruction Mix
ALU	1	50%
Load / Store	2	23%
Branch	3	17%
Memory reference	4	10%

If the clock frequency of the processor is 400 MHz, what is the average CPI of the processor?

(a) 3.75
(b) 2.87
(c) 1.87
(d) 1.54

Solution: Option (c)

Explanation:

(c)

Average CPI = Σ CiIi

$= 1 \times 0.5 + 2 \times 0.23 + 3 \times 0.17 + 4 \times 0.1$

$= 0.50 \times 0.46 + 0.51 \times 0.40 = 1.87$

2. Which of the following best characterize computer that uses memory mapped I/O?

(a) the computer provides special instruction for manipulating I/O port
(b) I/O ports are placed at addresses on bus and are accessed just like other memory location
(c) to perform an I/O operation, it is sufficient to place the data in an address and call the channel to perform the operation
(d) ports are reference only by memory mapped instruction of the computer and are located hard wired memory location

Solution: Option (b)

Explanation:

(b)

I/O ports are placed at addresses on bus and are accessed just like other memory location in computers that uses memory mapped I/O.

3. Suppose after analyzing a new cache design, you discover that the cache has far too many conflict misses and this needs to be resolved. You know that you must increase associativity in order to decrease the number of cache misses. What are the implications of increasing associativity?

(a) Slower cache access time
(b) Increase index bits
(c) Increase block size
(d) All of these

Solution: Option (a)

Explanation:

Increase in the associativity leads to increase in the number of tag comparisons. Hence it leads to increase in cache access time.

4. Identify the false statements:

S_1: Separate I/O address space does not necessarily mean that I/O address lines are physically separated.
S_2: Address decoder is an essential part of I/O interface.

(a) Only S_1
(b) Only S_2
(c) Both S_1 and S_2
(d) Neither S1 nor S_2

Solution: Option (d)

Explanation:

(d)

S_1: Separate I/O address space does not necessarily mean that I/O address lines are physically separated from the memory address lines. A special signal on the bus indicates that the requested read or write transfer is an I/O operation.

S_2: The address decoder, the data and status register and control circuitry required to coordinate I/O transfers constitute the interface circuit (Hence true).

5. DMA interface unit eliminates the need to use CPU registers to transfers data from

(a) MAR to MBR
(b) MBR to MAR
(c) I/O units to memory
(d) Memory to I/O units

Solution: Option (d)

Explanation:

(d)

DMA interface unit eliminates the need to use CPU registers to transfer data from Memory I/O units.

6. Compared to RISC processors, CISC processors contain _____.

(a) More registers and smaller instruction set
(b) Larger instruction set and less registers
(c) Less registers and smaller instruction set
(d) More transistor elements

Solution: Option (b)

Explanation:

(b)

CISC processor contains less registers and larger instruction set.

7. Which of the following miss is definite to occur in cache memory?

(a) Cold-start miss
(b) Capacity miss
(c) Conflict miss
(d) All of these

Solution: Option (a)

Explanation:

(a)

- Cold start miss also called compulsory miss, will occur when the cache is empty.
- Capacity miss occurs due to small size of cache memory, it cannot hold all the blocks required for program execution.
- Conflict miss occurs when too many blocks are mapped into same line or set.

8. Which of the following are not considered as part of I/O interface which connects bus and I/O device?

(i) Address decoder
(ii) Control circuitry
(iii) Data and status register

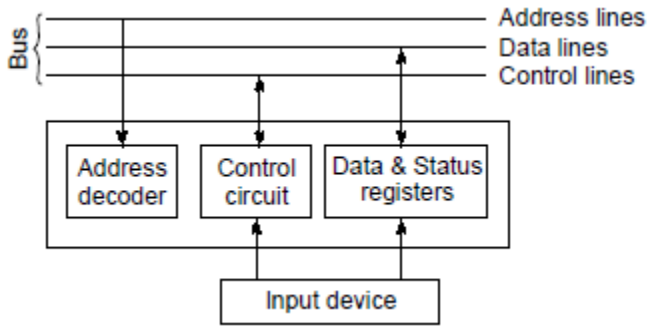
(a) Only (i) and (iii)
(b) Only (ii) and (iii)
(c) (i), (ii) and (iii)
(d) None of these

Solution: Option (d)

Explanation:

(d)

(i) The address decoder enables the device to recognize it's address when the address appears on the address lines.
(ii) Control circuitry is required to coordinate I/O transfers.
(iii) The data register holds the data being transferred to or from the processor. The status register contains information relevant to the operation of the I/O device.



9. A two way set associative cache has lines of 16 byte and a total cache size of 8 K bytes. The 256 M byte main memory is byte addressable. Which one of the following main memory block is mapped on to the set '0' of the cache memory?

(a) $(CFED09B)_{16}$
(b) $(FCED90C)_{16}$
(c) $(CFED00B)_{16}$
(d) $(FECD10C)_{16}$

Solution: Option (c)

Explanation:

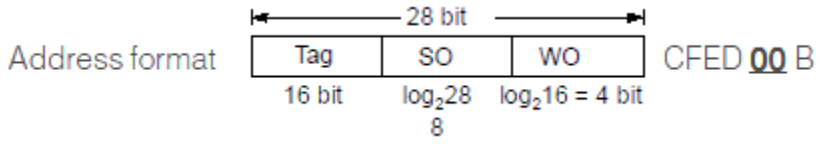
(c)

Number of lines = $\frac{8\,K}{16} \Rightarrow 2^9$

Number of sets = $\frac{2^9}{2} \Rightarrow 2^8$

Physical address size = 28 bits

2 way set associative cache.



10. Consider the following statements:

1. Time taken for a single instruction on a pipelined CPU is less than or equal to time taken on a non-pipelined (identical) CPU.
2. In a uniform delay pipeline execution time for a single instruction is equal to the execution time in non-pipelined processor. (Assume no buffer delay)

Which of the above statement(s) is correct?

(a) Only 1
(b) Only 2
(c) Both 1 and 2
(d) Neither 1 nor 2

Solution: Option (b)

Explanation:

(b)

1. For a single instruction time taken on pipeline CPU is always greater than or equal to the non-pipeline.
2. When all stages have same delay and buffer latency is zero then for a single instruction execution time of pipeline CPU is equal to the execution time of non-pipeline CPU.

11. Suppose the cache memory is 100 times faster than main memory and it is used 50% of the time. The performance is gained by introducing this cache is _____.

Solution: 1.98 (1.97-1.99)

Explanation:

1.98 (1.97-1.99)

Apply Amdhal's law

$S = 100$
$f = 50\%$

$$S_{overall} = \left[1 - 0.5 + \frac{0.5}{100}\right]^{-1}$$
$$= \left[0.5 + \frac{0.5}{100}\right]^{-1} = \left[\frac{101}{200}\right]^{-1} = \frac{200}{101} = 1.98$$

12. Consider a 16 bit processor in which the following one address instruction is loaded in main memory.

300	Opcode
301	500
302	Next instruction
⋮	⋮
500	999

The effective address using PC relative addressing mode when processor is executing an instruction at location 300 is _____.

Solution: 802

Explanation:

802

$EA \leftarrow PC + 500$
$EA \leftarrow 302 + 500$
$EA \leftarrow 802$

13. The number of micro-operations required to fetch an instruction from memory is _____.

Solution: 4

Explanation:

4

Fetch Cycle:

T_1: PC → MAR	PC_{out}, MAR_{in}
T_2: M[MAR] → MBR	MAR_{out}, MBR_{in}
T_3: MBR → IR	MBR_{out}, IR_{in}
T_4: PC → PC	PC_{out}, PC_{in}

14. The minimum size of the ROM which maintains truth table of square of 3 bit numbers is _____ (in bits).

Solution: 48

Explanation:

48

Square of largest 3 bit number (111) occupies 6 bits only. Thus 6 bits are sufficient to store squares of any 3 bit number in ROM.

Square of largest 3 bit number = 49 which needs minimum 6 bits.
∴ $8 \times 6 = 48$ bits

15. Consider a cache with 64 blocks and block size of 16 bits. The block number of byte address 1600 is _____.

Solution: 36

Explanation:

36

$$\frac{1600}{\text{Block size}} = \frac{1600}{16} = 100$$

100^{th} block in main memory.
∴ Location in cache = 100 mod 64 = 36^{th} block in cache.

16. Consider a 5 stage pipeline with IF, ID, EX, MEM and WB latencies 8, 6, 4, 6 and 4 respectively (in ns). If IF stage is made 50% faster, the percentage it will improve the performance CPU is _____.

Solution: 14.3 (14-15)

Explanation:

14.3 (14-15)

In non-pipeline total latency (without enhance)
= 8 + 6 + 4 + 6 + 4 = 28

with improvement = 4 + 6 + 4 + 6 + 4 = 24

% improvement = $\frac{28-24}{28} = \frac{4}{28} = 14.3\%$

17. A certain architecture supports indirect, direct and register addressing modes for use in identifying operands for arithmetic instructions. Which of the following cannot be achieved with a single instruction?

(a) specifying a register number in the instruction such that the register contains the value of an operand that will be used by the operation.
(b) specifying a register number in the instruction such that the register will serve as the destination for the operation's output.
(c) specifying an operand value in the instruction such that the value will be used by the operation.
(d) specifying a memory location in the instruction such that the memory location contains the value of an operand that will be used by the operation.

Solution: Option (c)

Explanation:

(c)

Choice A is "register" addressing, which is supported by this architecture. Choice B is also typically covered when manufacturers speak of "register" addressing, which is supported by this architecture. Choice C is "immediate" (or "literal") addressing, which is not supported by this architecture. Choice D is "direct" (or "absolute") addressing, which is supported by this architecture.

18. Consider a system in which DMA technique is used to transfer 16 MB of data from an I/O device into memory. The bandwidth of I/O device is 128 KB/s. What percentage of time is the CPU in busy mode (approximately)?

(a) 17 (b) 82
(c) 35 (d) 41

Solution: Option (b)

Explanation:

(b)

Time taken by I/O device = $\frac{16\ \text{MB}}{128\ \text{kB}} = 128\ \text{sec}$

Percentage time CPU is busy = $\frac{128}{128+28} \times 100 = 82.05$

19. Consider a 5 stage instruction pipeline having latencies (in ns) 1, 2, 3, 4 and 5 respectively. Find average CPI of non-pipeline CPU when speed up achieved with respect to pipeline is 4 (assume ideal case for pipelining)?

(a) 1.23 (b) 1.33
(c) 1.66 (d) 1.73

Solution: Option (b)

Explanation:

(b)

$$\text{Speed up} = \frac{t_n}{t_p} = \frac{\text{CPI}_n \times \#\text{instruction} \times \text{Cycle time}_n}{\text{CPI}_p \times \#\text{instruction} \times \text{Cycle time}_p}$$

$$4 = \frac{\text{CPI}_n \times (1+2+3+4+5)}{1 \times (5)}$$

$$\text{CPI}_n = \frac{20}{15} = \frac{4}{3} = 1.33$$

20. A Hypothetical control unit supports 5 groups of mutually exclusive signals

Group	G_1	G_2	G_3	G_4	G_5
Control Signal	2	1	4	27	17

Find size of control memory (in bytes) using vertical programming if control unit support 256 control word memory.

(a) 704 bytes (b) 672 bytes

(c) 604 bytes (d) 804 bytes

Solution: Option (a)

Explanation:

(a)

Number of bits for control signals in vertical programming:

$$\log_2(2) + \log_2(1) + \log_2(4) + \log_2(27) + \log_2(17)$$
$$= 1 + 1 + 2 + 5 + 5$$
$$= 14 \text{ bits}$$

256 CW = 8 bits

VCW size = 14 + 8 = 22 bits

Vertical control memory size = 256 × 22 bits

$$= \frac{256 \times 22}{8} \text{ bytes}$$
$$= 704 \text{ bytes}$$

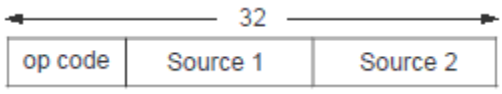
21. A system supports 2 address and 1 address instructions only. A 32 bit instruction is stored in 16 K words memory. What will be the number of one address instructions supported by this system when there are 12 two address instructions?

(a) 16 K (b) 32 K
(c) 64 K (d) 128 K

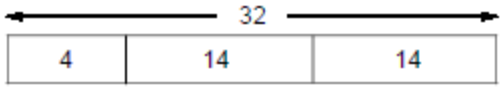
Solution: Option (c)

Explanation:

(c)



16 K words ⇒ 14 bits needed for addressing



Number of op-codes possible = $2^4 = 16$
Remaining op-codes = 16 – 12 = 4
Number of one address instructions = $4 \times 2^{14} = 64$ K

22. An instruction pipeline consist of 4 stages IF, ID, EX and WB. Four instructions need these stages for different number of cycles as shown by the table below

Instruction	# Cycle needed for			
	IF	ID	EX	WB
1	1	2	1	1
2	1	2	2	1
3	2	1	3	2
4	1	3	2	1

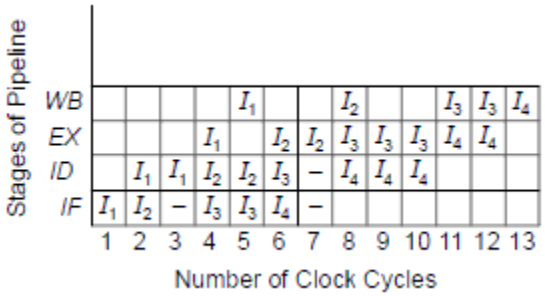
Find number of clock cycles needed to execute the above 4 instructions.

(a) 12 (b) 13
(c) 14 (d) 15

Solution: Option (b)

Explanation:

(b)



23. The main memory of a computer has 2×10×20 blocks while the cache has 2×10 blocks. If the cache uses the set associative mapping scheme with two blocks per set, then block 232 of main memory maps to set X. What is the value of X?

(a) 12 (b) 24

(c) 2 (d) 42

Solution: Option (c)

Explanation:

Number of sets = $\frac{2\times10}{2} = 10$

∴ 232 mod 10 = 2

Hence the block 232 will map to set 2.

24. Consider the addition of the two numbers 10001110 and 10000000 in an 8-bit ALU. Which of the following best summarizes the result and the status of the Z(zero), S(sin), C(carry) and O(overflow) flags? Assume that the numbers are represented in 2's Complement format and that S=1 if the result is negative.

(a) Sum = 100001110, Z = 0, C = 1, O = 0, S = 1
(b) Sum = 00001110, Z = 0, C = 0, O = 1, S = 0
(c) Sum = 10000110, Z = 0, C = 0, O = 1, S = 0
(d) Sum = 100001110, Z = 0, C = 1, O = 1, S = 0

Solution: Option (d)

Explanation:

(d)

```
  10001110
  10000000
 ----------
Sum =100001110
 ----------
```

Z = 0, C = 1, O = 1, S = 0

25. Consider a CPU shared bus system in which each CPU requests the bus 35% of the time. What is the probability that exactly 3 CPU's are requesting the bus, when there are 10 CPU's competing for bus?

(a) 0.40 (b) 0.25
(c) 0.35 (d) 0.15

Solution: Option (b)

Explanation:

(b)

The required probability = ${}^{10}C_3 (0.35)^3 (0.65)^7 = 0.252$

26. Consider a 4 way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates 20 bit addresses for words in main memory.

Match the following main memory addresses with the set number.

List-I	**List-II**
A. 1111 0101 1010 0011 1111	1. 16
B. 0000 1111 1100 0011 0011	2. 10
C. 1100 1100 1100 1100 0011	3. 8
D. 1010 1010 1010 1010 1010	4. 19

Codes:

	A	**B**	**C**	**D**
a.	3	1	4	2
b.	3	1	2	4
c.	3	2	4	1
d.	2	3	1	4

(a) a (b) b
(c) c (d) d

Solution: Option (a)

Explanation:

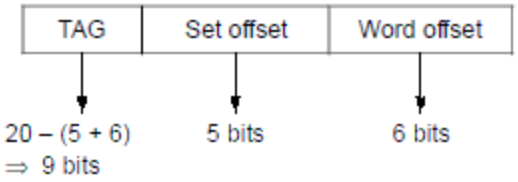
(a)

4 way set associative

Number of lines = 128

Number of sets = $\frac{128}{4} = 32$

Block size = 64 words



A: 1 1 1 1 0 1 0 1 **0 1 0 0 0** 1 1 1 1 1 1

In addresses bit numbers (10 – 14) will decide the set number in cache memory.

∴ A – 8, B – 16, C – 19, D – 10

27. During a program execution out of 1000 memory references there are 250 and 120 misses in L_1 (Level-1) and L_2 (Level-2) caches respectively. Hit times for L_1 and L_2 cache are 24 and 40 cycles respectively. If there are 2.5 memory references per instruction, how many averages stall cycles per instruction? (Assume L_2 to memory miss penalty is 250 cycles)

(a) 50 (b) 100

(c) 150 (d) 200

Solution: Option (b)

Explanation:

(b)

Average Number of stalls per instruction = (# misses per instruction in L_1 × Hit time in L_2)
+ (# misses per instruction in L_2 × Miss penalty of L_2)

2.5 memory references per instruction ⇒ $\frac{1000}{2.5}$ instructions for 1000 references = 400 instructions

∴ Average number of stalls per instruction

$$= \left(\frac{250}{400} \times 40\right) + \left(\frac{120}{400} \times 250\right)$$

= 25 + 75 = 100 cycles.

28. Array A contains 256 elements of 4 bytes each. Its first element is stored at physical address 4,096. Array B contains 512 elements of 4 bytes each. Its first element is stored at physical address 8,192. Assume that only arrays A and B can be cached in an initially empty, physically addressed, physically tagged, direct-mapped, 2K-byte cache with an 8-byte block size. The following loop is then executed.

```
for (i = 0; i < 256; i++)
A[i] = A[i] + B[2 * i];
```

During the execution of the loop, how many bytes will be written to memory if the cache has a write-through policy?

(a) 0
(b) 256
(c) 1,024
(d) 2,048

Solution: Option (c)

Explanation:

(c)

1. Since the cache line size is 8 bytes, the smallest unit of data transfer into cache from L2 cache or memory is 8 bytes. So if we have a miss for A[0], both A[0] and A[1] get fetched into cache.
2. The cache is addressed by the lower bits of the address. However the address is byte address, and since a cache line can hold 8 bytes, the lower three bits of the address are used to address bytes inside a cache line. Since the cache is 2K bytes large, it has 2K/8 = 256 cache lines, which are addressed by 8 bits. Hence:

bits 0-2 form the "offset", which is used to address inside a cache line
bits 3 through 10 of the address from the cache line address.
Bits 11-32 form the TAG. (assume a 32 bit architecture)

Now, Consider the sequence: (2 iterations of the loop)
load A[0] → causes A[0] and A[1] at cache line 0
load B[0] → *also addresses cache line 0* - so overwrites A[0] & A[1] above
store A[0] → Nothing happens to cache (no write allocate) → 8 bytes are written (8 is the unit of transfer)
load A[1] → Accesses the SAME cache line as A[0] So we load A[0] and A[1] again into line 0
load B[2] → addresses cache line 1 – load B[2] and B[3] into cache line 1
store A[1] → Again nothing happens as above.

So the pattern might be obvious:

At every iteration of the loop, B[2*i] accesses a new cache line, and A overwrites the cache lines every two iterations. Since the loop is 256 iterations, B will just reach cache line 255 when the loop will finish.
Since A has been erasing B half as fast, we would have A in the top half of the cache and B in the bottom half.
Thus the cache contains:
A[0] –A[255] (In the top half) and B[256] – B[511] in the bottom half.

Also, since the cache is write through, the entries in the cache will always be the freshly written entries. Since this is write through, we have to write 256 words = 1024 bytes (all of A) back to the next level (L2 cache or memory)

Assuming that the minimum transfer from a cache to a lower level is a cache line, this translated to 2048 bytes.

29. Consider the following program segment used to execute on a hypothetical processor. Consider all the registers are of 16 bit size

```
I1      MOV  CX,0005      ;  CX ← 0005
I2      MOV  BX,OFF7H     ;  BX ← OFF7H
I3      MOV  AX,OBCAH     ;  AX ← OBCAH
I4      OR   BX,AX        ;  BX ← BX (OR) AX
I5      AND  DX,AX        ;  DX ← DX (AND) AX
I6      LOOP I3           ;  LOOP till CX = 0
```

Processor clock frequency is 1 MHz. In which data transfer operations takes 6 cycles, data manipulation operations takes 4 cycles and transfer of control operations takes 2 cycles to execute. The time is required to execute the program is _____ (in μsec).

Solution: 92

Explanation:

92

```
        I1      6 cycles  ┐
        I2      6 cycles  │
Label   I3      6 cycles  │
        I4      4 cycles  ┘   5 times
        I5      4 cycles
        I6      2 cycles
```

Example:

Time = 12 cycles + 80 cycles = 92 cycles

Cycle time = $\frac{1}{1\ \text{MHz}}\text{sec} = 1\mu\text{sec}$

Program execution time = 92 cycles × 1 μsec = 92 μsec.

30. A 17 way set associative cache has 16 byte blocks and 32 bit byte addressable memory. The cache size is 17408 bytes. The total bits required for both tag and word offset for any CPU reference is _____.

Solution: 26

Explanation:

26

16 bytes per block, so there are $\log_2 16 = 4$ bits.
Cache size = 17408 bytes

$\therefore \quad \frac{17408}{16} = 1088 \text{ blocks}$

The cache is 17 way associative, so, there are $\frac{1088}{17} = 64$ sets

$\therefore \quad \log_2 64 = 6$ bits (set number)

Number of tag bits is 32 – 6 – 4 = 22 tag bits.

22 + 4 = 26

31. Consider a pipeline 'x' consist of 5 stages named as IF, ID, OF, EX and WB with the respective stage delays of 2 ns, 5 ns, 6 ns, 8 ns and 1 ns. The alternative pipeline 'y' contain the same number of stages but EX stage is divided into 4 sub stages, (EX1, EX2, EX3 and EX4) with equal delay i.e. (8 ns/4) and ID stage is divided into 2 substages (ID1 and ID2) with equal delays of (5 ns/2). In the pipeline x and y memory reference instructions are not overlapped so the penalty of memory reference instructions in the pipeline 'x' is 4 cycles and in the pipeline 'y' is 8 cycles. If the program contains 30% of the instructions which are memory based instructions, the speedup ratio of x is speedup ratio of y is _____.

Solution: 0.859 (0.85-0.87)

Explanation:

0.859 (0.85-0.87)

$$S_x = \frac{\text{Pipeline depth}}{(1 + \text{Frequency} \times \#\text{stalls per instruction})} = \frac{5}{1 + (0.3 \times 4)} = 2.27$$

$$S_y = \frac{9}{1 + (0.3 \times 8)} = 2.64$$

$$\frac{S_x}{S_y} = 0.859$$

32. Consider execution of 100 instructions on a 5 stage pipeline. Let P be the probability of an instruction being a branch. The value of P such that speed up is atleast 4 is _____. (Assume each stage takes 1 cycle to perform it's task and branch is predicted on fourth stage of the pipeline).

Solution: 0.083 (0.08-0.09)

Explanation:

0.083 (0.08-0.09)

$$\text{Speed up} = \frac{\text{Pipeline depth}}{(1 + \text{Branch frequency} \times \text{Branch penalty})} \geq 4$$

$$\frac{5}{1 + P \times 3} \geq 4$$

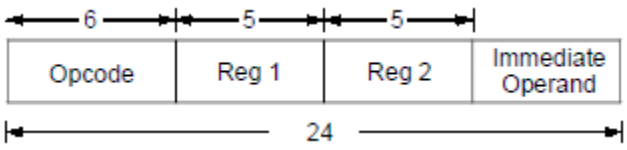
$$4 + 12P \leq 5$$
$$12P \leq 1$$
$$P \leq \frac{1}{12} = 0.0833$$

33. A machine has 24 bit instruction format. It has 32 registers and each of which is 32 bit long. It needs to support 49 instructions. Each instruction has two register operands and one immediate operand. If the immediate operand is signed integer, the minimum value of immediate operand is _____.

Solution: –128

Explanation:

–128



49 instructions ⇒ 6 bits needed for Op-code
32 registers ⇒ 5 bits needed for register operands
Immediate operand bits = 8
Minimum value = $-2^7 = -128$
Since 1 bit is gone for sign representation.