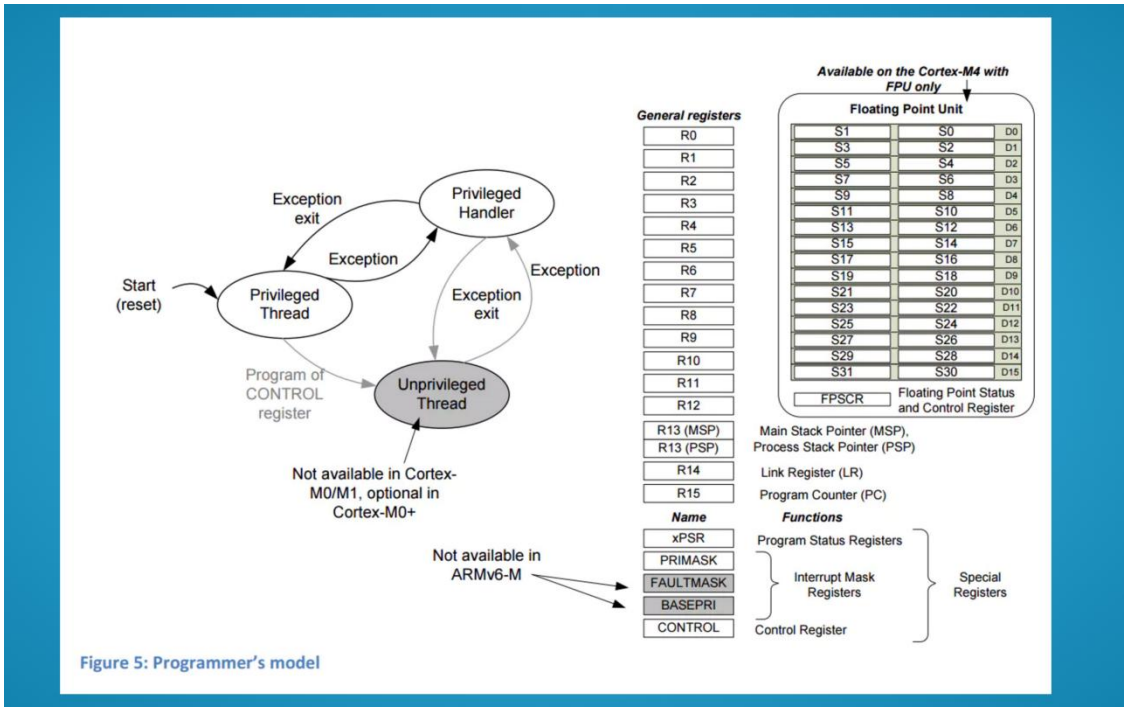
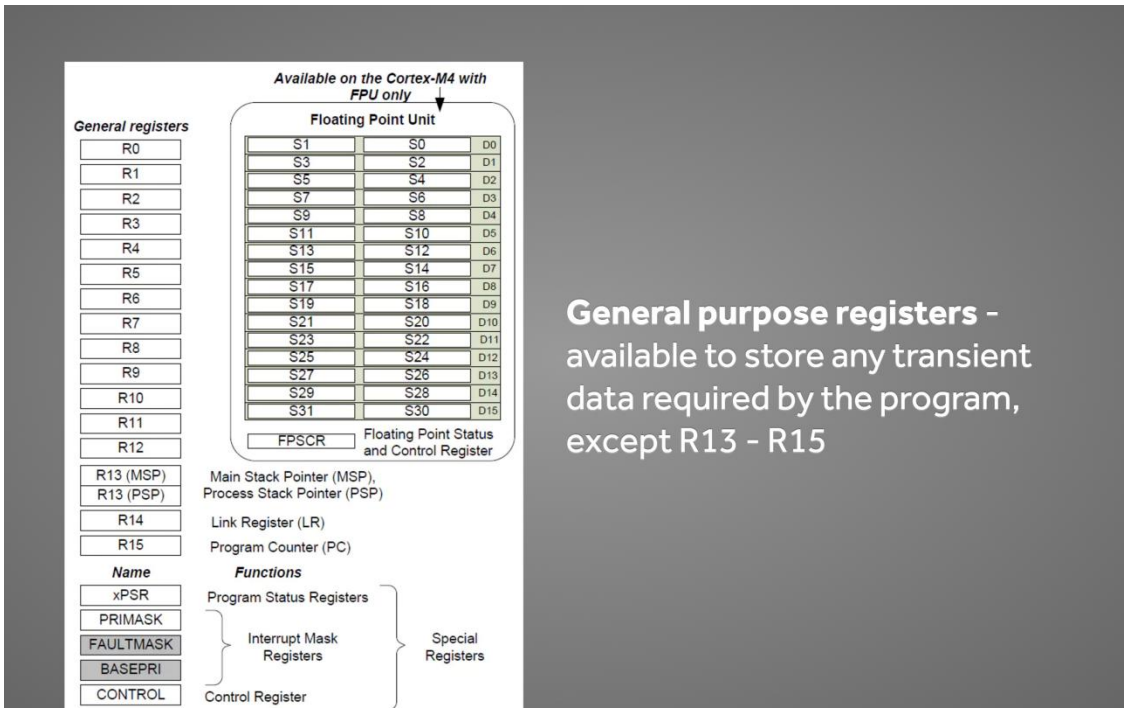
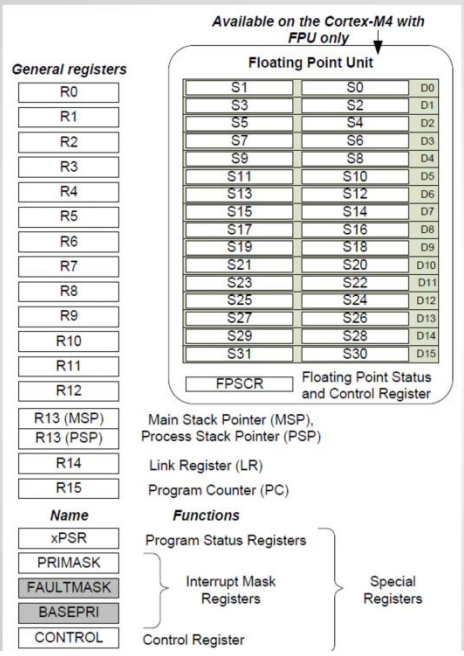


Figure 5: Programmer's model





The Stack Pointer (SP) is register R13. In Thread mode, bit[1] of the CONTROL register indicates the stack pointer to use:

- 0: Main Stack Pointer (MSP). This is the reset value.
- 1: Process Stack Pointer (PSP).

On reset, the processor loads the MSP with the value from address 0x00000000.

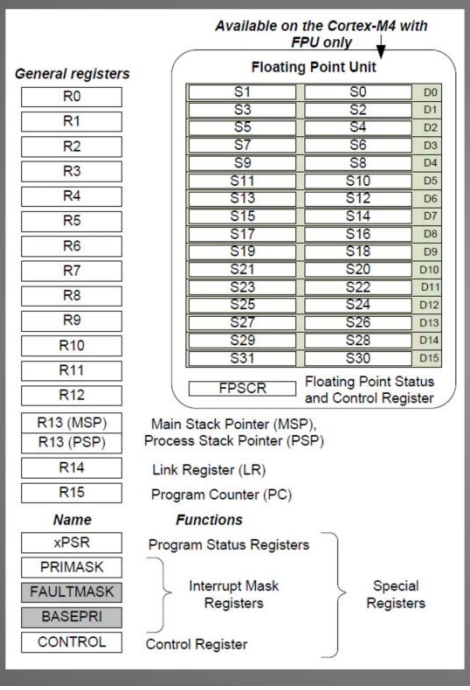
MSP and PSP

Having two separate stack pointers allows the operating system to be safer and more robust.

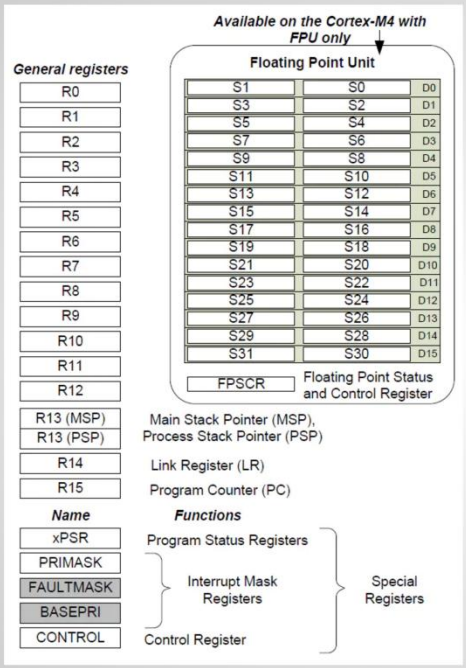
Main Stack Pointer (MSP) is meant for the OS
Process Stack Pointer (PSP) is meant for applications

This way OS can protect its stack and prevent applications from accessing or corrupting it.
This way you can ensure that the OS does not run out of stack space for exception handling, even if the application consumes all the PSP space.

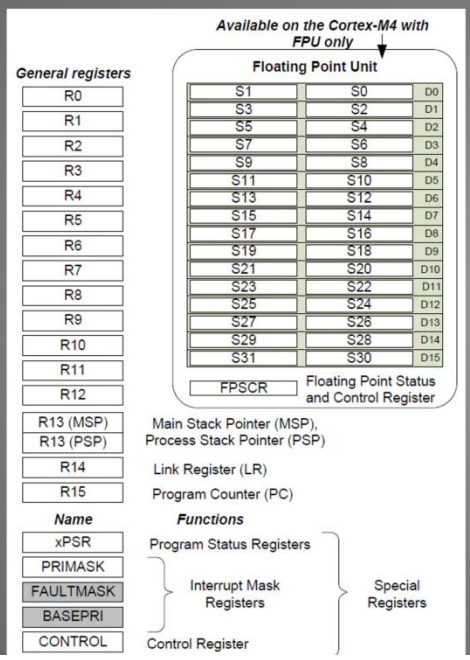
It is not necessary to use both stack pointers. By default, system will only use MSP. To use PSP, it must be manually configured.



The Link Register (LR) is register R14. It stores the return information for subroutines, function calls, and exceptions. On reset, the processor loads the LR value 0xFFFFFFFF.



The Program Counter (PC) is register R15. It contains the current program address. On reset, the processor loads the PC with the value of the reset vector, which is at address 0x00000004.



Program Status Register (PSR) - Application Program Status Register (APSR)

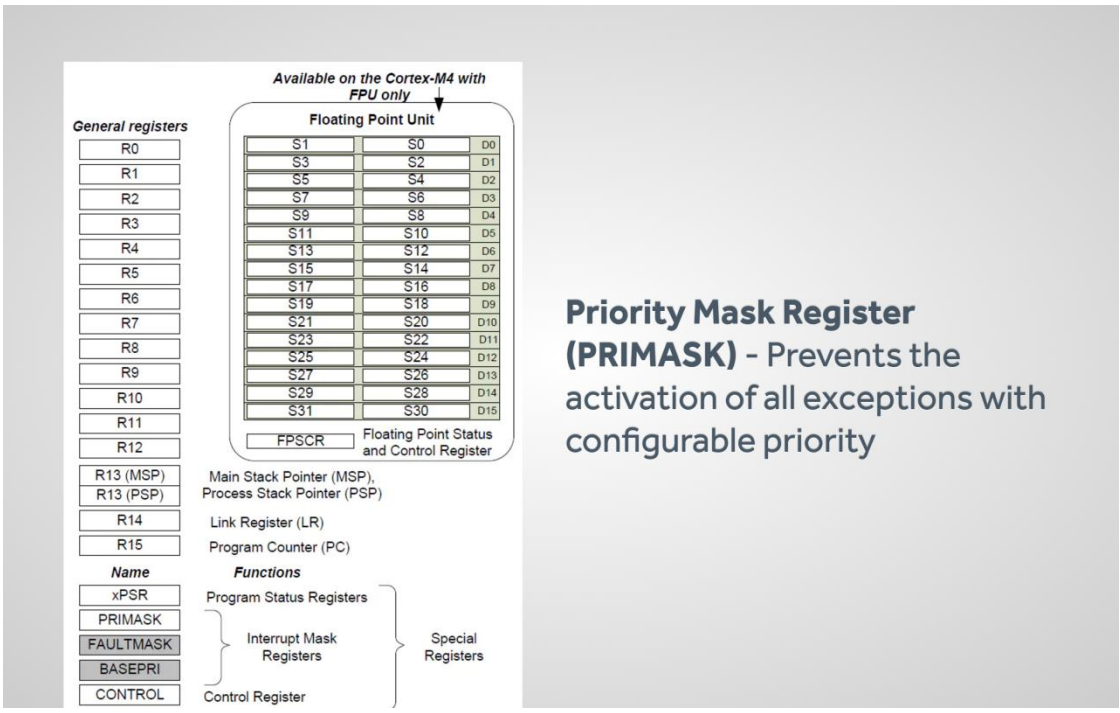
- Contains the current state of the condition flags from previous instruction executions

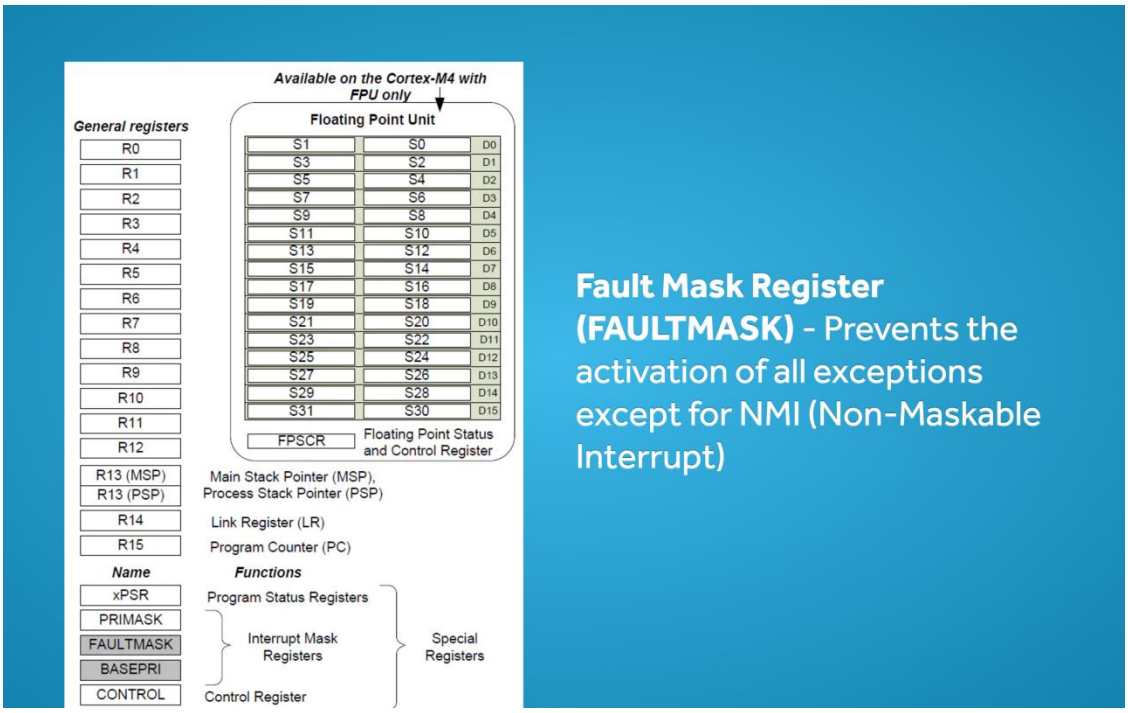
Interrupt Program Status Register (IPSR)

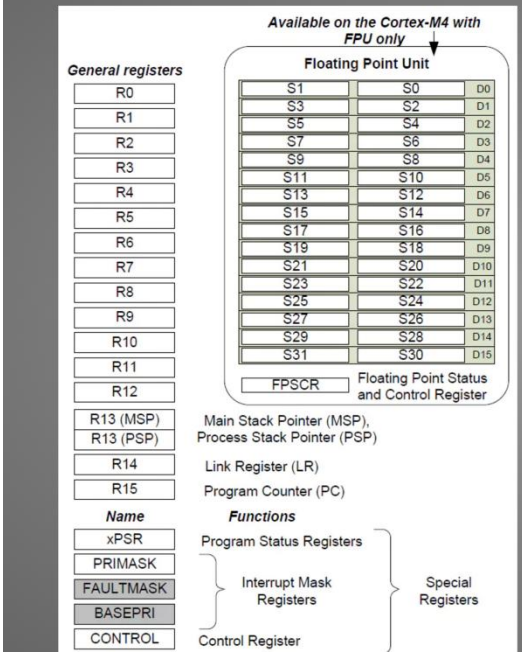
- Contains the exception type number of the current Interrupt Service Routine

Execution Program Status Register (EPSR)

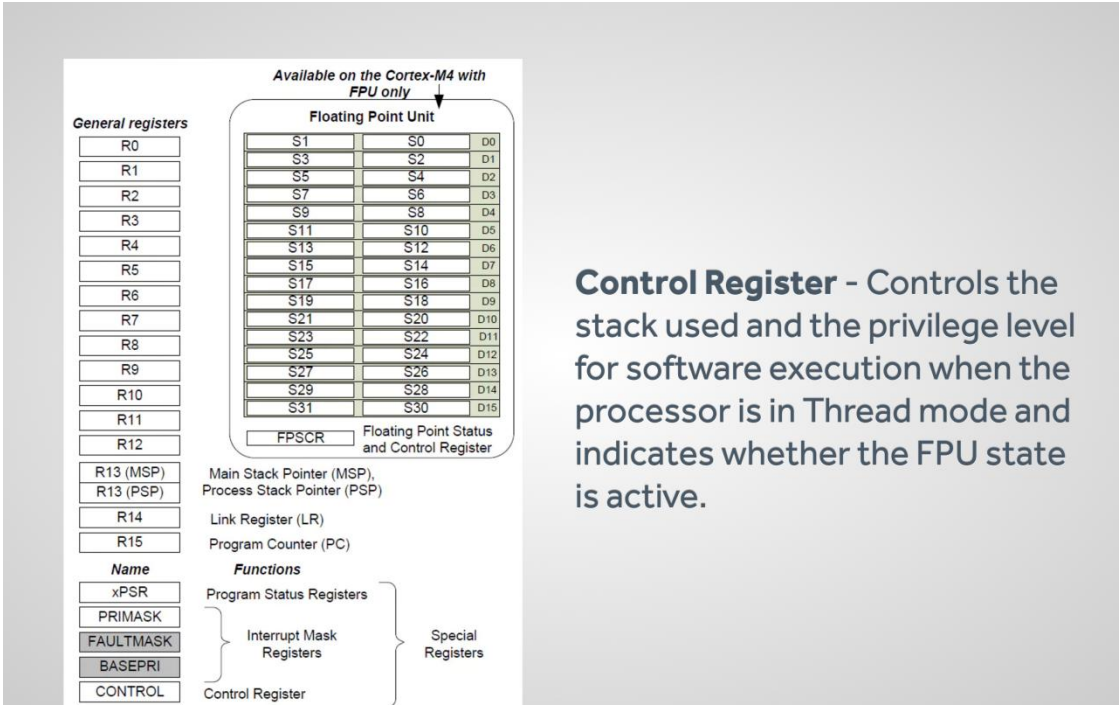
- Thumb state bit, and the execution state bits







Base Priority Mask Register (BASEPRI) - Defines the minimum priority for exception processing. When BASEPRI is set to a nonzero value, it prevents the activation of all exceptions with same or lower priority level as the BASEPRI value.



Cortex-M Registers

- R0 to R15, CONTROL and PRIMASK registers are available in all Cortex-M processors
- Two special registers FAULTMASK and BASEPRI are available only on M3, M4 and M7
- FPU register bank and FPSCR (Floating Point Status and Control Register) is available on M4, M7 (optional)