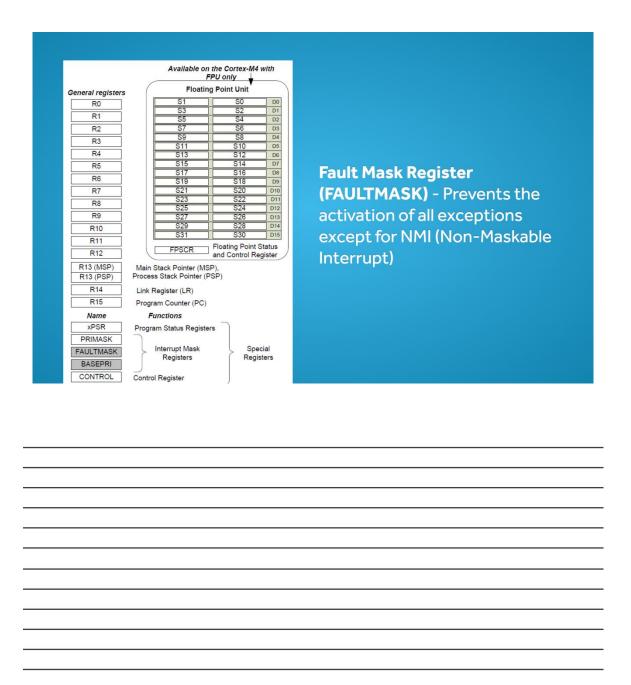
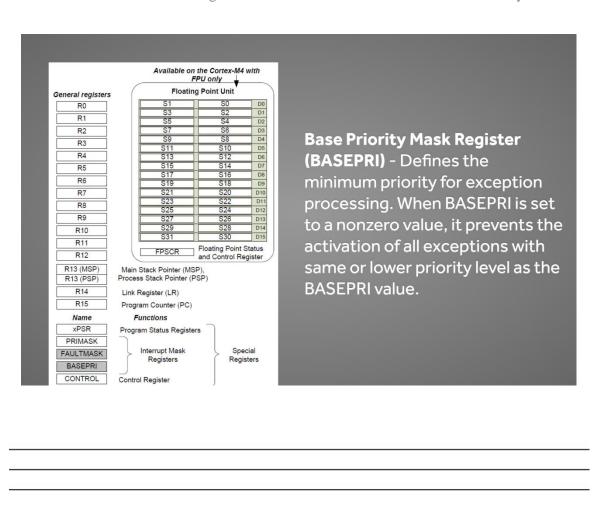


Floating Point Unit		Available on the Cortex-M4 with FPU only \downarrow	
S1		Flooring Boles Hols	
R1			
R2 S7 S6 D3		S3 S2 D1	
S9			
R3			
S15		S11 S10 D5	
R6			
R8 R8 R9 R10 R11 R11 R12 R13 (MSP) R13 (MSP) R14 R15 Program Counter (PSP) Link Register (LR) Program Status Registers RS PRIMASK RABI RITO R14 R15 R15 Program Status Registers PRIMASK RABI RITO R15 R16 R17 R17 R17 R17 R17 R18 R19			
R8 R9 R10 R11 R11 R12 R13 (MSP) R13 (PSP) R14 R15 Program Counter (PSP) Link Register (LR) Program Status Registers PRIMASK PAULTMASK BASEPRI R8 S22 S22 D13 S22 D13 S25 S24 D12 S27 S28 D14 S29 S28 Configurable priority Configurable priority Special Registers Registers			Priority Mask Register
R8 R9 R10 R10 R11 R11 R12 R13 (MSP) R13 (PSP) R14 Link Register (LR) R15 Program Counter (PC) Name XPSR PRIMASK BASEPRI R10 R10 S29 S29 S28 D13 S29 S28 D14 S27 S28 D18 Configurable priority (PRIMASK) - Prevents the activation of all exceptions with configurable priority (PRIMASK) - Prevents the activation of all exceptions with configurable priority			
R10 R11 R12 R13 (MSP) R14 (Link Register (LR) R15 Program Counter (PC) Name XPSR PRIMASK BASEPRI R10 S29 S28 D14 S31 S30 D15 R14 S31 S30 D15 R15 FPSCR Floating Point Status and Control Register R17 R18 R19 S29 S28 D18 R29 Configuration of all exceptions with configurable priority activation of all exceptions with configurable priority		S25 S24 D12	(PRIMASK) - Prevents the
R11 R12 R13 (MSP) R13 (MSP) R13 (PSP) R14 R15 R15 Program Counter (PC) Name xPSR PRIMASK BASEPRI FISCR Floating Point Status and Control Register Floating Point Status Configurable priority configurable priority configurable priority configurable priority should be priority configurable priority configurable priority Interrupt Mask Register Special Registers Registers			
R11 R12 R13 (MSP) R13 (MSP) R13 (PSP) R14 R15 R15 Program Counter (PC) Name xPSR PRIMASK BASEPRI FISCR Floating Point Status and Control Register Floating Point Status Configurable priority configurable priority configurable priority configurable priority should be priority configurable priority configurable priority Interrupt Mask Register Special Registers Registers			activation of all exceptions with
R13 (MSP) R13 (PSP) R14	10.0000	FDSCP Floating Point Status	
R13 (PSP) Process Stack Pointer (PSP) R14 Link Register (LR) R15 Program Counter (PC) Name Functions XPSR Program Status Registers PRIMASK FAULTMASK BASEPRI Process Stack Pointer (PSP) Link Register (LR) Program Counter (PC) Summer Functions Functions Special Registers Registers		and Control Register	configurable priority
R14 Link Register (LR) R15 Program Counter (PC) Name Functions XPSR Program Status Registers PRIMASK FAULTMASK BASEPRI Link Register (LR) Forgram Counter (PC) Special Registers Special Registers			
R15 Program Counter (PC) Name Functions xPSR Program Status Registers PRIMASK FAULTMASK BASEPRI Program Counter (PC) Functions Special Registers Special Registers			
Name Functions xPSR Program Status Registers PRIMASK FAULTMASK BASEPRI Functions Special Registers Registers Special Registers			
XPSR Program Status Registers PRIMASK FAULTMASK BASEPRI Registers Special Registers Registers			
PRIMASK FAULTMASK BASEPRI Interrupt Mask Registers Special Registers			
FAULTMASK Registers Special Registers		Program Status Registers	
BASEPRI Registers Registers		Interrupt Mask Special	
CONTROL Control Register			
	CONTROL	Control Register	





	Available on the Cortex-M4 with FPU only ↓	
General registers	Floating Point Unit	
R0	S1 S0 D0	
R1	S3 S2 D1	
R2	S5 S4 D2 S7 S6 D3	
R3	S9 S8 D4	
R4	S11 S10 D5 S13 S12 D6	
R5	S15 S14 D7	
R6	S17 S16 D8	Control Register - Controls the
R7	S19 S18 D9 S21 S20 D10	_
R8	S23 S22 D11	stack used and the privilege leve
R9	\$25 \$24 D12 \$27 \$26 D13	for software execution when the
R10	S29 S28 D14	
R11	S31 S30 D15	processor is in Thread mode and
R12	FPSCR Floating Point Status and Control Register	
R13 (MSP)	Main Stack Pointer (MSP).	indicates whether the FPU state
R13 (PSP)	Process Stack Pointer (NSP)	is active.
R14	Link Register (LR)	is active.
R15	Program Counter (PC)	
Name	Functions	
xPSR	Program Status Registers	
PRIMASK		
FAULTMASK	Interrupt Mask Special Registers Registers	
BASEPRI	Registers	
CONTROL	Control Register	

Cortex-M Registers

- R0 to R15, CONTROL and PRIMASK registers are available in all Cortex-M processors
- Two special registers FAULTMASK and BASEPRI are available only on M3, M4 and M7
- FPU register bank and FPSCR (Floating Point Status and Control Register) is available on M4, M7 (optional)

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