## Vector Table Offset Register (VTOR)

The VTOR is optional on Cortex-M0+ and Cortex-M23 processors.

The vector table starting address can be changed by programming VTOR. This is a useful feature for:

- Relocating vector table to SRAM to allow dynamically changing exception handler entrance points
- Relocating vector table to SRAM for faster vector fetch (if flash memory is slow)
- Relocating vector table to a different one in ROM (or flash), so that different stage of program execution can have different exception handlers.

## Vector Table Offset Register (VTOR)

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | | TBLOFF[29:16] | | | | | | | | | | | | | |
| | | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TBLOFF[15:9] | | | | | | | Reserved | | | | | | | | |
| rw | rw | rw | rw | rw | rw | rw | | | | | | | | | |

Bits 31:30 Reserved, must be kept cleared

Bits 29:9 **TBLOFF**: Vector table base offset field.
It contains bits [29:9] of the offset of the table base from memory address 0x00000000. When setting TBLOFF, you must align the offset to the number of exception entries in the vector table. The minimum alignment is 128 words. Table alignment requirements mean that bits[8:0] of the table offset are always zero.
Bit 29 determines whether the vector table is in the code or SRAM memory region.
0: Code
1: SRAM
*Note: Bit 29 is sometimes called the TBLBASE bit.*

Bits 8:0 Reserved, must be kept cleared

 