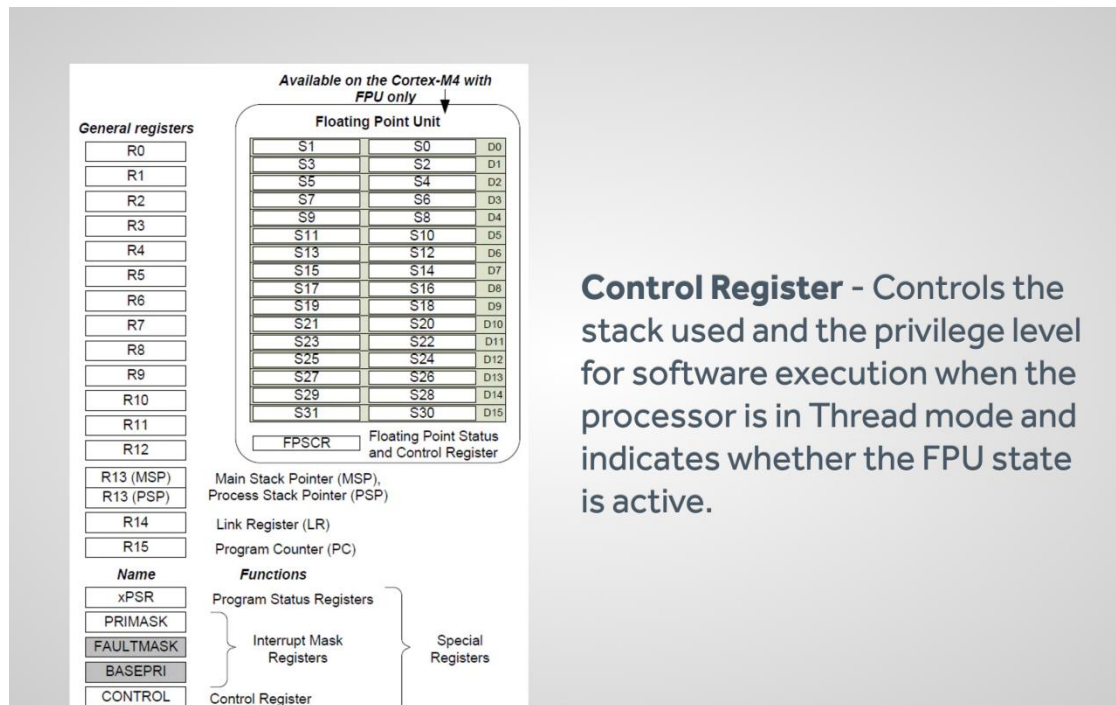


Base Priority Mask Register (BASEPRI) - Defines the minimum priority for exception processing. When BASEPRI is set to a nonzero value, it prevents the activation of all exceptions with same or lower priority level as the BASEPRI value.



Cortex-M Registers

- R0 to R15, CONTROL and PRIMASK registers are available in all Cortex-M processors
- Two special registers FAULTMASK and BASEPRI are available only on M3, M4 and M7
- FPU register bank and FPSCR (Floating Point Status and Control Register) is available on M4, M7 (optional)
