USB 2.0
Transceiver and Macrocell Tester
(T&MT) Interface
Specification

Version 1.2
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1 Preface

1.1 *Scope of this Revision*

This revision contains minor changes.

1.2 *Revision History*

Revision Number	Date	Description
1.2	4/4/01	1. Minor changes
1.1	01/12/01	1. In Table 3 changed VBUS_OUT to be no connect. 2. Specified USB connector B in para. 4.1
1.0	12/11/00	1. Added description for the VBUS_OUT pin in table 3. 2. Added description of the Data bus in section 4.3.
0.9	10/18/00	1. Removed sections 5 and 6. 2. Modified Figure 2 Connector Pin Layout. Added Daughter Card Present sense pin 49. Made pins 50 and 78 General Purpose IO (GPIO). 3. Modified Figure 1 Daughter Card Mechanical Dimensions to show the T&MT outline for reference only. 4. Modified table 3 to account for the pin changes as described in 1. 5. Modified Table 8 Data Interface Signals to include the IFType dependence.
0.41	9/13/00	1) Added IFType signals
0.4	9/12/00	1) Added Tables 9 & 10 2) Minor text changes
0.31	9/7/00	1) Added disclaimer 2) Added Mechanical section
0.3	9/1/00	Initial release

2   Introduction

2.1   General Description

This document specifies Transceiver and Macrocell Tester's (T&MT) mechanical and electrical interface to test the USB 2.0 Macrocell and Transceiver (PHY).   The PHY is a part of the Daughter Card (UUT) that will plug into the T&MT.

The Daughter Card dimensions and placement of the interfacing connector are shown in this document. The Connector pin assignment is described here using the naming convention of the USB 2.0 Universal Transceiver Macrocell Interface (UTMI) Specification.

The electrical interface depicts the timing diagrams for 30 and 60 MHz parallel digital interface.

2.2   Features of the T&MT

- Supplies 3.3 +/- .3 Volts to the Daughter Card;
- Interfaces through 100 pin Amp connector;
- Tests 8 bit uni-directional parallel digital interface @ 60 MHz;
- Tests 16 bit bi-directional parallel digital interface @30 MHz;
- Supports Tests Modes per USB 2.0 Standard;
- Supports USB 2.0 Protocol Layer in the Device Emulator mode;
- Behaves as a packet generator and receiver in the Packet Blaster Mode;
- Tests PHY in the High and Full Speed Modes;
- Allows for interactive user interface to set the test mode and to display pertinent information.

2.3   References:

- USB 2.0 Universal Transceiver Macrocell Interface (UTMI) Specification;
- USB 2.0 Specification;

3 Test Mode Description

3.1.1 USB 2.0 Test Modes

Test modes as required by the USB 2.0 Standard are supported as specified in the table below. The tests specified herein are executed and controlled by a combination of the hardware and firmware.

Table 1: USB 2.0 Test Modes

Test Modes	PHY Setup		
	Operational Mode (OpMode)	Data Pattern	XcvrSelect & TermSelect
SE0_NAK	Normal (0)	No transmit	HS
J	Disable (2)	All '1's	HS
K	Disable (2)	All '0's	HS
USB 2.0 Test Packet (*)	Normal (0)	Test Packet data	HS

(*) Data structure for the USB2.0 Test Packet is defined in Chapter 7 of the USB 2.0 Specification.

3.1.2 Operational and USB communication Tests

The purpose of the operational tests is to check the PHY capability of meeting operating modes and basic functionality as required by the USB2.0 UTMI specification. The USB communication tests allow for testing the UUT in the real operating system and environment. The tests specified herein are executed and controlled by a combination of hardware and firmware.

Table 2: Operational and USB2.0 Communication Test Modes

Test Modes	PHY Setup		
	Operational Mode (OpMode)	Data Pattern	XcvrSelect & TermSelect
Soft Disconnect	Non-Driving (1)	Tri-state	HS/FS
Suspend	Normal (0)	NC	FS
USB 2.0 Device communication with the HOST	Normal (0)	Various	HS and FS

4   Daughter Card (UUT) Specification

The PHY will be a part of the Daughter Card.   The T&MT provides 3.3 +/- .3 Volts supply. If the UUT requires anything besides 3.3V, it needs to be provided independently or derived from VDD on the Daughter Card. Unused pins of the interface connector must be terminated as described in the paragraph 4.2

4.1   Daughter Card Mechanical Dimensions

The USB connector type 'B' should be placed in the I/O window on the left side of the PCB as shown in figure below.

Figure 1 Daughter Card Mechanical Dimensions

All dimensions are in mm: Tolerances ±0.127mm unless noted
(Drawing is not to scale)
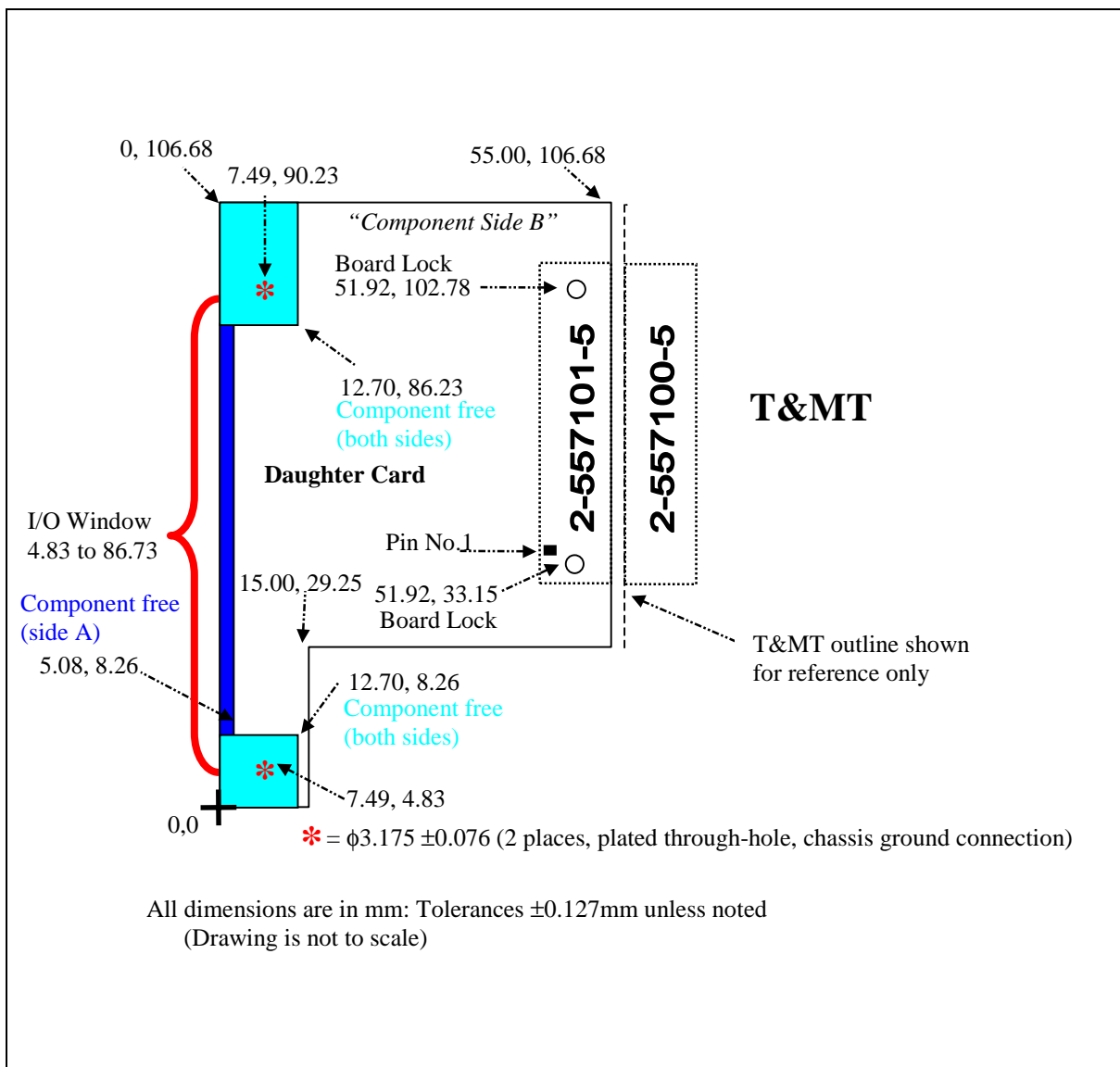
4.2   Daughter Card Connector Pin Layout

The IO connector (AMP PN 2-557101-5) on the daughter board has the following pins as shown in the figure below.

Figure 2 Connector Pin Layout

1	GPI0	26	GPIO1	51	GND	76	GND
2	GND	27	GND	52	System Clock	77	ValidH
3	GPIO2	28	VBUS_out	53	GND	78	GPIO14
4	GND	29	GPIO3	54	GND	79	Vctrl1
5	GPIO4	30	VendorID_0	55	Vctrl0	80	GND
6	GPIO5	31	Data15	56	GPIO6	81	VDD
7	GPIO7	32	GND	57	VDD	82	Data14
8	VDD	33	Data13	58	GPIO8	83	Data12
9	GND	34	Data11	59	Vctrl2	84	GND
10	Vctrl3	35	GND	60	Tx_Valid	85	Data10
11	GPIO9	36	Data9	61	GPIO10	86	Data8
12	GPIO11	37	Data7	62	GND	87	VDD
13	GND	38	VDD	63	GPIO12	88	Data6
14	VcLoadM	39	GND	64	IFType0	89	IFType1
15	Vstatus4	40	Force_RxErr	65	GND	90	Clk
16	VDD	41	Data5	66	Rx_Active	91	Data4
17	Reset	42	Data3	67	Op_Mode0	92	GND
18	Op_Mode1	43	GND	68	GND	93	Data2
19	Xcvr_Select	44	Data1	69	VDD	94	Data0
20	Term_Select	45	Vstatus0	70	Vstatus1	95	GND
21	GND	46	GND	71	Vstatus2	96	Vstatus3
22	SuspendM	47	VBUS_IN	72	Rx_Valid	97	Vstatus5
23	Line_State0	48	Vstaus6	73	GND	98	Vstatus7
24	GND	49	DC_PSNT_N	74	Rx_Error	99	VendorID_1
25	Line_State1	50	GPIO13	75	Tx_Ready	100	GND

The Daughter card must drive unused pins with 1 KOhm pull-ups to VDD or 200 Ohm pull-downs.

With the board viewed from the backside of the connector, "Side A", and with the IO connector at the bottom, the connector pin numbers are shown in the figure below.

Figure 3 Connector View

49	47	45	43	41	39	37	35	33	31	29	27	25	23	21	19	17	15	13	11	9	7	5	3	1
50	48	46	44	42	40	38	36	34	32	30	28	26	24	22	20	18	16	14	12	10	8	6	4	2
99	97	95	93	91	89	87	85	83	81	79	77	75	73	71	69	67	65	63	61	59	57	55	53	51
100	98	96	94	92	90	88	86	84	82	80	78	76	74	72	70	68	66	64	62	60	58	56	54	52

4.3   Connector (UUT Side) Signal Description

4.3.1   Tester Specific Control Interface Signals

Table 3: Tester Interface Signals

Name	Direction (relative to UUT)	Active Level	Description
System Clock	Input	Rising Edge	**30 MHz System Clock.** May not be used if PHY generates clock.
GPIO	I/O/Bi-dir	N/A	**General Purpose I/O.** Spare interconnects between the UUT and T&MT.
Force_RxErr	Input	High	**Force Rx Error**. This signal goes high every 16 clocks and can be used by the UUT to create Rx Error.
VendorID (1-0)	Output	N/A	**VendorID.** [1] [0] Description 0 0 UTMI Compliant. 0 1 To be assigned 1 0 To be assigned 1 1 Intel
IFType (0-1)	Output	N/A	**Interface Type.** These signals encode the type of data interface supported by the UUT. The T&MT will reconfigure its interface accordingly. [1] [0] Description 0 0 0: 8-Bit Bi-directional –60 MHz 0 1 1: 8-Bit Uni-Directional – 60 MHz 1 0 2: 16-Bit Bi-Directional – 30 MHz 1 1 3: Reserved
VBUS_out	IN	N/A	**VBUS_OUT (+5 VDC).** No connect.
VBUS_in	Output	HIGH	**VBUS_in.** This signal is used by the T&MT to monitor pin#1 of the USB Connector. When high is detected, the usb cable is connected.
DC_PSNT_N	Output	LOW	**Daughter Card Present.** When low, the T&MT detects presence of the Daughter Card. A 200 Ohms pull down resistor is required.

4.3.2   System Interface Signals

Table 4: System Interface Signals

Name	Direction (relative to UUT)	Active Level	Description
Clk	Output	Rising-Edge	**Clock**. This output is used for clocking receive and transmit parallel data. 60 MHz HS/FS, with 8-bit interface 30 MHz HS/FS, with 16-bit interface
Reset	Input	High	**Reset.**
Xcvr_Select	Input	N/A	**Transceiver Select.** This signal selects between the FS and HS transceivers: 0: HS transceiver enabled 1: FS transceiver enabled
Term_Select	Input	N/A	**Termination Select.** This signal selects between the FS and HS terminations: 0: HS termination enabled 1: FS termination enabled
SuspendM	Input	Low	**Suspend.** Places the PHY in a mode that draws minimal power from supplies. Shuts down all blocks not necessary for Suspend/Resume operation. While suspended, **TermSelect** must always be in FS mode to ensure that the 1.5K pull-up on **DP** remains powered. 0: PHY circuitry drawing suspend current 1: PHY circuitry drawing normal current

Line_State (0-1)	Output	N/A	**Line State.** These signals reflect the current state of the single ended receivers. They are combinatorial until a "usable" **CLK** is available then they are synchronized to **CLK**. They directly reflect the current state of the **DP** (LineState[0]) and **DM** (LineState[1]) signals:
			DM DP Description
			  0 0 0: SE0
			  0 1 1: 'J' State
			  1 0 2: 'K' State
			  1 1 3: SE1

Op_Mode (0-1)	Input	N/A	**Operational Mode.** These signals select between various operational modes:
			[1] [0] Description
			  0 0 0: Normal Operation
			  0 1 1: Non-Driving
			  1 0 2: Disable Bit Stuffing and NRZI encoding
			  1 1 3: Reserved

4.3.3 Vendor Control Signals

Table 5: Vendor Control Signals

Name	Direction (relative to UUT)	Active Level	Description
VControlLoadM	Input	Low	**Vendor Control Load.** Assertion of this signal loads the Vendor Control register: 0: Load Vendor Control Register 1: NOP
VControl0-3	Input	Vendor Defined	**Vendor Control**. Vendor defined 4-bit parallel input bus.
VStatus0-7	Output	Vendor Defined	**Vendor Status**. Vendor defined 8-bit parallel output bus.

4.3.4 Data Interface Signals

Table 6: Transmit Control Interface Signals

Name	Direction (relative to UUT)	Active Level	Description
Tx_Valid	Input	High	**Transmit Valid**. Indicates that the **Data** bus is valid. The assertion of Transmit Valid initiates SYNC on the USB. The negation of Transmit Valid initiates EOP on the USB.
Tx_Ready	Output	High	**Transmit Data Ready**. If **TXValid** is asserted, the T&MT must transmit data on the rising edge of **CLK**. If **TXReady** is low, the T&MT must hold the previously asserted data on the **Data** bus.

Table 7: Receive Control Interface Signals

Name	Direction (relative to UUT)	Active Level	Description
Rx_Valid	Output	High	**Receive Data Valid**. Indicates that the receive bus has valid data.
Rx_Active	Output	High	**Receive Active**. Indicates that the receive bus is active. **RXActive** is negated after a Bit Stuff Error or an EOP is detected.
Rx-Error	Output	High	**Receive Error**. 0 Indicates no error. 1 Indicates that a receive error has been detected.

Table 8: Data Interface Signals

Depending on the IFType state, the T&MT will configure Data0 through Data15, transceiver parallel data bus, accordingly:

- IFType1 and IFType0 are pulled low, Data0 through Data7 bus operates in the bi-directional mode @ 60 MHz, T&MT tri-states Data8 through Data 15;

- IFType1 is pulled low and IFtype0 is pulled high, Data0 through Data7 is the transmit bus and Data8 through Data15 is the receive bus @ 60 MHz;

- IFType1 is pulled high and IFType0 is pulled low, Data0 through Data15 bus operates in the bi-directional mode @ 30 MHz.

Note: For all multi-bit signal descriptions, bit[0] is always the least significant bit of the referenced value.

Name	Direction (relative to UUT)	Active Level	Description
Data0-7	Input / Bidir (tri-state)	N/A	**Data**. 8-bit parallel USB data input (transmit) bus when **IFType** = 01. Low byte of bi-directional parallel USB data bus when **IFType**= 10. In this mode the T&MT tri-states the bus, except when it is in transmit mode. 8 bit bi-directional parallel data bus when **IFType**= 00. In this mode the T&MT tri-states the bus, except when is in the transmit mode. During Reset this bus is tri-stated.
Data8-15	Output/ Bidir (tri-state)	N/A	**Data**. 8-bit parallel USB data output (receive) bus when **IFType**= 01. High byte of bi-directional parallel USB data bus when **IFType**= 10. In this mode the T&MT tri-states the bus, except when it is in transmit mode. Unused when the **IFType** is set 00. In this mode, the T&MT tri-states this bus. During Reset this bus is tri-stated.
ValidH	Bidir (tri-state)	High	**ValidH**. This signal indicates that the high order 8 bits of a 16-bit data word presented on the **Data8-15** bus are valid. When **IFType**= 10 and **TXValid** = 0 this signal indicates that the high order receive data byte on the **Data8-15** bus is valid. When **IFType** = 10 and **TXValid** = 1, this signal indicates that the high order transmit data byte, presented on the **Data8-15** bus by the transceiver is valid.

4.4 Parallel Digital Interface Timing

4.4.1 HS/FS Interface Timing – 60 MHz

The timing that is specified herein is for reference only and shown for the 8 bit uni-directional bus. It is assumed that the T&MT signals will need maximum ~8.6 ns second of set up time allowing for 8 ns of Daughter Card signals clock to output valid delay. A hold of 1 ns is required to account for parallel data lines group skew restively to clock. Also, the T&MT signals will have a maximum clock to output delay of 8.6 ns allowing for 8 ns setup to the Daughter Card signals.

Note that the timing here needs to be met at the connector driving a 50 Ohms and 20 pF load.
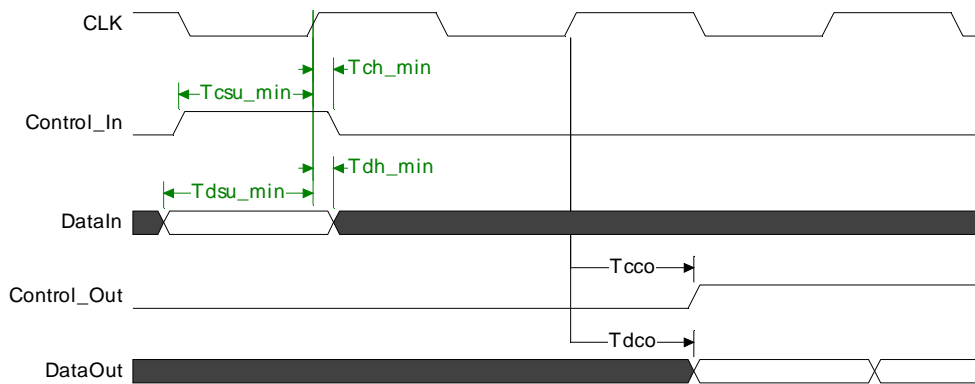
Figure 4 60 MHZ Interface Timing Constraints

Table 9 60 MHz Timing

Name	Min	Max	Comment
Tcsu_min	8		Minimum setup time for Tx_Valid
Tch_min	1		Minimum hold time for Tx_Valid
Tdsu_min	8		Minimum setup time for Data (transmit direction)
Tdh_min	1		Minimum hold time for Data (transmit direction)
Tcco	1	8	Clock to Control out time for Tx_Rdy, Rx_Valid, Rx_Active, Rx_Error
Tcdo	1	8	Clock to Data out time (receive direction)

4.4.2　HS/FS Interface Timing – 30 MHz

The timing that is specified herein is for reference only. It is assumed that the T&MT signals will need maximum ~13 ns of setup time allowing for 20 ns of Daughter Card signals clock to output valid delay. A hold of 1 ns is required to account for parallel data lines group skew relatively to the clock. Also, the T&MT signals will have a maximum clock to output delay of 13 ns allowing for 20 ns setup to the Daughter Card signals.

Note that the timing here needs to be met at the connector with a 50 Ohm and 20 pF load.
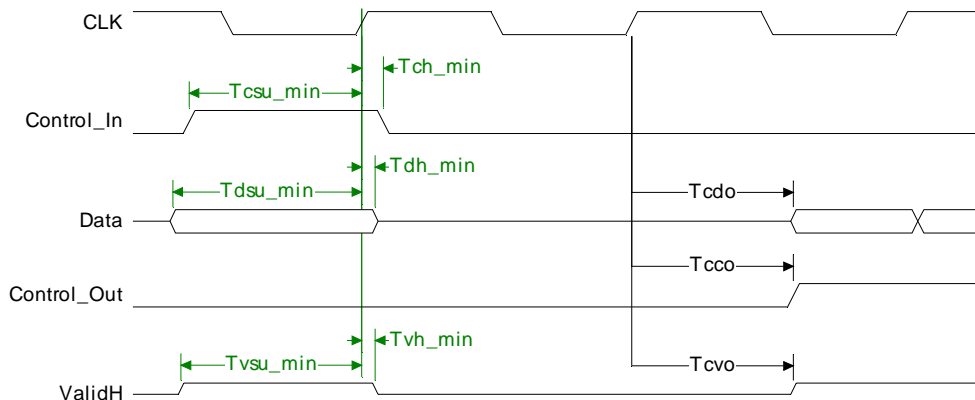
Figure 5 30 MHz Interface Timing Constraints

Table 10 30 MHz Timing

Name	Min	Max	Comment
Tcsu_min	20		Minimum setup time for Tx_Valid
Tch_min	1		Minimum hold time for Tx_Valid
Tdsu_min	20		Minimum setup time for Data (transmit direction)
Tdh_min	1		Minimum hold time for Data (transmit direction)
Tcco	1	20	Clock to Control out time for Tx_Ready, Rx_Valid, Rx_Active, Rx_Error
Tcdo	1	20	Clock to Data out time (receive direction)
Tvsu_min	20		Minimum setup time for ValidH (transmit direction)
Tvh_min	1		Minimum hold time for ValidH (transmit direction)
Tcvo	1	20	Clock to ValidH out time (receive direction)