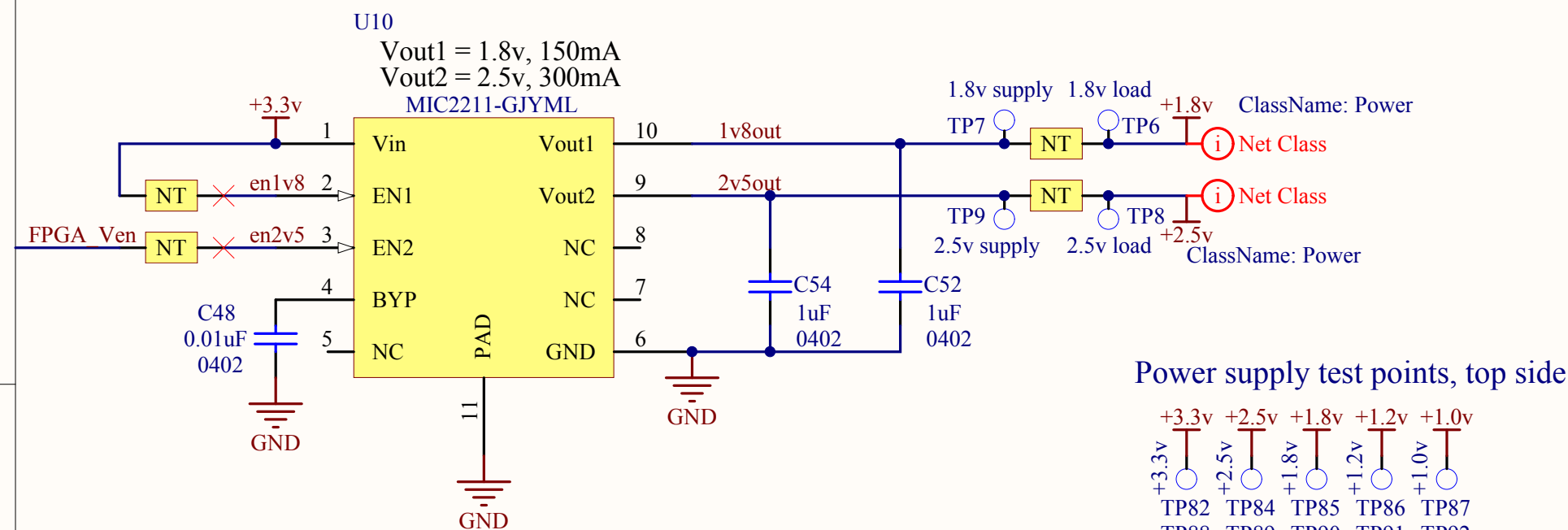
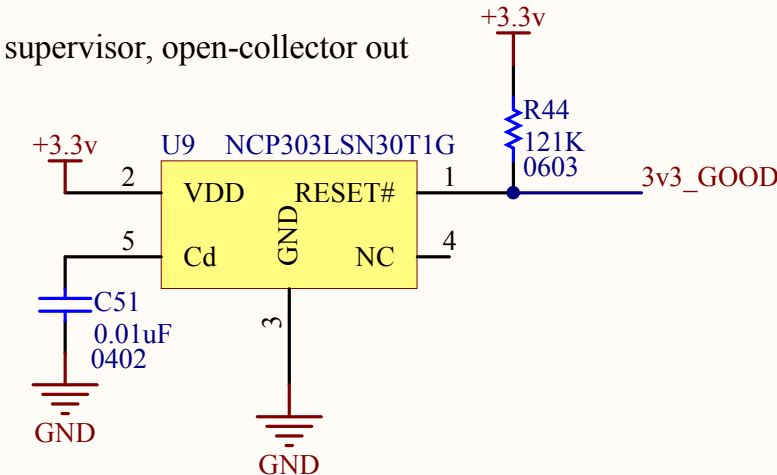


A

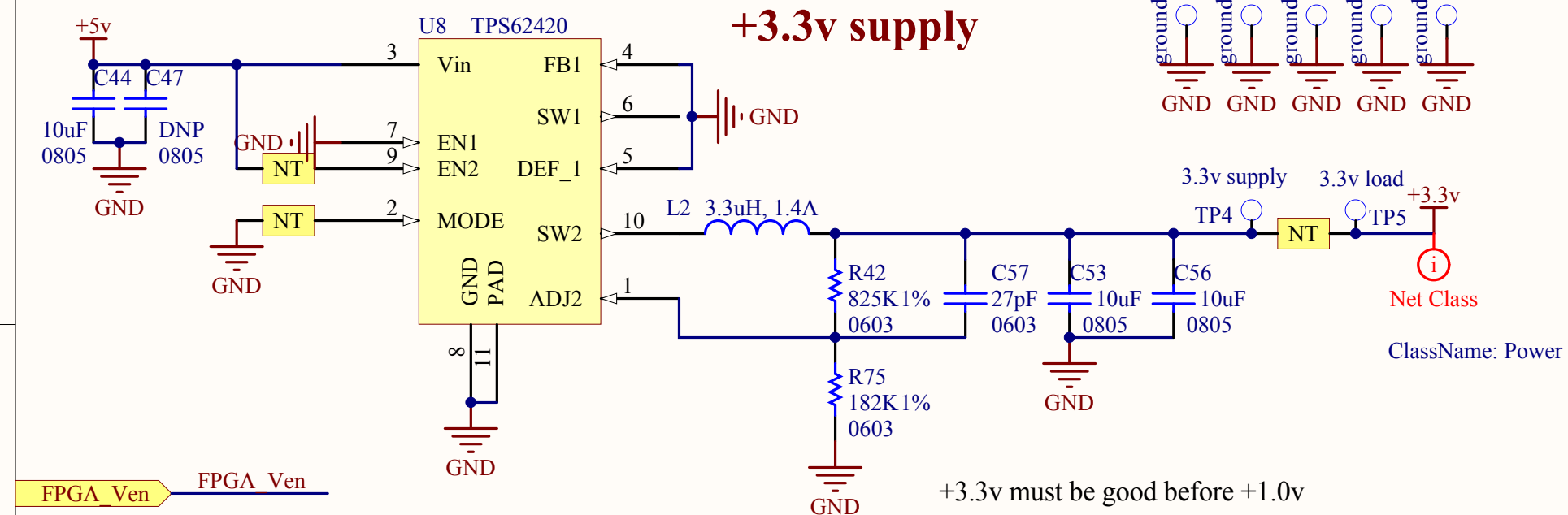


3.0v supervisor, open-collector out

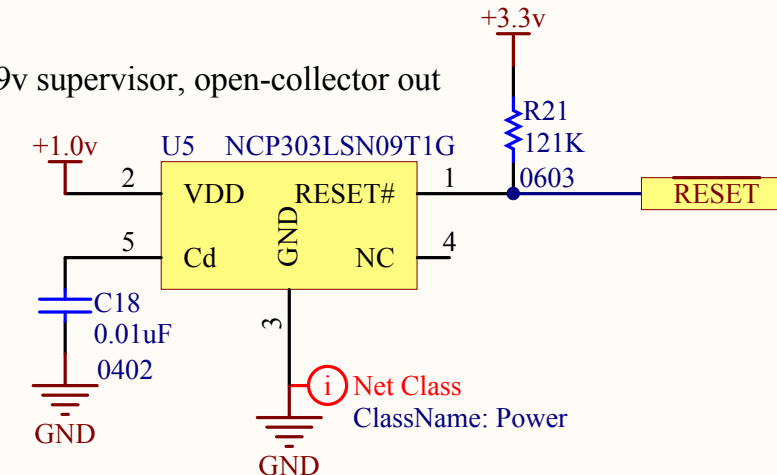


A

B

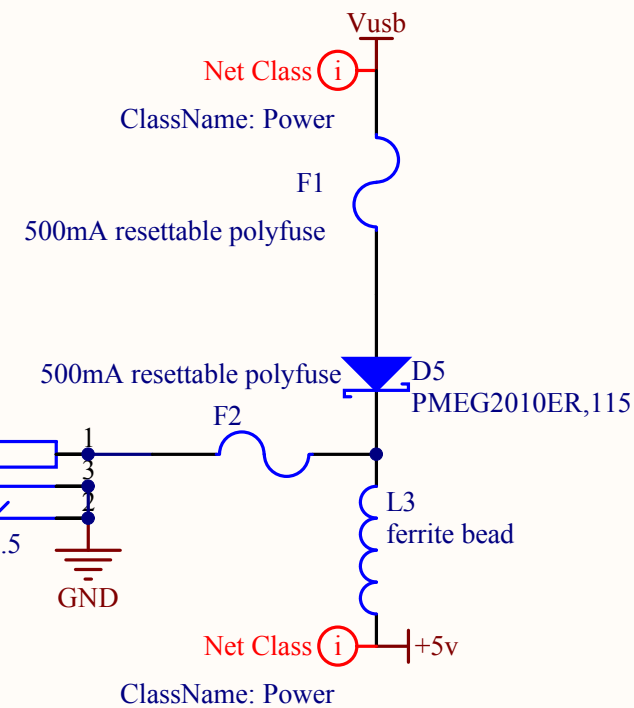
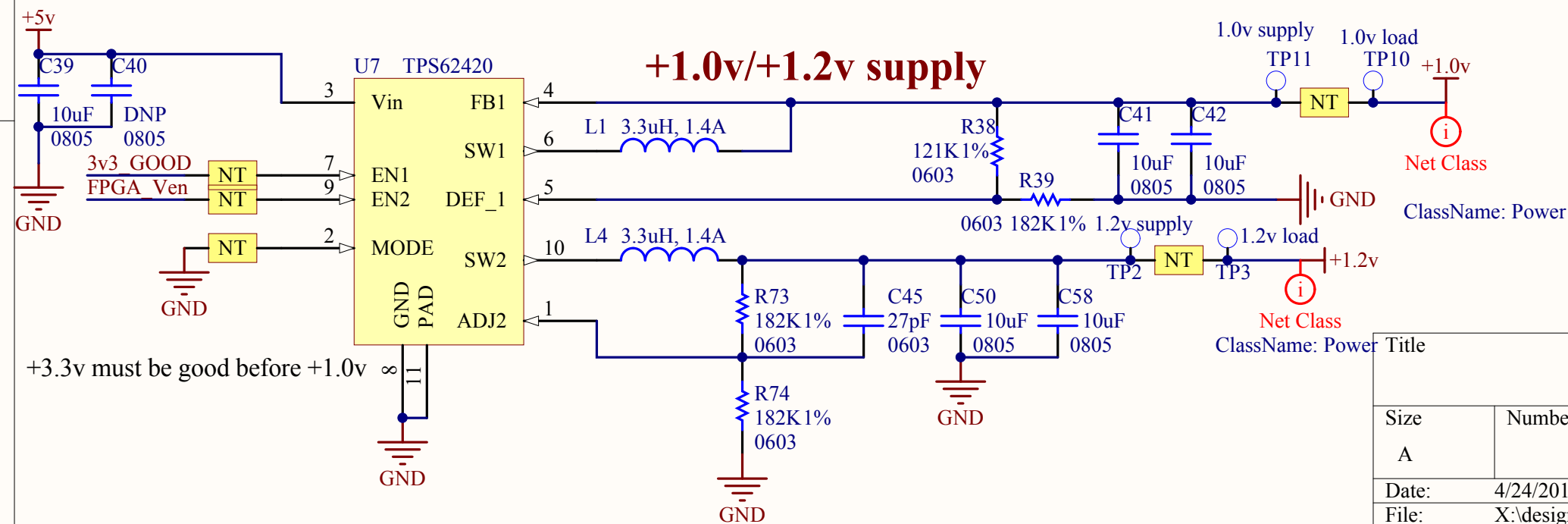


0.9v supervisor, open-collector out



B

C



C

D

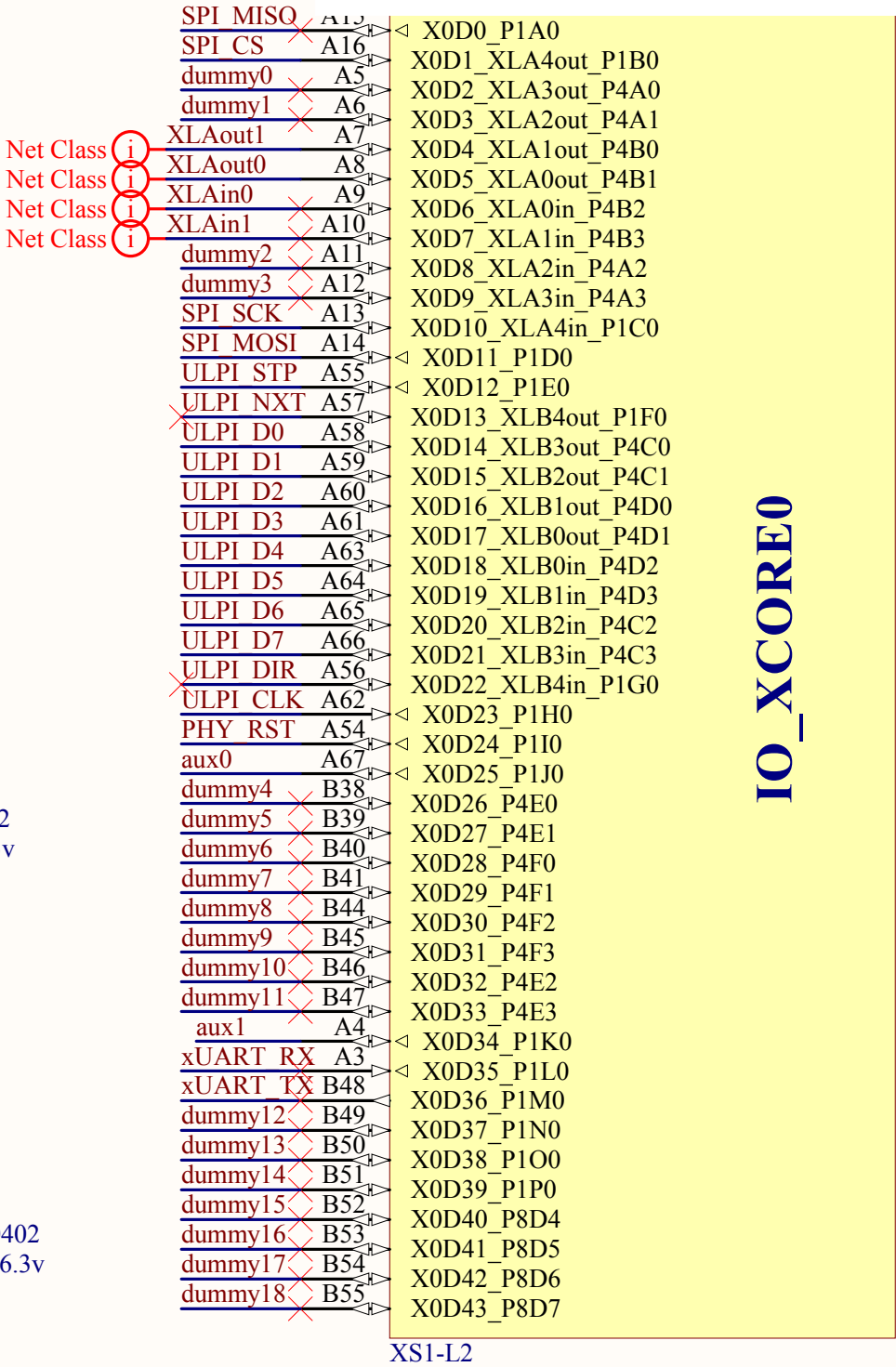
Title		
Size	Number	
A		
Date:	4/24/2011	Sheet 1 of
File:	X:\design\power supplies.SchDoc	Drawn By:

D

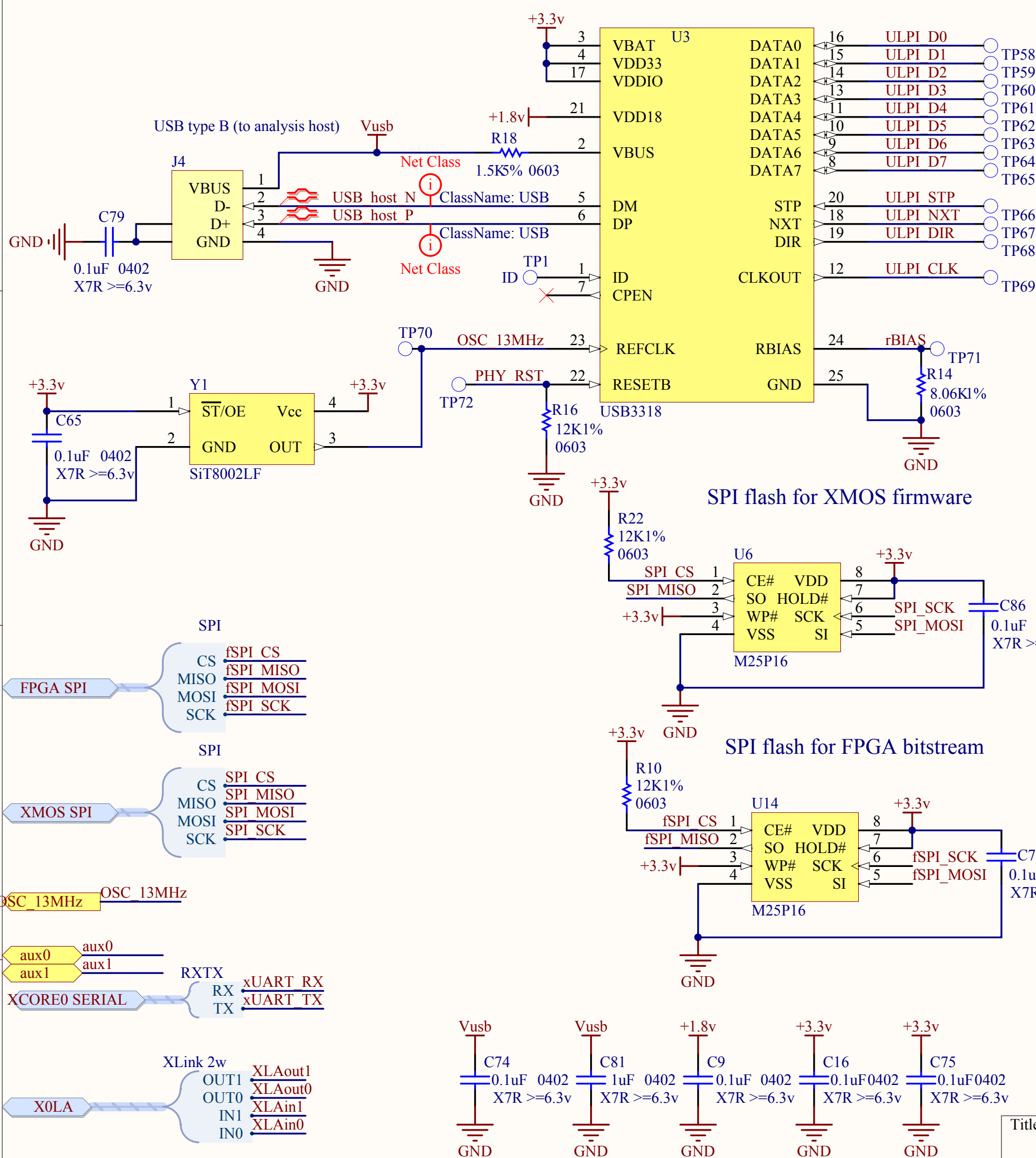
O nly the following I/Os are available in ULPI mode:

P1A0, P1B0, P1C0, P1D0,
P1I0, P1J0, P1K0, P1L0, P1M0

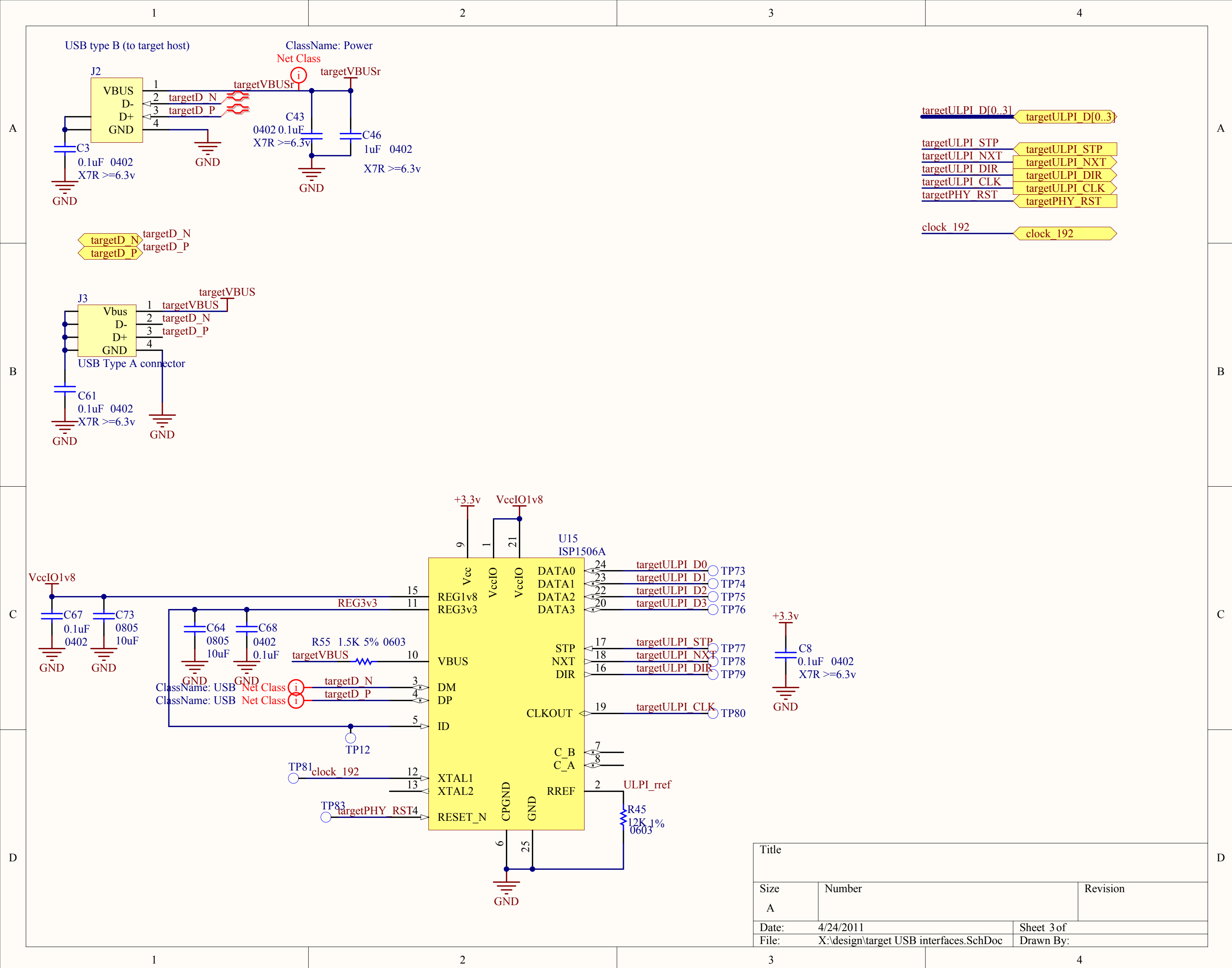
All other pins are unavailable and are marked with
dummy nets to ease layout.



2. P1A, P1D, P1E, P1H, P1I, P1J,
P1K and P1L are nominal 8mA
drivers, the remainder of the
general purpose I/O are 4mA.



Title		
Size	Number	Revision
A		
Date:	4/24/2011	Sheet2 of
File:	X:\design\host interface.SchDoc	Drawn By:



A

A

B

B

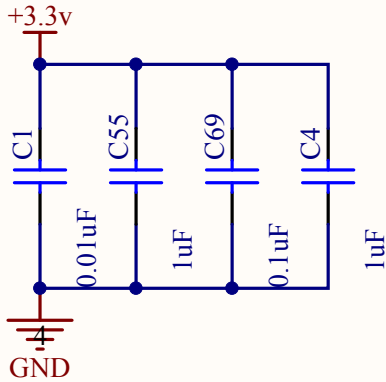
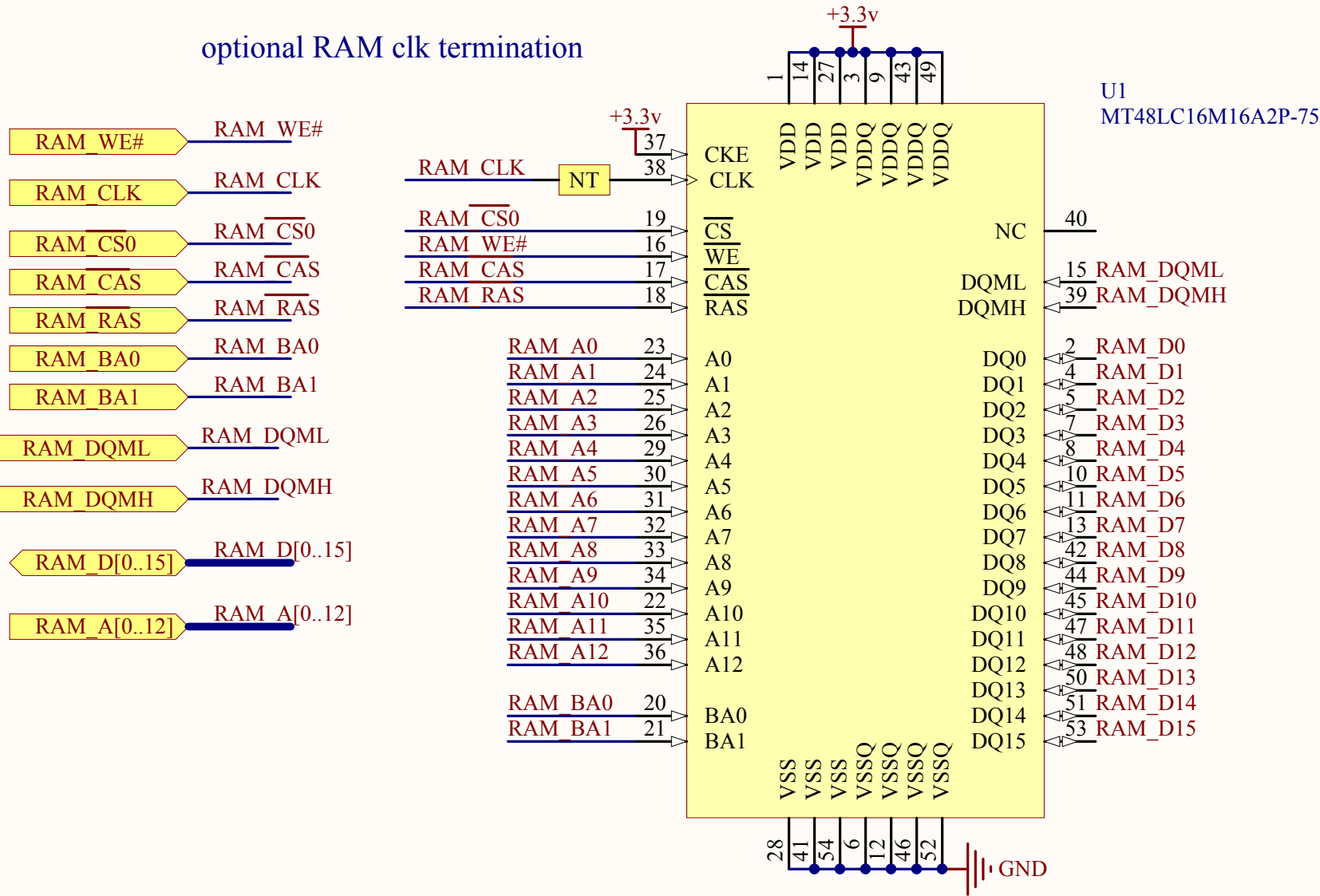
C

C

D

D

optional RAM clk termination



Title			
Size	Number		Revision
A			
Date:	4/24/2011		Sheet of
File:	X:\design\RAM.SchDoc		Drawn By:

A

B

C

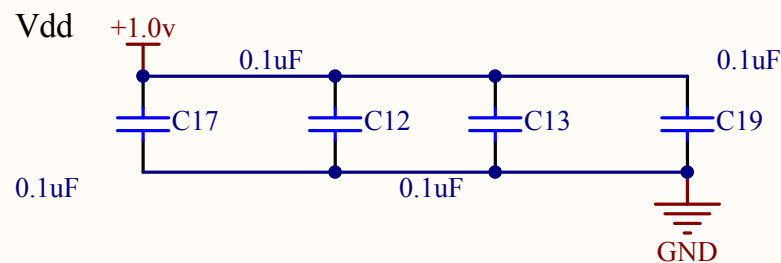
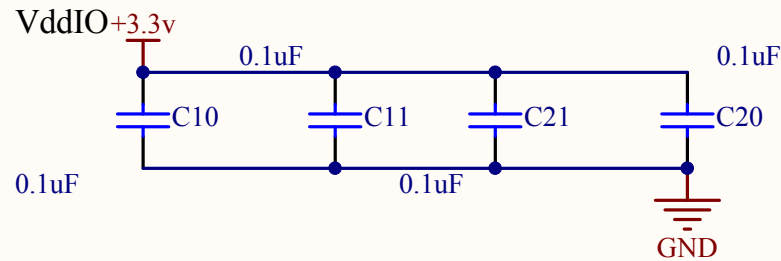
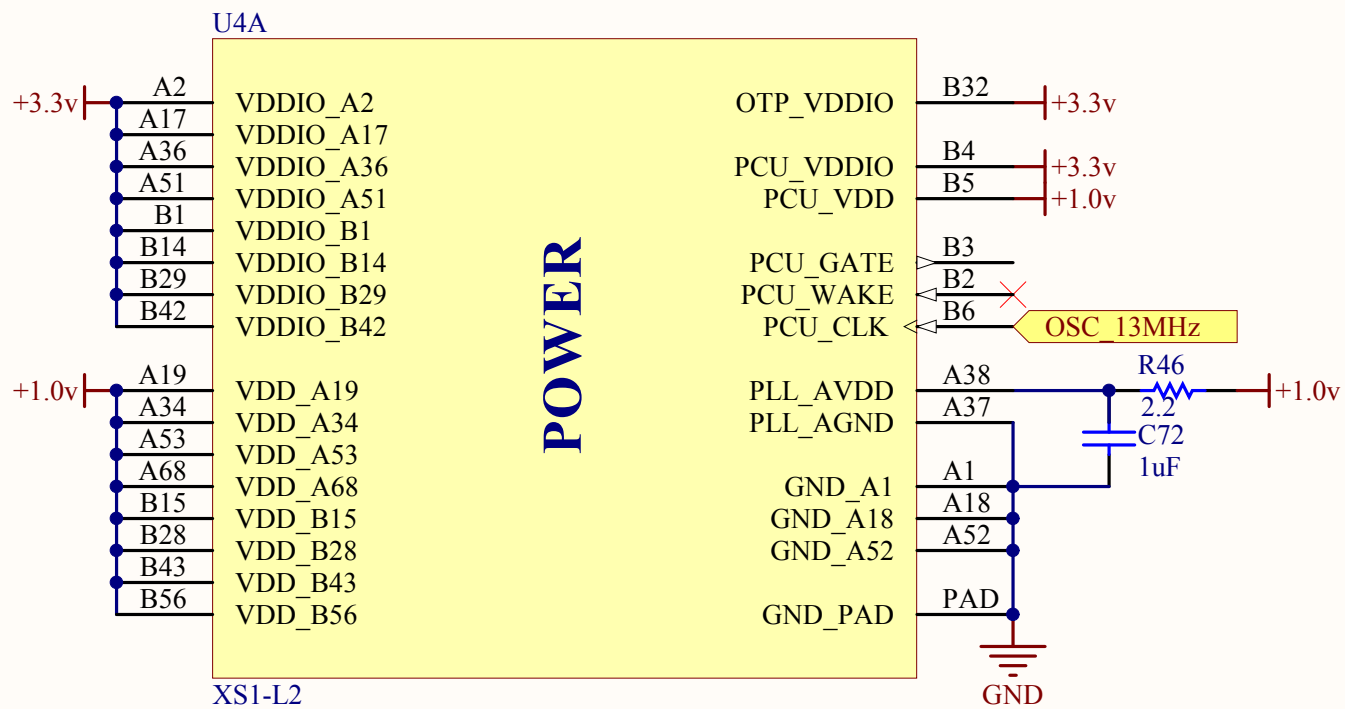
D

A

B

C

D



Title		
Size	Number	Revision
A		
Date:	4/24/2011	Sheet 5 of
File:	X:\design\XMOS power.SchDoc	Drawn By:

A

A

B

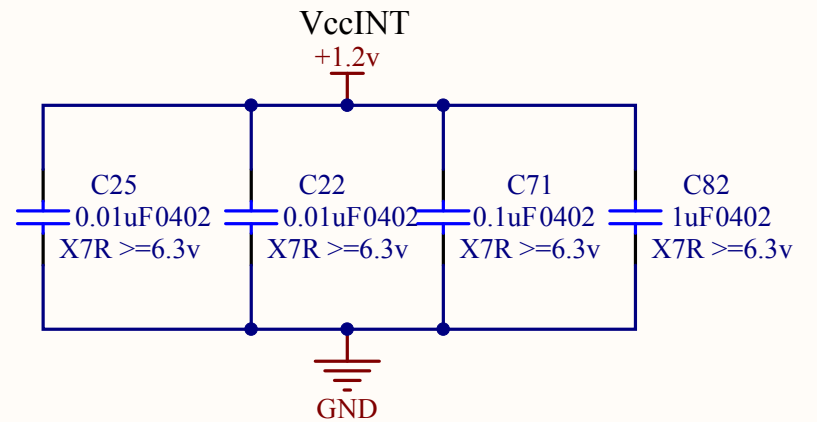
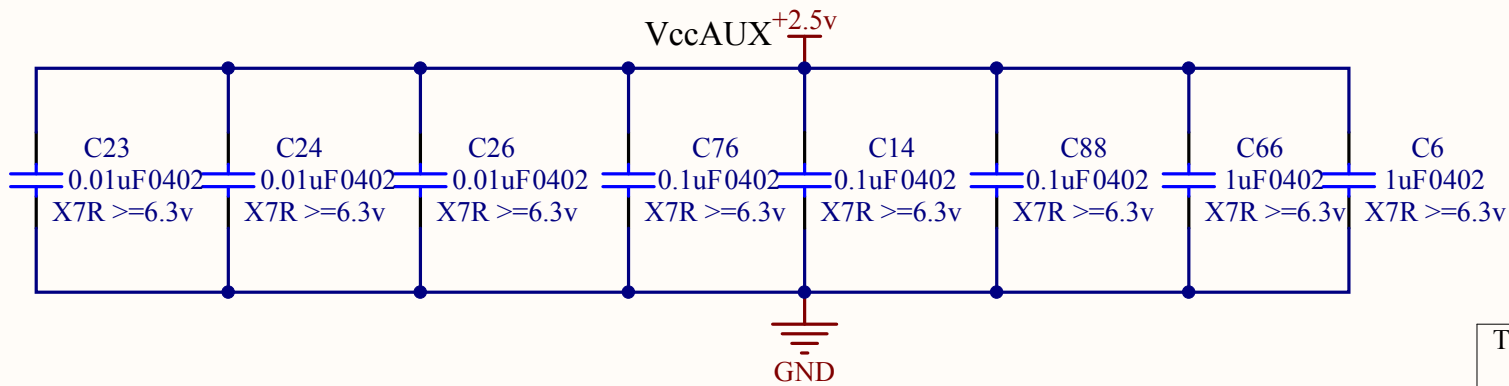
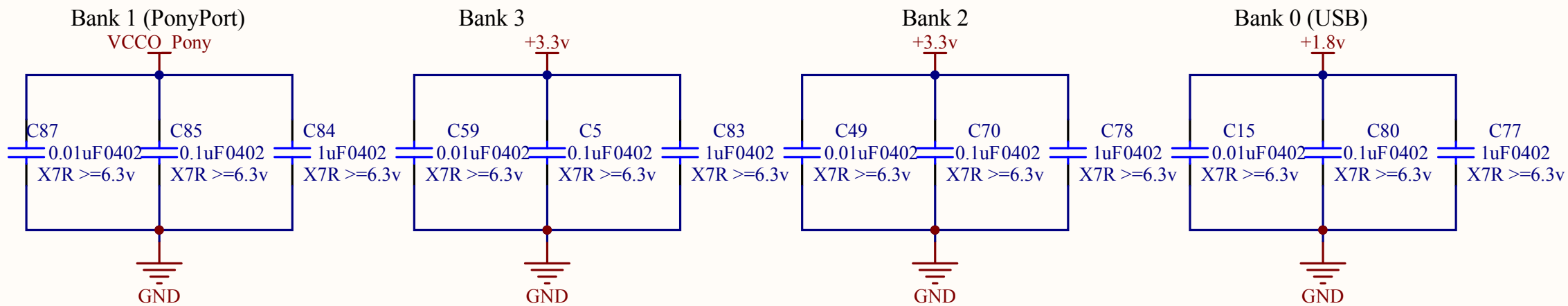
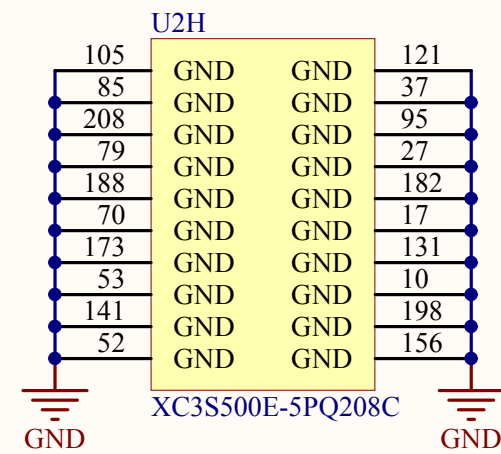
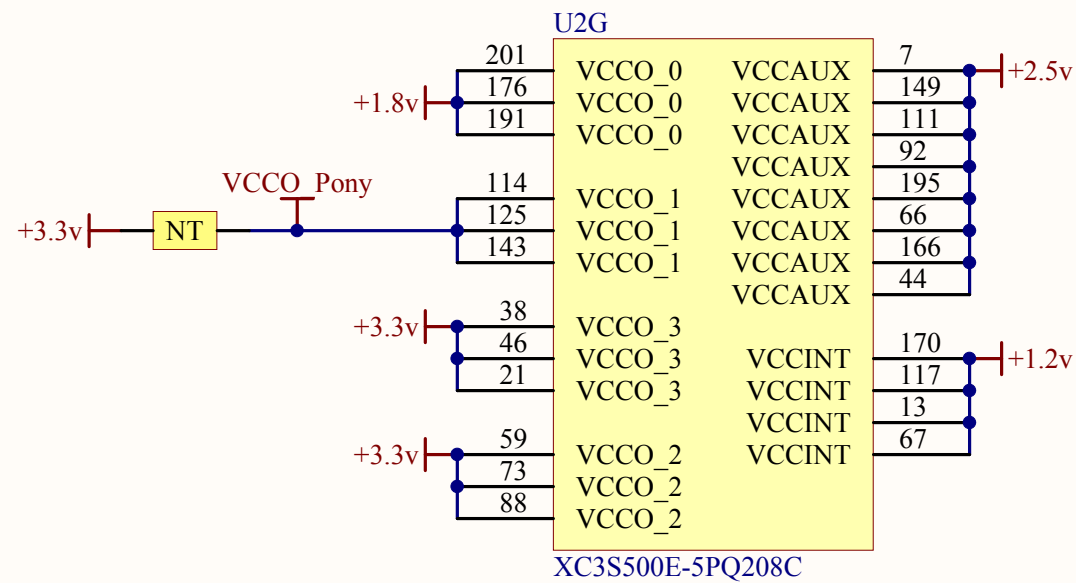
B

C

C

D

D

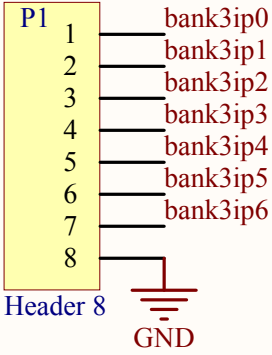
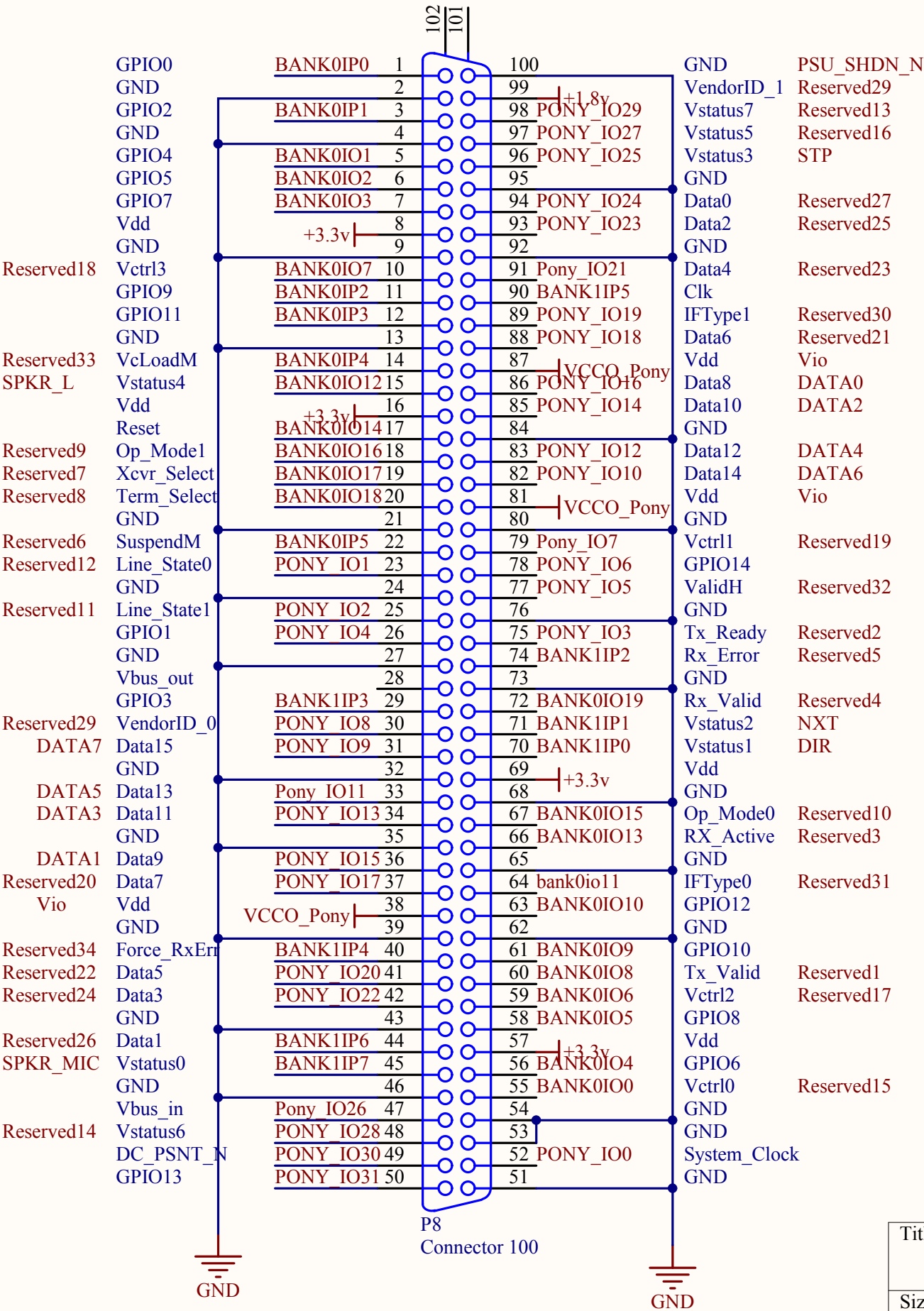


Title		
Size	Number	Revision
A		
Date:	4/24/2011	Sheet 6 of
File:	X:\design\FPGA power.SchDoc	Drawn By:



XC3S500E-5PQ208C		
Title		
Size A	Number	Revision
Date:	4/24/2011	Sheet 7 of
File:	X:\design\FPGA.SchDoc	Drawn By:

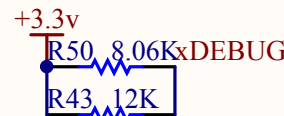
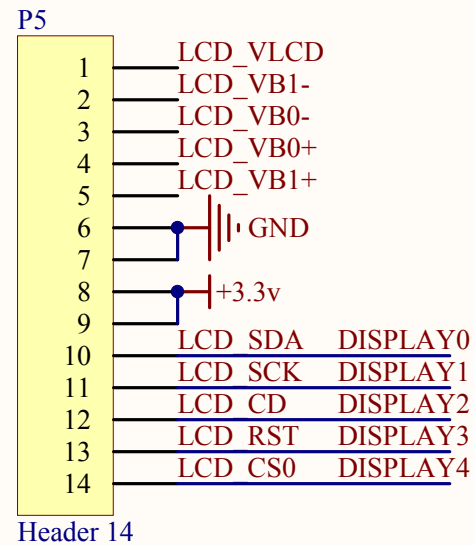
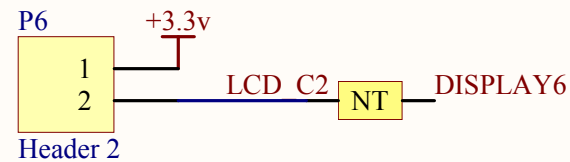
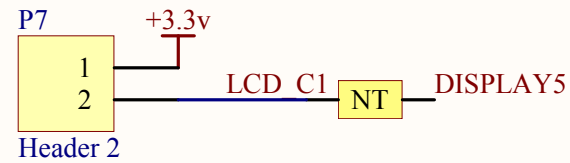
PonyPort



Title		
Size	Number	Revision
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Date:	4/24/2011	Sheet 8 of
File:	X:\design\PonyPort.SchDoc	Drawn By:

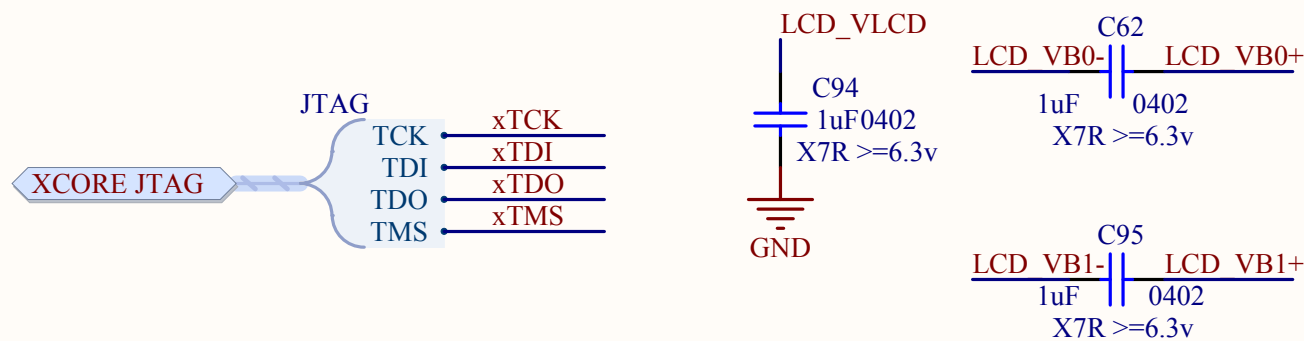
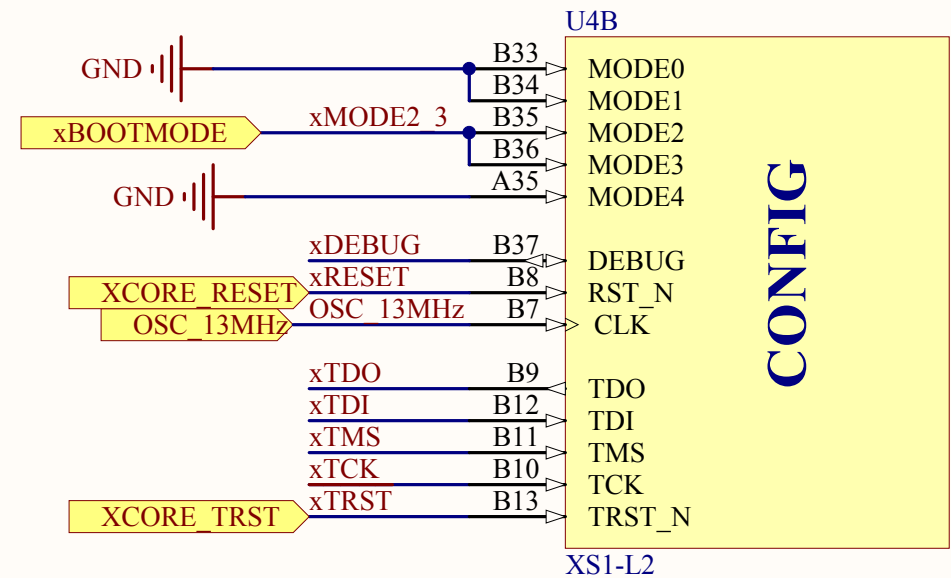
A

A

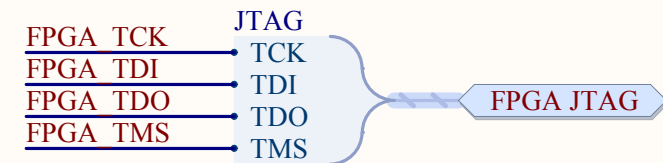
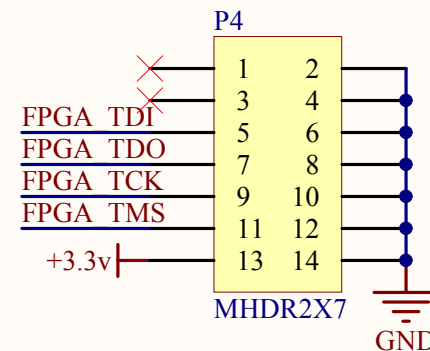


DISPLAY[0..6]

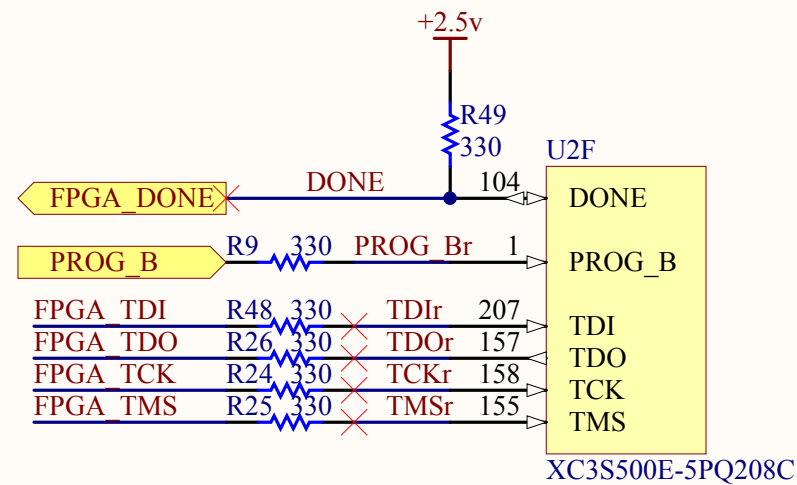
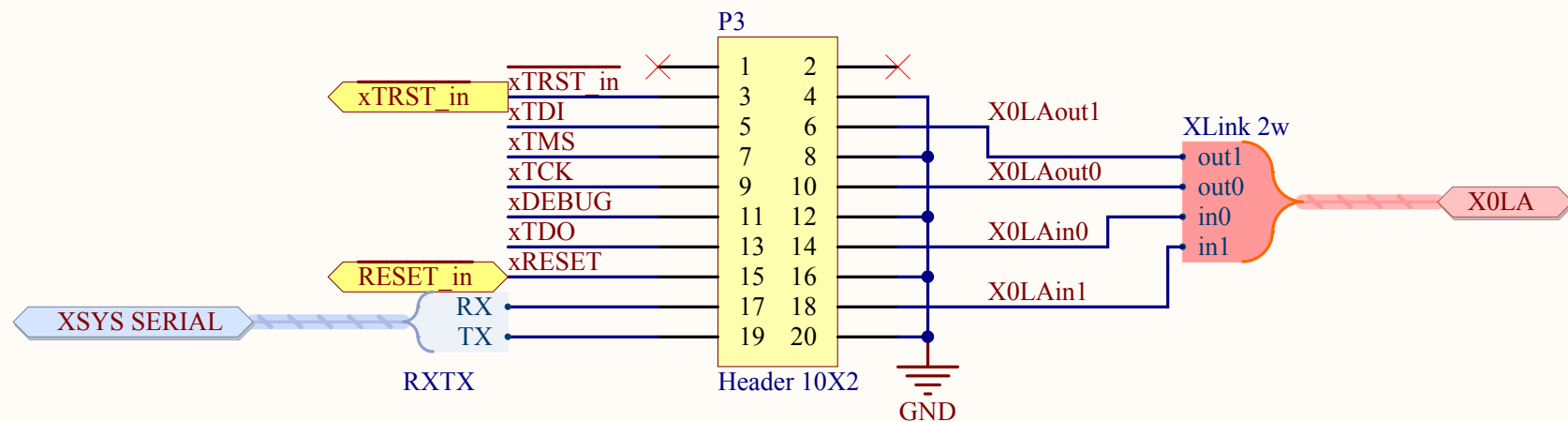
DISPLAY[0..6]



FPGA JTAG connector



XTAG Connector



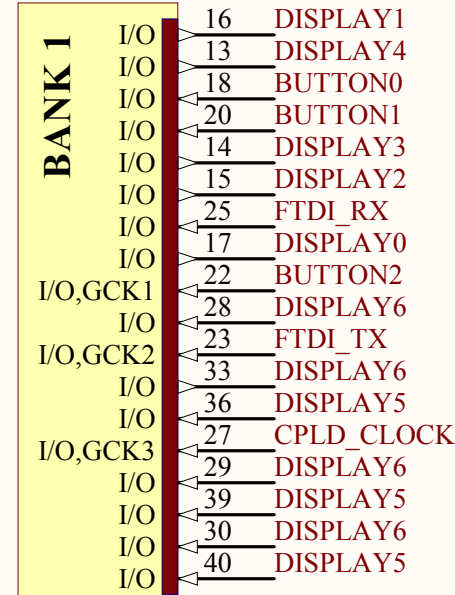
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D

Title		
Size	Number	Revision
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Date:	4/24/2011	Sheet 9 of
File:	X:\design\debug IO and ports.SchDoc	Drawn By:

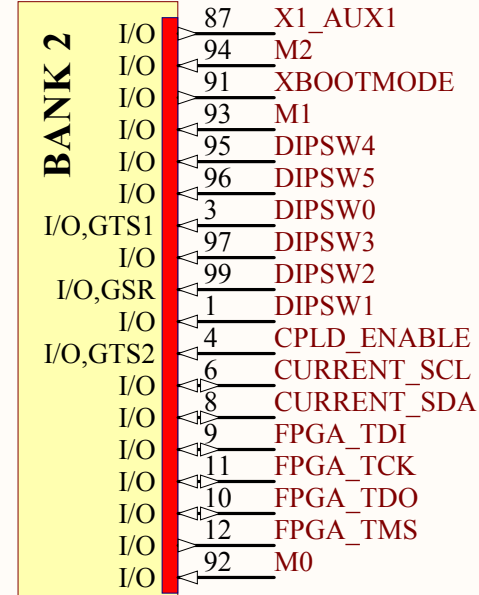
A

U16A



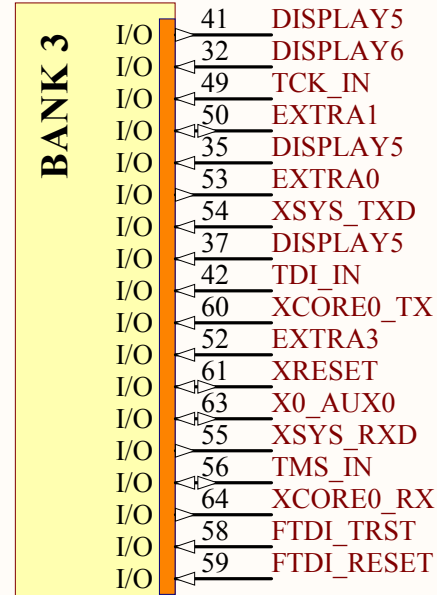
XC9572XL-10TQG100C

U16B



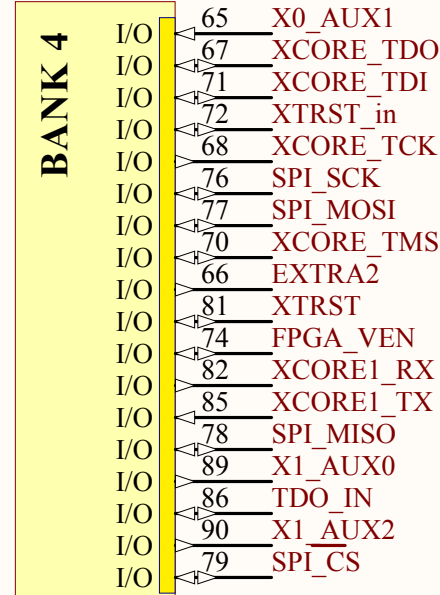
XC9572XL-10TQG100C

U16C

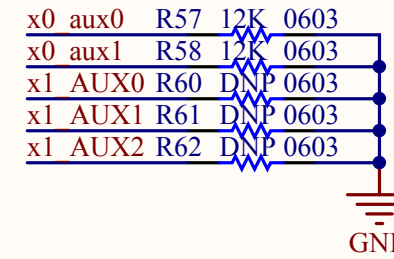
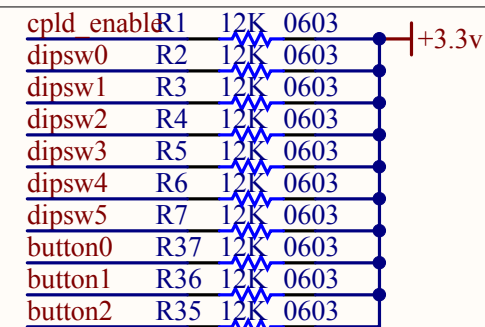
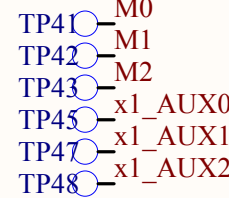
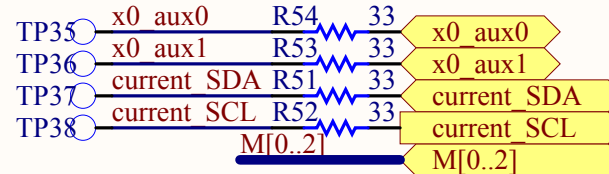


XC9572XL-10TQG100C

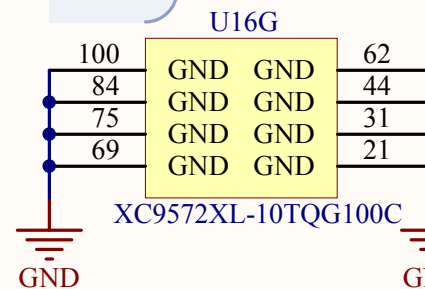
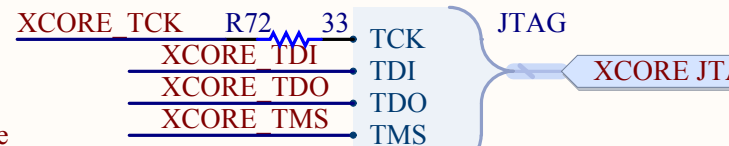
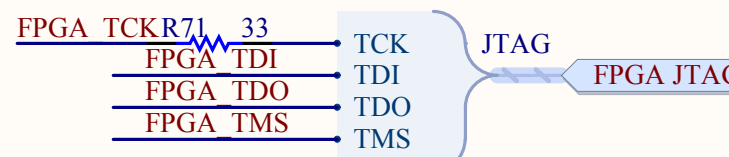
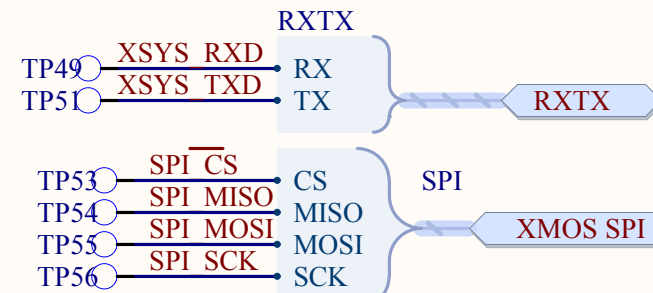
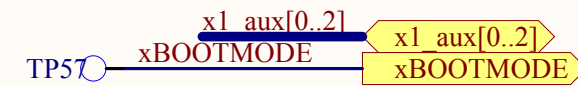
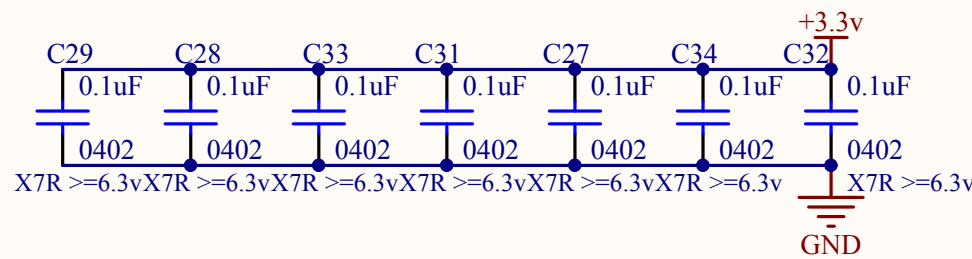
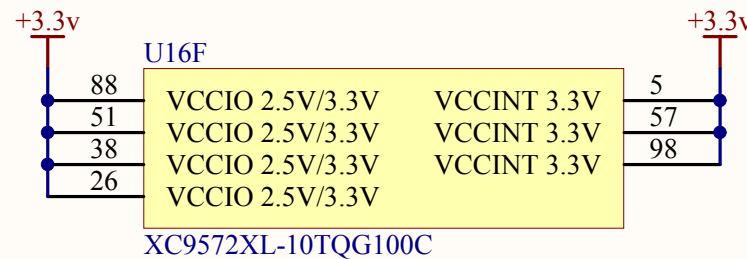
U16D



XC9572XL-10TQG100C

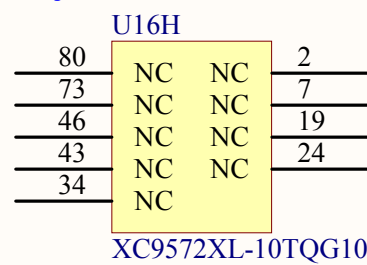
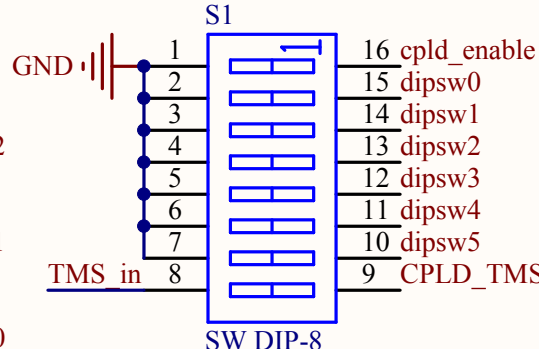
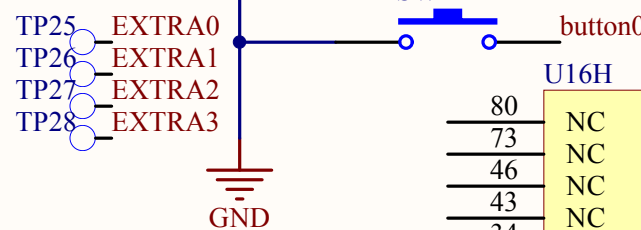
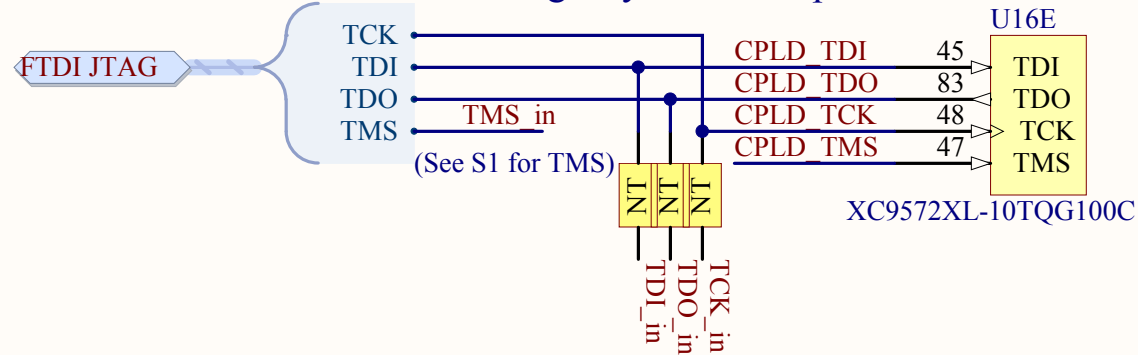


FPGA JTAG connector



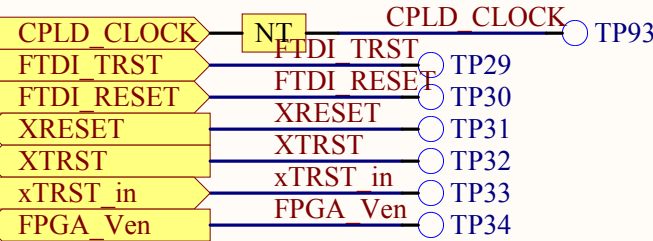
C

Emergency CPLD output disconnect



Title			
Size		Number	Revision
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Date:	4/24/2011		Sheet of
File:	X:\design\CPLD.SchDoc		Drawn By:

D

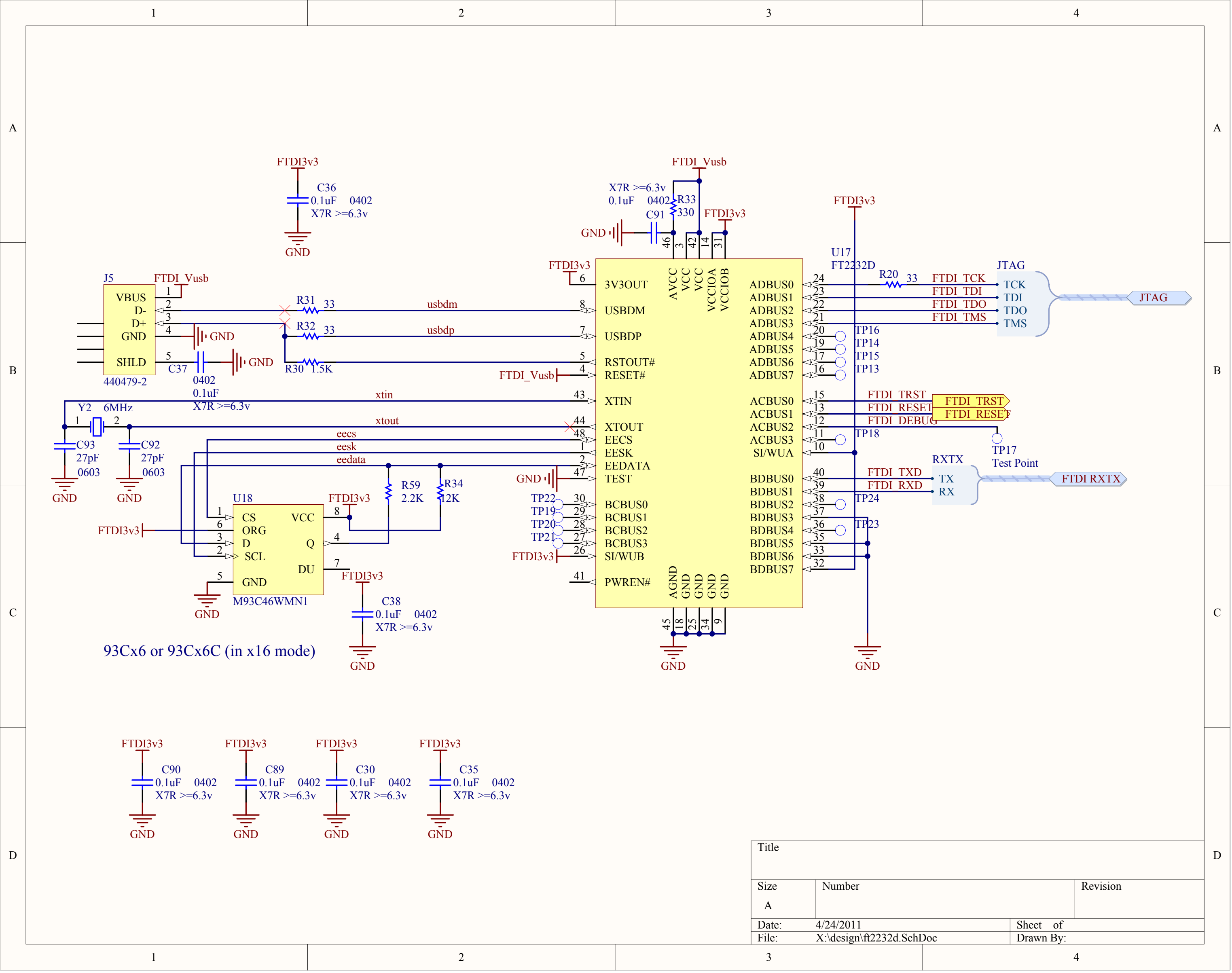


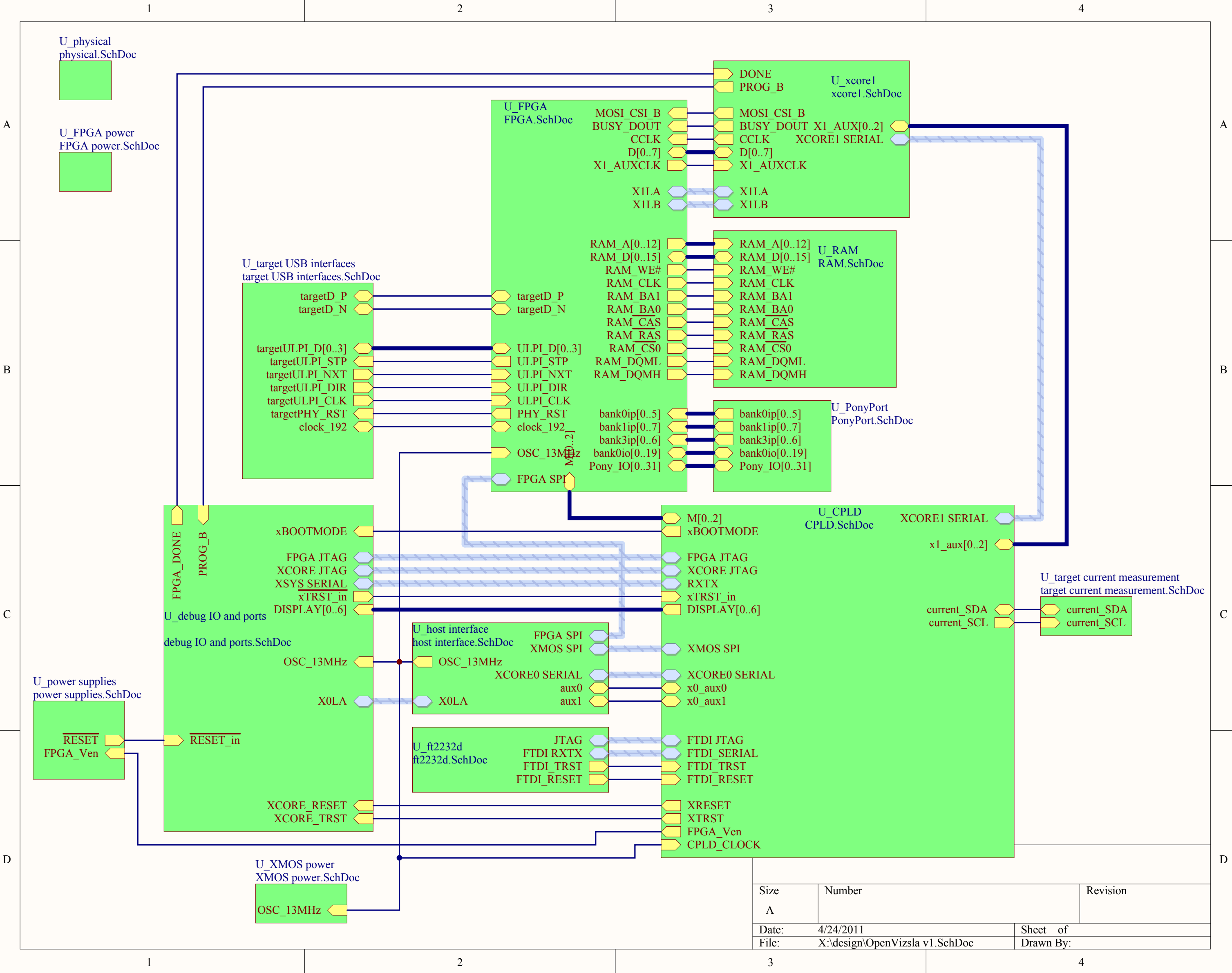
A

B

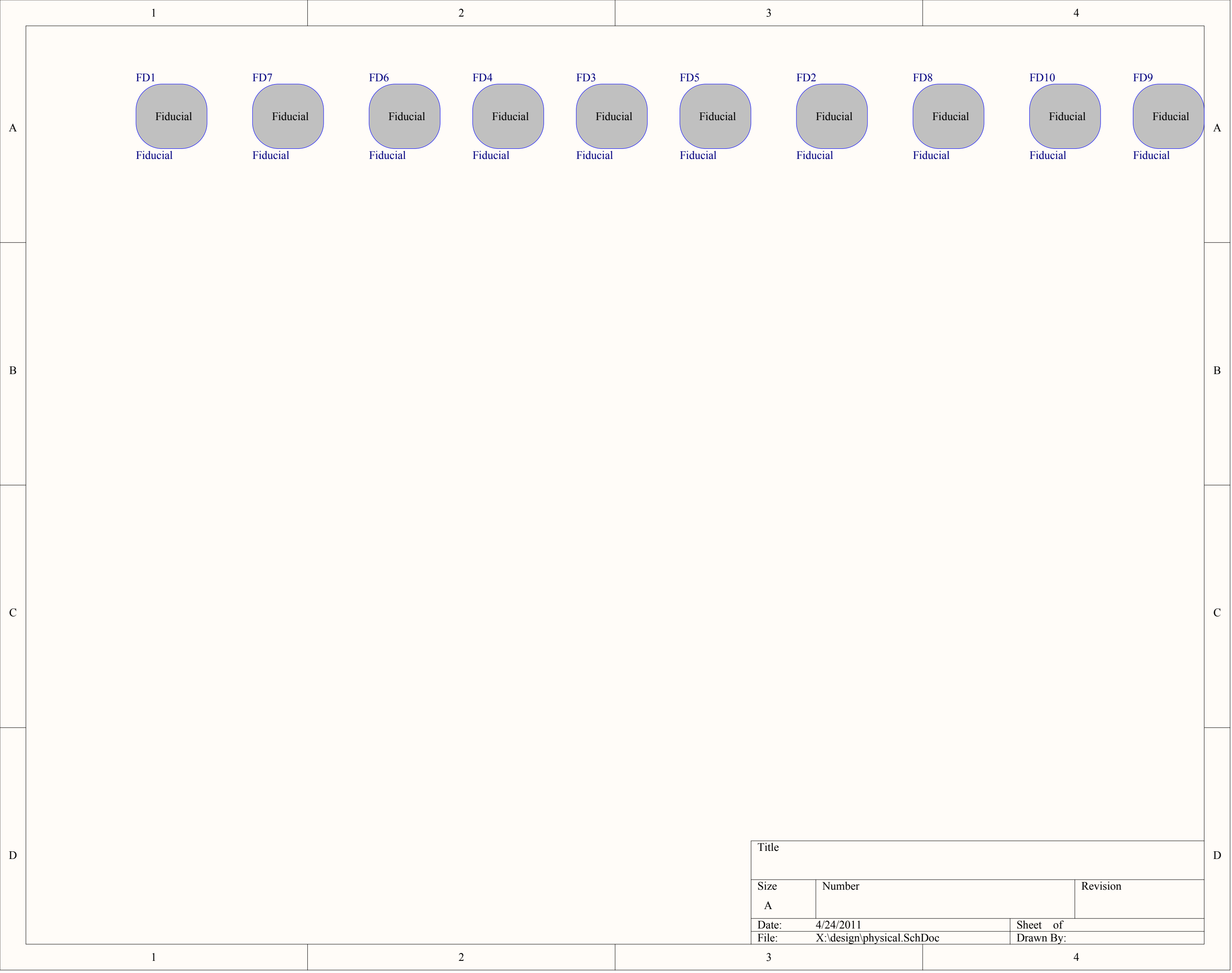
C

D





Size	Number	Revision
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Date:	4/24/2011	Sheet of
File:	X:\design\OpenVizsla v1.SchDoc	Drawn By:



1

2

3

4

FD1

FD7

FD6

FD4

FD3

FD5

FD2

FD8

FD10

FD9

Fiducial

Fiducial

Fiducial

Fiducial

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A

A

B

B

C

C

D

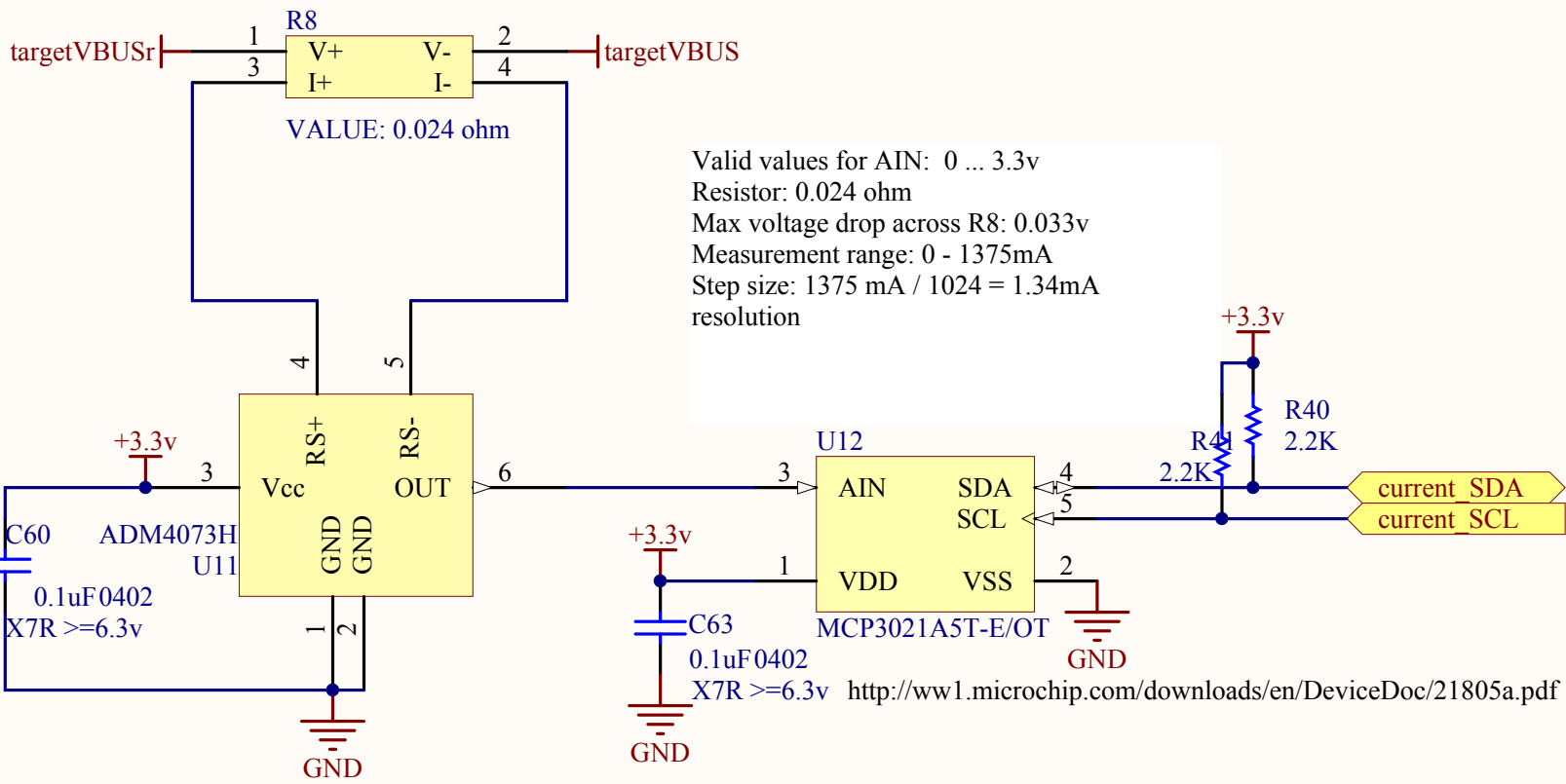
D

1

2

3

4



http://www.analog.com/static/imported-files/Data_Sheets/ADM4073.pdf

Title		
Size	Number	Revision
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Date:	4/24/2011	Sheet of
File:	X:\design\..target current measurement.SchDoc	Drawn By:

A

A

B

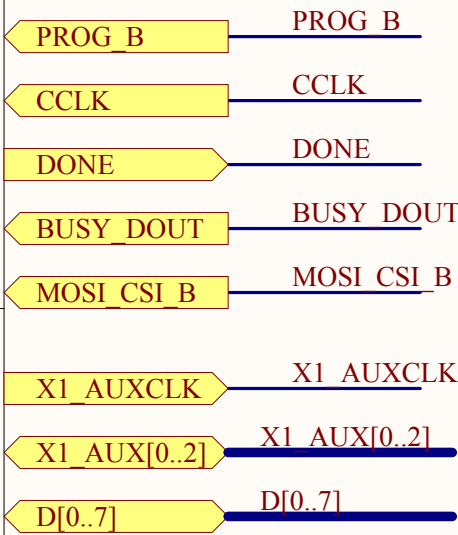
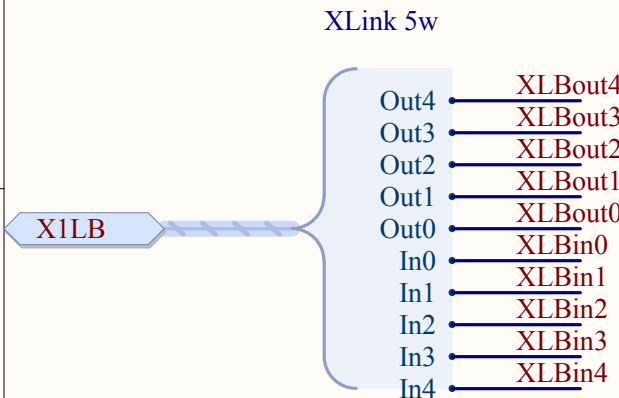
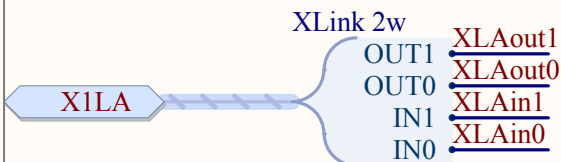
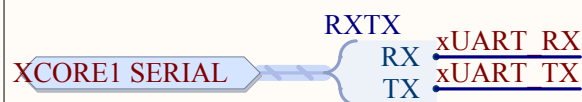
B

C

C

D

D



CCLK

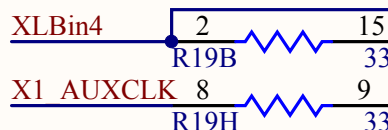
1

R19A

16

33

stupid layout tricks
ignore this resistor kthx



PROG_B A39

SD_CD A40

SD_DAT0 A41

SD_DAT1 A42

XLAout1r A43

XLAout0r A44

XLAin0 A45

XLAin1 A46

SD_DAT2 A47

SD_DAT3 A48

SD_CMD A49

SD_CLK A50

XLBout4r A23

XLBout3r A24

XLBout2r A25

XLBout1r A26

XLBout0r A27

XLBin0 A29

XLBin1 A30

XLBin2 A31

XLBin3 A32

DONE A28

MOSI_CSI_B A33

D0 B16

D1 B17

D2 B18

D3 B19

D4 B20

D5 B21

D6 B22

D7 B23

xUART RX B24

xUART TX B25

X1_AUX1 B26

X1_AUX0 B27

BUSY_DOUT B30

X1_AUX2 B31

U4D

< X1D0_P1A0

X1D1_XLA4out_P1B0

X1D2_XLA3out_P4A0

X1D3_XLA2out_P4A1

X1D4_XLA1out_P4B0

X1D5_XLA0out_P4B1

X1D6_XLA0in_P4B2

X1D7_XLA1in_P4B3

X1D8_XLA2in_P4A2

X1D9_XLA3in_P4A3

X1D10_XLA4in_P1C0

< X1D11_P1D0

< X1D12_P1E0

X1D13_XLB4out_P1F0

X1D14_XLB3out_P4C0

X1D15_XLB2out_P4C1

X1D16_XLB1out_P4D0

X1D17_XLB0out_P4D1

X1D18_XLB0in_P4D2

X1D19_XLB1in_P4D3

X1D20_XLB2in_P4C2

X1D21_XLB3in_P4C3

X1D22_XLB4in_P1G0

< X1D23_P1H0

< X1D24_P1I0

< X1D25_P1J0

X1D26_P4E0

X1D27_P4E1

X1D28_P4F0

X1D29_P4F1

X1D30_P4F2

X1D31_P4F3

X1D32_P4E2

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X1D36_P1M0

X1D37_P1N0

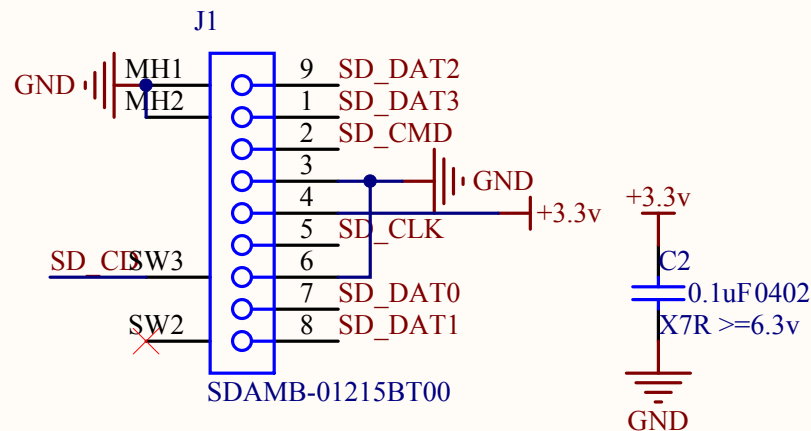
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X1D39_P1P0

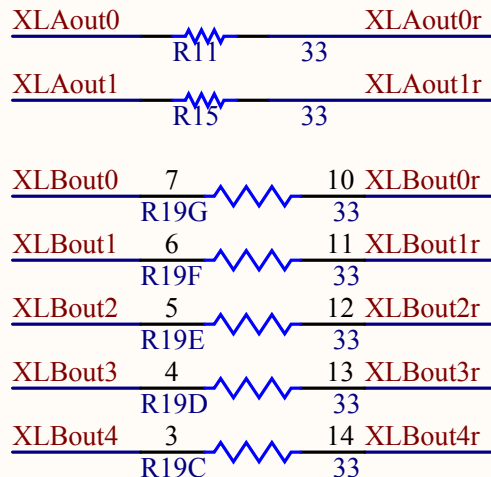
XS1-L2

IO_XCORE1

SD Card Slot



Source Termination Resistors



Title		
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