Name:Namathoti Srinivas
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GATE EE 2010 PAPER

The following karnaugh map represents a function F

F / X	00	01	11	10
0	1	1	1	0
1	0	0	1	0

52. A minimized form of the function F is

(A) $F = XY + YZ$

(B) $F = XY + YZ$

(C) $F = XY + YZ$

(D) $F = XYZ$

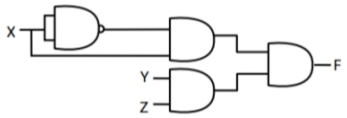
Solution: The minterms where $F = 1$ are:

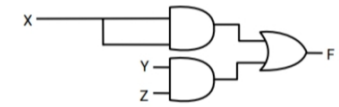
$$m_0 = \overline{X}\,\overline{Y}\,\overline{Z}, \quad m_1 = \overline{X}\,\overline{Y}\,Z, \quad m_3 = \overline{X}\,Y\,Z, \quad m_7 = X\,Y\,Z$$

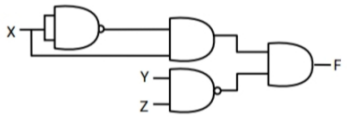
Simplifying, we get:

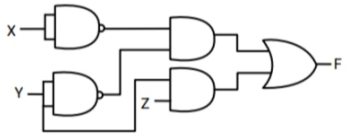
$$F = \overline{X}\,\overline{Y} + YZ$$

53. Which of the following circuits is a realization of the above function F

(A)


(B)


(C)


(D)


Solution:

1. We know that the function: $F = \overline{X}\,\overline{Y} + YZ$
2. Based on the function F, the realized circuit is:
   - AND gate for $\overline{X}\,\overline{Y}$
   - AND gate for YZ
   - OR gate to combine both outputs