Design of QCA-Serial Parallel Multiplier(QSPM) with Energy Dissipation Analysis

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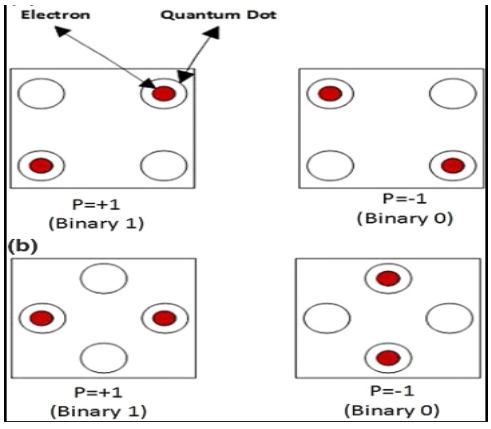
***Abstract*—%This paper shows the implementation of a 4-bit Multiplier and it's working using quantum cells. Also going to show the power dissipation in each cell, average power dissipation, and leakage power in the circuit. This circuit will be implemented using an Exclusive XOR gate(EXOR). All these circuits were implemented and verified in the QCA Designer tool (QCAD) and power dissipation and power leakage were observed in the QCA Pro tool.**

Keywords—Quantum cell, 4-bit Multiplier, Energy dissipation, cost.

I. INTRODUCTION

QCA means Quantum-Dot Cellular Automata. These quantum cells are mainly used or high performance, small in size, quick computations. These qca cells work on electrons shifting inside the cells. In this qca cell we will get two types of states -1 and 0 respectively. The respective types can be seen in Figure 1.

Figure 1: QCA cell types based on polarisations.



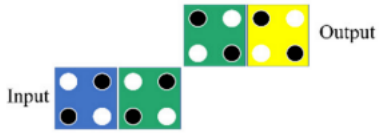
These cells work based on the property of repulsion between the electrons inside the cell. The next electron position will be decide based on the previous cells polarised values. If the previous cell have a electron then the corresponding space shouldn't contain any electrons to satisfy the electron stability. So the thumb rule is for a corresponding electron there need to be a hole in the surroundings and when there is a hole there need to be a electron to balance the stability.

In a case where there will be cells on both the sides and we need to decide where the electron need to be places in cell so that there will be no damage to the circuit. So in such cases there the domination will be taken by the fixed polarisation that was set on the circuit.

These cells not only work in series of the cells these also work when they are diagonal to each other.

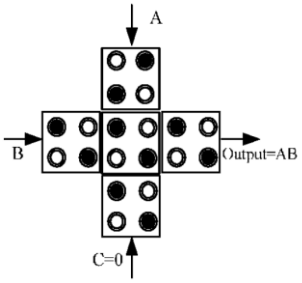
So when a series of cells are in serially connected to each other then we will be getting the output same as the input given to the circuit at input terminal. Similarly, when they are connected diagonally the we will be getting the opposite of the input that was given at the output side. The following theory can be seen in the figure 2 (a) and (b).

Figure 2 (a): When cells are connected in series

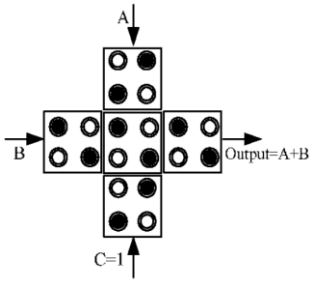


(b): When cells are connected diagonally

Also in Figure 2 (c) we can observe the implementation of the an AND gate using QCA cells in which we can see there was a fixed polarization given to one cell at the bottom in which that will be used for choosing the output when there is a clash between two or more cells at the same time. Similarly in Figure 2 (d) we can see the implementation of OR gate where here the fixed polarization was given as 1 in which we can change the output based o the input values A and B as shown in the figure.



(c)



(d)

So based on the basic introduction given so far we will now try to implement the required 4-bit serial-parallel Multiplier (QSPM) circuit using QCA cells and using that circuit we will try to find energy dissipations, leakage energy and switching energy dissipations. Also, we will find the are of the overall circuit that was going to be built. Then later that we will try to plot a graph between the area and the cost of the overall circuit.

II. Proposed Design

A. Bit-serial Adder

A Sit Serial Adder (BSA) is an adder that performs binary additions. According to the proposed data for this 3 majority gates and two inverter gates are required to get the sum and one majority gate for C_{out}. The expressions can be seen in equation 1 from [1], where x_i, and y_i are input bits and c_{in} is the carry-in bit.

$$\text{Sum} = x_i y_i c_{in} + x_i \bar{y}_i \bar{c}_{in} + x_i y_i \bar{c}_{in} + \bar{x}_i \bar{y}_i c_{in}$$

$$= M(\bar{M}(x, y_i, c_{in}), M(x_i, y_i, \bar{c}_{in}), c_{in}) \quad \ldots\ldots\ldots(1)$$

$$C_{out} = M(x_i, y_i, c_{in})$$

So from the previous information from [1], we can get to know about the full adder and a half adder using majority gates and their working. So from there, we can tell that making the full 4-bit multiplier using those methods is a bit complex and the circuit becomes difficult to implement. So to minimize the complexity of the design, we use an Exclusive-OR gate [20]. Since the EXOR has three inputs and one output, in our proposed design we will only be going to use two-point for giving inputs to the Exor gate. So for the third input, we will be giving the fixed polarization of -1. So this construction will be for output and since this is a multiplier the numbers need to be added up after getting multiplied except the first multiplication. So to do those further computations we will repeat the circuit and connect them accordingly to create a multiplier. The basic circuits of EXOR, the modified basic circuit and its working can be observed in figures 3.

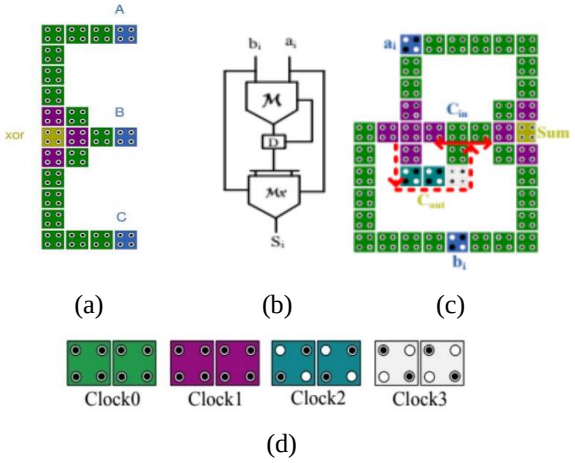
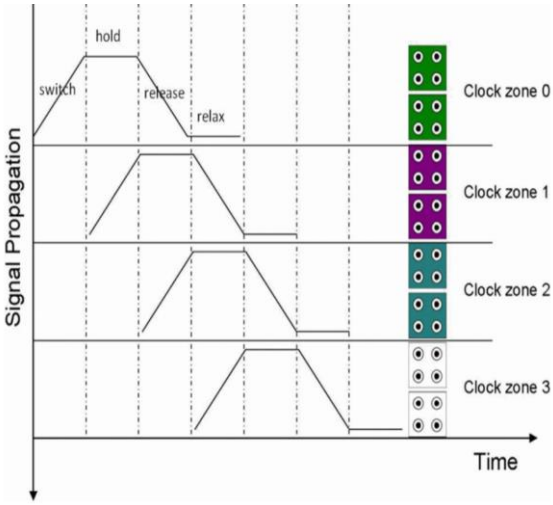


Figure-3: (a) 3 input EXOR gate, (b) Logic of the circuit working bit serial adder, (c) Basic circuit of qca circuit.

B. Clocks

As shown in figure(1-d) QCA cells, here different cells have different color which actually represents different clocks of the cell. These clocks are very much important while making a circuit using qca cells. As these clocks represent the different time intervals where they get started. The pictorial representation is shown in figure(3). In each clock it has a total of four phases, which are 'Switch state', 'Hold state', 'Release state', and 'Relax state'. Each of these state have different purposes in qca cell.



Figure(4): Different types of clocks and their different state

In the Switch state is used for switching or giving the polarization to the qca cell for a specified amount of time.

In the Hold state, the given polarization will be kept held.

In the Release state, the circuit will be left to get back to its normal state.

In the Relax state, the qca cell gets relaxed before giving the next polarization value.

Due to these phases in a clock and due to different types of clocks there will be a delay in the output. This delay can vary based on the circuit and based on its complexity. However we can consider a little bit of time delay due to wires that are used, also if the wires are so small it is very much a small value.

Since this is a circuit and we make it using a basic qca circuit, we modify the combined circuit as a properly deserved output circuit and get a generalized equation for the circuit as shown in figure 3 equation for this circuit.

$$K_i = \sum_{j=0}^{n-1} y(j)x(i-j)$$

Since there will be a delay, so by considering the full-cycle delay (T^{-1}). The delay for each unit will be $T^{-1/2}$. The resulting equation will be modified as

$$= T^{n/2} K_i$$

III. WORKING OF 4-BIT SPM

A. *Concept behind the circuit working*

In this circuit name serial-parallel multiplier, the multiplication happens as shown in figure 5. As in figure 5 each P1, P2, … Pn are obtained by adding up the components that came after the multiplication of each bit. So to implement the same here we build the circuit which has 'AND gates', 'Half Adders', and 'Fuller adders'.

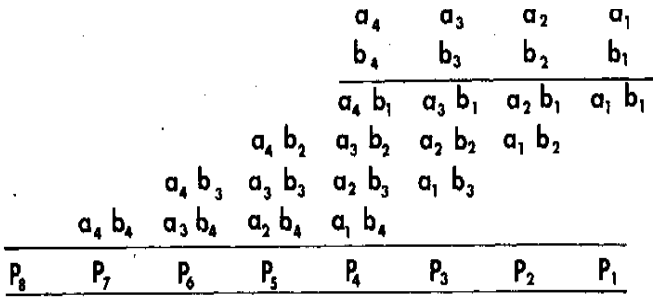


Figure 5: Serial Parallel Multiplier(SPM) procedure.

So to implement the multiplication here we use a total of 5 inputs that we give to the circuit. In this one input will be only with two combinations of 0 and 1, whereas the remaining 4 inputs will be as a combination of these 4 bits that are $2^{\wedge 4}$ = 16 combinations. So the total number of combinations will be $2^{\wedge 5}$= 32 number of combinations. For each combination, we will get different outputs. So to compute this multiplier we will first do an 'AND' operation for each of the bits then after that we first send the last bits to the base circuit gate as input, then after sending the input we will add them up using FA that we will be having internally in the overall circuit. The carryout that will be coming out after the adder performance, that carry out will be given as input to the next connect circuit. Then again the same process continues and carry goes to a further step. After all these steps the resultant can be seen in the output qca cell Pi. In this way, the multiplier circuit works. This working is represented as a schematic Figure 6. Also, the QCA circuit can be seen in Figure 7.

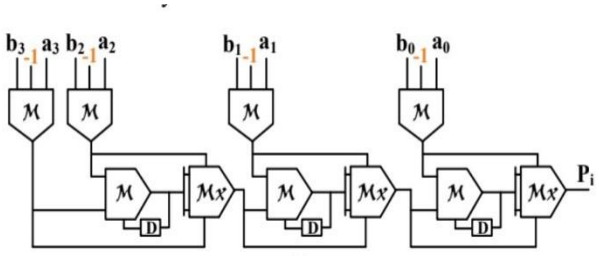


Figure 6: Schematic representation of the SPM circuit.

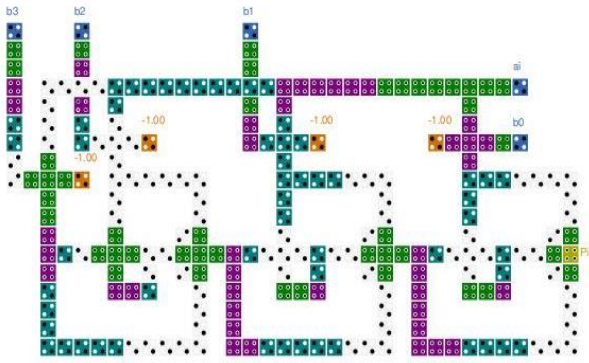


Figure 7: SPM circuit using QCA cells.

For this SPM circuit due to 'AND gates', Half adders, FA, and clock delays there will be a total delay of 1.25 clock cycles.

IV. ENERGY DISSIPATION ANALYSIS

- Since we can observe there are 4 different phases in a single clock cycle, which have raise, hold, release and relax due to these states during the transition from one state to another state there will be a power and energy dissipation from the circuit.
- Also when we do power dissipation analysis we can observe that there will be no uniform dissipation in the circuit, there will be different amounts of power dissipation at different cells in the overall circuit. This is due to those nodes it will be having more switching of state in a short span of time.
- Excluding these dissipations there will also be a leakage power which will be dissipated during the running of the circuit.
- We can observe these all power dissipations and leakage power in QCA pro tool. This is a special tool that helps us in observing the dissipations in the overall circuit. This pro tool requires a vector file, switching file, and a qca circuit file.

These power dissipations will be calculated for different voltages by changing them for different temperatures. Generally, we consider voltages $0.5E_K$, $1E_K$, $1.5E_K$, and temperatures are 1K and 2K are considered for evaluating power dissipations.

We can observe the power dissipations at different QCA cell in figure 8. Figure 8 gives a clear view of the energy dissipation at each cell in the qca circuit that was uploaded in qca pro tool, and also we can see the Average energy dissipations, leakage energy dissipations, and Switching energy dissipations at different energy levels at 2K in Table I.

Table – I: Energy dissipations from the circuit at different energy levels at 2K temperature.									
Multiplier bit size	Leakage energy dissipation (meV)			Switching energy dissipation (meV)			Average energy dissipation (meV)		
	$0.5E_K$	$1E_K$	$1.5E_K$	$0.5E_K$	$1E_K$	$1.5E_K$	$0.5E_K$	$1E_K$	$1.5E_K$
4-bit	69.03	211.55	379.56	366.74	317.01	269.48	435.76	528.57	649.03

From the table we can observe that the energy dissipation, switching energy dissipation and Leakage dissipation are increasing as the Energy Levels increases from $0.5E_K$ to $1.5E_K$ at 2K temperature. You can observe the dissipations in different quantum cells in the qca circuit in figures 8 (a), (b), and (c).

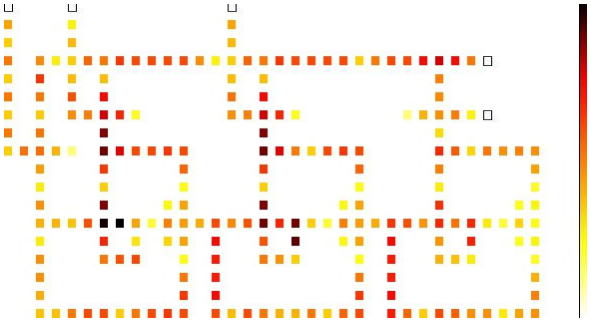


Figure 8 (a): Thermal hotspots of qca cells in a 4-bit multiplier at $0.5E_K$

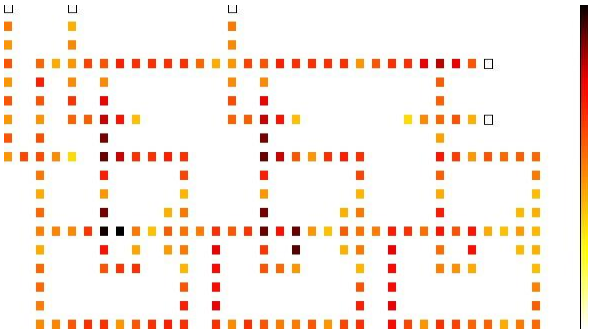


Figure 8 (b): Thermal hotspots of qca cells in a 4-bit multiplier at $1E_K$

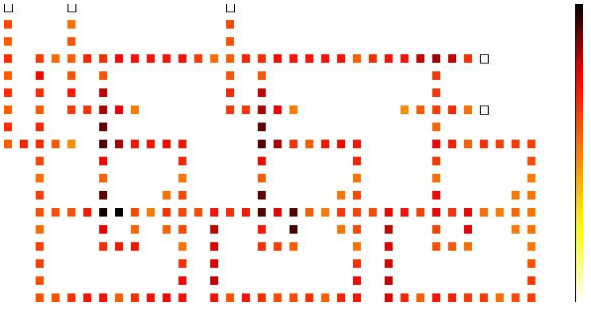


Figure 8(c): Thermal hotspots of qca cells in a 4-bit multiplier at $1.5E_K$

V. Overall Analysis

So from the above information we obtained we obtained we can now analyse the circuit and its properties. As mentioned before the quantum cells will have a specified width and height if they are changed the circuit properties and its functionalities will be altered accordingly. A quantum cell have various parameters like relative permittivity, clock high where the polarization starts, relaxation time means amount of time in which the circuit is in relax state. Like these the all parameters can be seen in Table II

Table II: Quantum cell parameters and their values

Parameters	Value
Cell Width	18.0 nm
Cell Height	18.0 nm
Relative Permittivity	12.900000
Clock High	9.800000e-022 J
Clock Low	3.800000e-023 J
Clock Amplitude Factor	2.000000
Time Step	1.000000e-016 s
Relaxation Time	1.000000e-015 s
Simulation Time	5.000000e-011 s
Radius Of Effect	80.000000 nm

Now based on the parameter values that are set the output of the circuit can be observed as a wave form with all inputs and at different clock cycles. The wave form of the circuit can be observed in Figure 9. In figure 9 we can observe how the output wave for comes with a delay with the clock cycles. If we want the output to be clearly visible with 1's and 0's. To obtain this type of wave form we need to create buses for each of the input's and for the output and run the circuit, then we can observe the wave form in a much clearer appearance with 1's and 0's, which can be observed in Figure 10.

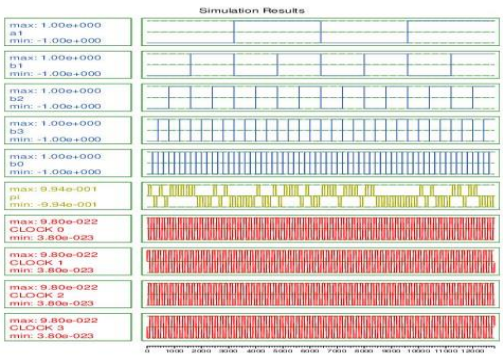


Figure 9: Output wave form of the circuit

Figure 10: 4-bit multiplier output using buses

In figure 10 we can observe the bit multiplications of the bits 1111 and 1001 in the output wave form Pi as 11100001. In similar way the remaining bit multiplications can be observed in the output Pi.

Since the main concept behind using qca cells is to make the circuit size minimum and be able to perform the circuit in small areas. So as the area terms came we can compute the area of the area of the overall circuit using the area of each cell and using that we can generalize the area formula for n-bit multiplier circuits. Since the height and width of each cell is 18nm then the area of one cell will be 18*18 nm^2. So using that the area formula for n-bit serial parallel multiplier is

$$\text{Area} = [(220B - 202) \times (358+40 \times \text{int}(B/11)) \times 10^{-6}]\ \mu m^2$$

B – Number of bit multiplier, int represents the integer part of the fraction. On using this, formula we can calculate the area of the overall circuit. Based on different base papers the area of the 4bit multiplier changes as shown in the Table III.

Table III: Area of circuits in different base papers and proposed

Word	Multiplier	#Cell	Area (um^2)	Latency (clock Cycle)	Crossover Type
4-bit	Area from [1]	406	0.493	1	Multilayer
	Area from [2]	329	0.299	1	Multilayer
	Area from [2]	330	0.319	1.25	Multilayer
	Area from [3]	264	0.27	0.75	Multilayer
	Area Proposed	229	0.243	1.25	Coplanar

Cost of the circuit can be given as

$$\text{Cost} = (Pn^a + Qn + Rn^b) \times Sn^g$$

Where $Pn = 3(B-1)+1$; $Qn = 0$; $Rn = B-2$; $Sn = \log_2(32)^{0.25}$

The graph between cost and word size can be seen in Figure 11.

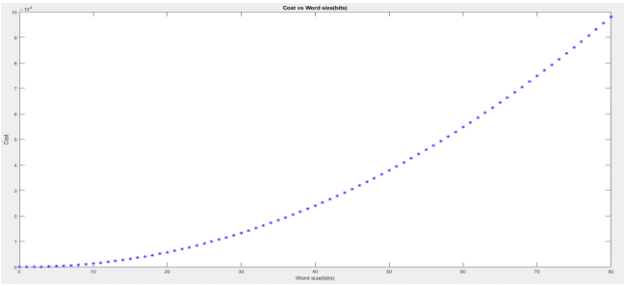


Figure 11: Graph between Word size and cost

CONCLUSION

In this way we can implement the 4-bit Serial parallel multiplier and obtain the power dissipations in the circuit, area of the circuit, and cost of the circuit. Also, we can observe various forms of wave forms at different time instances of clock. From this paper we are able to plot the graph for the bit multipliers other than 4-bit multiplier and able to estimate the cost for higher bit multipliers also.

REFERENCES

This project used few references from the following base papers.

[1] H. Cho and E. E. Swartzlander, "Adder and multiplier design in quantum-dot cellular automata," IEEE Trans. Comput., vol. 58, no. 6, pp. 721–727, 2009.

[2] Y. Zhang et al., "Modular design of QCA carry flow adders and multiplier with reduced wire crossing and number of logic gates," Int. J. Cir. Th. Appl., 44(7), pp. 1351–1366, 2016.

[3] I. E. Arani, and A. Rezai, "Novel circuit design of serial–parallel multiplier in quantum-dot cellular automata technology," Journal of Computational Electronics, 17(4), 1771-1779, 2018.