

# DisplayPort 2.1 Protocol Compliance: *Guided Tour*



M42de 80G Video Analyzer/ Generator



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# About Teledyne Test and Measurement



Extensive range of tools for electrical, physical, logical and protocol layer testing



Broad array of test solutions for serial data standards and next-gen technologies



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Austin Labs Testing and Training



Frontline Test Services



Consulting



Device and Systems Testing



# Agenda

- DisplayPort 2.1 Compliance: Status
- DisplayPort 2.1 Specification: What's New...
- DisplayPort 2.1 Compliance Overview
- Compliance Test Breakdown
  - DP 2.1 Source Test Examples
  - DP 2.1 Sink Test Examples
  - LTTPR & DP Tunneling
- Questions

# Goals for DP 2.1 Compliance

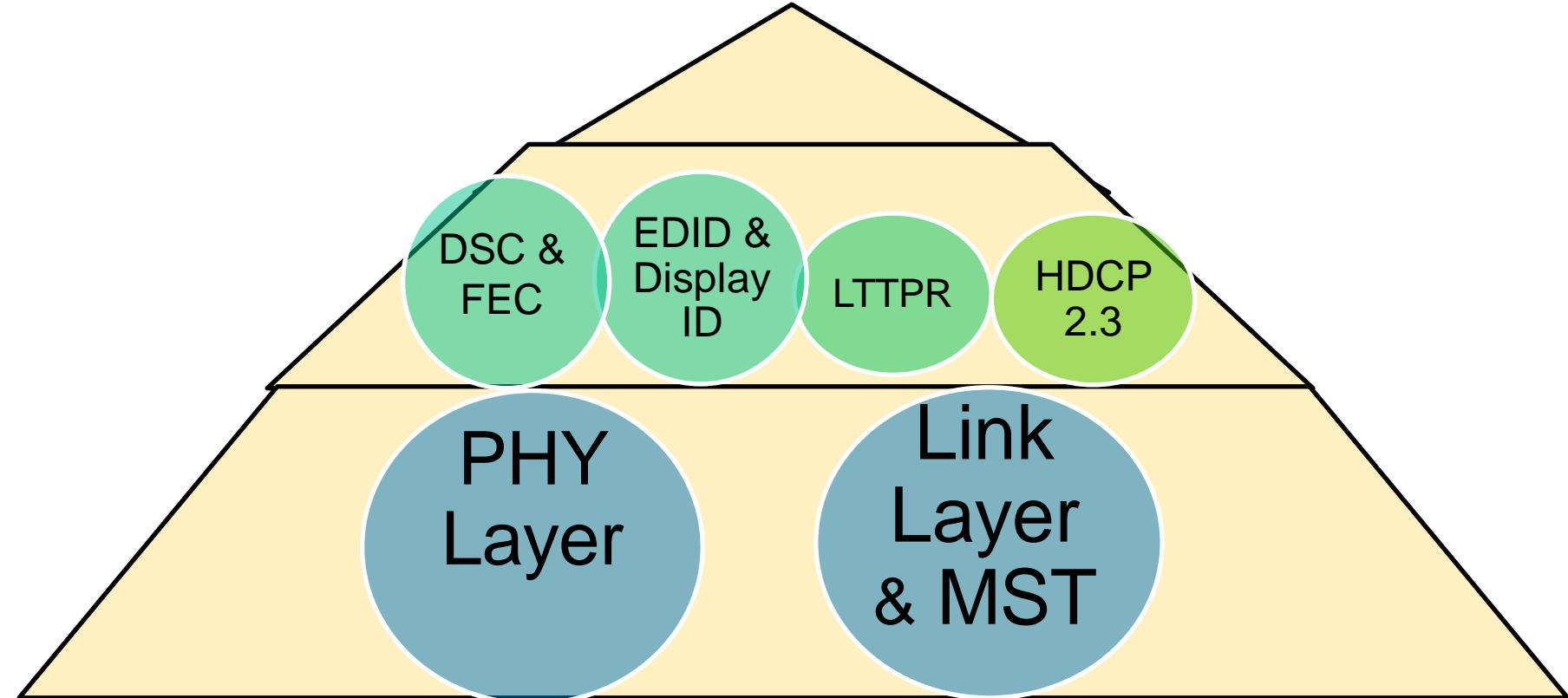
- Drive meaningful value for member companies to participate in Compliance development & testing
  - Get products added to Integrators List
  - Utilize the DisplayPort Logo
- Build positive brand association within the industry and consumer markets for DP technology
- Create a network of authorized test centers to allow easy certification of DP components

# DisplayPort Compliance Evolution

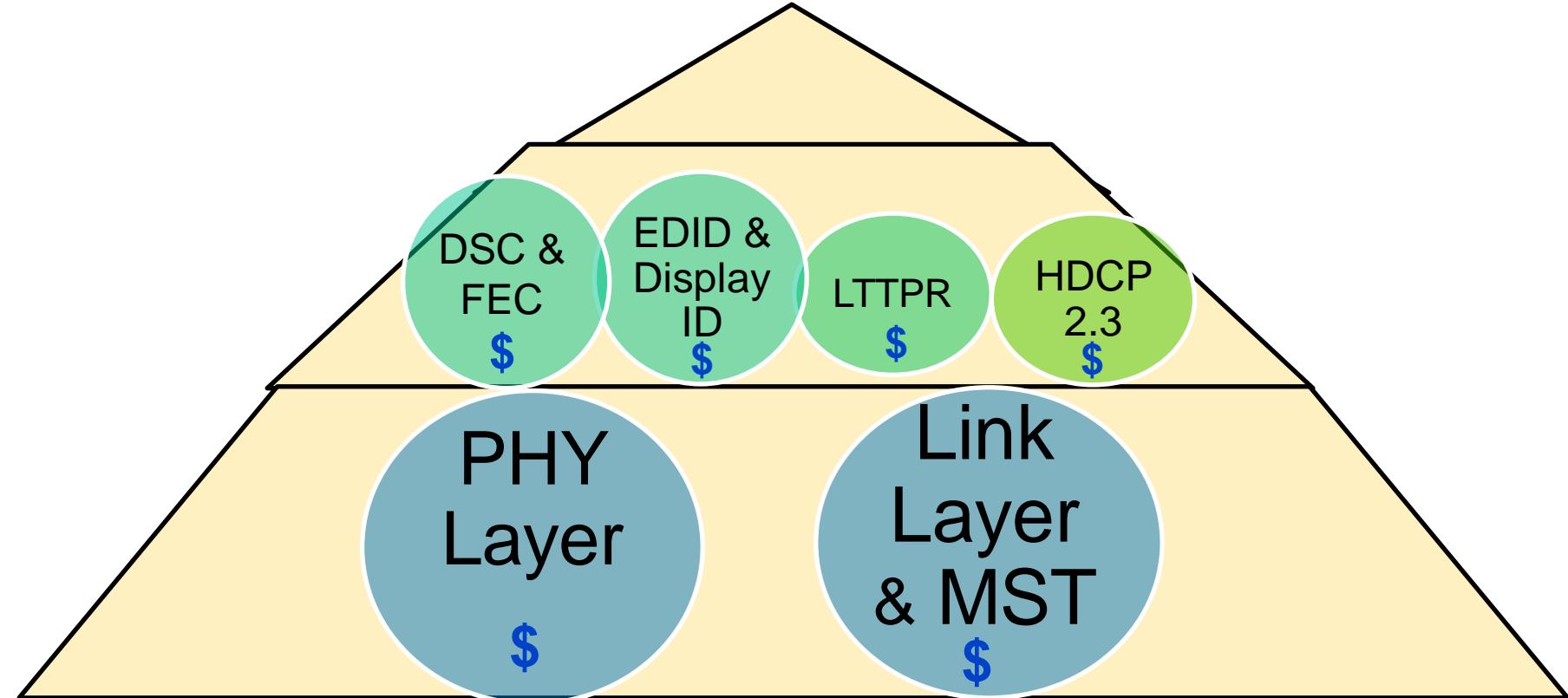


Areas of Compliance	DP 1.2	DP 1.4	DP 2.1
PHY Layer	●	●	●
Link Layer	●	●	●
HDCP 1.3 & 2.3	●	●	●
EDID / DisplayID		●	●
Adaptive Sync		●	●
Multi-Stream (MST)		●	○
DSC & FEC		●	●
DP Alt-mode over USBC		●	●
LTTPR		●	●
Panel Replay			○
Native DisplayID			○
○ Draft or Future Development			

# Areas for DP 2.1 Compliance



# Areas for DP 2.1 Compliance

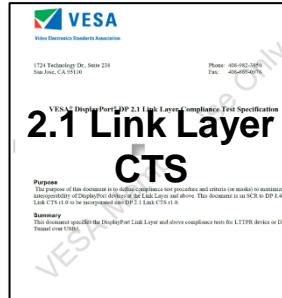
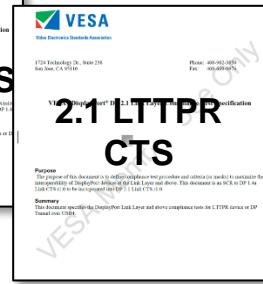
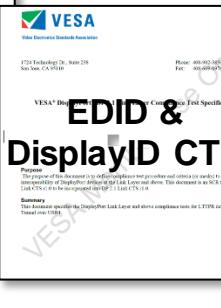


# DisplayPort 2.1 Compliance Status

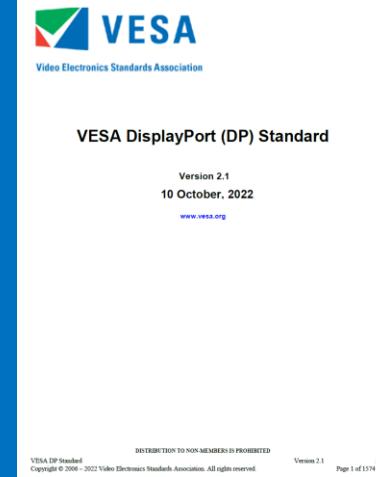


DP 2.1 Tests	Status
• <b>Phase 1:</b> Source UHBR Link training tests	Approved
• <b>Phase 2:</b> Sink AUX, Link training, maintenance and LTTPR (embedded) & Sink Capability tests	Approved
• <b>Phase 3:</b> Source AUX, Link training, link maintenance and LTTPR (emulated) Link training tests	Approved
• <b>Phase 4:</b> LTTPR device (and DP tunnel) tests	Correlation Stage
• <b>Phase 5:</b> Source and Sink Video and DSC tests	Correlation Stage
• <b>Phase 6:</b> MST and Power State Tests	Definition Stage

# DisplayPort 2.1 Compliance Status



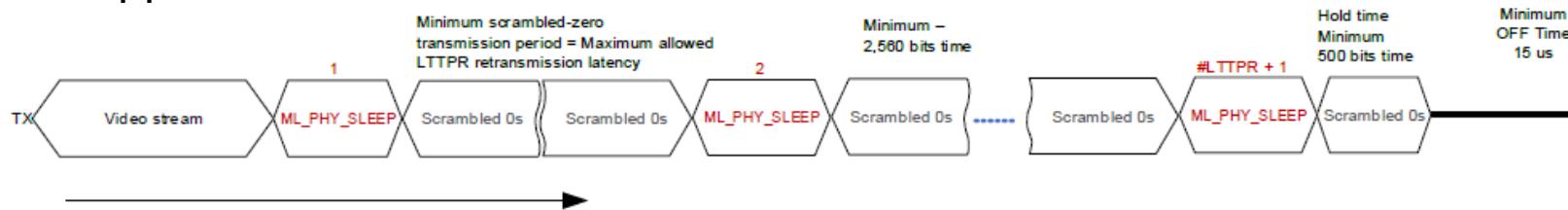
# DisplayPort 2.1: What's New



- Revised Link Training - DPCD registers as LTTPR “Intra-Hop AUX”
- DP40/DP80 – Allows UHBR20 ‘native’ DP cables/connectors; Link rates:
  - 10.0 Gbps
  - 13.5 Gbps
  - 20.0 Gbps
- Active Cables (LTTPR Retimer / LRD)
  - USB4 PHY Electrical specification Alignment (IR-loss...etc)
- CableID allows DP-Tx / DP-Rx to identify DP40 / DP80 cables



- AUX-less Advanced Link Power Mode (ALPM)
  - Source can set “Main-Link-Off” by sending *ML\_PHY\_SLEEP* (k.28.1 pattern)
  - Supported on both UHBR and HBR links
- Adaptive-Sync SDP payload enhancement (also from eDP1.5)
- Improvements to DP Protocol Converter (PCON) designs
- Changes allowing USB4-V2 to work with UHBR rates over “DP Tunnel”
  - Support for UHBR (128b/132b) requires USB4-V2



# DisplayPort 2.1 Compliance: Operational Overview



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quantum data™



M42de 80G Video Analyzer/ Generator

# M42de DP 2.1 Analyzer, Generator & Compliance Tester

## Sink Emulation Mode

Laptop DFP (Source)



M42de USB-C / DP Video Analyzer

## Source Emulation Mode

DisplayPort Monitor (Sink)



M42de USB-C / DP Video Generator



- ◆ Protocol Analysis - Source Testing
  - ◆ Sink emulation EDID, DPCD.
  - ◆ Protocol Analysis – Main Link, Aux Channel.
  - ◆ Compliance Testing - Link Layer, DSC / FEC, DisplayID, HDCP.
- ◆ Video Generation - Sink Testing
  - ◆ Source emulation and Link Training control.
  - ◆ Video Pattern Testing –generation of Display Stream Compression and Forward Error Correction DSC.
  - ◆ Compliance Testing (Link Layer, DSC / FEC, DisplayID, HDCP).
- ◆ DP Alt Mode Testing
  - ◆ Run all source and sink testing through the USB-C DP Alt Mode ports.

# DisplayPort Protocol Compliance Testing - Overview

## DP Compliance Test Process:

- Complete the Capabilities Declaration Form (CDF).
- Select the specific tests in the test suite (for source or sink).
- Set or modify test iterations.
- Initiate the test suite; monitor results in real time.
- View detailed results



# DisplayPort Protocol Compliance Testing - Overview

## DP Compliance Test Process:

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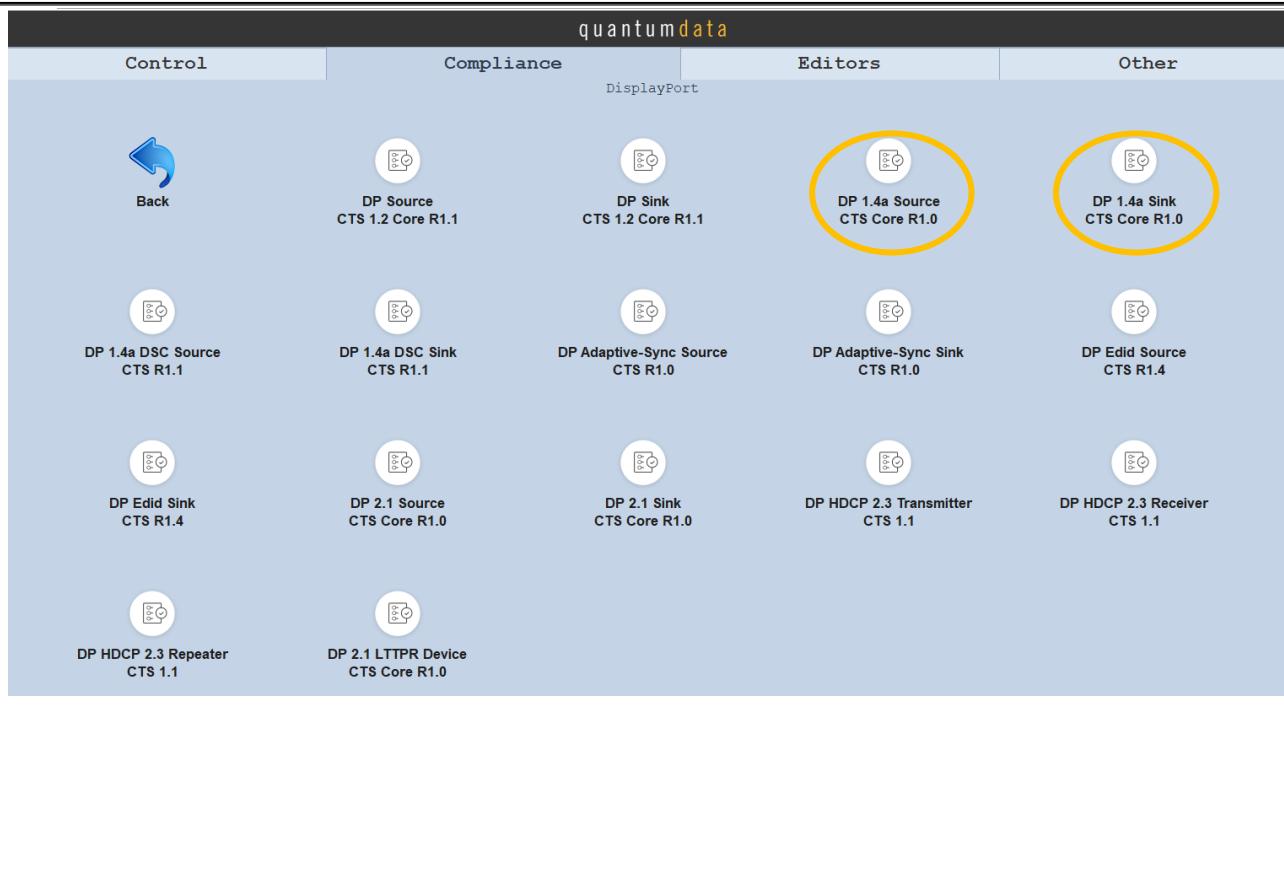
# Compliance: Specific Tests for Source / Sink / Repeater

The screenshot shows the 'Compliance' tab of the Quantumdata ATP Manager GUI. The interface has a header with 'Compliance' in large letters, a 'Control' button on the left, and an 'Other' button on the right. Below the header, there are several icons representing different test types, each with a small description below it. Two specific items, 'DP Source CTS 1.2 Core R1.1' and 'DP Sink CTS 1.2 Core R1.1', are highlighted with yellow circles. A 'Back' button is located on the left side of the main content area.

Test Type	Standard	Revision
DP Source	CTS	R1.1
DP Sink	CTS	R1.1
DP 1.4a Source	CTS	Core R1.0
DP 1.4a Sink	CTS	Core R1.0
DP 1.4a DSC Source	CTS	R1.1
DP 1.4a DSC Sink	CTS	R1.1
DP Adaptive-Sync Source	CTS	R1.0
DP Adaptive-Sync Sink	CTS	R1.0
DP Edid Source	CTS	R1.4
DP Edid Sink	CTS	R1.4
DP 2.1 Source	CTS	Core R1.0
DP 2.1 Sink	CTS	Core R1.0
DP HDCP 2.3 Transmitter	CTS	1.1
DP HDCP 2.3 Receiver	CTS	1.1
DP HDCP 2.3 Repeater	CTS	1.1
DP 2.1 LTTPR Device	CTS	Core R1.0

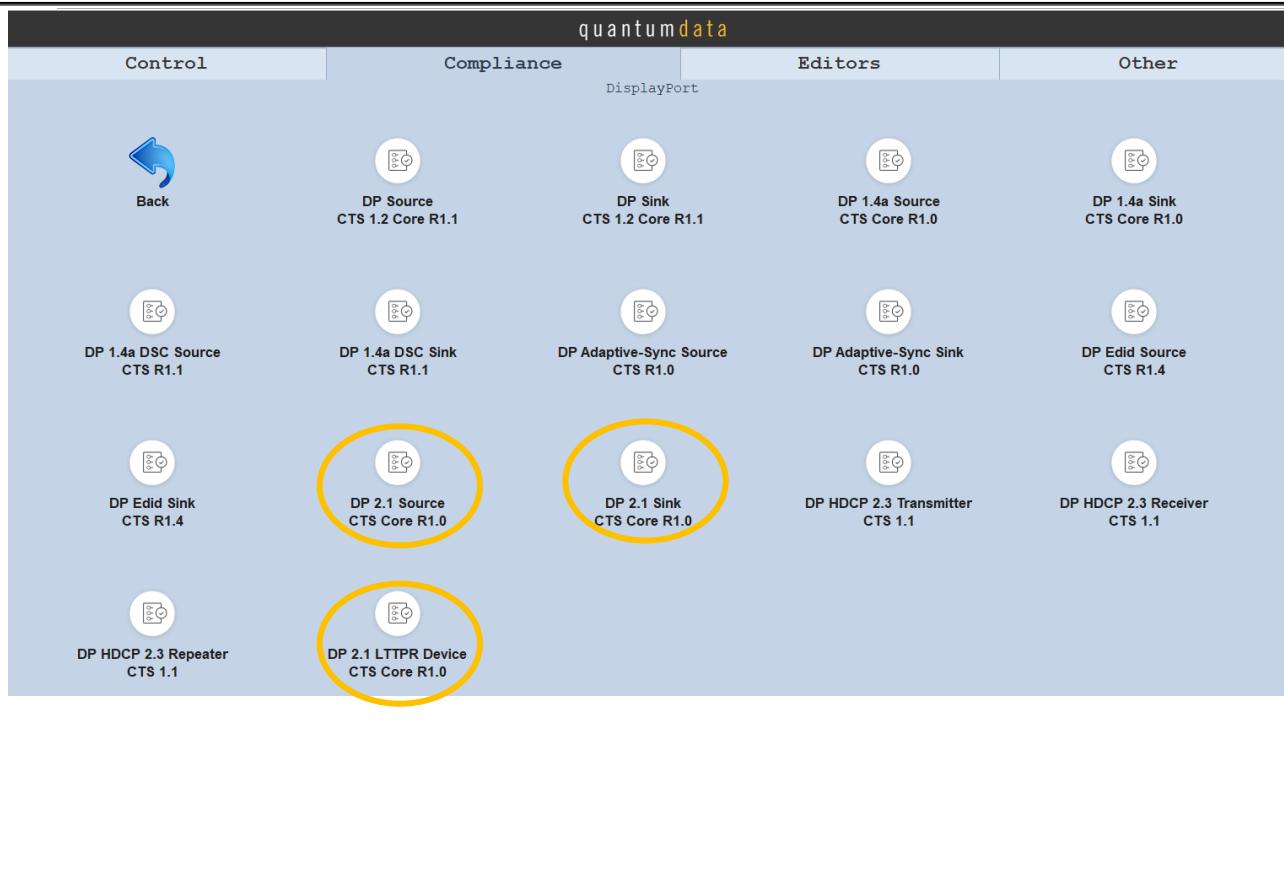
- Quantumdata ATP Manager GUI Compliance tab
- Separate test coverage for:
  - ◆ DP 1.2 CTS
  - ◆ DP 1.4a CTS
  - ◆ DP 2.1 CTS
- Separate libraries for:
  - ◆ SOURCE
  - ◆ SINK
  - ◆ Retimer
- Applications is free download from [TeledyneLecroy.com](http://TeledyneLecroy.com)

# Compliance: Specific Tests for Source / Sink / Repeater



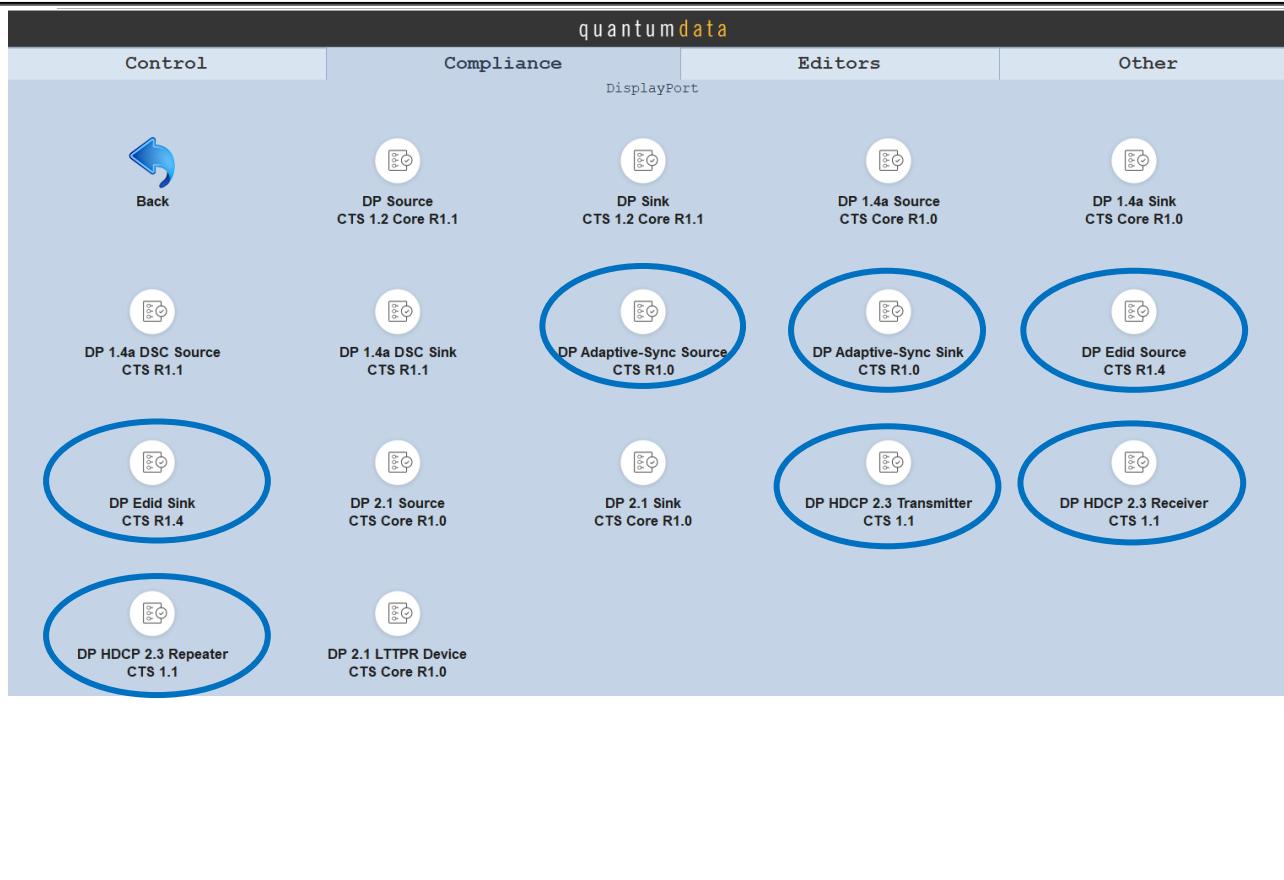
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  - ◆ DP 2.1 CTS
- Separate libraries for:
  - ◆ SOURCE
  - ◆ SINK
  - ◆ Retimer

# Source Link Layer Compliance - Entering the CDF Information

CDF Entry		Test Selection		Test Options / Preview	
New	Open	Save	Export	<not saved>	
Category		Manufacturer ⓘ		Source Platform	
General		Model ⓘ		DP 2.1 UHBR13.5	
Video		Port Tested ⓘ		h	
CDF Entry		Test Selection		Test Options / Preview	
New	Open	Save	Export	<not saved>	
Category		VIDEO_TRANSMISSION ⓘ		Yes	No
General		DP20_COLORIMETRY ⓘ		RGB	YCbCr 4:4:4
Video		DP20_BPC ⓘ		6	8
Audio		CDF Entry		10	12
Ds		Test Selection		14	16
Test Automation		Test Options / Preview		18	20
Fec		Category		22	24
Dsc		General		26	28
Test Automation		Video		30	32
Fec		SAMPLE_RATES ⓘ		34	36
Dsc		SAMPLE_SIZES ⓘ		38	40
Test Automation		MAX_CHANNEL_COUNT ⓘ		42	44
Fec		CMPR_AUDIO_SUPPORTED ⓘ		46	48
Dsc		AUDIO_INFOFRM_SUPPORTED ⓘ		50	52
Test Automation		AUDIO_SUPPORTED_WITHOUT_VIDEO ⓘ		54	56
Fec				58	60
Dsc				62	64
				66	68
				70	72
				74	76
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				90	92
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				970	972
				974	976
				978	980
				982	984
				986	988
				990	992
				994	996
				998	1000

- Capabilities Declaration Form (CDF) identifies which Link Layer features to test.
- Video – Described video capabilities of the sink.
- Audio – Described audio capabilities of the sink.
- Test Automation – Indicate if DUT supports Automated Testing register set (optional)

# Source Link Layer Compliance - Entering the CDF Information

Instrument: SupportM42D [10.30.245.19] Connect Cards

CDF Entry		Test Selection		Test Options / Preview	
New	Open	Save	Export	<not saved>	
Category	TEST_AUTOMATION ⓘ	<input checked="" type="checkbox"/> Yes	<input type="checkbox"/> No		
General	TEST_LINK_TRAINING ⓘ	<input checked="" type="checkbox"/> Yes	<input type="checkbox"/> No		
Video	TEST_EDID_READ ⓘ	<input checked="" type="checkbox"/> Yes	<input type="checkbox"/> No		
Audio	TEST_VIDEO_PATTERN ⓘ	<input checked="" type="checkbox"/> Yes	<input type="checkbox"/> No		
Test Automation	TEST_AUDIO_PATTERN ⓘ	<input checked="" type="checkbox"/> Yes	<input type="checkbox"/> No		
Fec					
Dsc					

- Capabilities Declaration Form (CDF) identifies which Link Layer features to test.
- Video – Described video capabilities of the sink.
- Audio – Described audio capabilities of the sink.
- Test Automation – Indicate if DUT supports Automated Testing register set (optional)

Support Automated Testing Register Set? (optional: DPCD 00218h through 002BFh )

- Link Training: [TEST\\_LINK\\_RATE](#) and [TEST\\_LANE\\_COUNT](#) registers
- Legacy EDID Read: [TEST\\_EDID\\_CHECKSUM\\_WRITE](#)
- Video & Audio Pattern Gen: [TEST\\_VIDEO\\_PATTERN](#) & [TEST\\_RESPONSE](#)

# Source Link Layer Compliance - Entering the CDF Information

Instrument: SupportM42D [10.30.245.19] Connect Cards

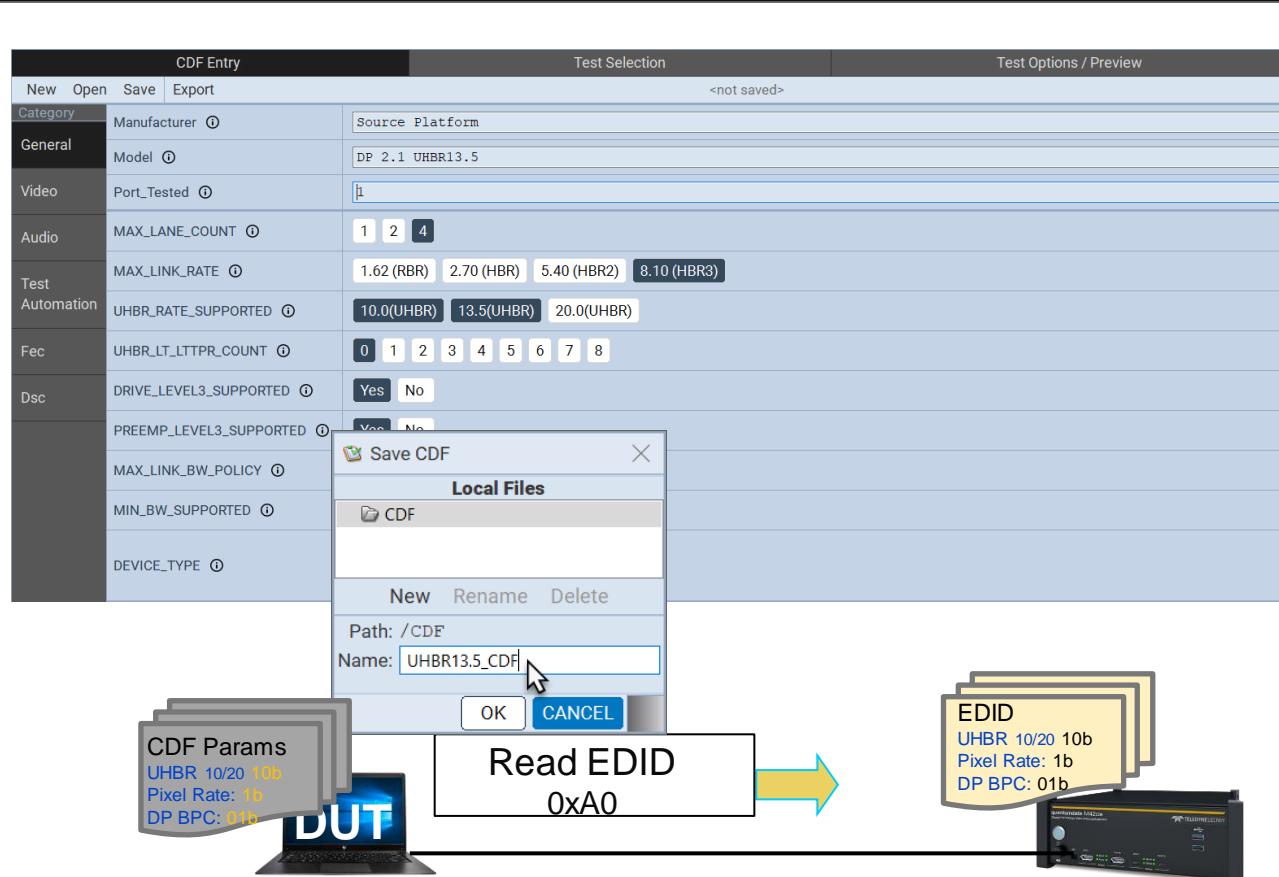
CDF Entry Test Selection Test Options / Preview

New Open Save Export <not saved>

Category	Setting	Value
General	DSC_TX_COLOR	RGB 4:4:4 Simple 4:2:2 Native 4:2:2 Native 4:2:0
Video	DSC_TX_COLOR_DEPTH	8 10 12
Audio	DSC_TX_BLOCK_PREDICTION	Yes No
Test Automation	DSC_DP20_TX_VIS_VAL	Yes No
Fec	DSC_TX_SLICE	1 2 4 8 10 12 16 20 24
Dsc		<input type="checkbox"/> 10240x4320p @ 60Hz CTA <input type="checkbox"/> 10240x4320p @ 30Hz CTA <input checked="" type="checkbox"/> 7680x4320p @ 120Hz CTA <input checked="" type="checkbox"/> 7680x4320p @ 60Hz CTA <input checked="" type="checkbox"/> 7680x4320p @ 30Hz CTA <input checked="" type="checkbox"/> 5120x2160p @ 240Hz OVT (RID = 13, FID = 18) <input checked="" type="checkbox"/> 5120x2160p @ 144Hz OVT (RID = 13, FID = 15)

- Capabilities Declaration Form (CDF) identifies which Link Layer features to test.
- Video – Described video capabilities of the sink.
- Audio – Described audio capabilities of the sink.
- Test Automation – Indicate if DUT supports Automated Testing register set (optional)

# Source Link Layer Compliance - Entering the CDF Information



- Capabilities Declaration Form (CDF) must be filled out prior to the running the test.
- CDF helps identify which Link Layer features to test.
- Video – Described video capabilities of the sink.
- Audio – Described audio capabilities of the sink.

# Source Link Layer Compliance – List of Tests

The screenshot shows a software application window titled "Test Selection". The window has tabs for "CDF Entry", "Test Selection", and "Test Options / Preview". The "Test Selection" tab is active. On the left, there is a sidebar with categories: "Link Training", "Link Maint.", "Video", "Power Management", "Fec", and "LTTPR". Under "Power Management", several test items are listed with checkboxes:

- 4.2.2.1: [DP2.1, Phase3] DPCD Receiver Capability and EDID Read upon HPD Plug Event
- 4.2.2.2: [DP2.1, Phase3] DPCD Extended Receiver Capability and EDID Read upon HPD Plug Event
- 4.2.2.4: [DP2.1, Phase3] EDID Read Failure #1: I2C-Over-AUX NACK
- 4.2.2.5: [DP2.1, Phase3] EDID Read Failure #2: I2C-Over-AUX DEFER
- 4.2.2.7: [DP2.1, Phase3] Branch Device Detection upon HPD Plug Event
- 4.2.2.8: [DP2.1, Phase3] EDID Read on IRQ HPD Event after Branch Device Detection
- 4.2.2.10: [DP2.1, Phase3] Link Status/Adjust Request AUX read interval during Link Training
- 4.2.2.11: [DP2.1, Phase1] Various UHBR AUX read interval verification in first EQ loop
- 4.2.2.12: [DP2.1, Phase1] Various UHBR AUX read interval verification in first EQ loop for 10 EQ loop

A yellow arrow points to the first item in the list, and a large black oval highlights the second item. The "Test Options / Preview" tab is visible on the right.

# Source Link Layer Compliance – List of Tests

DP 2.1 Source CT Core R1.0

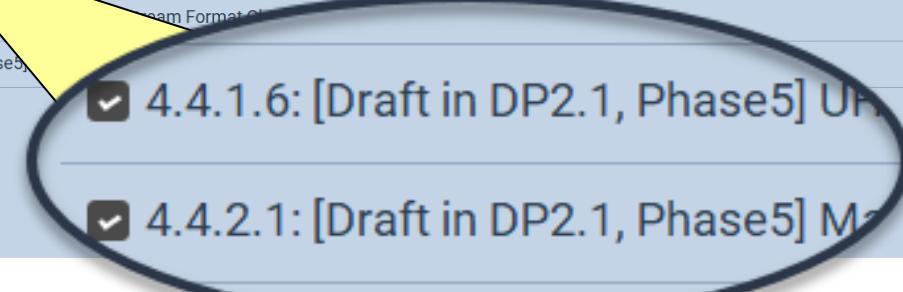
Instrument: SupportM42D [10.30.245.19] Connect Cards

CDF Entry Test Selection Test Options / Preview

Open Sav Open Save Select All Categories Deselect All Categories

Category Category Tests Select All Clear All

Category	Category	Tests	Select All	Clear All
AUX Rd. after HPD	AUX Rd. after HPD	<input checked="" type="checkbox"/> 4.3.3.1: [Draft in DP2.1, Phase5] Video Time Stamp Generation ⓘ		
EDID and DPCD Rd.	EDID and DPCD Rd.	<input checked="" type="checkbox"/> 4.3.3.2: [Draft in DP2.1, Phase5] UHBR Video Time Stamp Generation ⓘ		
Link Training	Link Training	<input checked="" type="checkbox"/> 4.4.1.1: [Draft in DP2.1, Phase5] Pixel Data Packing and Steering ⓘ		
Link Maint.	Link Maint.	<input checked="" type="checkbox"/> 4.4.1.2: [Draft in DP2.1, Phase5] Main Stream Data Packing and Stuffing Least Packed TU ⓘ		
Video	Video	<input checked="" type="checkbox"/> 4.4.1.3: [Draft in DP2.1, Phase5] Main Stream Data Packing and Stuffing Most Packed TU ⓘ		
Power Management	Power Management	<input checked="" type="checkbox"/> 4.4.1.4: [Draft in DP2.1, Phase5] UHBR Rate Pixel Data Packing and Steering ⓘ		
Audio	Audio	<input checked="" type="checkbox"/> 4.4.1.5: [Draft in DP2.1, Phase5] UHBR Rate Main Stream Data Packing and Stuffing Least Packed TU ⓘ		
Fec	Fec	<input checked="" type="checkbox"/> 4.4.1.6: [Draft in DP2.1, Phase5] UHBR Rate Main Stream Data Packing and Stuffing Most Packed TU ⓘ		
Dsc	Dsc	<input checked="" type="checkbox"/> 4.4.2.1: [Draft in DP2.1, Phase5] Main Stream Data Format Change ⓘ		
LTTPR	LTTPR	<input checked="" type="checkbox"/> 4.4.2.2: [Draft in DP2.1, Phase5] Main Stream Data Format Change ⓘ		



4.4.1.6: [Draft in DP2.1, Phase5] UHBR Rate Main Stream Data Packing and Stuffing Most Packed TU ⓘ

4.4.2.1: [Draft in DP2.1, Phase5] Main Stream Data Format Change ⓘ

# Source Link Layer Compliance – List of Tests

DP 2.1 Source CT Core R1.0

Instrument: SupportM42D [10.30.245.19] Connect Cards

CDF Entry Test Selection Test Options / Preview

Select All Count Options EXECUTE TESTS

**AUX Rd. after HPD**

- > 4.2.1.1: [DP2.1, Phase3]Source DUT Retry on No-Reply During AUX Read after HPD Plug Event 1 ✓
- > 4.2.1.2: [DP2.1, Phase3]Source Retry on Invalid Reply During AUX Read after HPD Plug Event 1 ✓
- > 4.2.1.3: [DP2.1, Phase3]Source Device HPD Event Pulse Length Test 1 ✓
- > 4.2.1.4: [DP2.1, Phase3]Source Device IRQ\_HPD Pulse Length Test 1 ✓
- > 4.2.1.5: [DP2.1, Phase3]Source Device Inactive HPD / Inactive AUX Test 1 ✓

**EDID and DPCD Rd.**

- > 4.2.2.5: [DP2.1, Phase3]EDID Read Failure #2: I2C-Over-AUX DEFER 1 ✓

◆ Validates backward

# DisplayPort 2.1 Compliance Test Breakdown



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quantum data™



M42de 80G Video Analyzer/ Generator

# DP 2.1 Compliance Coverage

	Source	Sink	Repeater / Device
Link Training	24	13	-
AUX specific	5	5	-
Link Maintenance	5	2	-
Main Stream Video	10	10	-
EDID & DPCD Reads	9	8	-
Power Management	1	2	-
Audio	5	5	-
FEC	2	12	-
DSC	9	45	-
LTTPR	23	15	66
HDCP 2.3	12	5	38
EDID / DisplayID	4	83	-
Adaptive Sync	2	3	-
Split SDP	-	5	-
DP Tunneling	-	-	7
<b>Total</b>	<b>111</b>	<b>213</b>	<b>111</b>



- 435 Total DP 2.1 Tests
- Future Development:
  - MST
  - Panel Replay
  - Native DisplayID

## ■ Link Training

- Successful Link Training at All Supported Lane Counts and UHBR Link Speeds (4.3.1.14)
- Successful Link Training 1 – 6 LTPPRs (all Lane Counts and Link Speeds) (4.9.1.4)

Link Train at all supported rates

## ■ AUX Reads after HPD Plug Event

- Source Retry on Invalid Reply During AUX Read after HPD Plug Event (4.2.1.2)
- Source Device HPD Event Pulse Length Test (4.2.1.3)

Check AUX behavior & timing after HPD

## ■ Link Maintenance

- Successful Link Re-training After IRQ HPD (Loss of Symbol Lock) (4.3.2.1)
- Handling of IRQ HPD Pulse with No Error Status Bits Set (4.3.2.4)
- Lane Count Reduction and Increase (4.3.2.5)

Link Operation; After interrupt / IRQ

## ■ Main Stream Video

- Main Video Stream Format Change Handling (4.4.2)
- Main Stream Data Packing and Stuffing – Most Packed TU (4.4.1.3)
- Configuring Video and Audio Parameters (4.4.4.1)

Correct handling & synchronization of video main

# Broad Categories for 2.1 Compliance: DP Tx

2 of 3

## ■ EDID & DPCD Reads

- DPCD Receive Capability and EDID Read upon HPD Plug Event (4.2.2.1)
- EDID Corruption Detection (4.2.2.6)

Properly Read EDID & DPCD protocol

## ■ Power Management

- Successful Entry / Exit Low Power (4.4.3)

Entry & Exit Low Power

## ■ FEC

- FEC Enable Verification for All Supported Lane Count and Link Speed (4.5.1.1)

Link Operation after interrupt / IRQ

## ■ DSC

- DSC enable sequence verification (4.6.1.1)
- DSC PPS convert RGB flag verification (4.6.1.3)

Comprehensive DSC encoding test

## ■ LTTPR

- With 6 emulated LTTPR, Successful Link Training at all Lane Counts & Link Speeds (7.1.4.7)
- With 5 emulated LTTPR, FEC status and error counter validation @ 128b/132b (7.1.7.6).

LTTPR support (up to 6)

- **HDCP 2.3**

- Regular procedure – Receiver disconnect aft Km (1A-04)
- Irregular procedure – Verify Receiver Certificate: (1A-08)

- **EDID / DisplayID**

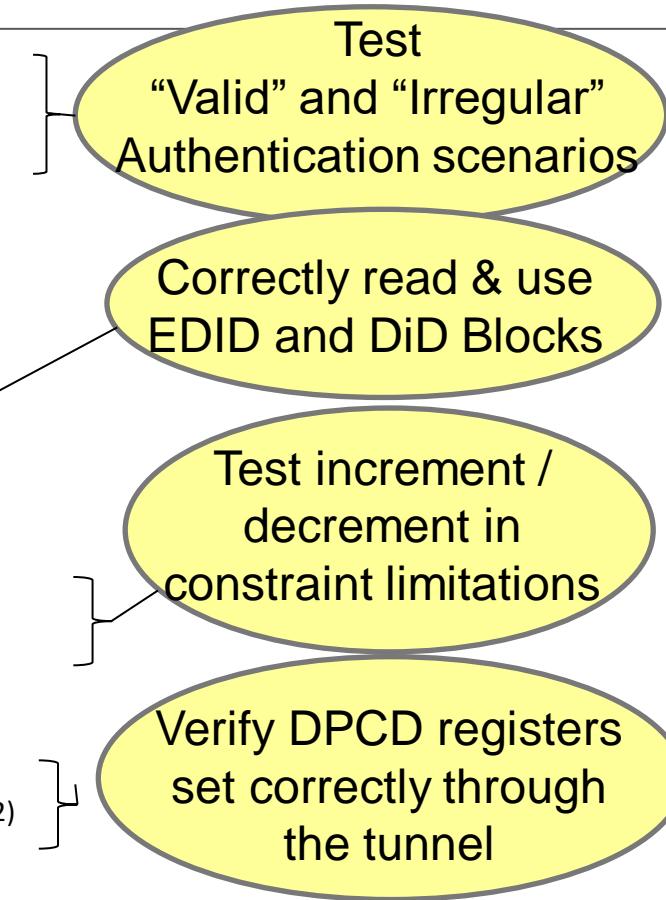
- Source device correctly read EDID (4.4.3)
- EDID Read with Unknown Extensions and Unknown Data Blocks (4.7.3.3)

- **Adaptive Sync**

- Fixed-Average VTotal Mode Duration Increase /Decrease Constraint Value (4.8.1.2 )

- **DP Tunneling**

- Source (DP Out adapter) sets correct DPCD registers at different link rates (7.2.1.3)
- FEC error counter check at max lane count & link rate: Non-Transparent mode (7.2.2.2)



# DP 2.1 Compliance Source DUT Example



**TELEDYNE LECROY**  
Everywhereyoulook™

quantum data™



# Source Link Layer Compliance – List of Tests

DP 2.1 Source (Core R1.0) Compliance Test Results			
Test Description	Test ID	Result	Notes
HTML Report	Instrument: SupportM42D [10.30.245.19]	CONTINUE TEST EXECUTION	
Results Name: Teledyne.	Manufacturer:		
Date Tested:	Model Name:		
Overall Status: Fail	Port Tested: 1		
> 4.2.2.11: [DP2.1, Phase1]Various UHBR AUX read interval verification in first EQ loop.	1	PASS	
> 4.2.2.12: [DP2.1, Phase1]UHBR Link Status/Adjust different FFE Request, different AUX read interval verification	1	PASS	
> 4.3.1.1: [DP2.1, Phase3]Successful Link Training at All Supported Lane Counts and 8b10b Link Spec	1	FAIL	
> 4.3.1.2: [DP2.1, Phase3]Successful Link Training Upon HPD Plug Event	1	PASS	
> 4.3.1.3: [DP2.1, Phase3]Successful Link Training (Higher Differential Voltage Swing during Clock Re	1	PASS	
> 4.3.1.4: [DP2.1, Phase3]Successful Link Training to a Lower Link Rate/BW #1: Iterate at Maximum V	1	PASS	
> 4.3.1.5: [DP2.1, Phase3]Successful Link Training to a Lower Link Rate/BW #2: Iterate at Minimum V	1	PASS	
> 4.3.1.6: [DP2.1, Phase3]Successful Link Training (Higher Pre-emphasis Setting during Channel Equ	1	PASS	
> 4.3.1.7: [DP2.1, Phase3]Successful Link Training (Lower Link Rate/BW During Channel Equalization)	1	PASS	
> 4.3.1.8: [DP2.1, Phase3]Unsuccessful Link Training at Lower Link Rate #1: Iterate at Maximum Volta	1	PASS	
> 4.3.1.9: [DP2.1, Phase3]Unsuccessful Link Training at Lower Link Rate #2: Iterate at Minimum Volta	1	PASS	
> 4.3.1.10: [DP2.1, Phase3]Unsuccessful Link Training (Failure in Channel Equalization)	1	PASS	
> 4.3.1.11: [DP2.1, Phase3]Successful Link Training (Simultaneous Request for Diff. Voltage Swing/P	1	PASS	
> 4.3.1.12: [DP2.1, Phase3]Source Device Link Training CR Fallback Test	1	PASS	
> 4.3.1.13: [DP2.1, Phase3]Source Device Link Training EQ Fallback Test	1	PASS	
> 4.3.1.14: [DP2.1, Phase1]Successful Link Training at All Supported Lane Counts and UHBR Link Spe	1	FAIL	
> 4.3.1.15: [DP2.1, Phase1]Successful Link Training Upon HPD Plug Event for UHBR speed	1	PASS	
> 4.3.1.16: [DP2.1, Phase1]Successful Link Training when EQ done at 20th loop during channel EQ ph	1	PASS	
> 4.3.1.17: [DP2.1, Phase1]Successful Link Training to a Lower Bandwidth, when CHANNEL_EQ_DONE	1	PASS	
> 4.3.1.18: [DP2.1, Phase1]Successful Link Training to a Lower Bandwidth. When LT Failed received ir	1	PASS	
> 4.3.1.19: [DP2.1, Phase1]Successful Link Training to a Lower Bandwidth. When LT Failed received a	1	PASS	
> 4.3.1.20: [DP2.1, Phase1]Successful Link Training to a Lower Bandwidth. When LT Failed received a	1	PASS	
> 4.3.1.21: [DP2.1, Phase1]Successful Link Training to a Lower Bandwidth. When EQ_INTERLANE_ALI	1	PASS	
> 4.3.1.22: [DP2.1, Phase1]Successful Link Training to a Lower Bandwidth. When Symbols not locked	1	PASS	
> 4.3.1.23: [DP2.1, Phase1]Successful Link Training to a Lower Bandwidth. When CDS_INTERLANE_ALI	1	PASS	



# Test 4.3.1.14: Successful Link Training: UHBR

> 4.3.1.10: [DP2.1, Phase3]Unsuccessful Link Training (Failure in Channel Equalization)	1	PASS
> 4.3.1.11: [DP2.1, Phase3]Successful Link Training (Simultaneous Request for Diff. Voltage Swing/Pre-emphasis)	1	PASS
> 4.3.1.12: [DP2.1, Phase3]Source Device Link Training CR Fallback Test	1	PASS
> 4.3.1.13: [DP2.1, Phase3]Source Device Link Training EQ Fallback Test	1	PASS
4.3.1.14: [DP2.1, Phase1]Successful Link Training at All Supported Lane Counts and UHBR Link Speeds	1	FAIL
↳ Iter 01:	-	1
> 01: [1] Link Training test for lane count = 1 and lane_rate = 10.00		FAIL
> 02: [2] Link Training test for lane count = 2 and lane_rate = 10.00		FAIL
> 03: [3] Link Training test for lane count = 4 and lane_rate = 10.00		PASS
> 04: [4] Link Training test for lane count = 1 and lane_rate = 13.50		FAIL
> 05: [5] Link Training test for lane count = 2 and lane_rate = 13.50		FAIL
> 06: [6] Link Training test for lane count = 4 and lane_rate = 13.50		PASS
> 07: [7] Link Training test for lane count = 1 and lane_rate = 20.00		FAIL
> 08: [8] Link Training test for lane count = 2 and lane_rate = 20.00		FAIL
> 09: [9] Link Training test for lane count = 4 and lane_rate = 20.00		PASS
4.3.1.15: [DP2.1, Phase1]Successful Link Training Upon HPD Plug Event for UHBR speed	1	PASS
4.3.1.16: [DP2.1, Phase1]Successful Link Training when EQ done at 20th loop during channel EQ phase	1	PASS
4.3.1.17: [DP2.1, Phase1]Successful Link Training to a Lower Bandwidth, when CHANNEL_EQ_DONE bit is set	1	PASS
4.3.1.18: [DP2.1, Phase1]Successful Link Training to a Lower Bandwidth. When LT Failed received in mid loop	1	PASS
4.3.1.19: [DP2.1, Phase1]Successful Link Training to a Lower Bandwidth. When LT Failed received at 20th loop	1	PASS
4.3.1.20: [DP2.1, Phase1]Successful Link Training to a Lower Bandwidth. When LT Failed received at after 20th loop	1	PASS
4.3.1.21: [DP2.1, Phase1]Successful Link Training to a Lower Bandwidth. When EQ_INTERLANE_ALIGN_	1	PASS
4.3.1.22: [DP2.1, Phase1]Successful Link Training to a Lower Bandwidth. When Symbols not locked during training	1	PASS
4.3.1.23: [DP2.1, Phase1]Successful Link Training to a Lower Bandwidth. When CDS_INTERLANE_ALIGN	1	PASS
4.3.1.24: [DP2.1, Phase3] UHBR Fallback rate table validation.	1	PASS



# Test 4.3.1.14: Successful Link Training: UHBR

> 4.3.1.10: [DP2.1, Phase3]Unsuccessful Link Training (Failure in Channel Equalization)		1	PASS
> 4.3.1.11: [DP2.1, Phase3]Successful Link Training (Simultaneous Request for Diff. Voltage Swing/Pre-em		1	PASS
> 4.3.1.12: [DP2.1, Phase3]Source Device Link Training CR Fallback Test		1	PASS
> 4.3.1.13: [DP2.1, Phase3]Source Device Link Training EQ Fallback Test		1	PASS
▽ 4.3.1.14: [DP2.1, Phase1]Successful Link Training at All Supported Lane Counts and UHBR Link Speeds		1	FAIL
▽ Iter 01:	-	1	FAIL
> 01: [1] Link Training test for lane count = 1 and lane_rate = 10.00			FAIL
> 02: [2] Link Training test for lane count = 2 and lane_rate = 10.00			FAIL
• Applying EDID: test_edid_2.bin			
• Source DUT sets 128b132b encoding before TPS1 .			
• Source DUT waits for status register 205h to verify LT termination before TPS1.			
• Source DUT sets expected Link Rate= 10.00Gbps.			
• Source DUT sets expected Lane count= 0x2.			
• Source DUT sets TPS1 (DPCD 102h 3:0 bits=1) for Training.			
• Source DUT reads 128b132b AUX read interval register 2216h before TPS2.			
• Source DUT Reads FFE Values Adjustment for all lanes before TPS2.			
• Source DUT sets TP2 (DPCD 102h 3:0 bits=2) for EQ Training .			
• Source DUT writes DPCD 00102h through 00104h in a single AUX transaction.			
• Source DUT Writes FFE preset Values Adjustment for all lanes with TPS2.			
• Source DUT does not set TPS2 CDS Sequence (DPCD 102h 3:0 bits=3) before Training Finish.			
• Source DUT does not read status register 202h to verify Symbol lock status after TPS2 CDS Sequence.			
• Source DUT does not wait for symbol lock on all lanes before Training Finish.			
• Source DUT does not wait for TPS2 CDS Sequence Done before Training Finish.			
• Source DUT sets TPS0 (DPCD 102h 3:0 bits=0) to Finish Training.			
• Source DUT finished Link Training under 650ms (actual time 160216us).			

# Test 4.3.1.14: Successful Link Training: UHBR

			Open	Close	Export	Options	Filter	Find
[ACA-4_3_1_14_01] Events: 16246 (37288)								
3090	DPLT	13	> W:100	LINK_BW_SET	L=1 06			
3091	DPLT	13	< ACK					
3092	DPLT	13	> W:102	TRAINING_PATTERN_SET:	L=2 21 00			
3093	DPLT	13	< ACK					
3094	DPLT	13	> R:202	LANE0_1_STATUS:	L=6			
3095	DPLT	13	< DEFER					
3096	DPLT	13	> R:202	LANE0_1_STATUS:	L=6			
3097	DPLT	13	< DEFER					
3098	DPLT	13	> R:202	LANE0_1_STATUS:	L=6			
3099	DPLT	13	< DEFER					
3100	DPLT	13	> R:202	LANE0_1_STATUS:	L=6			
3101	DPLT	13	< DEFER					
3102	DPLT	13	> R:202	LANE0_1_STATUS:	L=6			
3103	DPLT	13	< DEFER					
3104	DPLT	13	> R:202	LANE0_1_STATUS:	L=6			
3105	DPLT	13	< DEFER					
3106	DPLT	13	> R:202	LANE0_1_STATUS:	L=6			
3107	DPLT	13	< ACK 01 00 80 00 00 00					
3108	DPLT	13	> W:102	TRAINING_PATTERN_SET:	L=2 07 00			
3109	DPLT	13	< ACK					
3110	DPLT	13	> R:202	LANE0_1_STATUS:	L=6			
3111	DPLT	13	< ACK 03 00 81 00 04 00					
3112	DPLT	13	> W:103	TRAINING_LANE0_SET	L=1 08			
3113	DPLT	13	< ACK					
3114	DPLT	13	> R:202	LANE0_1_STATUS:	L=6			
3115	DPLT	13	< ACK 03 00 01 00 08 00					
3116	DPLT	13	> W:103	TRAINING_LANE0_SET	L=1 10			
...	...	...	...	...	...	...	...	...

<p>Start Time: +00:24:36.735283 Type: Native Direction: Request Command: Write Address: 0x00102 (TRAINING_PATTERN_SET:)</p> <p>Length: 2</p> <p>00102: TRAINING_PATTERN_SET: 8b/10b Link Layer</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>3-0</td> <td>TRAINING_PATTERN_SELECT</td> <td>1</td> <td>Pattern 1</td> </tr> <tr> <td>4</td> <td>RECOVERED_CLOCK_OUT_EN</td> <td>N(0)</td> <td></td> </tr> <tr> <td>5</td> <td>SCRAMBLING_DISABLE</td> <td>Y(1)</td> <td></td> </tr> <tr> <td>7-6</td> <td>SYMBOL_ERROR_COUNT_SEL</td> <td>0</td> <td>Disparity and Symbol err</td> </tr> </tbody> </table> <p>128b/132b Link Layer</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>3-0</td> <td>TRAINING_PATTERN_SELECT</td> <td>1</td> <td>128b/132b TPS1</td> </tr> <tr> <td>4</td> <td></td> <td>0</td> <td>Reserved</td> </tr> </tbody> </table> <p>00102: TRAINING_PATTERN_SET: 8b/10b Link Layer</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>3-0</td> <td>TRAINING_PATTERN_SELECT</td> <td>7</td> <td>Pattern 4</td> </tr> <tr> <td>4</td> <td>RECOVERED_CLOCK_OUT_EN</td> <td>N(0)</td> <td></td> </tr> <tr> <td>5</td> <td>SCRAMBLING_DISABLE</td> <td>N(0)</td> <td></td> </tr> <tr> <td>7-6</td> <td>SYMBOL_ERROR_COUNT_SEL</td> <td>0</td> <td>Disparity and Symbol err</td> </tr> </tbody> </table> <p>128b/132b Link Layer</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>3-0</td> <td>TRAINING_PATTERN_SELECT</td> <td>7</td> <td>Reserved</td> </tr> <tr> <td>4</td> <td></td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>5</td> <td></td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>6</td> <td></td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>7</td> <td></td> <td>0</td> <td>Reserved</td> </tr> </tbody> </table> <p>00103: TRAINING_LANE0_SET 8b/10b Link Layer</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>3-0</td> <td>TRAINING_PATTERN_SELECT</td> <td>7</td> <td>Reserved</td> </tr> <tr> <td>4</td> <td></td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>5</td> <td></td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>6</td> <td></td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>7</td> <td></td> <td>0</td> <td>Reserved</td> </tr> </tbody> </table> <p>128b/132b Link Layer</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>3-0</td> <td>TRAINING_PATTERN_SELECT</td> <td>7</td> <td>Reserved</td> </tr> <tr> <td>4</td> <td></td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>5</td> <td></td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>6</td> <td></td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>7</td> <td></td> <td>0</td> <td>Reserved</td> </tr> </tbody> </table>	Bit	Name	Value	Description	3-0	TRAINING_PATTERN_SELECT	1	Pattern 1	4	RECOVERED_CLOCK_OUT_EN	N(0)		5	SCRAMBLING_DISABLE	Y(1)		7-6	SYMBOL_ERROR_COUNT_SEL	0	Disparity and Symbol err	Bit	Name	Value	Description	3-0	TRAINING_PATTERN_SELECT	1	128b/132b TPS1	4		0	Reserved	Bit	Name	Value	Description	3-0	TRAINING_PATTERN_SELECT	7	Pattern 4	4	RECOVERED_CLOCK_OUT_EN	N(0)		5	SCRAMBLING_DISABLE	N(0)		7-6	SYMBOL_ERROR_COUNT_SEL	0	Disparity and Symbol err	Bit	Name	Value	Description	3-0	TRAINING_PATTERN_SELECT	7	Reserved	4		0	Reserved	5		0	Reserved	6		0	Reserved	7		0	Reserved	Bit	Name	Value	Description	3-0	TRAINING_PATTERN_SELECT	7	Reserved	4		0	Reserved	5		0	Reserved	6		0	Reserved	7		0	Reserved	Bit	Name	Value	Description	3-0	TRAINING_PATTERN_SELECT	7	Reserved	4		0	Reserved	5		0	Reserved	6		0	Reserved	7		0	Reserved		
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# TD 4.3.1.12: Source Link Training CR Fallback Test

ACa Data Viewer

Open Close Export Options Filter Find

[ACA-4.3\_1\_12\_01] Events: 620 (1956)

49 DNAT 13 < ACK 00  
50 DNAT 13 > W:111 MSTM\_CTRL L=1 00  
51 DNAT 13 < ACK  
52 DPDT 13 > W:102 TRAINING\_PATTERN\_SET: L=1 00  
53 DPDT 13 < ACK  
54 DPDT 13 > W:100 LINK\_BW\_SET L=1 1E  
55 DPDT 13 < ACK  
56 DPDT 13 > W:101 LANE\_COUNT\_SET L=1 84  
57 DPDT 13 < ACK  
58 DPDT 13 > W:102 TRAINING\_PATTERN\_SET: L=5 21 00 00 00 00  
59 DPDT 13 < DEFER  
60 DPDT 13 < ACK  
61 DPDT 13 < DEFER

Start Time: +01:44:27.939637  
Type: Native  
Direction: Request  
Command: Write  
Address: 0x00100 (LINK\_BW\_SET)  
Length: 1  
00100: LINK\_BW\_SET  
Bit Name Value Description  
7-0 LINK\_BW\_SET 1EH 8.1 Gbps/lane

ACa Data Viewer

Open Close Export Options Filter Find

[ACA-4.3\_1\_12\_01] Events: 620 (1956)

122 DPDT 13 > W:102 TRAINING\_PATTERN\_SET: L=1 00  
123 DPDT 13 < ACK  
124 DPDT 13 > W:100 LINK\_BW\_SET L=1 14  
125 DPDT 13 < ACK  
126 DPDT 13 > W:101 LANE\_COUNT\_SET L=1 84  
127 DPDT 13 < ACK  
128 DPDT 13 > W:102 TRAINING\_PATTERN\_SET: L=5 21 00 00 00 00  
129 DPDT 13 < ACK  
130 DPDT 13 > R:202 LANE\_1\_STATUS: L=6  
131 DPDT 13 < DEFER  
132 DPDT 13 < ACK  
133 DPDT 13 < DEFER

Start Time: +01:44:28.036554  
Type: Native  
Direction: Request  
Command: Write  
Address: 0x00100 (LINK\_BW\_SET)  
Length: 1  
00100: LINK\_BW\_SET  
Bit Name Value Description  
7-0 LINK\_BW\_SET 14H 5.4 Gbps/lane  
f00001f80 01 00 00 14 -- -- -1f 1

ACa Data Viewer

Open Close Export Options Filter Find

[ACA-4.3\_1\_12\_01] Events: 620 (1956)

193 DNAT 13 < ACK 00  
194 DNAT 13 > W:111 MSTM\_CTRL L=1 00  
195 DNAT 13 < ACK  
196 DPDT 13 > W:102 TRAINING\_PATTERN\_SET: L=1 00  
197 DPDT 13 < ACK  
198 DPDT 13 > W:100 LINK\_BW\_SET L=1 1E  
199 DPDT 13 < ACK  
200 DPDT 13 > W:101 LANE\_COUNT\_SET  
201 DPDT 13 < ACK  
202 DPDT 13 > W:102 TRAINING\_PATTERN\_SET: L=5 21 00 00 00 00  
203 DPDT 13 < ACK  
204 DPDT 13 > R:202  
205 DPDT 13 < DEFER

Start Time: +01:44:28.117418  
Type: Native  
Direction: Request  
Command: Write  
Address: 0x00100 (LINK\_BW\_SET)  
Length: 1

LINK BW SET  
1EH 8.1 Gbps/lane

ACa Data Viewer

Open Close Export Options Filter Find

[ACA-4.3\_1\_12\_01] Events: 620 (1956)

190 DNAT 13 > W:120 FEC\_CONFIGURATION L=1 00  
191 DNAT 13 < ACK  
192 DNAT 13 > R:111 MSTM\_CTRL L=1  
193 DNAT 13 < ACK 00  
194 DNAT 13 > W:111 MSTM\_CTRL L=1 00  
195 DNAT 13 < ACK  
196 DPDT 13 > W:102 TRAINING\_PATTERN\_SET: L=1 00  
197 DPDT 13 < ACK  
198 DPDT 13 > W:100 LINK\_BW\_SET L=1 1E  
199 DPDT 13 < ACK  
200 DPDT 13 > W:101 LANE\_COUNT\_SET L=1 82  
201 DPDT 13 < ACK  
202 DPDT 13 > W:102 TRAINING\_PATTERN\_SET: L=5 21 00 00 00 00 00  
203 DPDT 13 < ACK

Start Time: +01:44:28.117918  
Type: Native  
Direction: Request  
Command: Write  
Address: 0x00101 (LANE\_COUNT\_SET)  
Length: 1  
00101: LANE\_COUNT\_SET  
Bit Name Value Description  
4-0 LANE\_COUNT\_SET 2 2 lanes  
5 POST\_LT\_ADJ\_REQ\_GRANTED N(0) 0 Reserved  
7 ENHANCED\_FRAME\_CAP Y(1) 1  
[0000][80 01 01 00 82 -- -- -] [.....]

8.1Gb/s & 4 Lanes

5.4Gb/s & 4 Lanes

LINK BW SET  
1EH 8.1 Gbps/lane

8.1Gb/s & 2 Lanes

2.7 Gb/s &  
4 Lanes  
Expected

# Source EDID & Display ID vs EDID Link Layer test

DP Edid Source CTR1.4

Instrument: SupportM42D [10.30.245.19] Connect Cards **Included with DP EDID Source test**

CDF Entry	Test Selection	Test Options / Preview
Select All	Count Options	<b>EXEC</b>
Video		
> 4.7.1.1: Basic Supported Formats		1
> 4.7.1.2: Preferred Timing		1
> 4.7.1.3: Out-of-Range Request		1
> 4.7.1.4: Invalid EDID		
Audio		
> 4.7.2.1: Basic Supported Formats		
> 4.7.2.2: Out-of-Range Request		
EDDC		
> 4.7.3.1: EDID Read with More than 16 bytes		
> 4.7.3.2: EDID Read with Greater than 16 bytes		
> 4.7.3.3: EDID Read with Unknown Address		
DisplayID		
> 4.7.4.1: DisplayID Detailed Timing		
Adaptive-Sync		
> 4.7.5.1: DisplayID Adaptive-Sync		

DP 2.1 Source CT Core R1.0

Instrument: SupportM42D [10.30.245.19] Connect Cards **Included with DP 2.1 Link Layer Source tests**

CDF Entry	Test Selection	Test Options / Preview
Select All	Count Options	<b>EXECUTE TESTS</b>
EDID and DPCD Rd.		
> 4.2.2.1: [DP2.1, Phase3]DPCD Receiver Capability and EDID Read upon HPD Plug Event		1 ✓
> 4.2.2.2: [DP2.1, Phase3]DPCD Extended Receiver Capability and EDID Read upon HPD Plug Event		1 ✓
> 4.2.2.4: [DP2.1, Phase3]EDID Read Failure #1: I2C-Over-AUX NACK		1 ✓
> 4.2.2.5: [DP2.1, Phase3]EDID Read Failure #2: I2C-Over-AUX DEFER		1 ✓
> 4.2.2.7: [DP2.1, Phase3]Branch Device Detection upon HPD Plug Event		1 ✓
> 4.2.2.8: [DP2.1, Phase3]EDID Read on IRQ HPD Event after Branch Device Detection		1 ✓
> 4.2.2.10: [DP2.1, Phase3]Link Status/Adjust Request AUX read interval during Link Training		1 ✓
> 4.2.2.11: [DP2.1, Phase1]Various UHBR AUX read interval verification in first EQ loop.		1 ✓
> 4.2.2.12: [DP2.1, Phase1]UHBR Link Status/Adjust different FFE Request, different AUX read interval for 10 EQ loop		1 ✓

# TD 4.2.2.11 Various UHBR AUX read intervals in first EQ loop

	Open	Close	Export	Options	Filter	Find																																
[ACA-4_2_2_11_01] Events: 25304																																						
538	DNAT	13	-00:00:00.009065	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1	Start Time: -00:00:00.00874	Test Case # 128b/132b_TRAINING_AUX_RD_INTERVAL (02216h)																																
539	DPFRE	13	-00:00:00.008743	Precharge/Sync Count: 32	Type: Native																																	
540	DNAT	13	-00:00:00.008743	< ACK 80	Direction: Reply	80h																																
541	DPFRE	13	-00:00:00.007978	Precharge/Sync Count: 45	Command: ACK	1a																																
542	DPLT	13	-00:00:00.007978	> R:202 LANE0_1_STATUS: L=6	Reply to Read Request.	00h																																
543	DPPRE	13	-00:00:00.007656	Precharge/Sync Count: 32	02216: 128b/132b_TRAINING_AUX_RD	1c																																
544	DPLT	13	-00:00:00.007656	< DEFER	Bit Name	83h																																
545	DPPRE	13	-00:00:00.006904	Precharge/Sync Count: 45	6-0 128b/132b_TRAINING_AUX_E	1d																																
546	DPLT	13	-00:00:00.006904	> R:202 LANE0_1_STATUS: L=6	Length: 5	88h																																
547	Open	Close	Export	Options	Start Time: +00:00:00.001538	1e																																
548	[ACA-4_2_2_11_01] Events: 25304																																					
549	DPFRE	13	-00:00:00.001538	Precharge/Sync Count: 45	Type: Native	B1h																																
556	DPLT	13	-00:00:00.001538	> R:202 LANE0_1_STATUS: L=6	Direction: Request	E3h																																
567	DPFRE	13	-00:00:00.001216	Precharge/Sync Count: 32	Command: Write	63h																																
568	DPLT	13	-00:00:00.001216	< ACK 11 11 80 00 00 00	Address: 0x00102																																	
569	DPFRE	13	+00:00:00.000000	Precharge/Sync Count: 45	Length: 5	7Fh																																
570	DPLT	13	+00:00:00.000000	> R:102 TRAINING_PATTERN_SET: L=5 02 00 00 00 00 00	00102: TRAINING_PATTERN_SET:																																	
571	DPFRE	13	+00:00:00.000113	Precharge/Sync Count: 32	8b/10b Link Layer																																	
572	DPLT	13	+00:00:00.000113	< ACK	Bit Name																																	
573	DPFRE	13	+00:00:00.001876	Precharge/Sync Count: 45	Value Description																																	
574	DPLT	13	+00:00:00.001876	> R:202 LANE0_1_STATUS: L=6	3-0 TRAINING_PATTERN_SELECT	2 Pattern 2																																
575	DPFRE	13	+00:00:00.001949	Precharge/Sync Count: 32																																		
576	Open	Close	Export	Options	Start Time: +00:00:00.001876																																	
578	[ACA-4_2_2_11_01] Events: 25304																																					
579	DPLT	13	-00:00:00.001216	< ACK 11 11 80 00 00 00	Type: Native																																	
580	DPFRE	13	+00:00:00.000000	Precharge/Sync Count: 45	Direction: Request																																	
581	DPLT	13	+00:00:00.000000		Command: Write																																	
571	DPFRE	13	+00:00:00.000000	Precharge/Sync Count: 45	Address: 0x00102																																	
<p style="text-align: center;">Verify &gt; 1 MS</p> <table border="1"> <tr> <td>PRE</td> <td>13</td> <td>+00:00:00.000000</td> <td>Precharge/Sync Count: 45</td> </tr> <tr> <td>DPLT</td> <td>13</td> <td>+00:00:00.000113</td> <td>&gt; W:102 TRAINING_PATTERN_SET: L=5 02 00 00 00 00 00 00</td> </tr> <tr> <td>PRE</td> <td>13</td> <td>+00:00:00.000113</td> <td>Precharge/Sync Count: 32</td> </tr> <tr> <td></td> <td></td> <td>&lt; ACK</td> <td></td> </tr> <tr> <td></td> <td></td> <td>Precharge/Sync Count: 45</td> <td></td> </tr> <tr> <td></td> <td></td> <td>&gt; R:202 LANE0_1_STATUS: L=6</td> <td></td> </tr> <tr> <td></td> <td></td> <td>Precharge/Sync Count: 32</td> <td></td> </tr> <tr> <td></td> <td></td> <td></td> <td>574: &gt; R:202 LANE0_1_STATUS: L=6</td> </tr> </table>							PRE	13	+00:00:00.000000	Precharge/Sync Count: 45	DPLT	13	+00:00:00.000113	> W:102 TRAINING_PATTERN_SET: L=5 02 00 00 00 00 00 00	PRE	13	+00:00:00.000113	Precharge/Sync Count: 32			< ACK				Precharge/Sync Count: 45				> R:202 LANE0_1_STATUS: L=6				Precharge/Sync Count: 32					574: > R:202 LANE0_1_STATUS: L=6
PRE	13	+00:00:00.000000	Precharge/Sync Count: 45																																			
DPLT	13	+00:00:00.000113	> W:102 TRAINING_PATTERN_SET: L=5 02 00 00 00 00 00 00																																			
PRE	13	+00:00:00.000113	Precharge/Sync Count: 32																																			
		< ACK																																				
		Precharge/Sync Count: 45																																				
		> R:202 LANE0_1_STATUS: L=6																																				
		Precharge/Sync Count: 32																																				
			574: > R:202 LANE0_1_STATUS: L=6																																			

- Tester waits for SRC to read 0x2216 Training AUX Read Interval
- Tester Replies "80" (indicates 1ms Interval)
- Tester waits for SRC to Assert "TPS2"
- Tester Verifies Source waits at 1 MS before reading "Sink Status":
  - Actual: 1.876 MS

# DP 2.1 Compliance Sink DUT Example



**TELEDYNE LECROY**  
Everywhereyoulook™



M42de operating as DP  
2.1 Reference Source:



# Sink Video Compliance – List of Tests

DP 2.1 Sink (Core R1.0) Compliance Test Results					
HTML Report		Instrument: SupportM42D [10.30.245.19] ▾	CONTINUE TEST EXECUTION		
Results Name: <b>Teledyne</b> , Date Tested: <b>March: 2023</b>		Manufacturer: <b>UHBR Sink OEM</b> Model Name: Port Tested: <b>USBC</b>			
Overall Status: <b>CTS Core R1.0 - Pass</b>					
<ul style="list-style-type: none"><li>&gt; 5.4.1.1: [Draft in DP2.1, Phase5]Pixel Data Reconstruction</li><li>&gt; 5.4.1.2: [Draft in DP2.1, Phase5]Main Stream Data Unpacking and Unstuffing - Least Packed TU</li><li>&gt; 5.4.1.3: [Draft in DP2.1, Phase5]Main Stream Data Unpacking and Unstuffing - Most Packed TU</li><li>&gt; 5.4.1.4: [Draft in DP2.1, Phase5]Pixel Clock Recovery</li><li>  ↳ 5.4.1.5: [Draft in DP2.1, Phase5]UHBR rate Pixel Data Reconstruction<ul style="list-style-type: none"><li>↳ Iter 01:<ul style="list-style-type: none"><li>&gt; 01: Link Training at lane count = 1 and lane rate = 13.50 Gbps</li><li>&gt; 02: Link Training at lane count = 2 and lane rate = 13.50 Gbps</li><li>&gt; 03: Link Training at lane count = 4 and lane rate = 13.50 Gbps</li></ul></li><li>&gt; 5.4.1.6: [Draft in DP2.1, Phase5]UHBR rate Main Stream Data Unpacking and Unstuffing - 1080p Fallback</li><li>&gt; 5.4.1.7: [Draft in DP2.1, Phase5]UHBR Main Stream Data Unpacking and Unstuffing - Most Packed TU</li><li>&gt; 5.4.1.8: [Draft in DP2.1, Phase5]UHBR Pixel Clock Recovery</li></ul></li><li>  ↳ 5.4.2.1: [Draft in DP2.1, Phase5]Main Video Stream Format Change Handling</li><li>  ↳ 5.4.2.2: [Draft in DP2.1, Phase5] UHBR-Main Video Stream Format Change Handling</li></ul>					

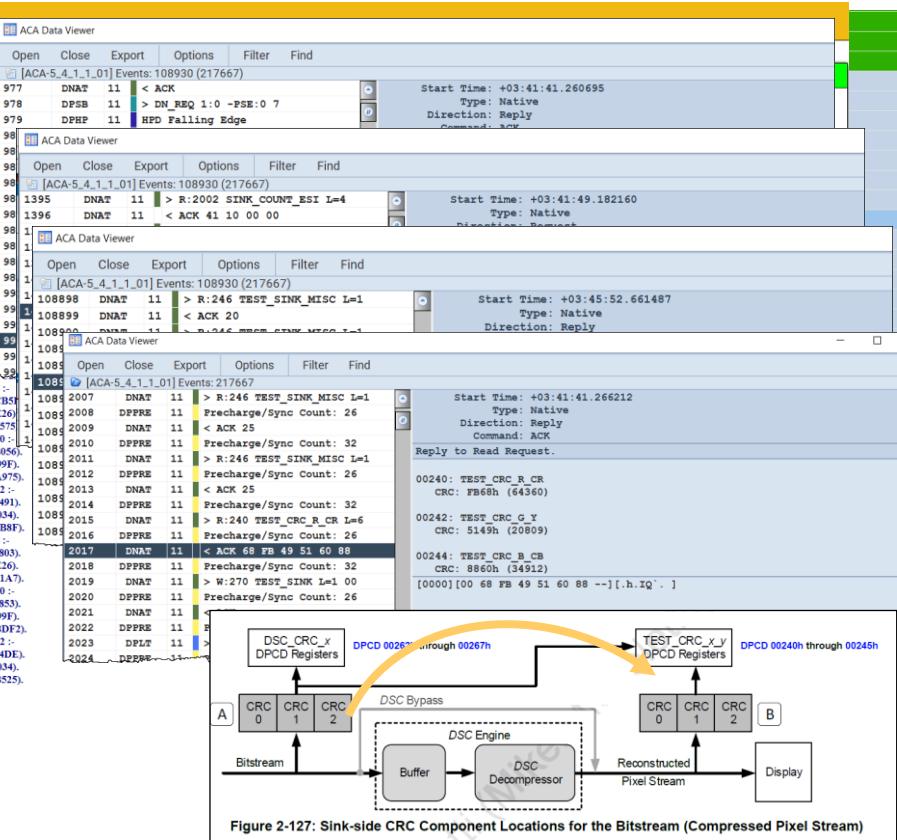
# Sink Link Layer Compliance – Test 5.4.1.5: UHBR Pixel Data Reconstruction

Test 5.4.1.5  
[Draft in DP2.1, Phase5]UHBR rate Pixel Data Reconstruction

\* Iter 01:

\* #1: Link Training at lane count = 1 and lane rate = 13.50 Gbps

- HPD is asserted
- Value of DPCD F0000h is 0
- Reference Source receives AUX\_ACK at 1 attempts
- Reference Source receives AUX\_ACK from either write request
- Sink DUT Capability supports UHBR RATE = 13.50 Gbps and MAX\_LANE\_COUNT = 1
- Link Training at lane count 1 and link rate 13.50 successful
- After sending test pattern at 1920X1080 @60Hz, colorimetry = RGB VESA and bpc = 6
- TEST\_CRC\_R\_Cr field equals to the Reference Source's internal CRC calculations (0x8)
- TEST\_CRC\_G\_Y field equals to the Reference Source's internal CRC calculations (0x5)
- TEST\_CRC\_B\_Cb field equals to the Reference Source's internal CRC calculations (0x0)
- After sending test pattern at 1920X1080 @60Hz, colorimetry = RGB VESA and bpc = 8
- TEST\_CRC\_R\_Cr field equals to the Reference Source's internal CRC calculations (0x0)
- TEST\_CRC\_G\_Y field equals to the Reference Source's internal CRC calculations (0x0)
- TEST\_CRC\_B\_Cb field equals to the Reference Source's internal CRC calculations (0x0)
- After sending test pattern at 1920X1080 @60Hz, colorimetry = RGB VESA and bpc = 12
- TEST\_CRC\_R\_Cr field equals to the Reference Source's internal CRC calculations (0x8)
- TEST\_CRC\_G\_Y field equals to the Reference Source's internal CRC calculations (0x5)
- TEST\_CRC\_B\_Cb field equals to the Reference Source's internal CRC calculations (0x0)
- After sending test pattern at 1920X1080 @60Hz, colorimetry = YCbCr 4:4:4 and bpc = 8
- TEST\_CRC\_R\_Cr field equals to the Reference Source's internal CRC calculations (0x8E26)
- TEST\_CRC\_G\_Y field equals to the Reference Source's internal CRC calculations (0x2575)
- After sending test pattern at 1920X1080 @60Hz, colorimetry = YCbCr 4:4:4 and bpc = 12
- TEST\_CRC\_R\_Cr field equals to the Reference Source's internal CRC calculations (0xA975)
- After sending test pattern at 1920X1080 @60Hz, colorimetry = YCbCr 4:4:4 and bpc = 12
- TEST\_CRC\_R\_Cr field equals to the Reference Source's internal CRC calculations (0x491)
- TEST\_CRC\_G\_Y field equals to the Reference Source's internal CRC calculations (0x934)
- TEST\_CRC\_B\_Cb field equals to the Reference Source's internal CRC calculations (0x5B9F)
- After sending test pattern at 1920X1080 @60Hz, colorimetry = YCbCr 4:2:2 and bpc = 8
- TEST\_CRC\_R\_Cr field equals to the Reference Source's internal CRC calculations (0x2B03)
- TEST\_CRC\_G\_Y field equals to the Reference Source's internal CRC calculations (0x9E26)
- TEST\_CRC\_B\_Cb field equals to the Reference Source's internal CRC calculations (0x01A7)
- After sending test pattern at 1920X1080 @60Hz, colorimetry = YCbCr 4:2:2 and bpc = 12
- TEST\_CRC\_R\_Cr field equals to the Reference Source's internal CRC calculations (0x9853)
- TEST\_CRC\_G\_Y field equals to the Reference Source's internal CRC calculations (0xE99F)
- TEST\_CRC\_B\_Cb field equals to the Reference Source's internal CRC calculations (0xB1DF)
- After sending test pattern at 1920X1080 @60Hz, colorimetry = YCbCr 4:2:2 and bpc = 12
- TEST\_CRC\_R\_Cr field equals to the Reference Source's internal CRC calculations (0x84DE)
- TEST\_CRC\_G\_Y field equals to the Reference Source's internal CRC calculations (0xC034)
- TEST\_CRC\_B\_Cb field equals to the Reference Source's internal CRC calculations (0xB525)



- ◆ Tester sends the test pattern at 1920x1080p @60Hz
- ◆ Tester reads the TEST\_CRC\_SUPPORTED bit
- ◆ Tester sets the TEST\_SINK\_START bit
- ◆ Tester Reads the TEST\_CRC\_COUNT field; Waits until > 0
- ◆ Tester reads the TEST\_CRC\_x\_x fields
- ◆ then clears the TEST\_SINK\_START bit
- ◆ Verify that TEST\_CRC\_x\_x fields = to Testers internal CRC calculations

## Test 5.3.2.2: Sink IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock

> 5.2.2.3: [DP2.1, Phase2]Sink Status		1	PASS
<b>5.3.2.2: [DP2.1, Phase2]IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock</b>		1	PASS
↳ Iter 01:	-	1	PASS
> 01: HBR- Initial Link Training successful			PASS
> 02: HBR- Check IRQ HPD pulse from Sink DUT			PASS
> 03: HBR- Verify behavior based on IRQ HPD pulse status			PASS
↳ 04: UHBR- Initial Link Training successful			PASS
◦ HPD is asserted			
◦ Value of DPCD F0000h is 0			
◦ Reference Source receives AUX_ACK at 1 attempts			
◦ Reference Source receives AUX ACK from either write request			
◦ Sink DUT Capability supports UHBR RATE = 13.50 Gbps and MAX_LANE_COUNT = 4			
◦ Link Training at lane count 4 and link rate 13.5 successful			
↳ 05: UHBR- Check IRQ HPD pulse from Sink DUT			PASS
◦ Sink DUT did NOT transmit an IRQ HPD pulse			
↳ 06: UHBR- Verify behavior based on IRQ HPD pulse status			PASS
◦ TEST_CRC_R_Cr field equals to the Reference Source's internal CRC calculations (0x0ABD).			
◦ TEST_CRC_G_Y field equals to the Reference Source's internal CRC calculations (0xB491).			
◦ TEST_CRC_B_Cb field equals to the Reference Source's internal CRC calculations (0xC636).			

HBR

UHBR

# Test 5.3.2.2: Sink IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock

[ACA-5_3_2_2_01] Events: 2254 (5295)						
750	DNAT	11	> R:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1		Start Time: +03:38:42.996160	
751	DNAT	11	< ACK 06		Type: Native	
752	DNAT	11			Direction: Reply	
753	DNAT	11			Command: ACK	
754	DPLT	11			Reply to Read Request.	
755	DPLT	11				
756	DNAT	11			00246: TEST_SINK_MISC	
757	DNAT	11			Bit Name	Value Description
758	DNAT	11			3-0 TEST_CRC_COUNT	0 Reserved
759	DNAT	11				
760	DNAT	11				
761	DNAT	11				
762	DNAT	11				
763	DNAT	11				
764	DNAT	11				
765	DNAT	11				
766	DPLT	11				
767	DPLT	11				
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999	DNAT	11				

## UHBR Loop

- Tester Link Trains to highest supported rate (13.5Gb/s) at lane count: 4
- Tester adds inter-lane skew
  - (64-bit skew delay for lanes 1,2, and 3, with respect to lane 0)
- Verify if DUT transmits an IRQ HPD pulse
  - If no IRQ HPD:
  - Verify Sink DUT maintains Interlane alignment:
    - TEST\_CRC\_R\_Cr field
    - TEST\_CRC\_G\_Y field
    - TEST\_CRC\_B\_Cb field

# DP Tunnel Compliance



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# USB4 DP Tunneling

## USB4 DP Tunneling tests



From the USB4 DP Tunneling CTS

### DP CTS Link Layer Tests

Below is the meaning of the tests classifications:

- Yes – The test is required to run as part of the Compliance certification.
- Skipped – The test is not required to run as part of the Compliance certification, but there should not be any technical barrier to execute it over DP Tunneling setup.
- NA – The test can not be executed over DP Tunneling

### Source Testing Tables

- For DP IN Adapter UUT:
  - If the DP TX can be tested in a manner other than DP Tunneling, then the full Source Testing according to VESA CTS shall be used in the alternative manner and the test to run as part of DP Tunneling CTS are the tests which states 'Yes' in the "DP Tunneling Subset" column, otherwise the tests to run are the tests which states 'Yes' in the "DP Tunneling Only".

- For DP OUT Adapter UUT:
  - The test to run as part of DP Tunneling CTS are the tests which states 'Yes' in the "DP OUT Adapter UUT" column.

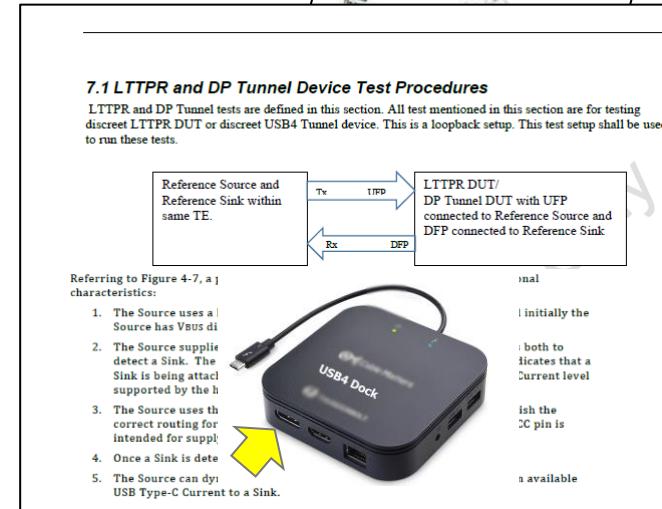
Table 5 – DP CTS Source Device Services Test Procedures

DP CTS Test Number	Test Name	DP Tunneling Subset	DP Tunneling Only	DP OUT Adapter UUT
4.2.1 AUX Reads after HPD Plug Event				
4.2.1.1	Source DUT Retry on No-Reply During AUX Read after HPD Plug Event	Yes	Yes	Yes
4.2.1.2	Source Retry on Invalid Reply During AUX Read after HPD Plug Event	Skipped	Yes	Yes

These are all M42d link layer tests

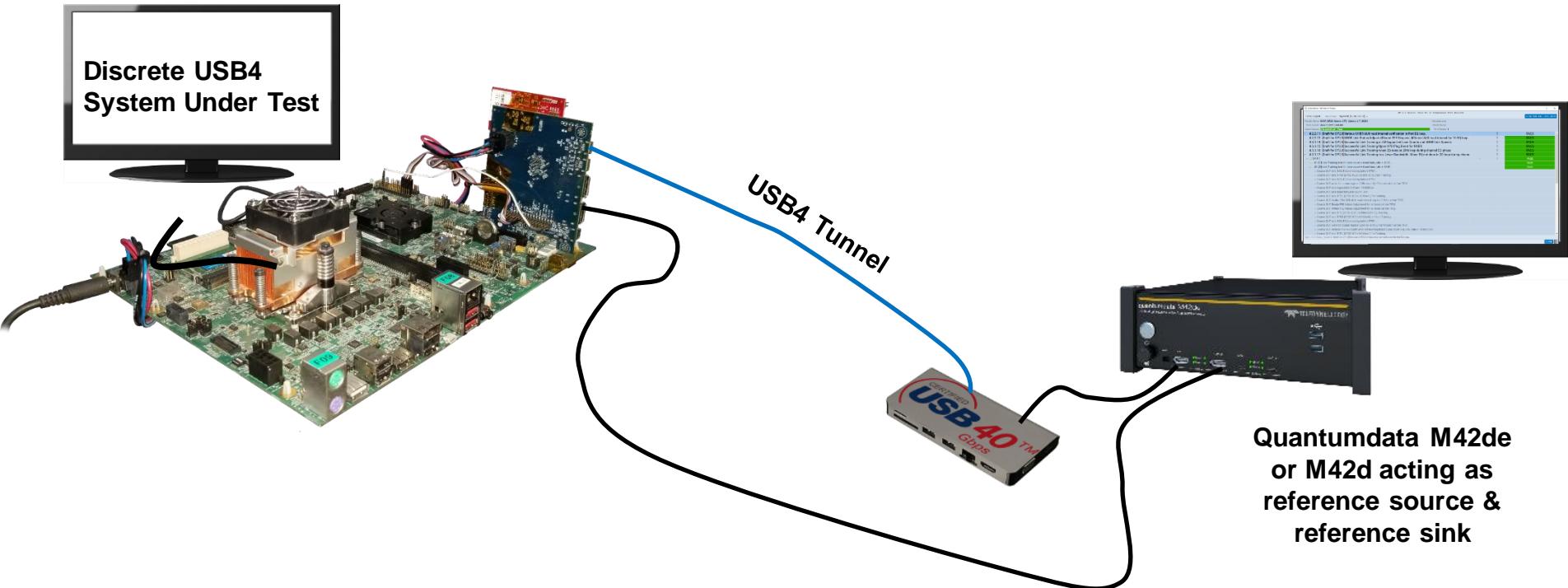
## VESA DP Tunneling tests

From the LTTPR & Tunneling CTS



# VESA DP Tunneling tests

Testing the DP tunnel behaviors



# DP 2.1 Compliance Testing: Do's and Dont's

- Dont's
  - Don't submit CDF with Errors
  - Don't skip the automation support
  - Don't use non-VESA approved components
- Do's
  - Always pre-test before submitting for certification
  - Always run the latest M42de beta release
  - Reduce test time with Parallel strategies



# Webinars-on-Demand

Check out these other detailed DisplayPort Webinars-on-Demand:

- ◆ [Essentials of DisplayPort 2.0 Link Layer Protocols & LTTPR Devices](#)
- ◆ [Essentials of HDCP 2.2 Protocols](#)
- ◆ [Essentials of DisplayPort Display Stream Compression \(DSC\) Protocols](#)
- ◆ [Essentials of DisplayPort Link Layer Compliance Testing](#)
- ◆ [Essentials of DisplayPort Forward Error Correction \(FEC\)](#)
- ◆ [Essentials of DisplayPort USB-C DP Alt Mode Protocols](#)
- ◆ [Essentials of DisplayPort 2.0 Protocols](#)

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- Questions

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# Thank You

# 谢谢