

Essentials of DisplayPort 2.0 Link Layer Protocols with LTTPR Device Testing

Featuring the M42d 80G Video Analyzer/Generator for DisplayPort 2.0 Testing

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Webinar – November – 2021



*M42d...A complete solution
for DisplayPort 2.0 testing*



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About the Presenter



Neal Kendall
Product Marketing Manager
Teledyne LeCroy -
quantumdata Product Family

Product Marketing Manager Teledyne LeCroy for the quantumdata family of products. Nearly eighteen (18) years in the Video Protocols industry.

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Agenda

- ◆ DisplayPort 2.0 Brief Overview.
- ◆ DisplayPort 2.0 Main Link Layer Frame Structure.
- ◆ DisplayPort Link Layer Training Operation with LTTPR at 128b/132b at UHBR rates.
- ◆ MST Configuration.

DisplayPort 2.0 – Brief Overview

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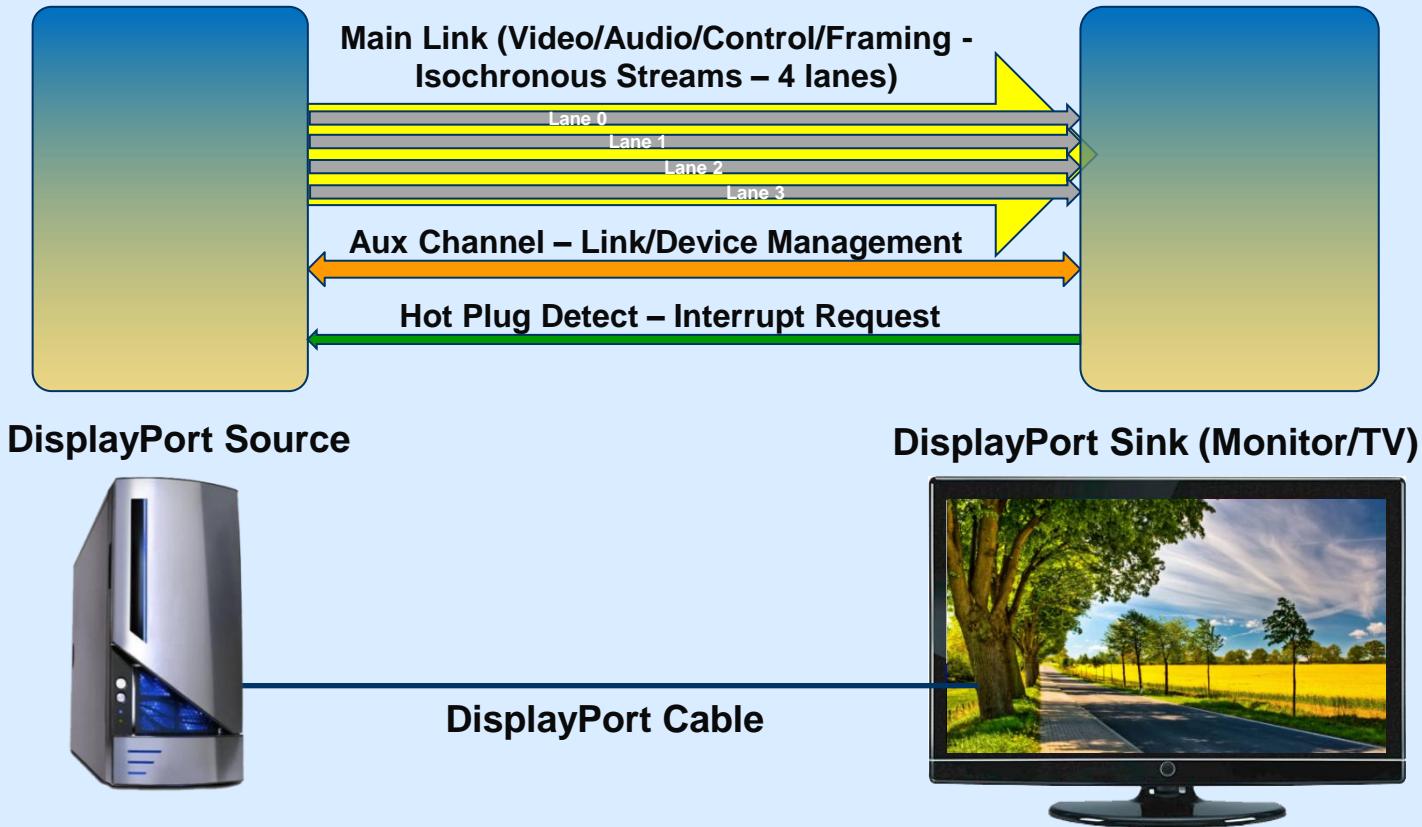
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M42d 80G Video Analyzer/ Generator



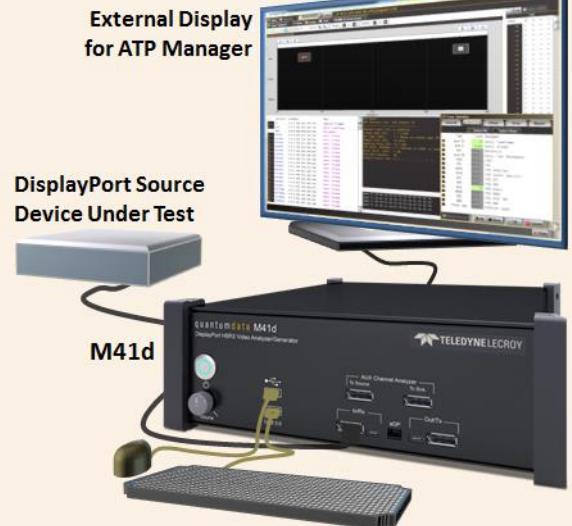
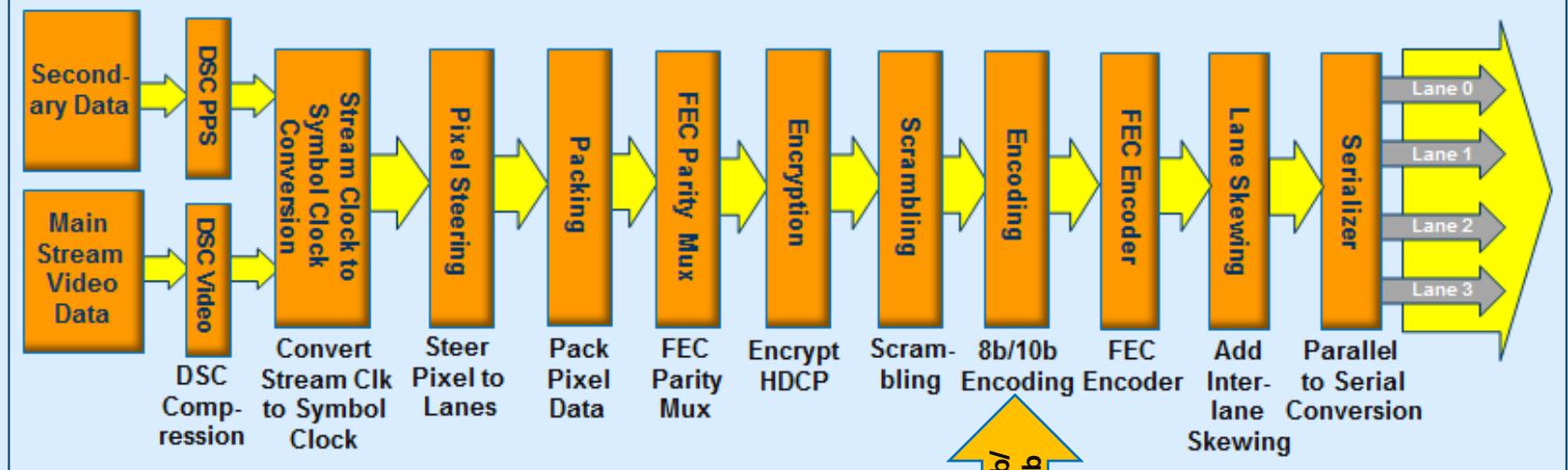
DisplayPort Anatomy – DisplayPort 2.0 Updates



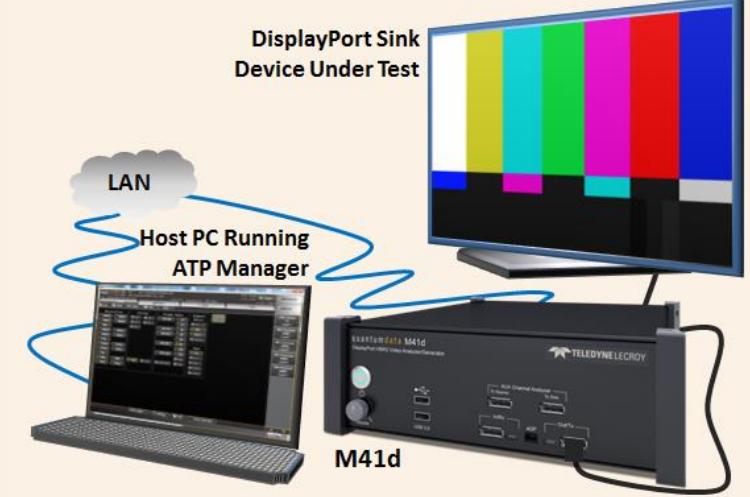
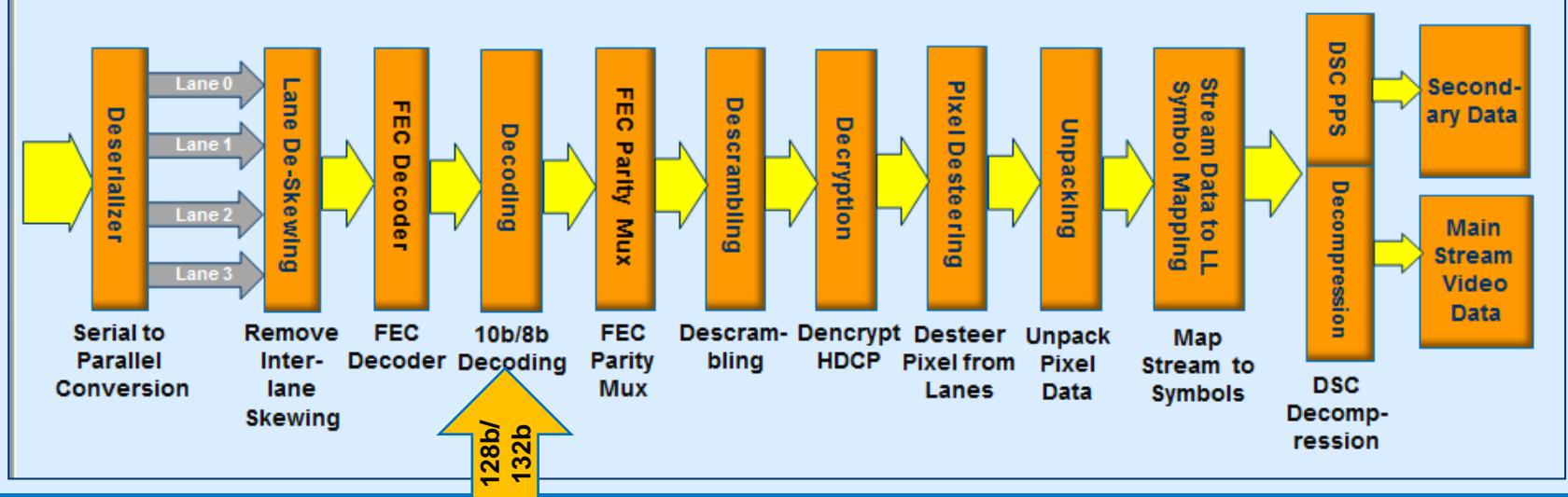
- ◆ Main Link: Unidirectional, high-bandwidth channel used to transport video, audio, metadata and protocol control elements.
- ◆ Main Link 1, 2 or 4 Lane Configurations.
- ◆ **New Line Coding: 128b/132b.**
- ◆ **New symbol size - Thirty-Two (32) bit.**
- ◆ **Multi-Stream Transport (MST) is now standard protocol.**
- ◆ **New Main Link rates:**
 - ◆ **10.0 Gbps** (DP or USB-C cable)
 - ◆ **13.5 Gbps** (USB-C cable [captive on sink])
 - ◆ **20.0 Gbps** (USB-C cable [captive on sink])
- ◆ No clock channel. Sink recovers clock using link transitions.
- ◆ Aux Channel: Bidirectional, half duplex channel at 1Mbps. Link Training, DSC and FEC Configuration, DPCD Register status, HDCP authentication & EDID exchange.
- ◆ Hot plug.

DisplayPort Main Link Functional Blocks

DisplayPort Transmitter Block



DisplayPort Receiver Block



DisplayPort Main Link Protocol – One Video Frame



- Video packets occur during the active video period.
- Metadata: Main Stream Attributes (MSA) and Secondary Data Packets (SDP) occur during the vertical blanking period and are identified with Framing control characters.
- Fill characters used to stuff the unused link symbols.
- DSC slices used to partition video frame.

Video	Fill Characters
Metadata MSA, IF	Control Symbols
Audio (SDP)	Control VBID w/ Compression Flag Set
PPS	EoC

Overview of DisplayPort 2.0 Protocols Main Stream Protocols

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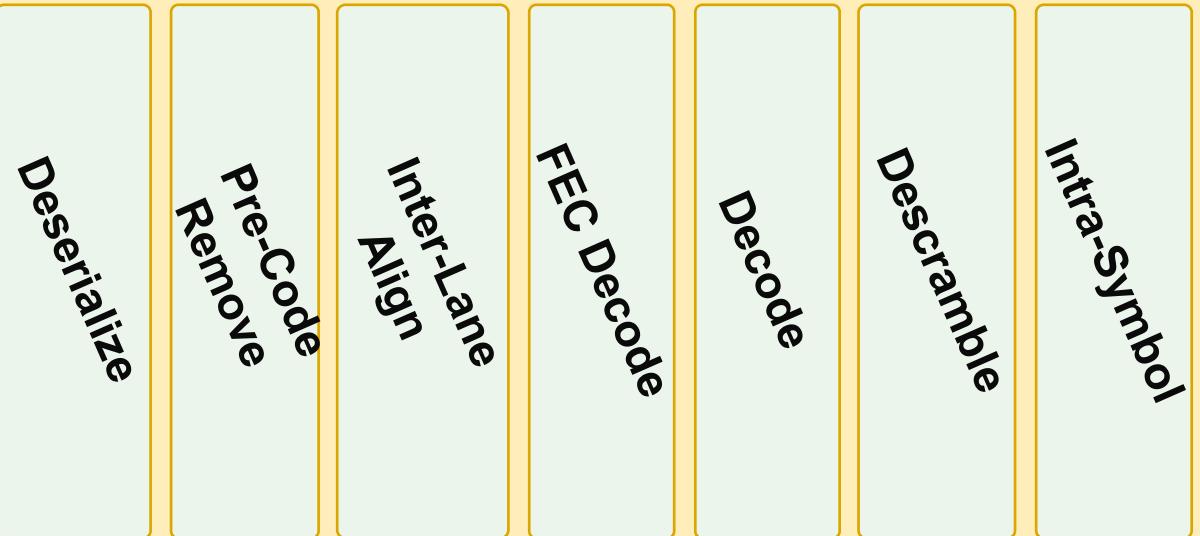
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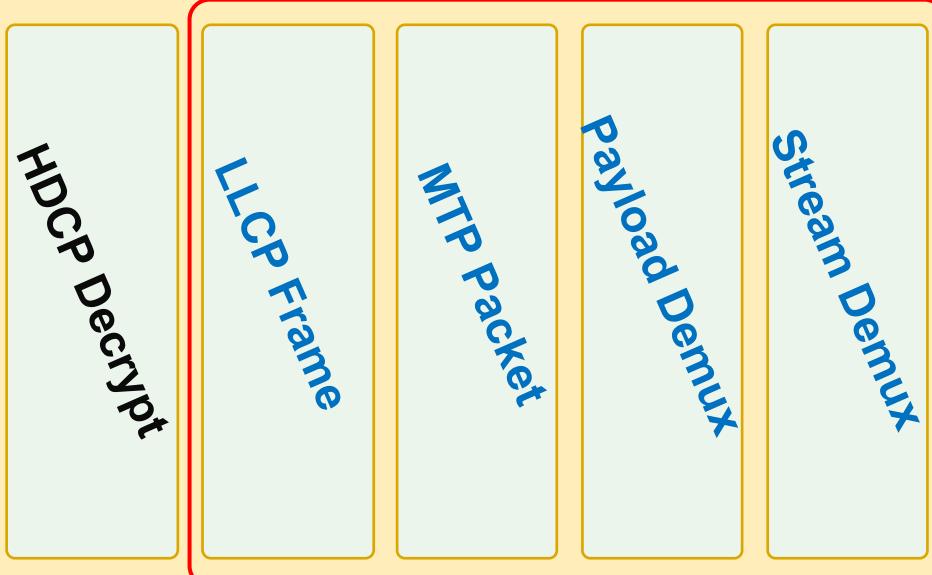
DisplayPort 2.0 Receiver Functional Blocks

Phy Elec
Layer

Phy Logical Layer Functional Blocks

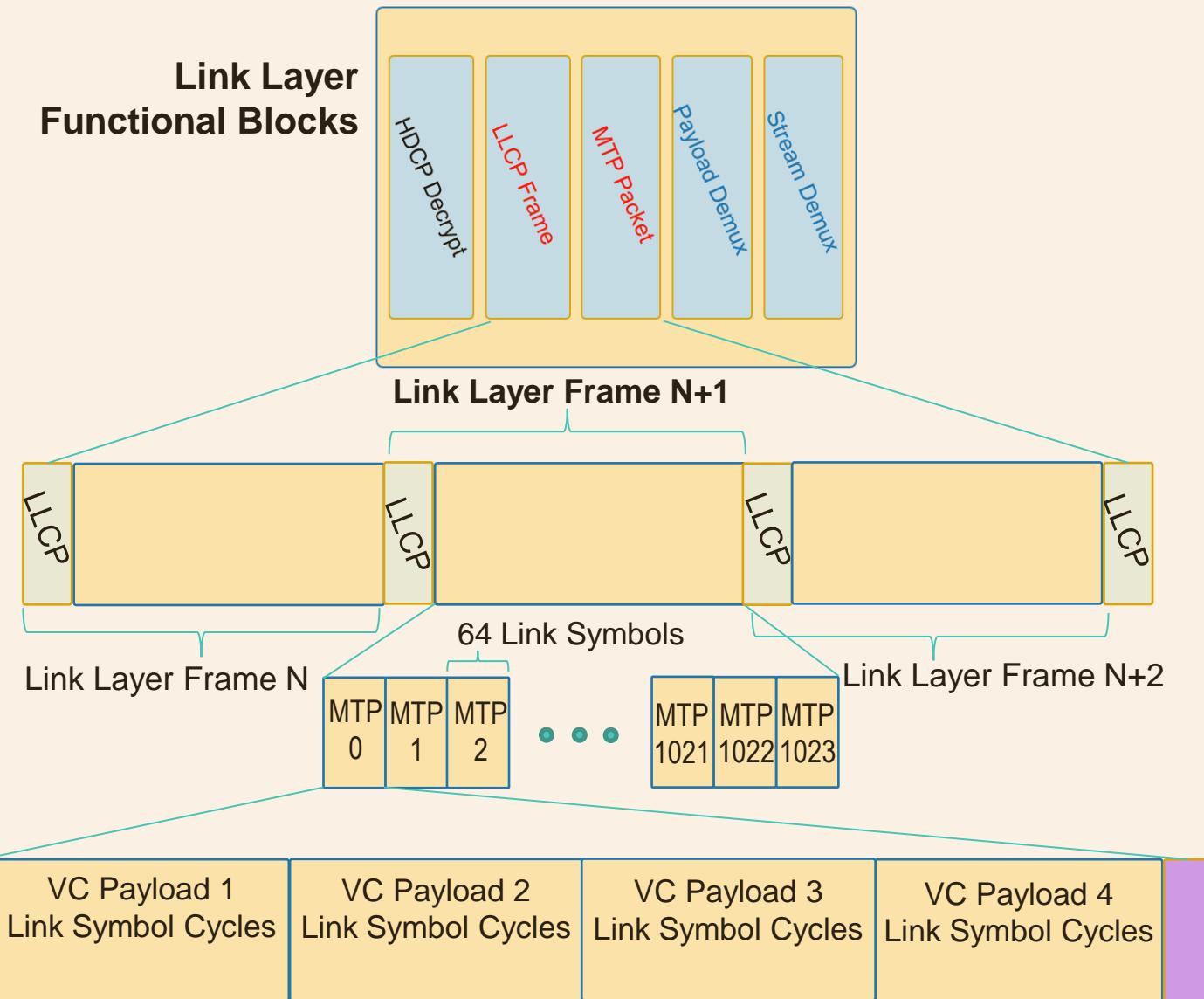


Link Layer Functional Blocks



Protocol Capture

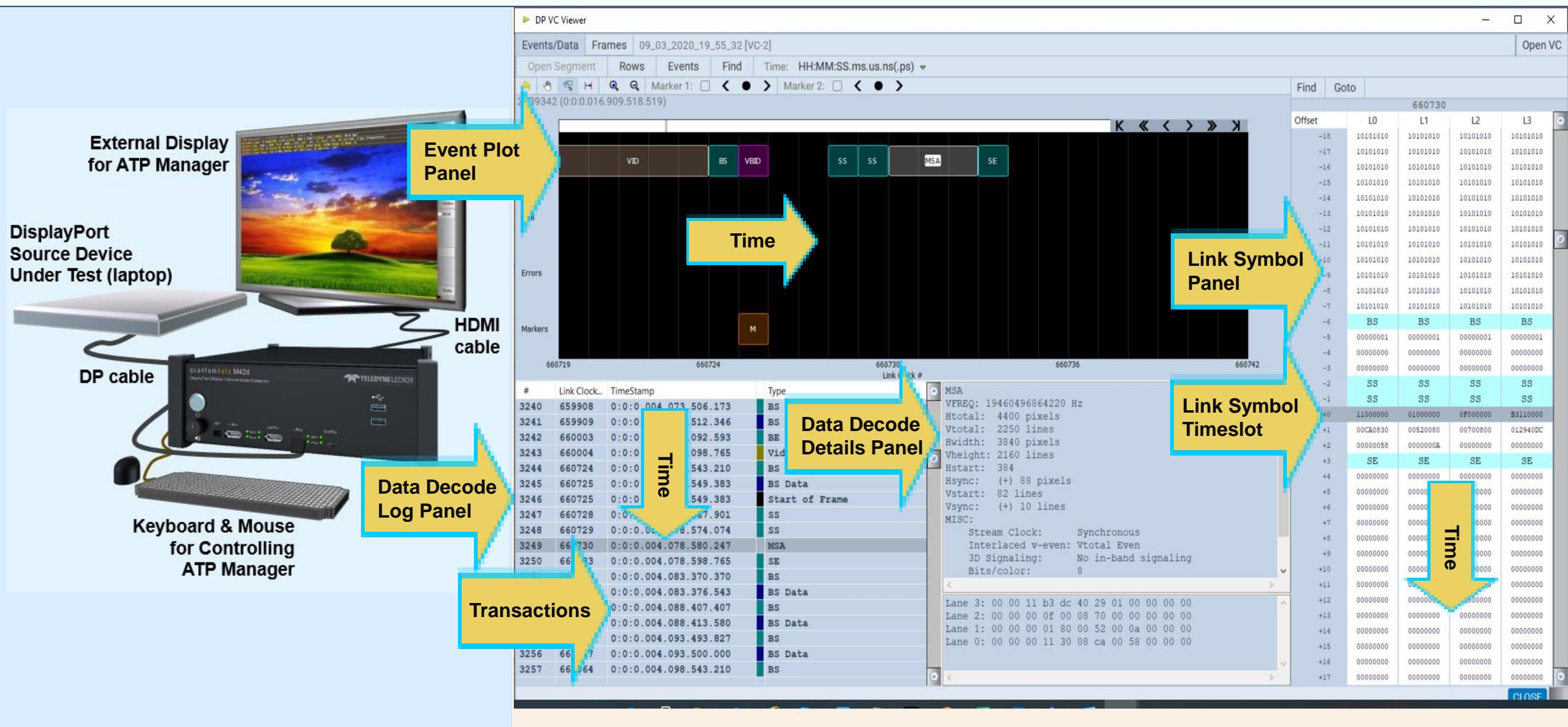
DisplayPort 2.0 Receiver Link Layer Functional Blocks



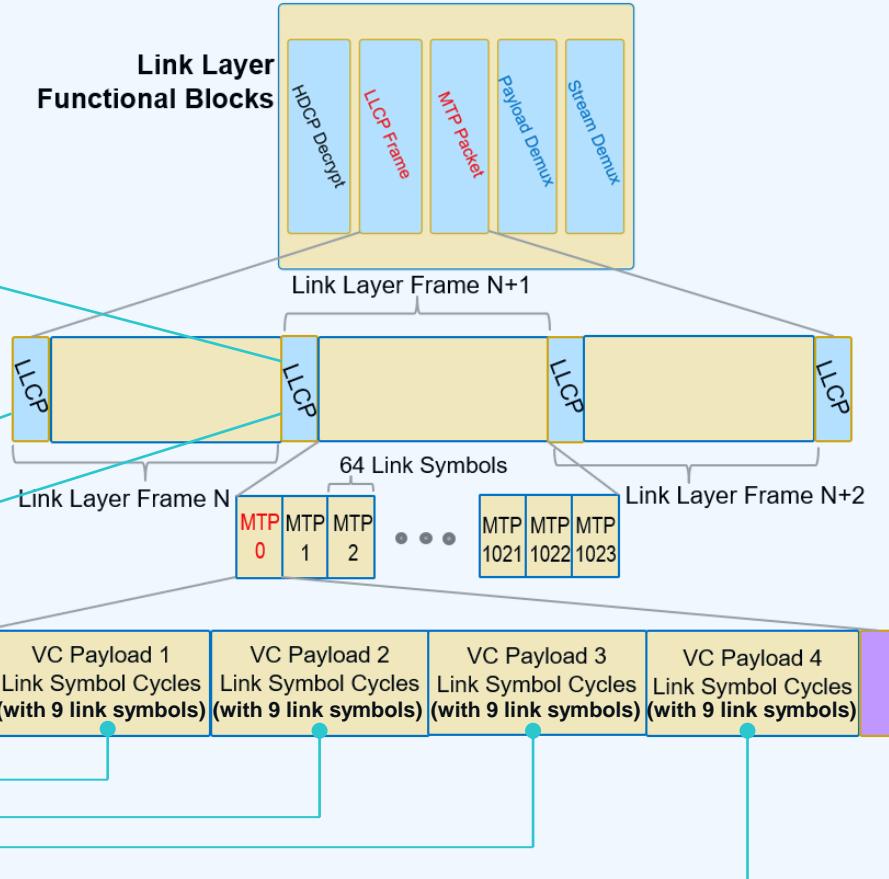
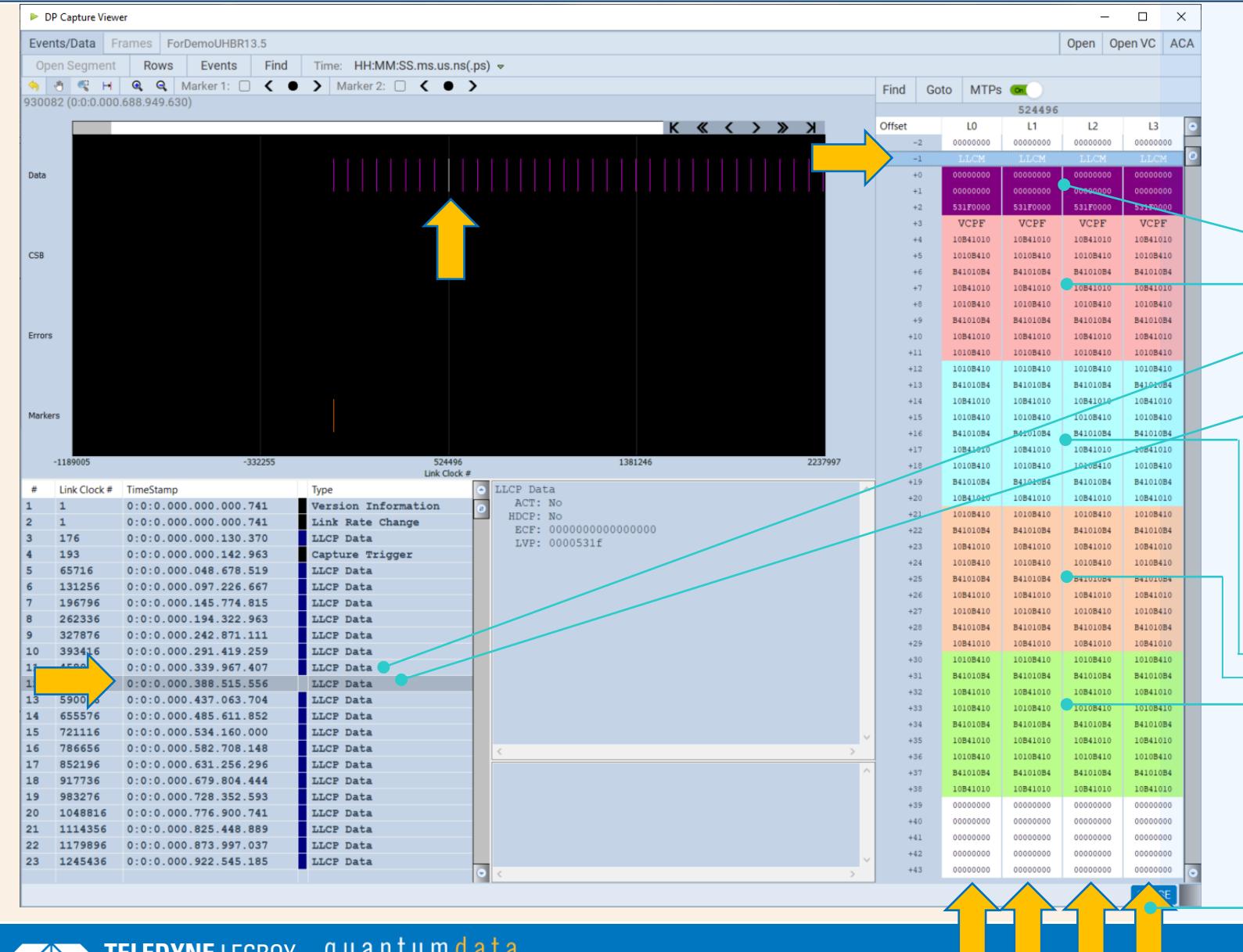
- ◆ **Link Layer Protocol**
 - ◆ Link Layer Frame consists of 1024 Multi-Stream Transport Packets (MTPs).
 - ◆ MTPs consist of 64 link symbols.
 - ◆ Link symbols consist of 32-bits.
- ◆ **Two types of link symbols:**
 - ◆ Control Symbols – K-Characters such as: Blanking Start (BS), Blanking End (BE), Secondary Data Start (SS), Secondary Data End (SE), End of Chunk (EoC), Stream Fill (SF), Link Layer Control Packet Marker (LLCP-M), Virtual Channel Payload Fill (VCPF).
 - ◆ Data Link Symbols – Primarily Pixel data, LLCP bytes 1-3, Secondary Data packets, VB-ID packets.

Note: All symbols in a particular link symbol timeslot are the same type of link symbol (Control or Data Link) across all lanes.

M42d Main Link Capture Analyzer Panel

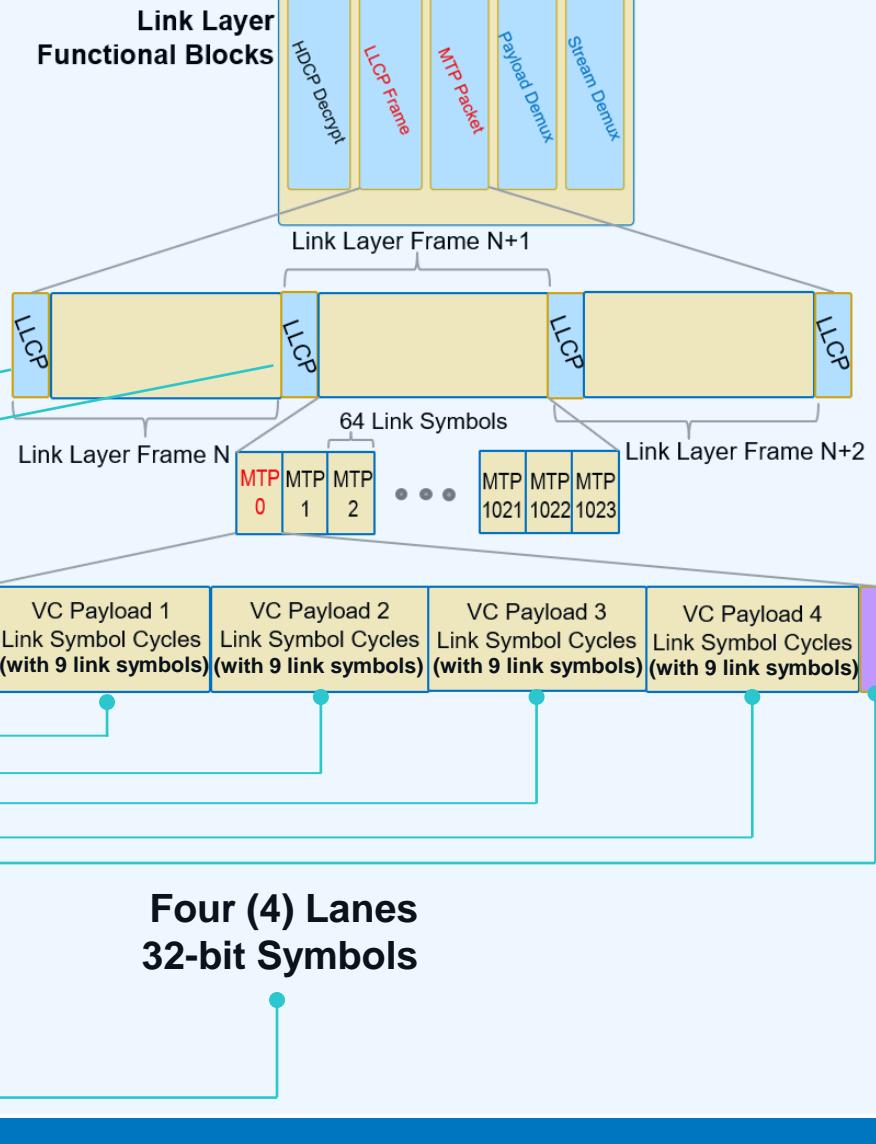
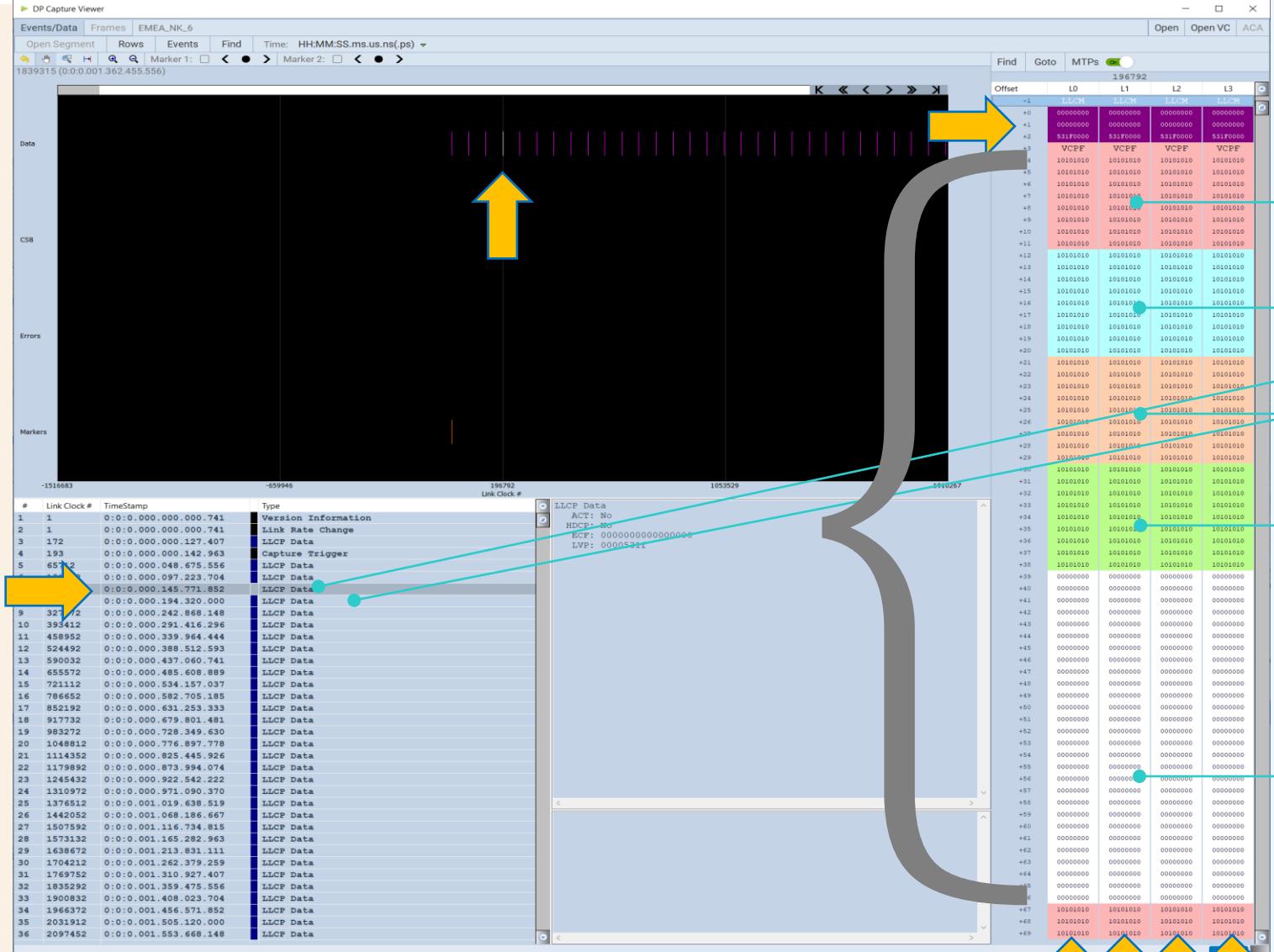


Main Link Protocols – Viewed through M42d Protocol Analyzer

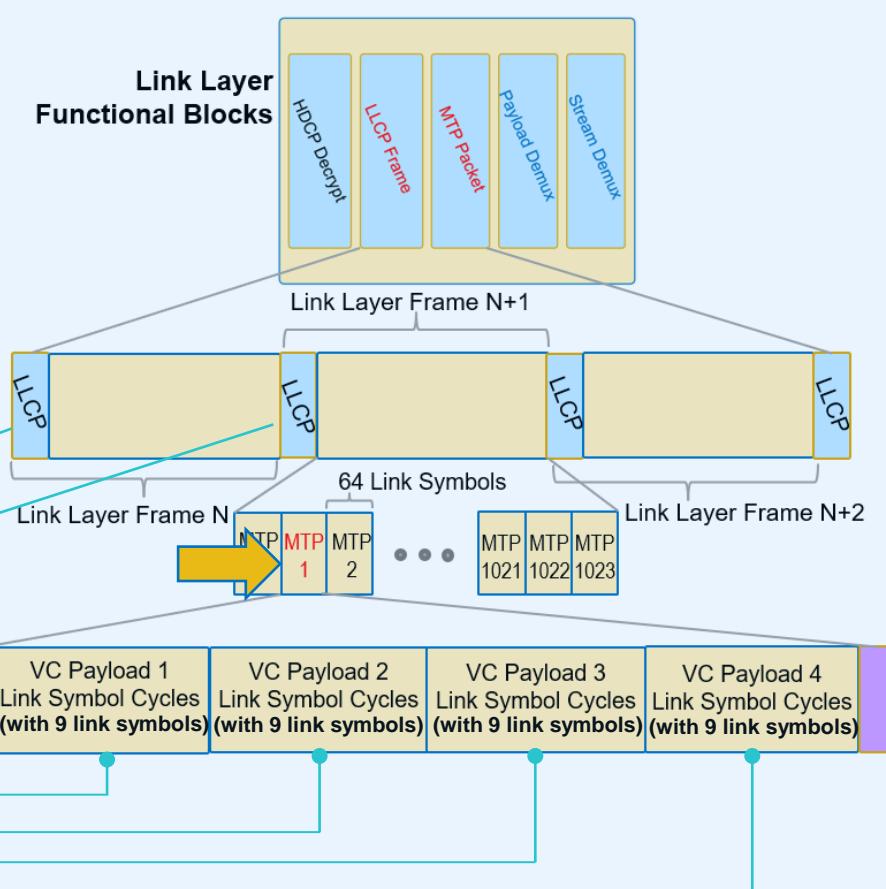
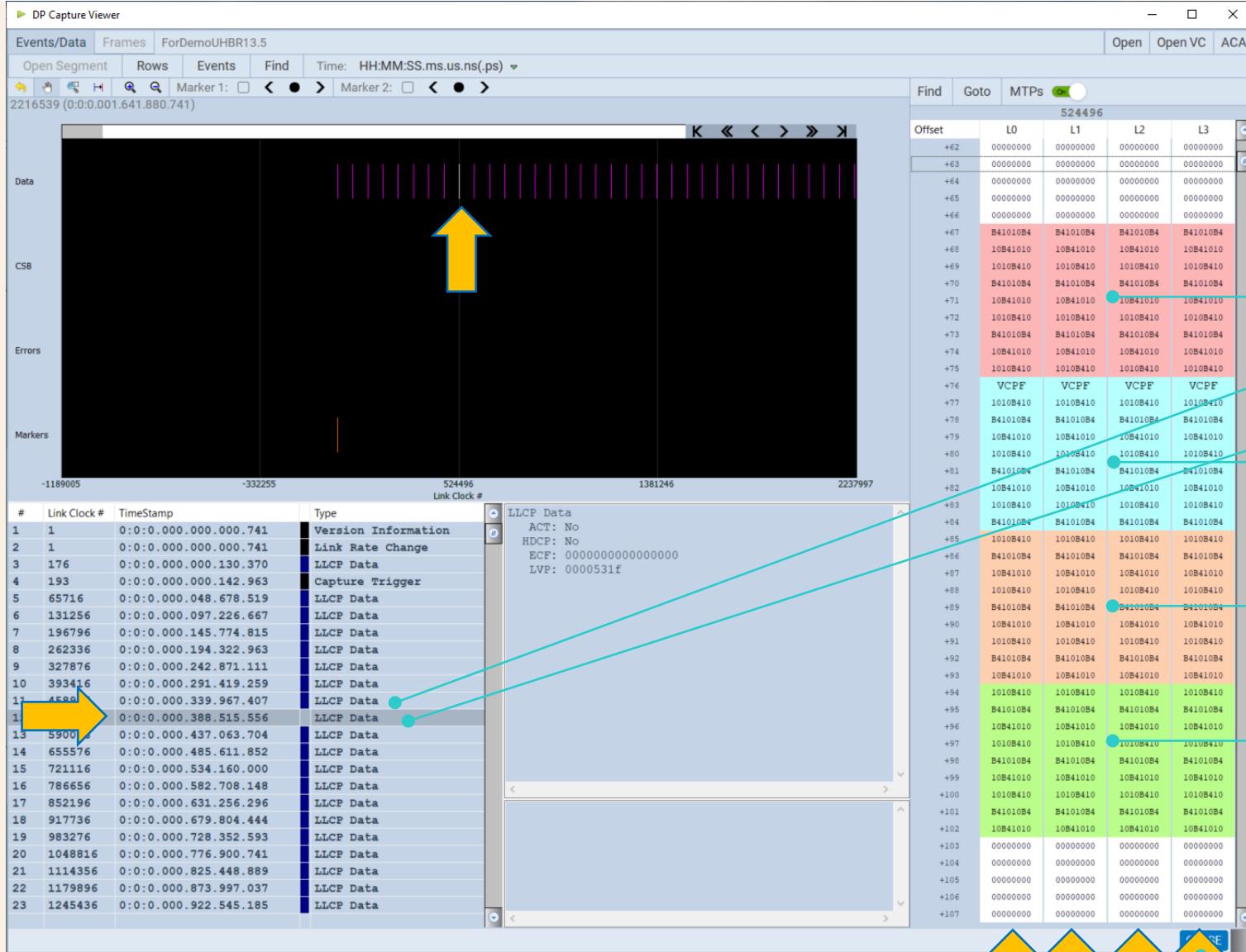


Four (4) Lanes 32-bit Symbols

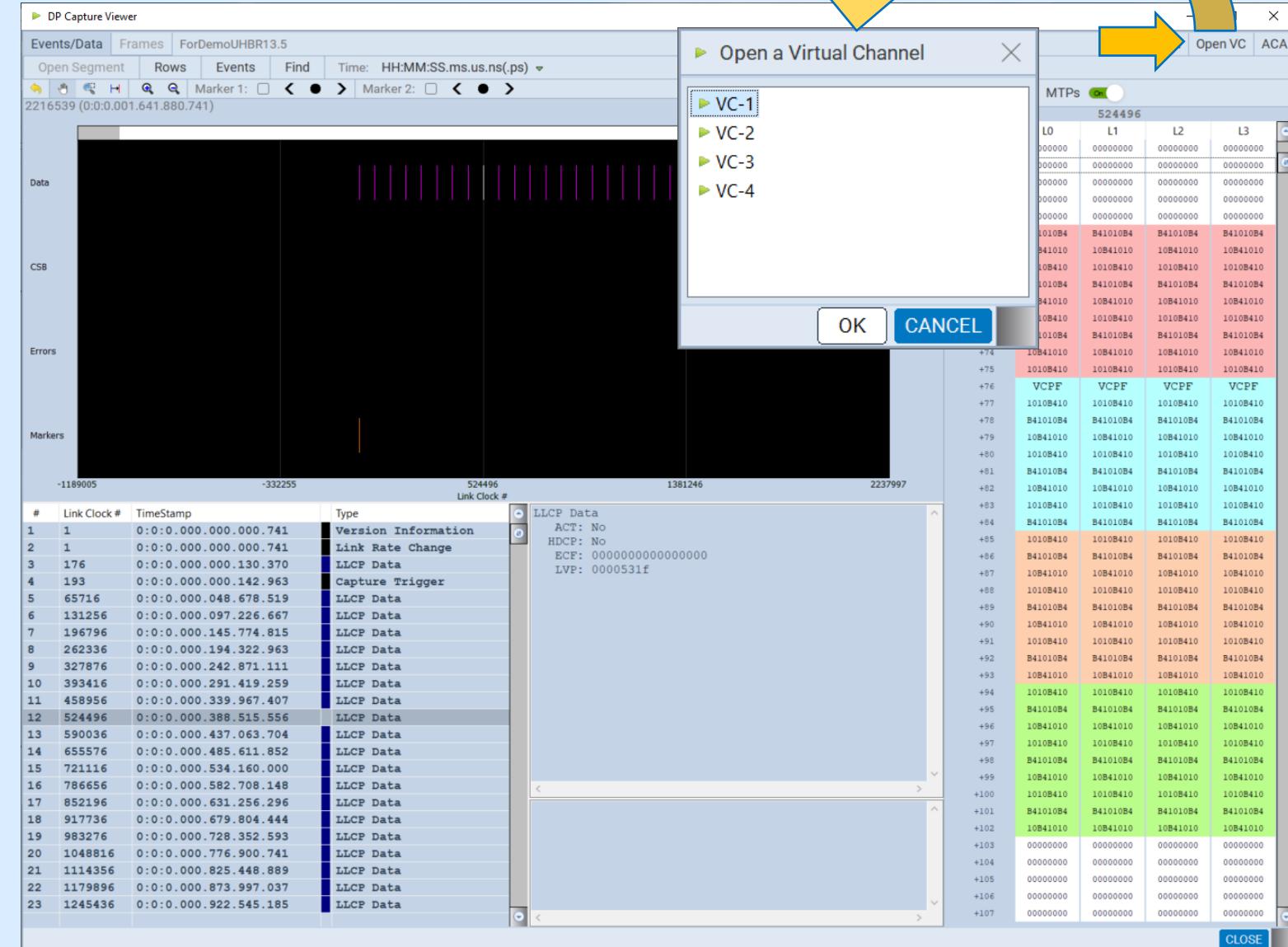
Main Link Protocols



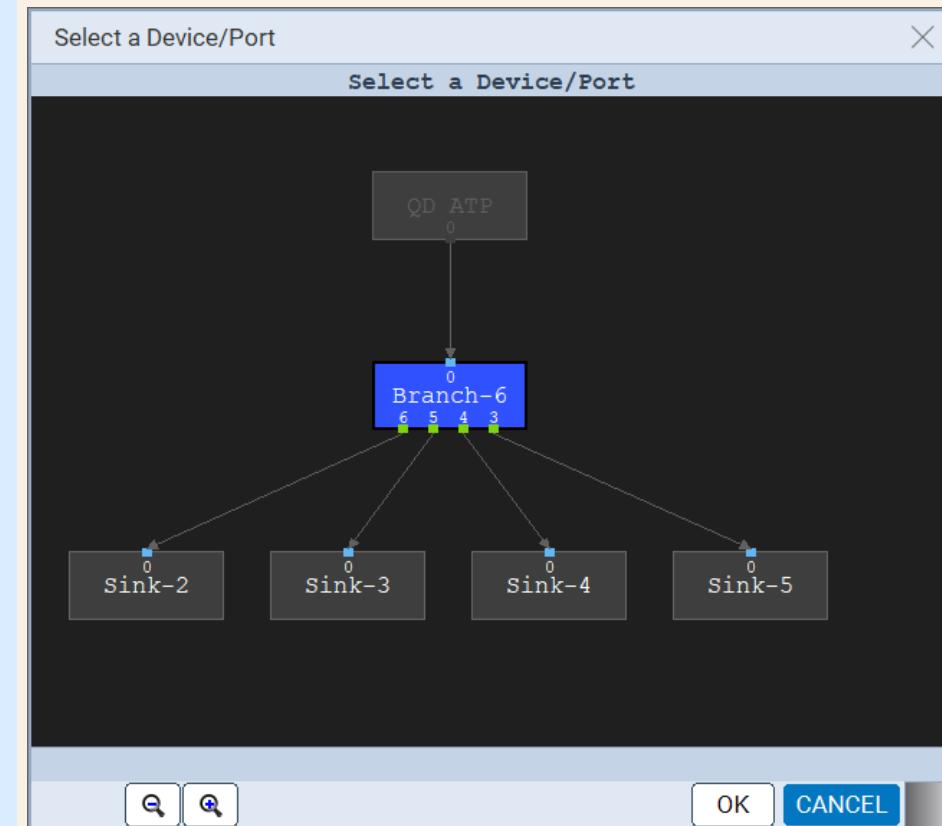
Main Link Protocols



Main Link Protocols – Link to Virtual Channel Capture



- ◆ View Captures
 - ◆ Source to Branch.
 - ◆ Branch to Sink.



Main Link Protocols – Virtual Channel Protocol Capture View

DP VC Viewer

Events/Data Frames ForDemoUHBR13.5 [VC-1] (arrow)

Open Segment Rows Events Find Time: HH:MM:SS.ms.us.ns(.ps) Open VC

Marker 1: < ● > Marker 2: < ● >

1360889 (0:0:0.008.400.549.383)

Data CSB Errors Markers

980630 1096126 1211622 1327118 1442614

Link Clock #

#	Link Clock...	TimeStamp	Type
5947	1210805	0:0:0.007.474.104.938	BS Data
5948	1210895	0:0:0.007.474.660.494	BE
5949	1210896	0:0:0.007.474.666.667	Video Data
5950	1211616	0:0:0.007.479.111.111	BS
5951	1211617	0:0:0.007.479.117.284	BS Data
5952	1211617	0:0:0.007.479.117.284	Start of Frame
5953	1211620	0:0:0.007.479.135.802	SS
5954	1211621	0:0:0.007.479.141.975	SS
5955	1211622	0:0:0.007.479.148.148	MSA
5956	1211625	0:0:0.007.479.166.667	SE
5957	1212394	0:0:0.007.483.913.580	BS
5958	1212395	0:0:0.007.483.919.753	BS Data
5959	1213214	0:0:0.007.488.975.309	BS
5960	1213215	0:0:0.007.488.981.481	BS Data
5961	1214030	0:0:0.007.494.012.346	BS
5962	1214031	0:0:0.007.494.018.519	BS Data
5963	1214856	0:0:0.007.499.111.111	BS

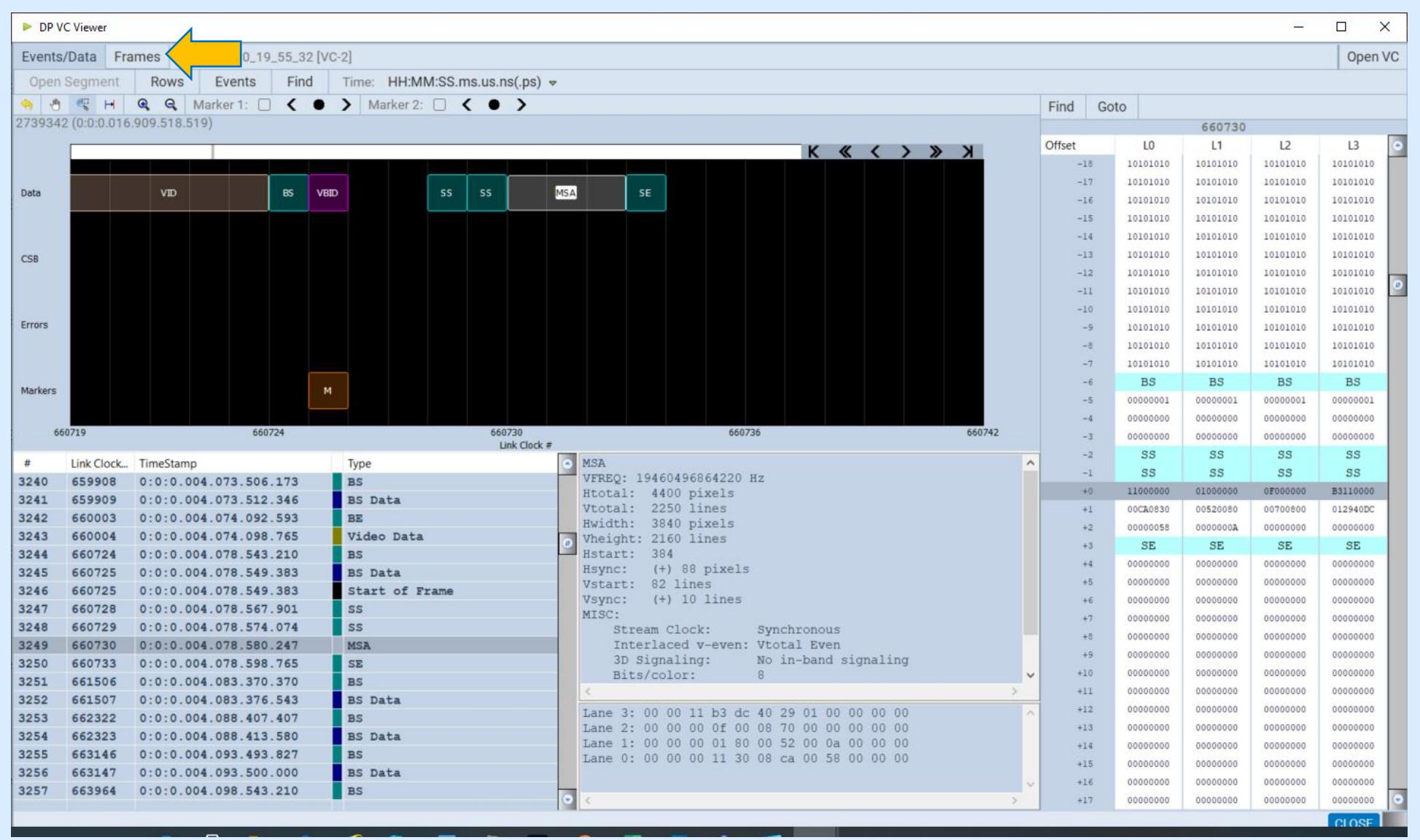
Find Goto 1211622

Offset	L0	L1	L2	L3
-16	10101010	10101010	10101010	10101010
-15	10101010	10101010	10101010	10101010
-14	10101010	10101010	10101010	10101010
-13	10101010	10101010	10101010	10101010
-12	10101010	10101010	10101010	10101010
-11	10101010	10101010	10101010	10101010
-10	10101010	10101010	10101010	10101010
-9	10101010	10101010	10101010	10101010
-8	10101010	10101010	10101010	10101010
-7	10101010	10101010	10101010	10101010
-6	BS	BS	BS	BS
-5	00000001	00000001	00000001	00000001
-4	00000000	00000000	00000000	00000000
-3	00000000	00000000	00000000	00000000
-2	SS	SS	SS	SS
-1	SS	SS	SS	SS
+0	11000000	01000000	0F000000	B3110000
+1	00CA0830	00520080	00700800	012940DC
+2	00000058	0000000A	00000000	00000000
+3	SE	SE	SE	SE
+4	00000000	00000000	00000000	00000000
+5	00000000	00000000	00000000	00000000
+6	00000000	00000000	00000000	00000000
+7	00000000	00000000	00000000	00000000
+8	00000000	00000000	00000000	00000000
+9	00000000	00000000	00000000	00000000
+10	00000000	00000000	00000000	00000000
+11	00000000	00000000	00000000	00000000
+12	00000000	00000000	00000000	00000000
+13	00000000	00000000	00000000	00000000
+14	00000000	00000000	00000000	00000000
+15	00000000	00000000	00000000	00000000
+16	00000000	00000000	00000000	00000000

CLOSE

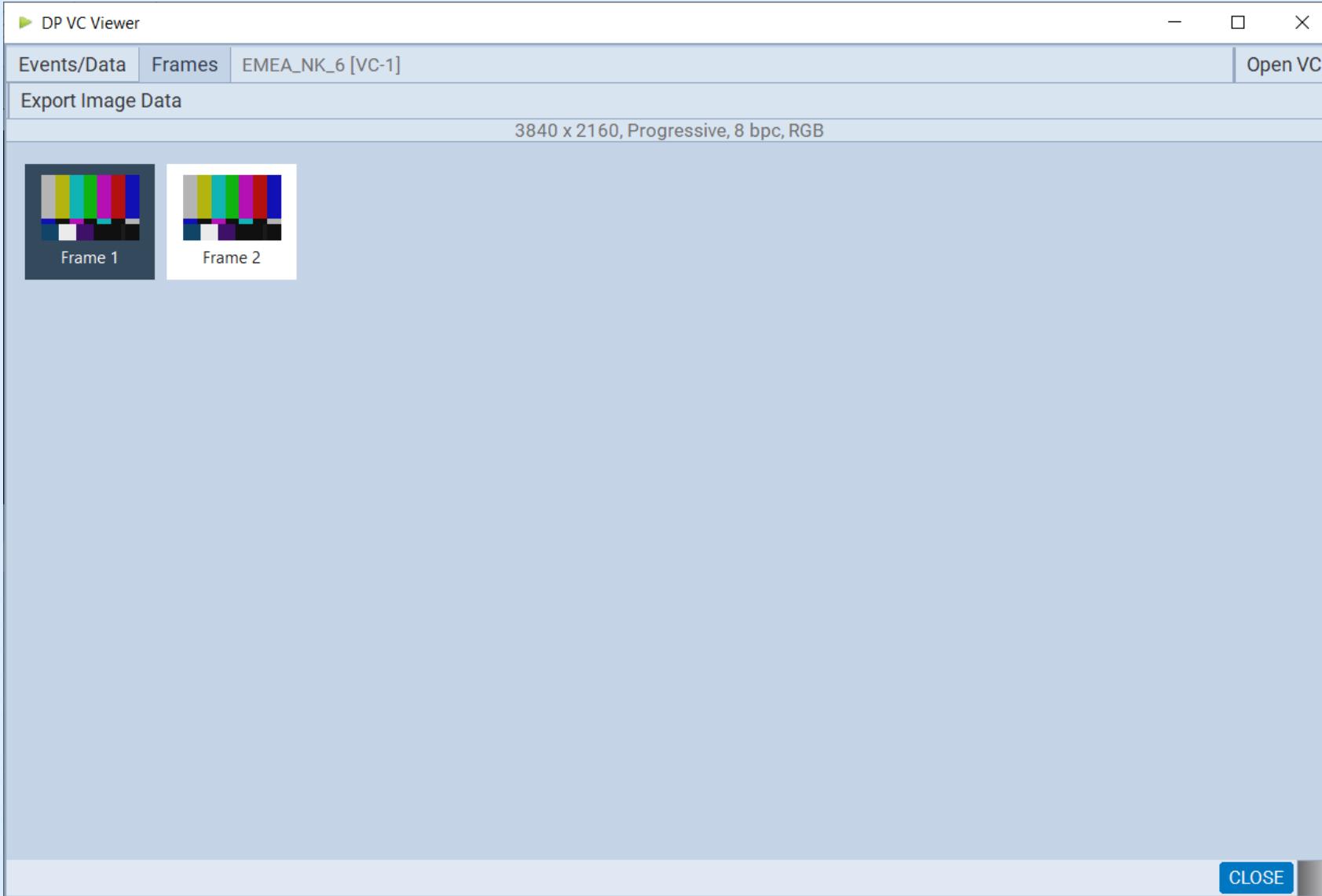
- ◆ View Virtual Channel Capture
 - ◆ Main Stream Attribute (MSA) Packet.

Main Link Protocols – Virtual Channel Protocol Capture View



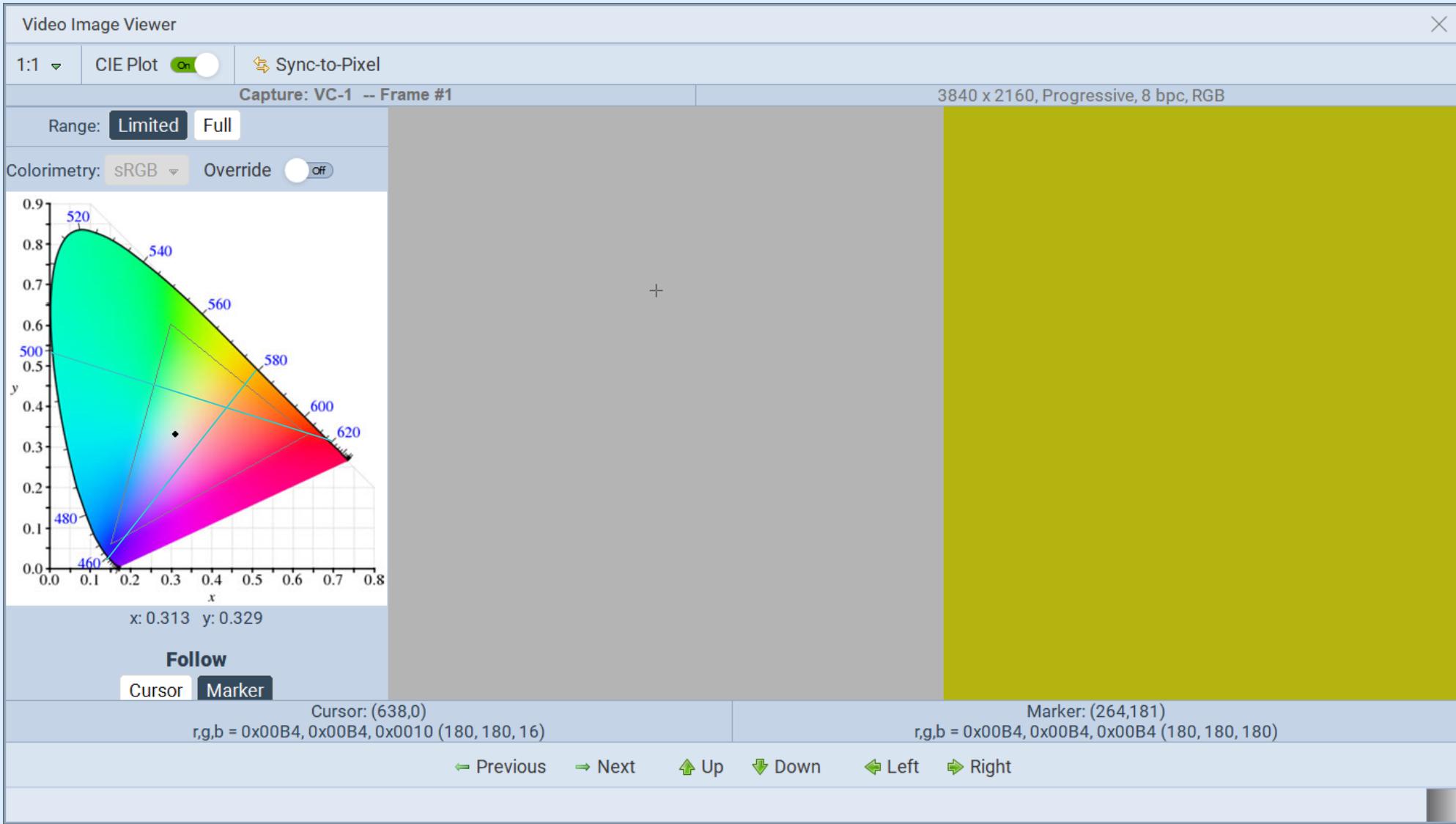
◆ Access the capture video frames.

Main Link Protocols – Video Frames (Thumbnails)



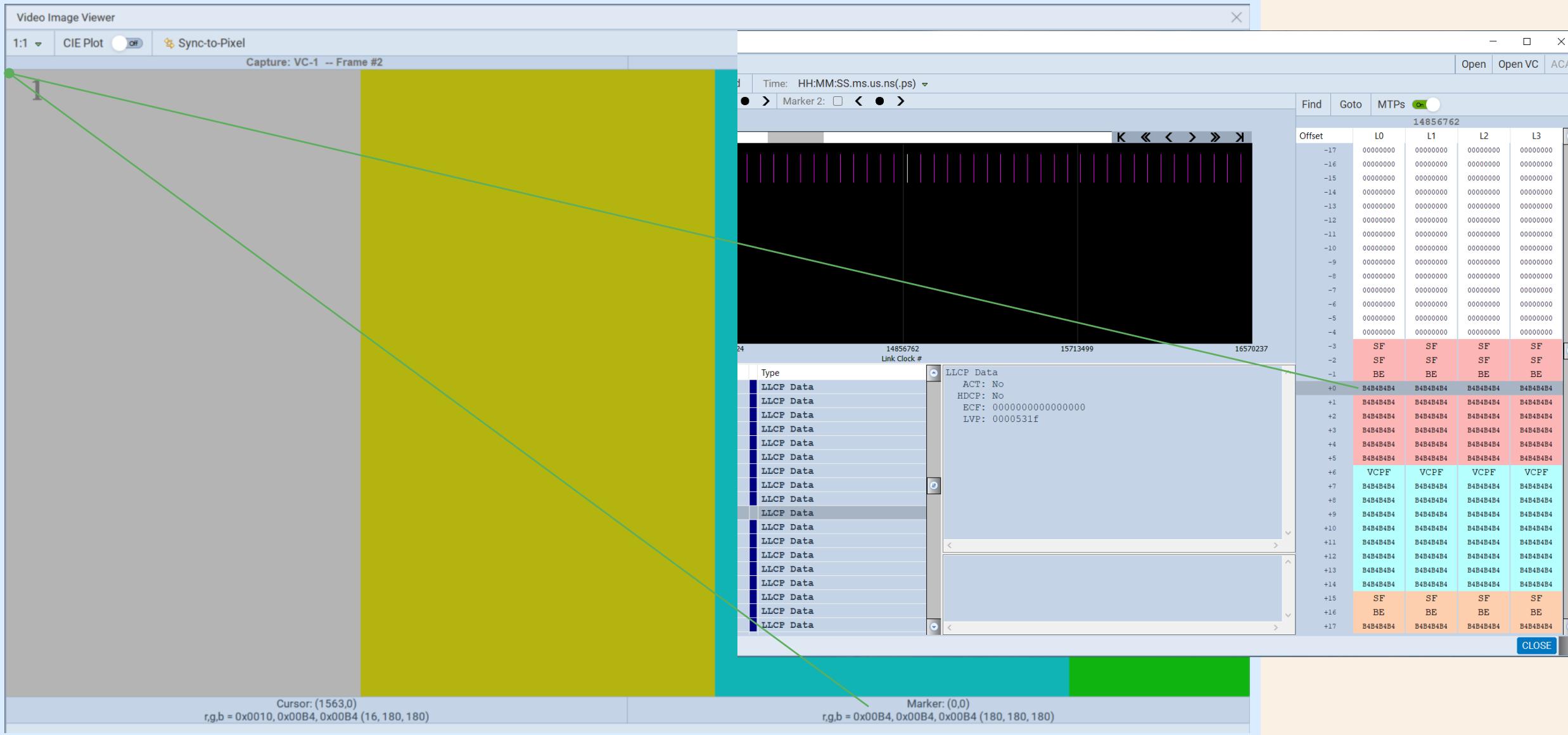
- ◆ View any of the captured frames (example shows only two frames).

Main Link Protocols – Video Frame

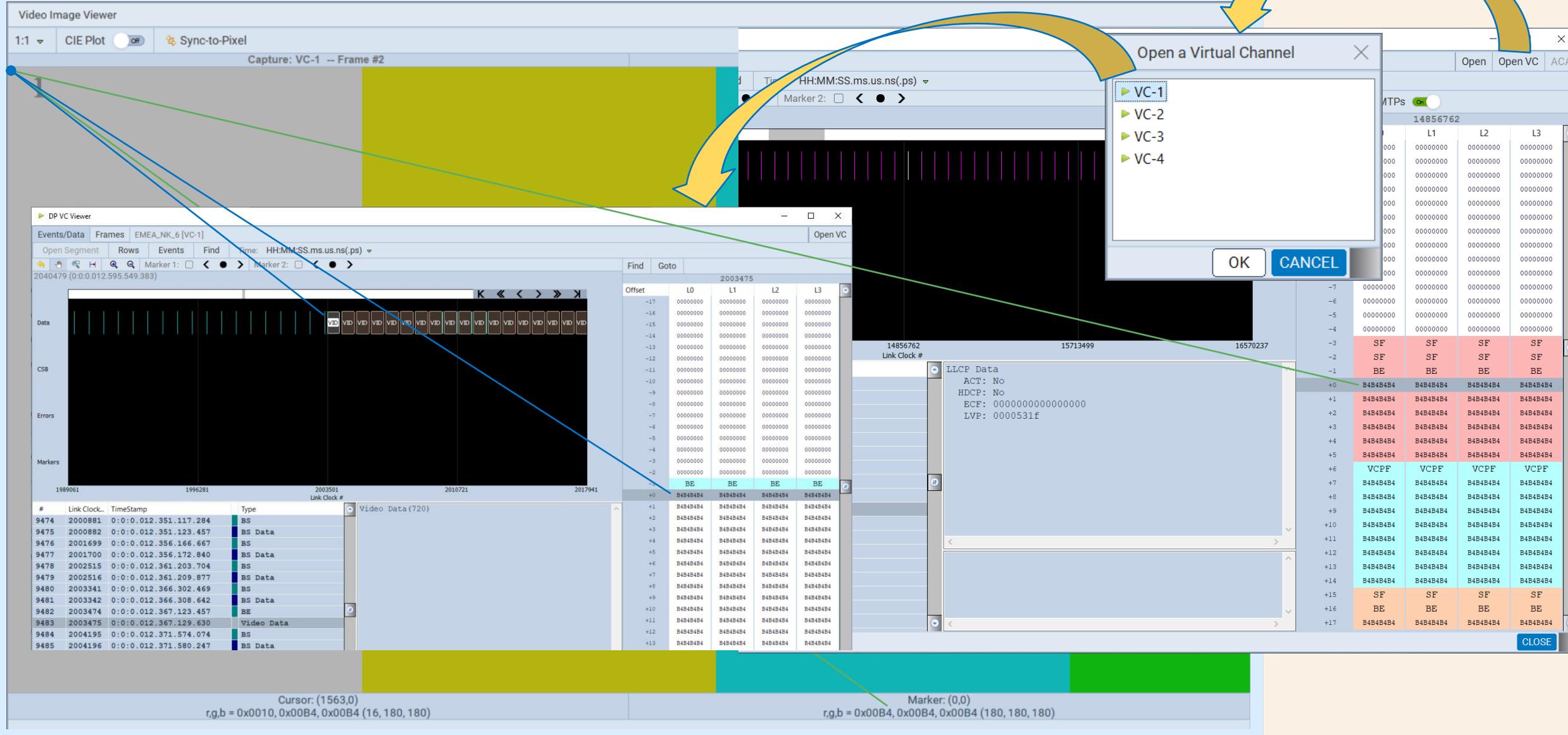


- ◆ View the pixel data values on the CIE color chart for any Colorimetry.
- ◆ Example shows BT.709.

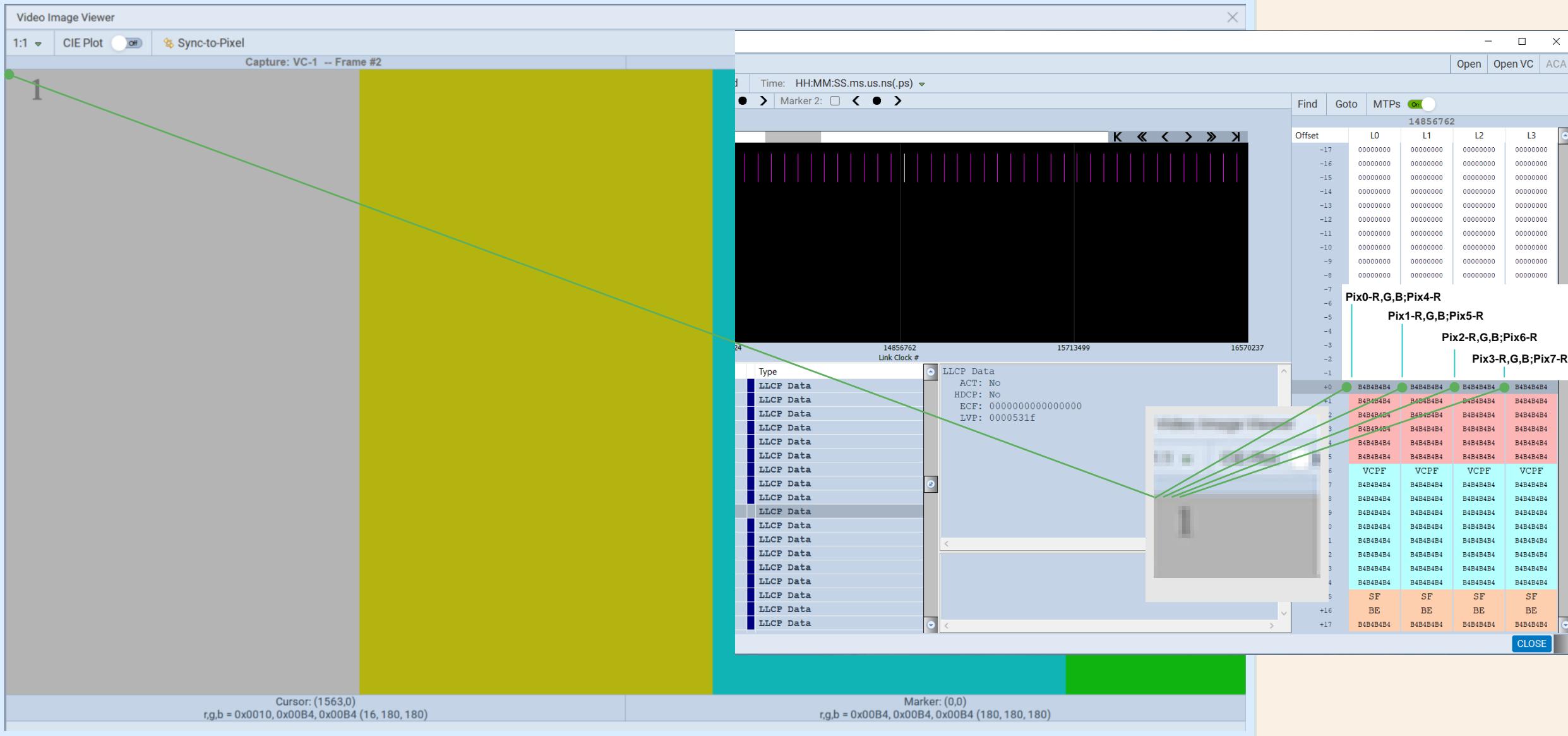
Main Link Protocols – Video Pixel Data to Link Data Symbol Mapping



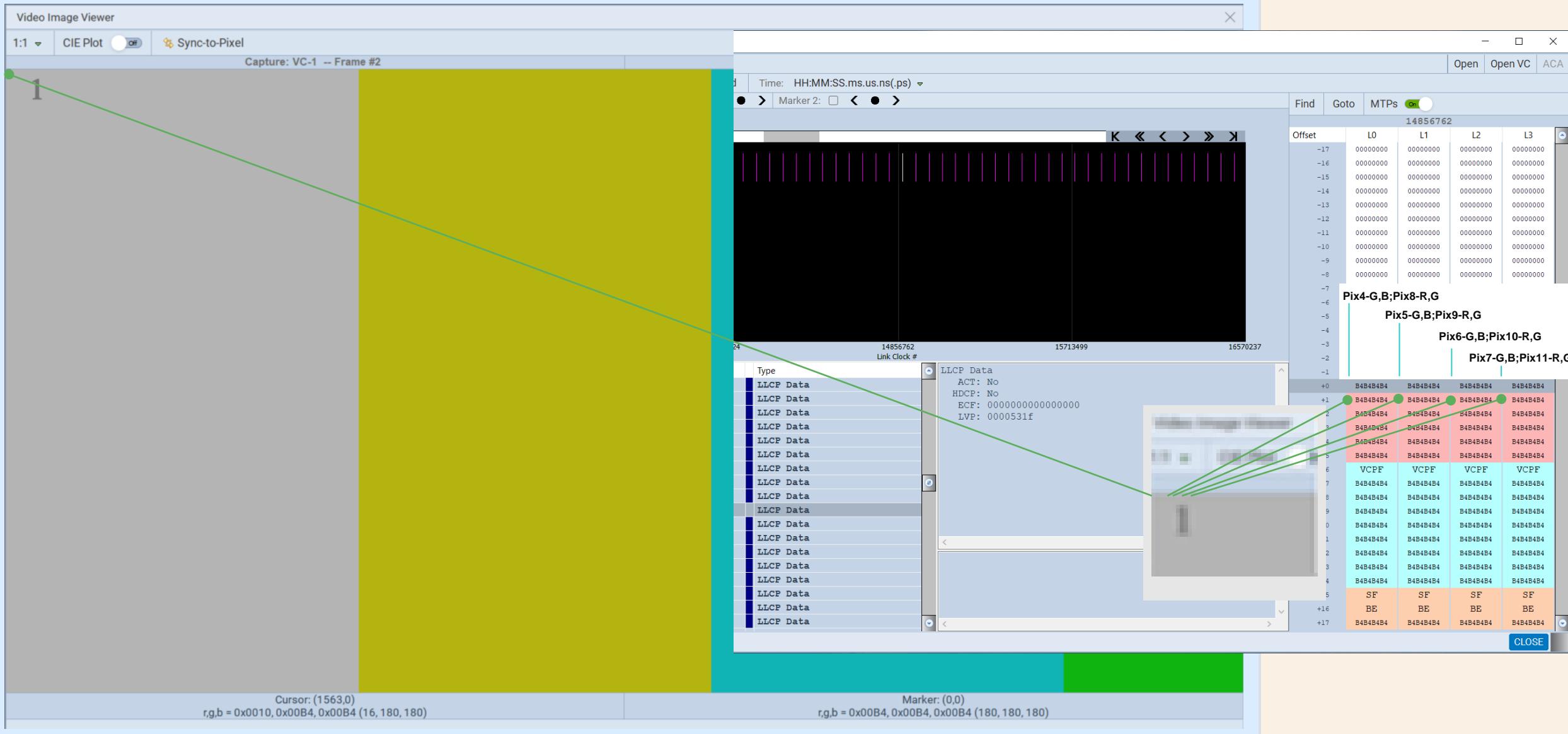
Main Link Protocols – Video Pixel Data to Link Data Symbol Mapping



Main Link Protocols – Video Pixel Data to Link Data Symbol Mapping



Main Link Protocols – Video Pixel Data to Link Data Symbol Mapping



Overview of DisplayPort 2.0 Protocols Connection Events – Aux Channel

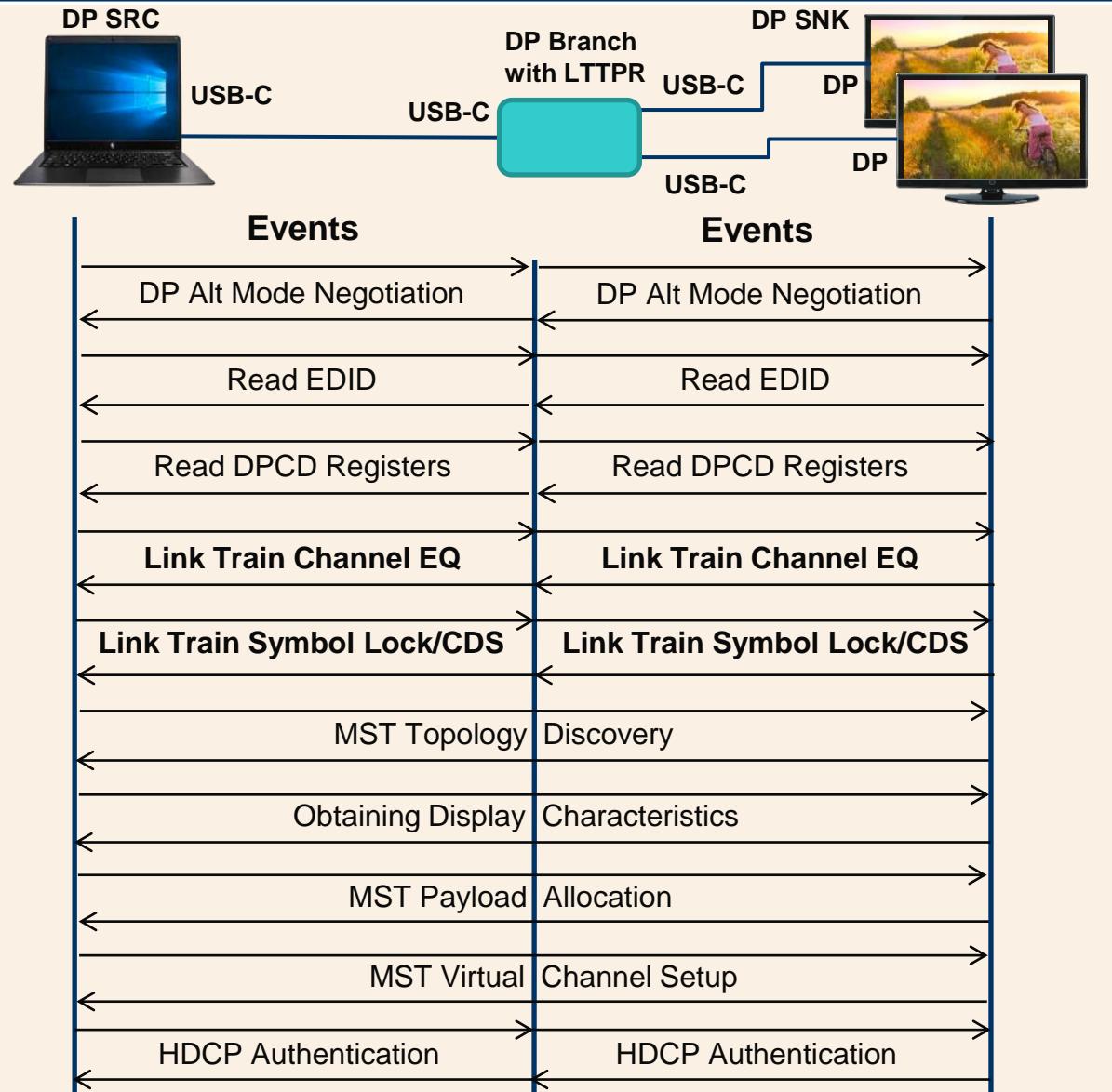
128b/132b Example with 8 LTTPRs @ 20G – Non-Transparent Mode

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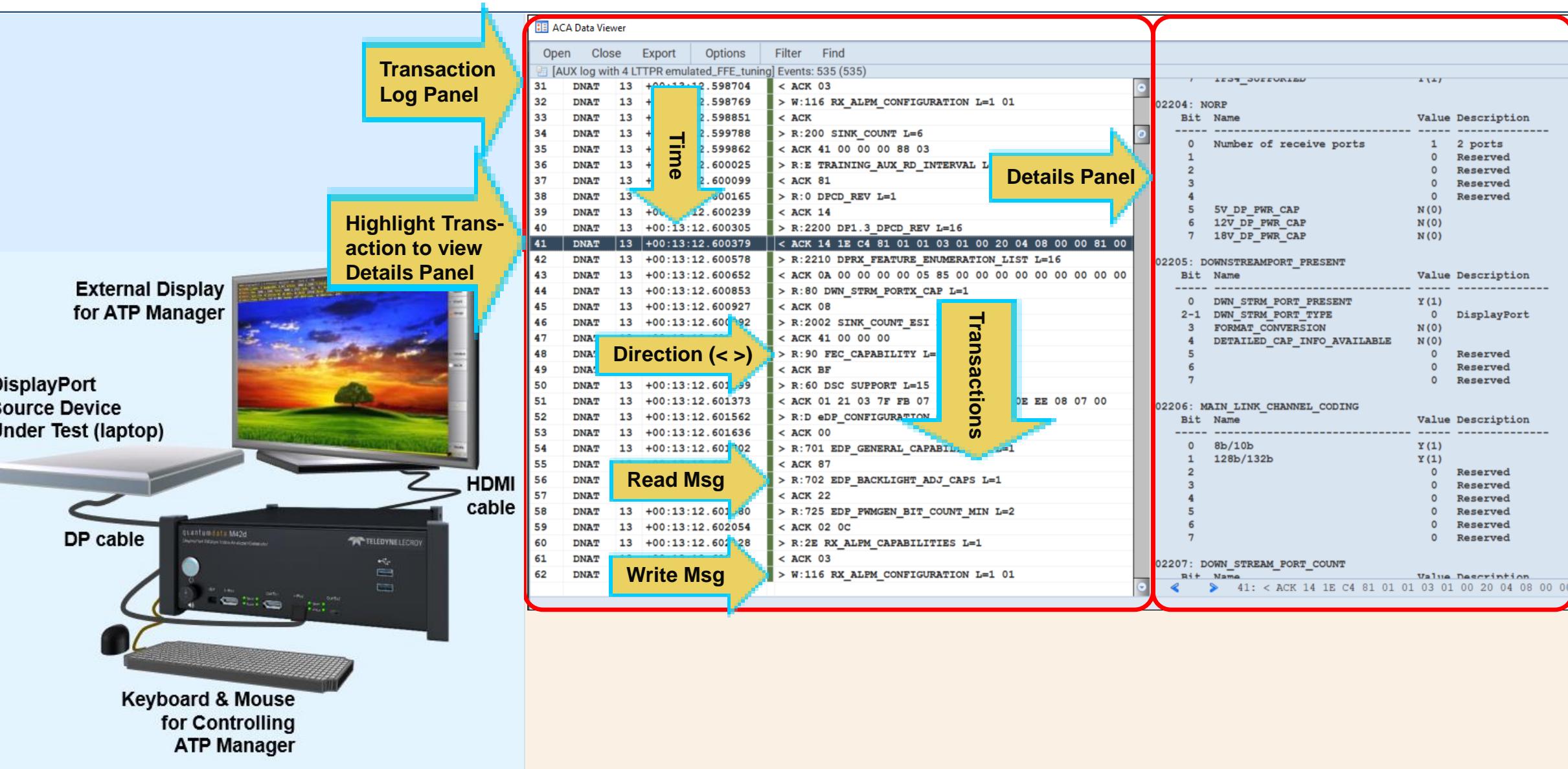


Connection Sequence



- ◆ DP Alt Mode Negotiation.
 - ◆ Phase I - Connection Detection/Power Contract.
 - ◆ Phase II – Negotiate into DP Alt Mode (Uses VDMs)
 - ◆ Phase III – DisplayPort Mode/Signaling Config.
- ◆ Read EDID for sink capabilities.
 - ◆ Read VESA, CTA block and any extension blocks.
- ◆ Read DPCD Registers for link capabilities.
 - ◆ Read Link capabilities.
 - ◆ Read FEC and DSC capabilities.
- ◆ **128b/132b Link Training – Must complete in 650 msec with up to eight (8) LTTPR devices.**
 - ◆ Phase I – Channel Equalization – must complete within 450 msec.
 - ◆ Phase II – Symbol Lock and Clock Data Switch – must complete within 20 msec per LTTPR.
- ◆ MST Configuration
 - ◆ Phase I – Topology Discovery.
 - ◆ Phase II – Payload Allocation.
 - ◆ Virtual Channel Setup
- ◆ HDCP Authentication (optional)

M42d Auxiliary Channel Analyzer (ACA)



Pre-Link Training Discovery and Configuration

Pre-Link Training - Discovery – Read DPRx Line Coding Capabilities

The screenshot shows the ACA Data Viewer interface with the following details:

- Header:** Open, Close, Export, Options, Filter, Find.
- Title Bar:** [20G LTPR_AUX_LT_FFE5] Events: 522 (996)
- Table:** A list of 108 events. The first 79 rows are shown in the main pane, and the last 30 are in a scrollable list below. Each row contains:
 - Event Number (e.g., 74, 75, 76, ..., 108).
 - Event Type (e.g., DNAT, DPLT).
 - Source MAC (e.g., DPUSBC-T11).
 - Timestamp (e.g., +03:50:27.001942).
 - Message Content (e.g., > R:E TRAINING_AUX_RD_INTERVAL L=1, < ACK 81, etc.).
- Details Panel:** On the right, there are four sections of bit definitions:
 - 02204: NORP**: Describes receive port configuration. Bit 0 is "Number of receive ports" (2 ports). Bits 5-7 are power capabilities (5V, 12V, 18V DP PWR CAP) all marked as N(0).
 - 02205: DOWNSTREAMPORT_PRESENT**: Describes downstream port presence. Bit 0 is "DWN_STRM_PORT_PRESENT" (Y(1)). Bits 2-7 are reserved.
 - 02206: MAIN_LINK_CHANNEL_CODING**: Describes main link channel coding. Bit 0 is "8b/10b" (Y(1)). Bit 1 is "128b/132b" (Y(1)). Bits 2-7 are reserved.
- Bottom Status:** A status bar at the bottom shows the last event number (79) and its content (< ACK 14 1E C4 81 01 01 03 01 00 20 04 08 00 00 81 00).

- ◆ Source (DPTx) reads the Extended Receiver Capabilities registers 2200-2206 of the Sink (DPRx) to verify support for 128b/132b line coding.

Pre-Link Training - Discovery – Read DPRx Link Rate Capabilities

The screenshot shows the ACA Data Viewer interface with the following details:

- Header:** Open, Close, Export, Options, Filter, Find.
- Title Bar:** [20G LTTPR_AUX_LT_FFE5] Events: 522 (996)
- Table View (Left):** A list of 108 events. The first few rows are:
 - 74 DNAT DPUSBC-T11 +03:50:27.0001942 > R:E TRAINING_AUX_RD_INTERVAL L=1
 - 75 DNAT DPUSBC-T11 +03:50:27.0002016 < ACK 81
 - 76 DNAT DPUSBC-T11 +03:50:27.0002113 > R:0 DPCD_REV L=1
 - 77 DNAT DPUSBC-T11 +03:50:27.0002187 < ACK 14
 - 78 DNAT DPUSBC-T11 +03:50:27.0002305 > R:2200 DP1.3_DPCD_REV L=16
- Details View (Right):** A series of tables showing bit descriptions for various fields. A yellow arrow points from the event list to the first table.
 - 02213: VSC_EXT_CEA_SD_MAX_CHAINING
 - 02214: FEATURE_ENUMERATION_LIST_CONT
 - 02215: 128b/132b_SUPPORTED_LINK_RATES
 - 02216: 128b/132b_TRAINING_AUX_RD_INTERVAL
 - 02217: Reserved
- Bottom Navigation:** Buttons for back, forward, and search (81: < ACK OA 00 00 00 00 07 85 00 00 00 00 00 00 00 00 00).

- ◆ Source (DPTx) reads registers 2210-2215 of the Sink (DPRx) to verify support for the UHBR link rates.
 - ◆ Example shows all UHBR rates supported.

Pre-Link Training - Discover LTTPR Line Code and Link Rate Capabilities

ACA Data Viewer

Open Close Export Options Filter Find

[20G LTTPR_AUX_LT_FFE5] Events: 522 (996)

92	DNAT	11	+03:50:27.004004	> R:701 EDP_GENERAL_CAPABILITY_1 L=1
93	DNAT	11	+03:50:27.004078	< ACK 87
94	DNAT	11	+03:50:27.004216	> R:702 EDP_BACKLIGHT_ADJ_CAPS L=1
95	DNAT	11	+03:50:27.004290	< ACK 22
96	DNAT	11	+03:50:27.004388	> R:725 EDP_PWMGEN_BIT_COUNT_MIN L=2
97	DNAT	11	+03:50:27.004462	< ACK 02 0C
98	DNAT	11	+03:50:27.004562	> R:2E RX_ALPM_CAPABILITIES L=1
99	DNAT	11	+03:50:27.004636	< ACK 03
100	DNAT	11	+03:50:27.004717	> W:116 RX_ALPM_CONFIGURATION L=1 01
101	DNAT	11	+03:50:27.004799	< ACK
102	DNAT	11	+03:50:27.004877	> R:F0000 LTTPR_FIELD_DATA_STRUCTURE_REV L=8
103	DNAT	11	+03:50:27.004951	< ACK 20 1E 01 AA 04 10 01 07
104	DNAT	11	+03:50:27.005169	> W:F0003 PHY_REPEAT_MODE L=1 AA
105	DNAT	11	+03:50:27.005251	< ACK
106	DPLT	11	+03:50:27.005382	> W:108 MAIN_LINK_CHANNEL_CODING_SET L=1 02
107	DPLT	11	+03:50:27.005464	< ACK
108	DPLT	11	+03:50:27.005531	> W:100 LINK_BW_SET L=1 02
109	DPLT	11	+03:50:27.005613	< ACK
110	DPLT	11	+03:50:27.005723	> W:101 LANE_COUNT_SET L=1 84
111	DPLT	11	+03:50:27.005805	< ACK
112	DPLT	11	+03:50:27.107033	> W:107 DOWNSPREAD_CTRL L=1 00
113	DPLT	11	+03:50:27.107115	< ACK
114	DNAT	11	+03:50:27.107256	> W:600 SINK_SET_POWER L=1 01
115	DNAT	11	+03:50:27.107338	< ACK
116	DNAT	11	+03:50:27.107410	> R:E TRAINING_AUX_RD_INTERVAL L=1
117	DNAT	11	+03:50:27.107484	< ACK 81
118	DPLT	11	+03:50:27.107612	> W:102 TRAINING_PATTERN_SET L=1 00
119	DPLT	11	+03:50:27.107694	< ACK
120	DPLT	11	+03:50:27.107755	> R:205 SINK_STATUS L=1
121	DPLT	11	+03:50:27.107829	< ACK 03

Start Time: +03:50:27.004951
Type: Native
Direction: Reply
Command: ACK
Reply to Read Request.

F0000: LTTPR_FIELD_DATA_STRUCTURE_REV

Bit	Name	Value	Description
3-0	Minor Revision Number	0	
7-4	Major Revision Number	2	

F0001: 8b/10b_MAX_LINK_RATE_PHY_REPEAT

Bit	Name	Value	Description
7-0	MAX_LINK_RATE	1Eh	8.1 Gbps/lane

F0002: PHY_REPEAT_CNT

Bit	Name	Value	Description
7-0	LTTPR Count	01h	8

F0003: PHY_REPEAT_MODE

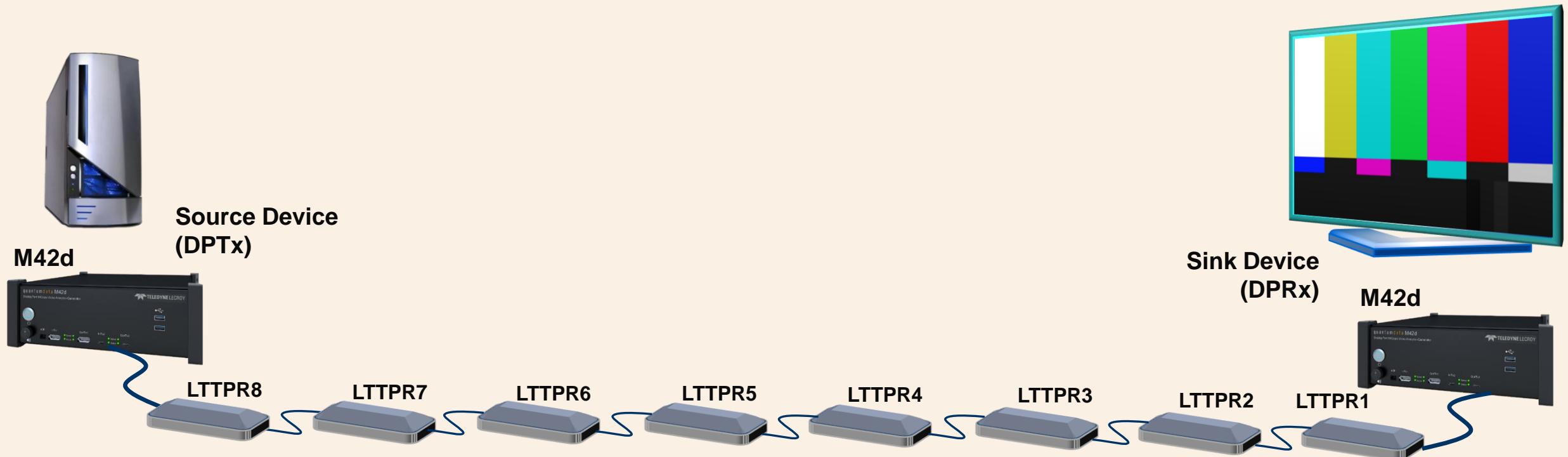
Bit	Name	Value	Description
7-0	Mode	AAh	Non-transparent

F0004: MAX_LANE_COUNT_PHY_REPEAT

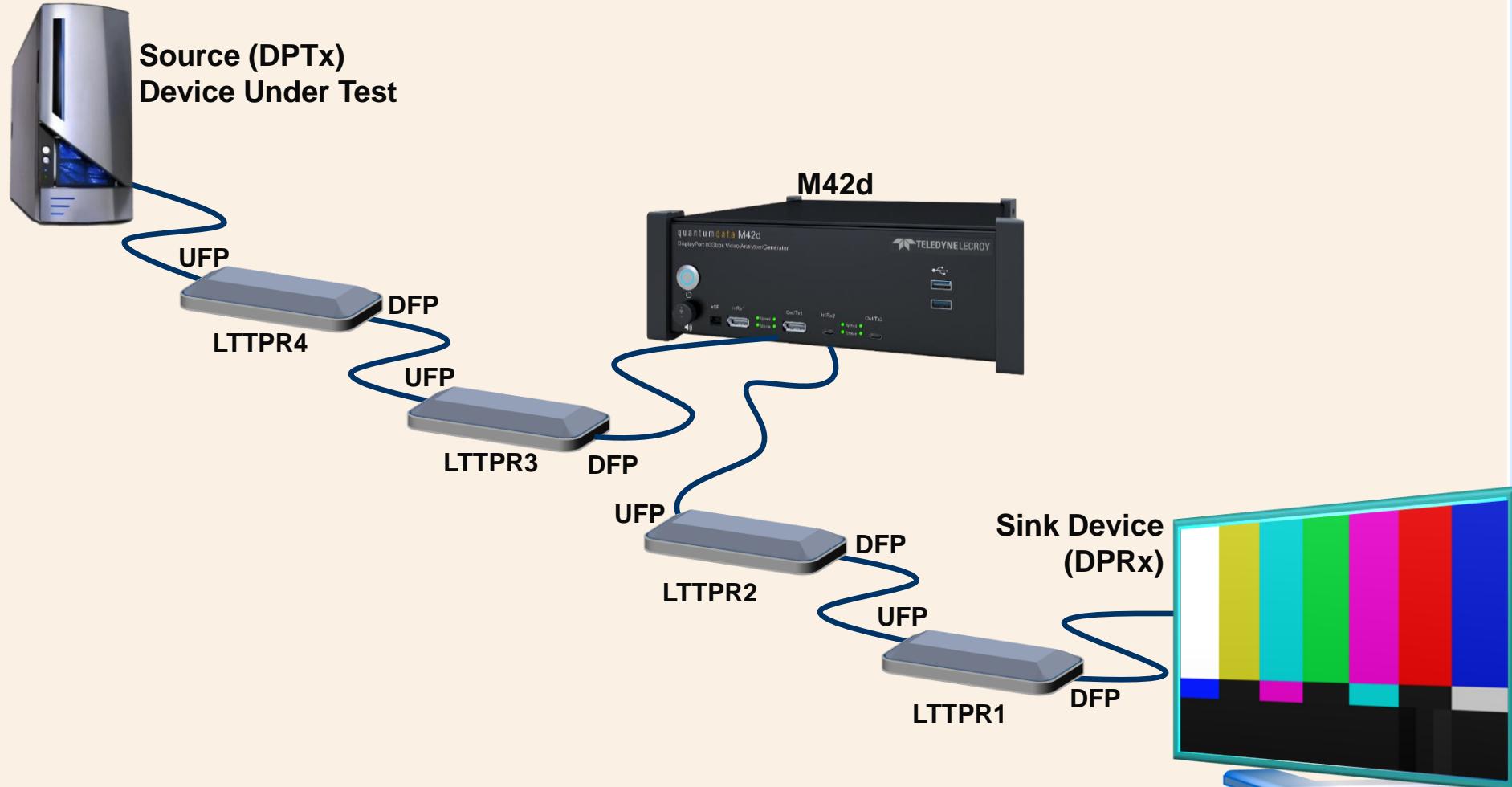
Bit	Name	Value	Description
4-0	MAX_LANE_COUNT	04h	Four lanes
5		0	Reserved
6		0	Reserved
7		0	Reserved

- ◆ Source (DPTx) reads registers F0000-F0007 to discover capability of all LTTPR devices (e.g. 8).
 - ◆ F0000 register shows the revision of the LTTPRs in the network. This determines what mode the DPTx will use for link training.
 - ◆ F0001 register shows the max 8b/10b rate supported by the LTTPR network.
 - ◆ F0002 register shows number of LTTPRs in the network connected to DPTx.
 - ◆ F0003 register shows the current status of the LTTPR mode.
 - ◆ F0004 register shows the max number of lanes supported by the LTTPRs in the chain connected to the DPTx.

Sample Network Used in The Example in This Webinar



Sample Network Depicting Passive Monitoring



- ◆ M42d supports passive monitoring between DisplayPort 2.0 device as well.
- ◆ This includes both the main link even at the UHBR rates and the Aux Channel.

What are DisplayPort LTTPRs?

- ◆ What are DisplayPort Link Training Tunable Phy Repeater (LTTPRs) devices?
 - ◆ LTTPRs are repeater devices that are situated between the DPTx at the source end to the DPRx at the sink end.
 - ◆ LTTPRs operate at the phy layer to achieve signal integrity from the DPTx at the source end to the DPRx at the sink end.
 - ◆ LTTPRs are essential due to the high data rates over distances.
 - ◆ LTTPRs achieve link training with adjacent devices (hops) between DPTx, LTTPRs or DPRx).
 - ◆ Once LTTPR devices achieve link training, they should appear transparent to DisplayPort main link transmission above the phy layer.
 - ◆ LTTPRs ensure phy level signal integrity using Redrivers and Retimers.



What are LTTPRs – Redrivers and Retimers

- ◆ LTTPR devices provide physical layer signal integrity functions using Redrivers and Retimers.

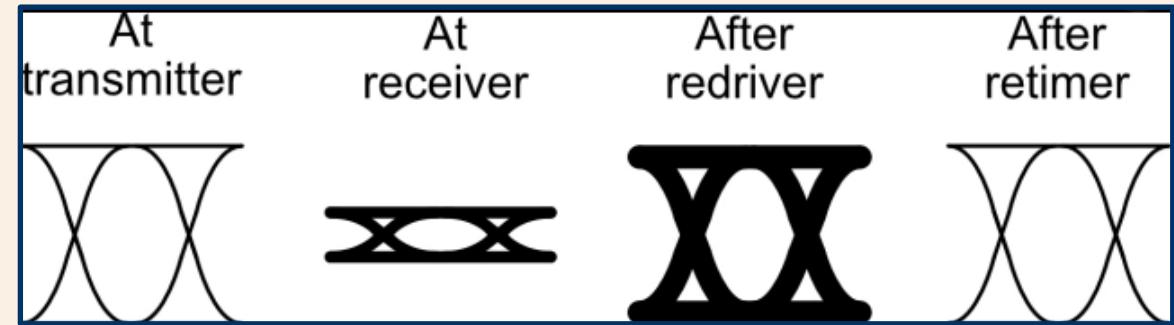
- ◆ A Redriver is a high-bandwidth amplifier with receive (RX) side equalizer (EQ) to compensate for frequency-dependent attenuation on PCB traces or cables.

Note: Redrivers not only amplify the data signal but they also **amplify any noise** and jitter that is in the signal path.

- ◆ A Retimer recovers the embedded clock along with the data to **remove jitter** and retransmits the data with a **clean clock**.

Retimers are more complex than redrivers.

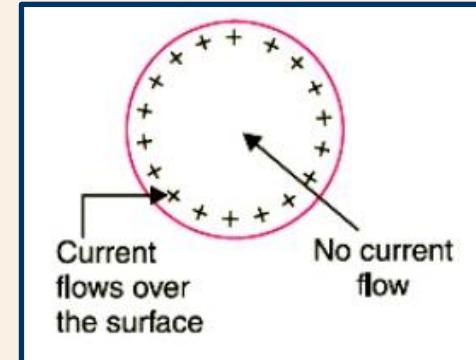
Note: LTTPR devices typically have both redriver and retimer functions.



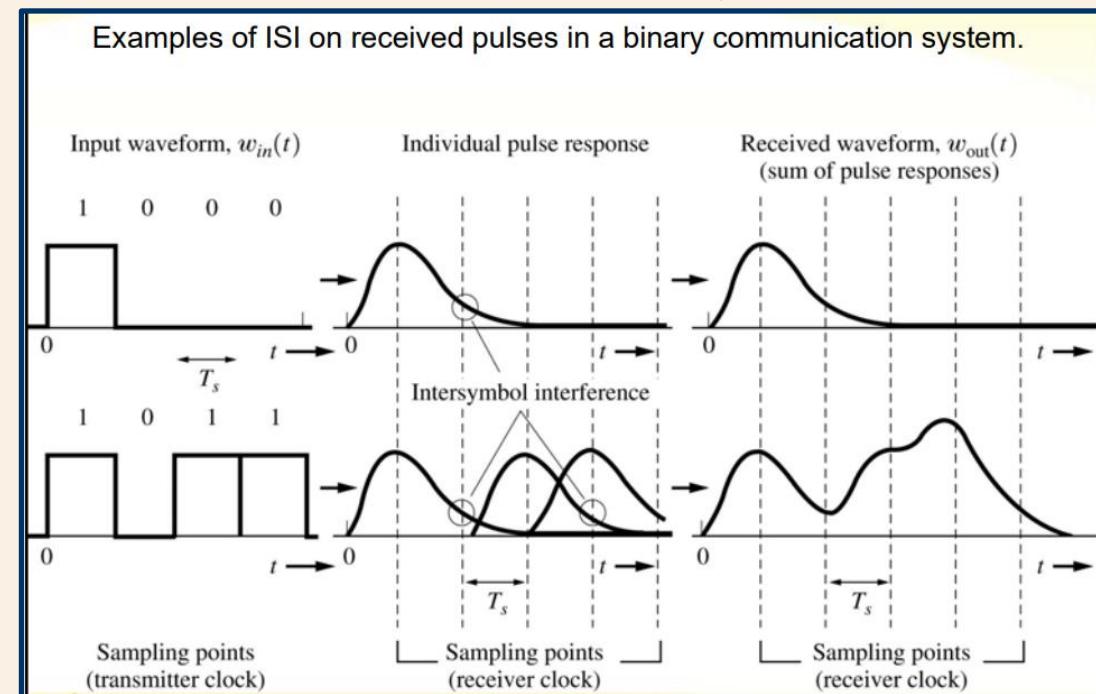
Redrivers vs Retimers

Why LTTPRs Needed?

- ◆ Why are LTTPRs Needed?
 - ◆ High bit rate transmission (20G) at longer distances distorts the signal.
 - ◆ At high data rates, the signal is only transmitted on the outer “skin” of PCB traces and copper cable medium.
 - ◆ This “skin effect” causes Inter-Symbol Interference (ISI).
 - ◆ ISI results in smearing the signal across multiple bit times.
 - ◆ ISI makes it difficult for the far end receiver to distinguish a logical 1 from a logical 0 even in binary transmission using NRZ line coding.



Skin Effect



Inter-Symbol Interference

Pre-Link Training - Discover LTTPR Line Code and Link Rate Capabilities

ACA Data Viewer

Open Close Export Options Filter Find

[20G LTTPR_AUX_LT_FFE5] Events: 522 (996)

92	DNAT	11	+03:50:27.004004	> R:701 EDP_GENERAL_CAPABILITY_1 L=1
93	DNAT	11	+03:50:27.004078	< ACK 87
94	DNAT	11	+03:50:27.004216	> R:702 EDP_BACKLIGHT_ADJ_CAPS L=1
95	DNAT	11	+03:50:27.004290	< ACK 22
96	DNAT	11	+03:50:27.004388	> R:725 EDP_PWMGEN_BIT_COUNT_MIN L=2
97	DNAT	11	+03:50:27.004462	< ACK 02 0C
98	DNAT	11	+03:50:27.004562	> R:2E RX_ALPM_CAPABILITIES L=1
99	DNAT	11	+03:50:27.004636	< ACK 03
100	DNAT	11	+03:50:27.004717	> W:116 RX_ALPM_CONFIGURATION L=1 01
101	DNAT	11	+03:50:27.004799	< ACK
102	DNAT	11	+03:50:27.004877	> R:F0000 LTTPR FIELD DATA STRUCTURE REV L=8
103	DNAT	11	+03:50:27.004951	< ACK 20 1E 01 AA 04 10 01 07
104	DPLT	11	+03:50:27.005169	> W:F0003 PHY_REPEAT_MODE L=1 AA
105	DNAT	11	+03:50:27.005251	< ACK
106	DPLT	11	+03:50:27.005382	> W:108 MAIN_LINK_CHANNEL_CODING_SET L=1 02
107	DPLT	11	+03:50:27.005464	< ACK
108	DPLT	11	+03:50:27.005531	> W:100 LINK_BW_SET L=1 02
109	DPLT	11	+03:50:27.005613	< ACK
110	DPLT	11	+03:50:27.005723	> W:101 LANE_COUNT_SET L=1 84
111	DPLT	11	+03:50:27.005805	< ACK
112	DPLT	11	+03:50:27.107033	> W:107 DOWNSPREAD_CTRL L=1 00
113	DPLT	11	+03:50:27.107115	< ACK
114	DNAT	11	+03:50:27.107256	> W:600 SINK_SET_POWER L=1 01
115	DNAT	11	+03:50:27.107338	< ACK
116	DNAT	11	+03:50:27.107410	> R:E TRAINING_AUX_RD_INTERVAL L=1
117	DNAT	11	+03:50:27.107484	< ACK 81
118	DPLT	11	+03:50:27.107612	> W:102 TRAINING_PATTERN_SET: L=1 00
119	DPLT	11	+03:50:27.107694	< ACK
120	DPLT	11	+03:50:27.107755	> R:205 SINK_STATUS L=1
121	DPLT	11	+03:50:27.107829	< ACK 03

MAX_LANE_COUNT
04h Four lanes
5
6
7
0 Reserved
0 Reserved
0 Reserved

F0005: PHY_REPEAT_EXTENDED_WAKE_TIMEOUT
Bit Name Value Description
6-0 EXT_WAKE_TIMEOUT_REQUEST 16
7 EXT_WAKE_TIMEOUT_GRANT N(0)

F0006: MAIN_LINK_CHANNEL_CODING_PHY_REPEAT
Bit Name Value Description
0 128b/132b SUPPORTED Y(1)
1
2
3
4
5
6
7
0 Reserved
0 Reserved
0 Reserved
0 Reserved
0 Reserved
0 Reserved
0 Reserved

F0007: PHY_REPEAT_128B/132B_RATES
Bit Name Value Description
0 10 Gbps/lane Support Y(1)
1 20 Gbps/lane Support Y(1)
2 13.5 Gbps/lane Support Y(1)
3
4
5
6
7
0 Reserved
0 Reserved
0 Reserved
0 Reserved
0 Reserved
0 Reserved
0 Reserved

[0000] [00 20 1E 01 AA 04 10 01] [.....]

103: < ACK 20 1E 01 AA 04 10 01 07

- ◆ Source (DPTx) reads registers F0000-F0007 to discover capability of all LTTPR devices (e.g. 8).
 - ◆ F0006 register shows the line code supported by the LTTPRs in the chain.
 - ◆ F0007 register shows the UHBR rates supported by the LTTPRs in the chain.

Pre-Link Training – Configure LTTPRs into Non-Transparent Mode

The screenshot shows the ACA Data Viewer interface with the following details:

- Menu Bar:** Open, Close, Export, Options, Filter, Find.
- Panel Title:** [20G LTTPR_AUX_LT_FFE5] Events: 522 (996)
- Message Log:** A list of 25 messages. Message 104 is highlighted with a blue background and a yellow arrow pointing to its details. The log includes:
 - 91 DNAT DPUSBC-T11 +03:50:27.0003915 < ACK 00
 - 92 DNAT DPUSBC-T11 +03:50:27.0004004 > R:701 EDP_GENERAL_CAPABILITY_1 L=1
 - 93 DNAT DPUSBC-T11 +03:50:27.0004078 < ACK 87
 - 94 DNAT DPUSBC-T11 +03:50:27.0004216 > R:702 EDP_BACKLIGHT_ADJ_CAPS L=1
 - 95 DNAT DPUSBC-T11 +03:50:27.0004290 < ACK 22
 - 96 DNAT DPUSBC-T11 +03:50:27.0004388 > R:725 EDP_PWMGEN_BIT_COUNT_MIN L=2
 - 97 DNAT DPUSBC-T11 +03:50:27.0004462 < ACK 02 0C
 - 98 DNAT DPUSBC-T11 +03:50:27.0004562 > R:2E RX_ALPM_CAPABILITIES L=1
 - 99 DNAT DPUSBC-T11 +03:50:27.0004636 < ACK 03
 - 100 DNAT DPUSBC-T11 +03:50:27.0004717 > W:116 RX_ALPM_CONFIGURATION L=1 01
 - 101 DNAT DPUSBC-T11 +03:50:27.0004799 < ACK
 - 102 DNAT DPUSBC-T11 +03:50:27.0004877 > R:F0000 LTTPR_FIELD_DATA_STRUCTURE_REV L=8
 - 103 DNAT DPUSBC-T11 +03:50:27.0004951 < ACK 20 1E 01 AA 04 10 01 07
 - 104 DNAT DPUSBC-T11 +03:50:27.0005169** > W:F0003 PHY REPEATER MODE L=1 AA
 - 105 DNAT DPUSBC-T11 +03:50:27.0005251 < ACK
 - 106 DPLT DPUSBC-T11 +03:50:27.0005382 > W:108 MAIN_LINK_CHANNEL_CODING_SET L=1 02
 - 107 DPLT DPUSBC-T11 +03:50:27.0005464 < ACK
 - 108 DPLT DPUSBC-T11 +03:50:27.0005531 > W:100 LINK_BW_SET L=1 02
 - 109 DPLT DPUSBC-T11 +03:50:27.0005613 < ACK
 - 110 DPLT DPUSBC-T11 +03:50:27.0005723 > W:101 LANE_COUNT_SET L=1 84
 - 111 DPLT DPUSBC-T11 +03:50:27.0005805 < ACK
 - 112 DPLT DPUSBC-T11 +03:50:27.107033 > W:107 DOWNSPREAD_CTRL L=1 00
 - 113 DPLT DPUSBC-T11 +03:50:27.107115 < ACK
 - 114 DNAT DPUSBC-T11 +03:50:27.107256 > W:600 SINK_SET_POWER L=1 01
 - 115 DNAT DPUSBC-T11 +03:50:27.107338 < ACK
 - 116 DNAT DPUSBC-T11 +03:50:27.107410 > R:E TRAINING_AUX_RD_INTERVAL L=1
 - 117 DNAT DPUSBC-T11 +03:50:27.107484 < ACK 81
 - 118 DPLT DPUSBC-T11 +03:50:27.107612 > W:102 TRAINING_PATTERN_SET: L=1 00
 - 119 DPLT DPUSBC-T11 +03:50:27.107694 < ACK
 - 120 DPLT DPUSBC-T11 +03:50:27.107755 > R:205 SINK_STATUS L=1
 - 121 DPLT DPUSBC-T11 +03:50:27.107829 < ACK 03
 - 122 DPLT DPUSBC-T11 +03:50:27.108465 > W:108 MAIN_LINK_CHANNEL_CODING_SET L=1 02
 - 123 DPLT DPUSBC-T11 +03:50:27.108547 < ACK
 - 124 DPLT DPUSBC-T11 +03:50:27.108612 > W:100 LINK_BW_SET L=1 02
 - 125 DPLT DPUSBC-T11 +03:50:27.108694 < ACK
- Detailed View (Right Panel):** Shows a request message to register F0003. The message details are:
 - Start Time: +03:50:27.005169
 - Type: Native
 - Direction: Request
 - Command: Write
 - Address: 0xF0003 (PHY REPEATER MODE)
 - Length: 1

Bit Name	Value Description
7-0 Mode	AAh Non-transparent

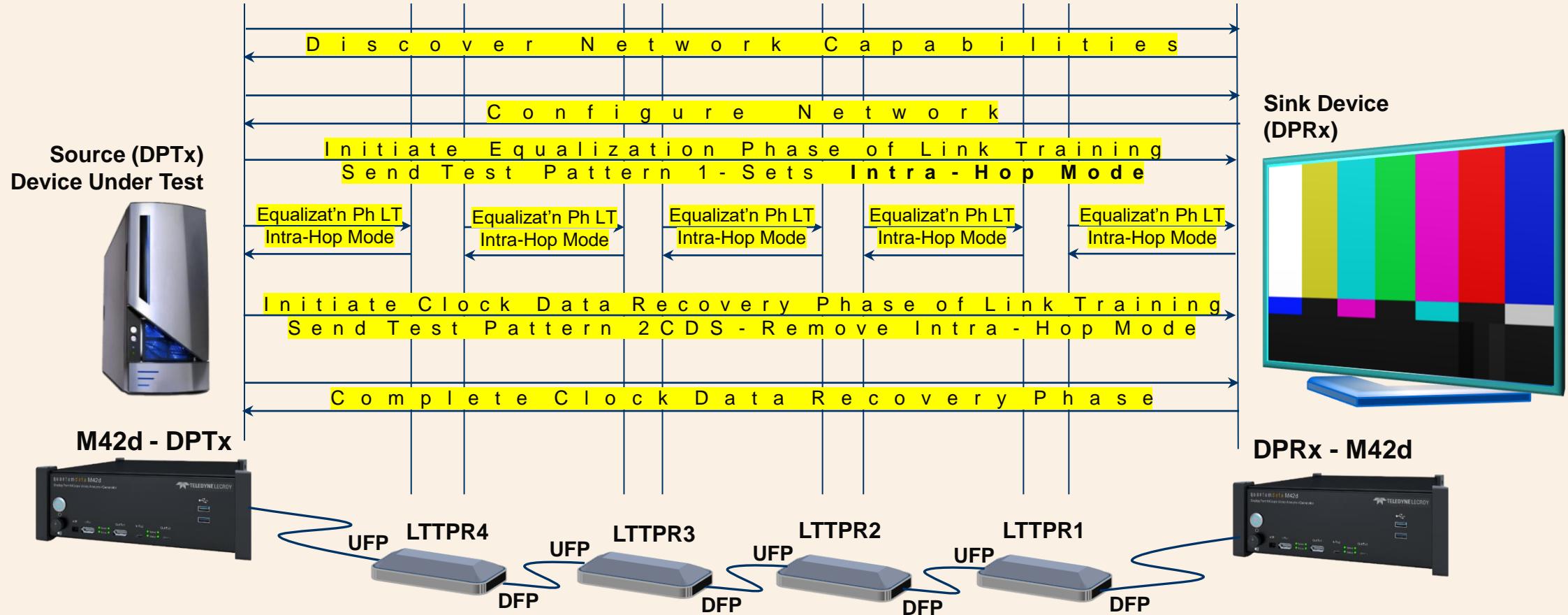
The value field shows the binary representation [0000][8F 00 03 00 AA --- - - -] followed by an ellipsis [.....].

- Source (DPTX) writes to register F0003 to set the LTTPRs Phy Repeater Mode to “Non-Transparent.”
- In the Non-Transparent mode for 128b/132b each LTTPR is trained independently in the link with the adjacent device (either another LTTPR or DPTx or DPRx). This ensures better signal quality for the end-to-end link.

Note 1: Register F0003 is shared for all LTTPRs and one write is sufficient.

Note 2: This setting does not need to be completed for each link training unless there is a hot plug event following a disconnection.

128b/132b Non-Transparent Mode Link Training



Pre-Link Training – LTTPR Network Initialization

ACA Data Viewer

Open Close Export Options Filter Find

[20G LTTPR_AUX_LT_FFE5] Events: 522 (996)

107	DPLT	DPUSBC-T11	+03:50:27.005464	< ACK
108	DPLT	DPUSBC-T11	+03:50:27.005531	> W:100 LINK_BW_SET L=1 02
109	DPLT	DPUSBC-T11	+03:50:27.005613	< ACK
110	DPLT	DPUSBC-T11	+03:50:27.005723	> W:101 LANE_COUNT_SET L=1 84
111	DPLT	DPUSBC-T11	+03:50:27.005805	< ACK
112	DPLT	DPUSBC-T11	+03:50:27.107033	> W:107 DOWNSPREAD_CTRL L=1 00
113	DPLT	DPUSBC-T11	+03:50:27.107115	< ACK
114	DNAT	DPUSBC-T11	+03:50:27.107256	> W:600 SINK_SET_POWER L=1 01
115	DNAT	DPUSBC-T11	+03:50:27.107338	< ACK
116	DNAT	DPUSBC-T11	+03:50:27.107410	> R:E TRAINING_AUX_RD_INTERVAL L=1
117	DNAT	DPUSBC-T11	+03:50:27.107484	< ACK 81
118	DPLT	DPUSBC-T11	+03:50:27.107612	> W:102 TRAINING_PATTERN_SET: L=1 00
119	DPLT	DPUSBC-T11	+03:50:27.107694	< ACK
120	DPLT	DPUSBC-T11	+03:50:27.107755	> R:205 SINK_STATUS L=1
121	DPLT	DPUSBC-T11	+03:50:27.107829	< ACK 03
122	DPLT	DPUSBC-T11	+03:50:27.108465	> W:108 MAIN_LINK_CHANNEL_CODING_SET L=1 02
123	DPLT	DPUSBC-T11	+03:50:27.108547	< ACK
124	DPLT	DPUSBC-T11	+03:50:27.108612	> W:100 LINK_BW_SET L=1 02
125	DPLT	DPUSBC-T11	+03:50:27.108694	< ACK
126	DPLT	DPUSBC-T11	+03:50:27.108810	> W:101 LANE_COUNT_SET L=1 84
127	DPLT	DPUSBC-T11	+03:50:27.108892	< ACK
128	DPLT	DPUSBC-T11	+03:50:27.108974	> W:102 TRAINING_PATTERN_SET: L=1 01
129	DPLT	DPUSBC-T11	+03:50:27.109255	< ACK
130	DNAT	DPUSBC-T11	+03:50:27.109329	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
131	DNAT	DPUSBC-T11	+03:50:27.109602	< DEFER
132	DNAT	DPUSBC-T11	+03:50:27.110168	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
133	DNAT	DPUSBC-T11	+03:50:27.110441	< DEFER
134	DNAT	DPUSBC-T11	+03:50:27.111015	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
135	DNAT	DPUSBC-T11	+03:50:27.111288	< DEFER
136	DNAT	DPUSBC-T11	+03:50:27.111875	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
137	DNAT	DPUSBC-T11	+03:50:27.112148	< DEFER
138	DNAT	DPUSBC-T11	+03:50:27.112719	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
139	DNAT	DPUSBC-T11	+03:50:27.112992	< DEFER
140	DNAT	DPUSBC-T11	+03:50:27.113562	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
141	DNAT	DPUSBC-T11	+03:50:27.113835	< DEFER

Start Time: +03:50:27.107612
Type: Native
Direction: Request
Command: Write
Address: 0x00102 (TRAINING_PATTERN_SET:)

Length: 1

00102: TRAINING_PATTERN_SET:
8b/10b Link Layer

Bit	Name	Value	Description
3-0	TRAINING_PATTERN_SELECT	0	None
4	RECOVERED_CLOCK_OUT_EN	N(0)	
5	SCRAMBLING_DISABLE	N(0)	
7-6	SYMBOL_ERROR_COUNT_SEL	0	Disparity and Symbol error

128b/132b Link Layer

Bit	Name	Value	Description
3-0	TRAINING_PATTERN_SELECT	0	None
4		0	Reserved
5	SCRAMBLING_DISABLE	N(0)	
6		0	Reserved
7		0	Reserved

[0000] [80 01 02 00 00 -- -- --] [.....]

118: > W:102 TRAINING_PATTERN_SET: L=1 00

- Source (DPTx) transmits Training Pattern 0 to ensure that the downstream LTTPRs are not still, or yet, in Intra-Hop mode.

Pre-Link Training – Network Initialization

ACA Data Viewer

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[20G LTTPR_AUX_LT_FFE5] Events: 522 (996)

107	DPLT	DPUSBC-T11	+03:50:27.005464	< ACK
108	DPLT	DPUSBC-T11	+03:50:27.005531	> W:100 LINK_BW_SET L=1 02
109	DPLT	DPUSBC-T11	+03:50:27.005613	< ACK
110	DPLT	DPUSBC-T11	+03:50:27.005723	> W:101 LANE_COUNT_SET L=1 84
111	DPLT	DPUSBC-T11	+03:50:27.005805	< ACK
112	DPLT	DPUSBC-T11	+03:50:27.107033	> W:107 DOWNSPREAD_CTRL L=1 00
113	DPLT	DPUSBC-T11	+03:50:27.107115	< ACK
114	DNAT	DPUSBC-T11	+03:50:27.107256	> W:600 SINK_SET_POWER L=1 01
115	DNAT	DPUSBC-T11	+03:50:27.107338	< ACK
116	DNAT	DPUSBC-T11	+03:50:27.107410	> R:E TRAINING_AUX_RD_INTERVAL L=1
117	DNAT	DPUSBC-T11	+03:50:27.107484	< ACK 81
118	DPLT	DPUSBC-T11	+03:50:27.107612	> W:102 TRAINING_PATTERN_SET: L=1 00
119	DPLT	DPUSBC-T11	+03:50:27.107694	< ACK
120	DPLT	DPUSBC-T11	+03:50:27.107755	> R:205 SINK_STATUS L=1
121	DPLT	DPUSBC-T11	+03:50:27.107829	< ACK 03
122	DPLT	DPUSBC-T11	+03:50:27.108465	> W:108 MAIN_LINK_CHANNEL_CODING_SET L=1 02
123	DPLT	DPUSBC-T11	+03:50:27.108547	< ACK
124	DPLT	DPUSBC-T11	+03:50:27.108612	> W:100 LINK_BW_SET L=1 02
125	DPLT	DPUSBC-T11	+03:50:27.108694	< ACK
126	DPLT	DPUSBC-T11	+03:50:27.108810	> W:101 LANE_COUNT_SET L=1 84
127	DPLT	DPUSBC-T11	+03:50:27.108892	< ACK
128	DPLT	DPUSBC-T11	+03:50:27.108974	> W:102 TRAINING_PATTERN_SET: L=1 01
129	DPLT	DPUSBC-T11	+03:50:27.109255	< ACK
130	DNAT	DPUSBC-T11	+03:50:27.109329	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
131	DNAT	DPUSBC-T11	+03:50:27.109602	< DEFER
132	DNAT	DPUSBC-T11	+03:50:27.110168	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
133	DNAT	DPUSBC-T11	+03:50:27.110441	< DEFER
134	DNAT	DPUSBC-T11	+03:50:27.111015	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
135	DNAT	DPUSBC-T11	+03:50:27.111288	< DEFER
136	DNAT	DPUSBC-T11	+03:50:27.111875	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
137	DNAT	DPUSBC-T11	+03:50:27.112148	< DEFER
138	DNAT	DPUSBC-T11	+03:50:27.112719	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
139	DNAT	DPUSBC-T11	+03:50:27.112992	< DEFER
140	DNAT	DPUSBC-T11	+03:50:27.113562	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
141	DNAT	DPUSBC-T11	+03:50:27.113835	< DEFER

Start Time: +03:50:27.107829
Type: Native
Direction: Reply
Command: ACK
Reply to Read Request.

00205: SINK_STATUS

Bit	Name	Value	Description
0	RECEIVE_PORT_0_STATUS	Y(1)	
1	RECEIVE_PORT_1_STATUS	Y(1)	
2	STREAM_REGENERATION_STATUS	N(0)	
3	Intra-Hop AUX Reply Indication	N(0)	
4		0	Reserved
5		0	Reserved
6		0	Reserved
7		0	Reserved

[0000] [00 03 -- -- -- -- -- --] [..]

121: < ACK 03

- Source (DPTx) reads register 205 to verify that the downstream LTTPRs are not currently in the Intra-Hop mode.

Pre-Link Training – Network Configuration – Set Line Coding

ACA Data Viewer

Open Close Export Options Filter Find

[20G LTTPR_AUX_LT_FFE5] Events: 522 (996)

Line	Type	Address	Value	Description
107	DPLT	DPUSBC-T11	+03:50:27.005464	< ACK
108	DPLT	DPUSBC-T11	+03:50:27.005531	> W:100 LINK_BW_SET L=1 02
109	DPLT	DPUSBC-T11	+03:50:27.005613	< ACK
110	DPLT	DPUSBC-T11	+03:50:27.005723	> W:101 LANE_COUNT_SET L=1 84
111	DPLT	DPUSBC-T11	+03:50:27.005805	< ACK
112	DPLT	DPUSBC-T11	+03:50:27.107033	> W:107 DOWNSPREAD_CTRL L=1 00
113	DPLT	DPUSBC-T11	+03:50:27.107115	< ACK
114	DNAT	DPUSBC-T11	+03:50:27.107256	> W:600 SINK_SET_POWER L=1 01
115	DNAT	DPUSBC-T11	+03:50:27.107338	< ACK
116	DNAT	DPUSBC-T11	+03:50:27.107410	> R:E TRAINING_AUX_RD_INTERVAL L=1
117	DNAT	DPUSBC-T11	+03:50:27.107484	< ACK 81
118	DPLT	DPUSBC-T11	+03:50:27.107612	> W:102 TRAINING_PATTERN_SET: L=1 00
119	DPLT	DPUSBC-T11	+03:50:27.107694	< ACK
120	DPLT	DPUSBC-T11	+03:50:27.107755	> R:205 SINK_STATUS L=1
121	DPLT	DPUSBC-T11	+03:50:27.107829	< ACK 03
122	DPLT	DPUSBC-T11	+03:50:27.108465	> W:108 MAIN_LINK_CHANNEL_CODING_SET L=1 02
123	DPLT	DPUSBC-T11	+03:50:27.108547	< ACK
124	DPLT	DPUSBC-T11	+03:50:27.108612	> W:100 LINK_BW_SET L=1 02
125	DPLT	DPUSBC-T11	+03:50:27.108694	< ACK
126	DPLT	DPUSBC-T11	+03:50:27.108810	> W:101 LANE_COUNT_SET L=1 84
127	DPLT	DPUSBC-T11	+03:50:27.108892	< ACK
128	DPLT	DPUSBC-T11	+03:50:27.108974	> W:102 TRAINING_PATTERN_SET: L=1 01
129	DPLT	DPUSBC-T11	+03:50:27.109255	< ACK
130	DNAT	DPUSBC-T11	+03:50:27.109329	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL...
131	DNAT	DPUSBC-T11	+03:50:27.109602	< DEFER
132	DNAT	DPUSBC-T11	+03:50:27.110168	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL...
133	DNAT	DPUSBC-T11	+03:50:27.110441	< DEFER
134	DNAT	DPUSBC-T11	+03:50:27.111015	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL...
135	DNAT	DPUSBC-T11	+03:50:27.111288	< DEFER
136	DNAT	DPUSBC-T11	+03:50:27.111875	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL...
137	DNAT	DPUSBC-T11	+03:50:27.112148	< DEFER
138	DNAT	DPUSBC-T11	+03:50:27.112719	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL...
139	DNAT	DPUSBC-T11	+03:50:27.112992	< DEFER
140	DNAT	DPUSBC-T11	+03:50:27.113562	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL...

Start Time: +03:50:27.108465
Type: Native
Direction: Request
Command: Write
Address: 0x00108 (MAIN_LINK_CHANNEL_CODING_SET)
Length: 1

00108: MAIN_LINK_CHANNEL_CODING_SET

Bit	Name	Value	Description
0	8b/10b	N(0)	
1	128b/132b	Y(1)	
2		0	Reserved
3		0	Reserved
4		0	Reserved
5		0	Reserved
6		0	Reserved
7		0	Reserved

[0000] [80 01 08 00 02 -- -- --] [.....]

122: > W:108 MAIN_LINK_CHANNEL_CODING_SET L=1 02

- Source (DPTx) sets the line coding to 128b/132b by writing to register 108.
- Note:** All LTTPRs and DPRx read these register writes to set their line coding properly.

Pre-Link Training – Network Configuration – Set Link Bandwidth

ACA Data Viewer

Open Close Export Options Filter Find

[20G LTTPR_AUX_LT_FFE5] Events: 522 (996)

107	DPLT	DPUSBC-T11	+03:50:27.005464	< ACK
108	DPLT	DPUSBC-T11	+03:50:27.005531	> W:100 LINK_BW_SET L=1 02
109	DPLT	DPUSBC-T11	+03:50:27.005613	< ACK
110	DPLT	DPUSBC-T11	+03:50:27.005723	> W:101 LANE_COUNT_SET L=1 84
111	DPLT	DPUSBC-T11	+03:50:27.005805	< ACK
112	DPLT	DPUSBC-T11	+03:50:27.107033	> W:107 DOWNSPREAD_CTRL L=1 00
113	DPLT	DPUSBC-T11	+03:50:27.107115	< ACK
114	DNAT	DPUSBC-T11	+03:50:27.107256	> W:600 SINK_SET_POWER L=1 01
115	DNAT	DPUSBC-T11	+03:50:27.107338	< ACK
116	DNAT	DPUSBC-T11	+03:50:27.107410	> R:E TRAINING_AUX_RD_INTERVAL L=1
117	DNAT	DPUSBC-T11	+03:50:27.107484	< ACK 81
118	DPLT	DPUSBC-T11	+03:50:27.107612	> W:102 TRAINING_PATTERN_SET: L=1 00
119	DPLT	DPUSBC-T11	+03:50:27.107694	< ACK
120	DPLT	DPUSBC-T11	+03:50:27.107755	> R:205 SINK_STATUS L=1
121	DPLT	DPUSBC-T11	+03:50:27.107829	< ACK 03
122	DPLT	DPUSBC-T11	+03:50:27.108465	> W:108 MAIN_LINK_CHANNEL_CODING_SET L=1 02
123	DPLT	DPUSBC-T11	+03:50:27.108547	< ACK
124	DPLT	DPUSBC-T11	+03:50:27.108612	> W:100 LINK_BW_SET L=1 02
125	DPLT	DPUSBC-T11	+03:50:27.108694	< ACK
126	DPLT	DPUSBC-T11	+03:50:27.108810	> W:101 LANE_COUNT_SET L=1 84
127	DPLT	DPUSBC-T11	+03:50:27.108892	< ACK
128	DPLT	DPUSBC-T11	+03:50:27.108974	> W:102 TRAINING_PATTERN_SET: L=1 01
129	DPLT	DPUSBC-T11	+03:50:27.109255	< ACK
130	DNAT	DPUSBC-T11	+03:50:27.109329	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL...
131	DNAT	DPUSBC-T11	+03:50:27.109602	< DEFER
132	DNAT	DPUSBC-T11	+03:50:27.110168	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL...
133	DNAT	DPUSBC-T11	+03:50:27.110441	< DEFER
134	DNAT	DPUSBC-T11	+03:50:27.111015	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL...
135	DNAT	DPUSBC-T11	+03:50:27.111288	< DEFER
136	DNAT	DPUSBC-T11	+03:50:27.111875	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL...
137	DNAT	DPUSBC-T11	+03:50:27.112148	< DEFER
138	DNAT	DPUSBC-T11	+03:50:27.112719	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL...
139	DNAT	DPUSBC-T11	+03:50:27.112992	< DEFER
140	DNAT	DPUSBC-T11	+03:50:27.113562	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL...

- Source (DPTX) sets the link bandwidth by writing to register 101. In this example 20G link rate.
- Note:** All LTTPRs and DPRx read these register writes to set their link rate properly.

Pre-Link Training – Network Configuration – Set Number of Lanes

The screenshot shows the ACA Data Viewer interface. On the left, a list of network events is displayed, mostly from DPUSBC-T11, showing various control messages like 'LINK_BW_SET' and 'LANE_COUNT_SET'. A yellow arrow points from the event at index 126 to the register dump on the right. The event details for index 126 are as follows:

Start Time: +03:50:27.108810
Type: Native
Direction: Request
Command: Write
Address: 0x00101 (LANE_COUNT_SET)
Length: 1

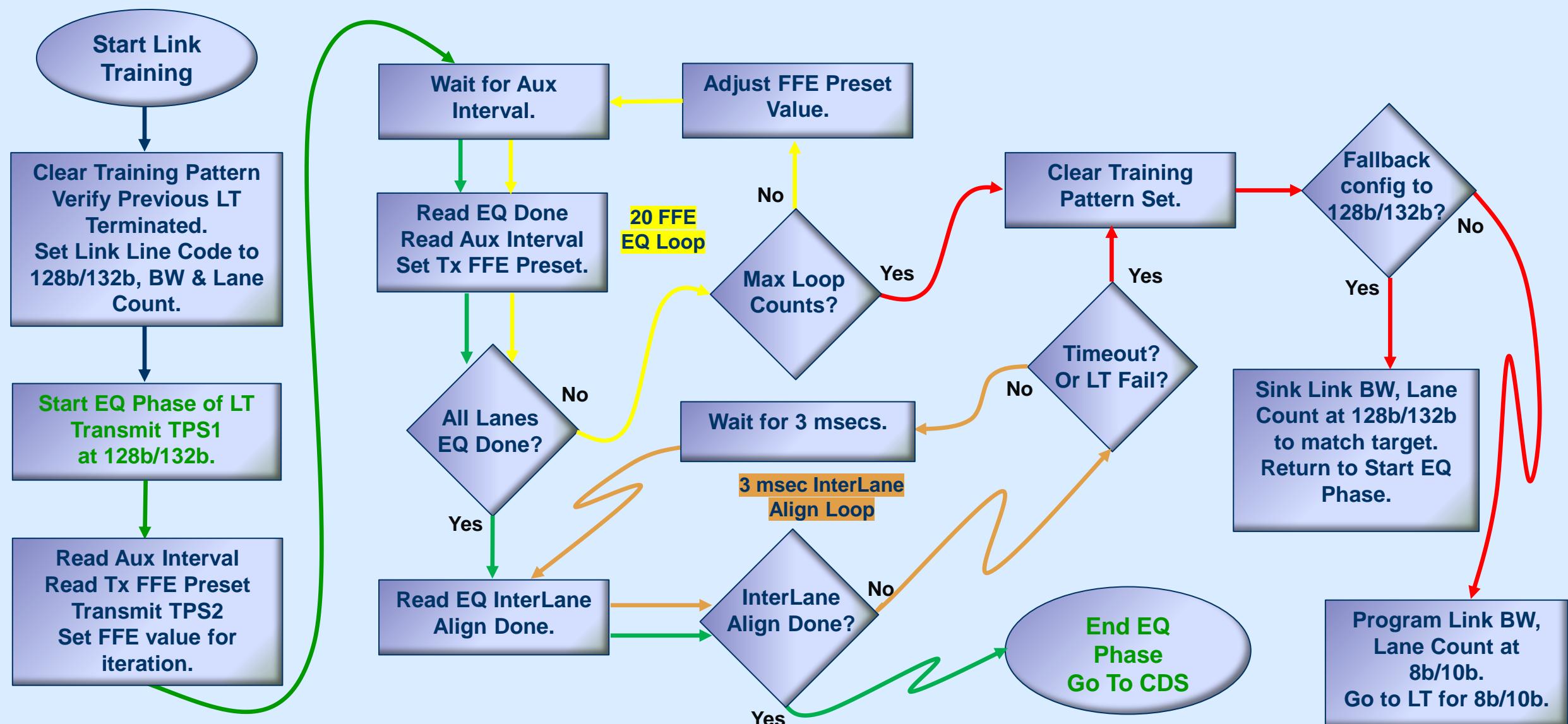
On the right, a register dump for '00101: LANE_COUNT_SET' is shown with the following bit descriptions:

Bit	Name	Value	Description
4-0	LANE_COUNT_SET	4	4 lanes
5	POST_LT_ADJ_REQ_GRANTED	N(0)	
6		0	Reserved
7	ENHANCED_FRAME_CAP	Y(1)	

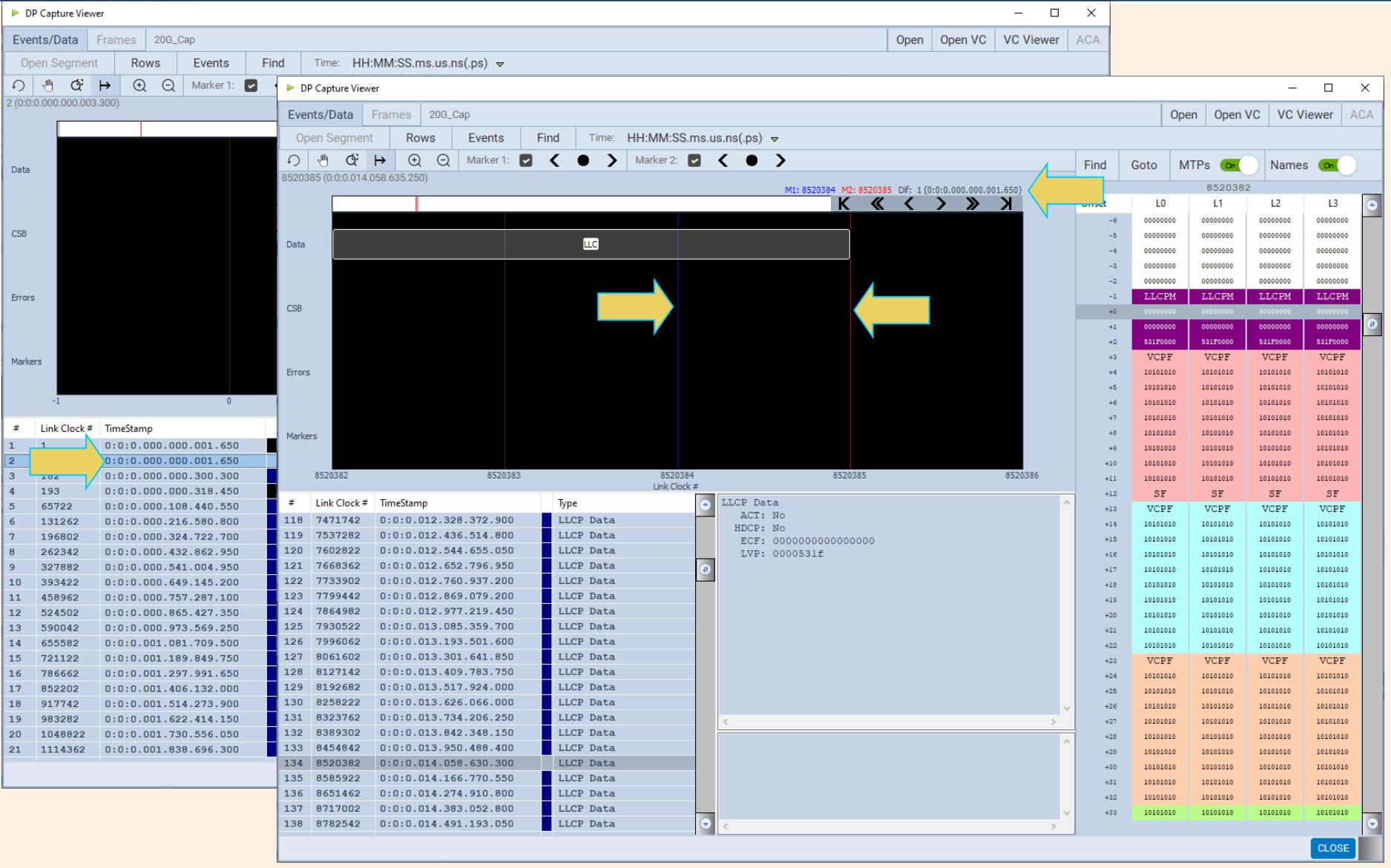
The hex value [0000][80 01 01 00 84 ---] is shown below the bit descriptions.

- Source (DPTX) setting the number of lanes to 4 by writing to register 101.
Note: All LTTPRs and DPRx read these register writes to set their number of lanes properly.
- Note:** If any LTTPR does not support 4 lanes then the network will be configured with the lower lane count.

Link Training - Equalization Phase (Simplified)



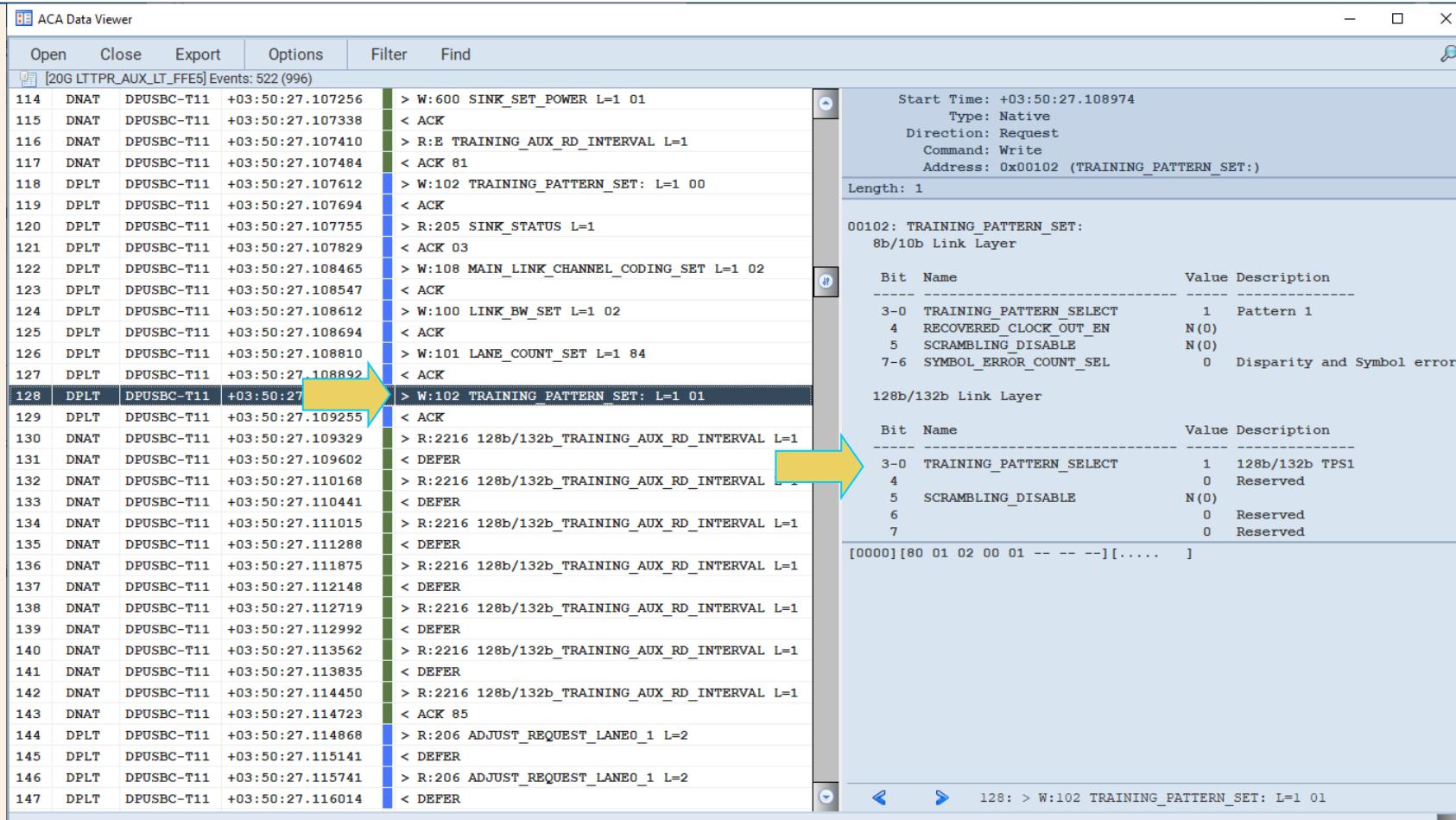
Main Link Protocols – Showing Link Symbol Rate at 20G Data Rate



- ◆ Showing 20G capture with high link symbol rate.
- ◆ Link Symbols are 1.65 nanoseconds.
- ◆ 32 bits per symbol.
- ◆ Equals 5.28×10^{-8} .
- ◆ $1 / 5.28 \times 10^{-8} = 18,939,393.93 \times 132/128 (1.03125) \approx 20G$

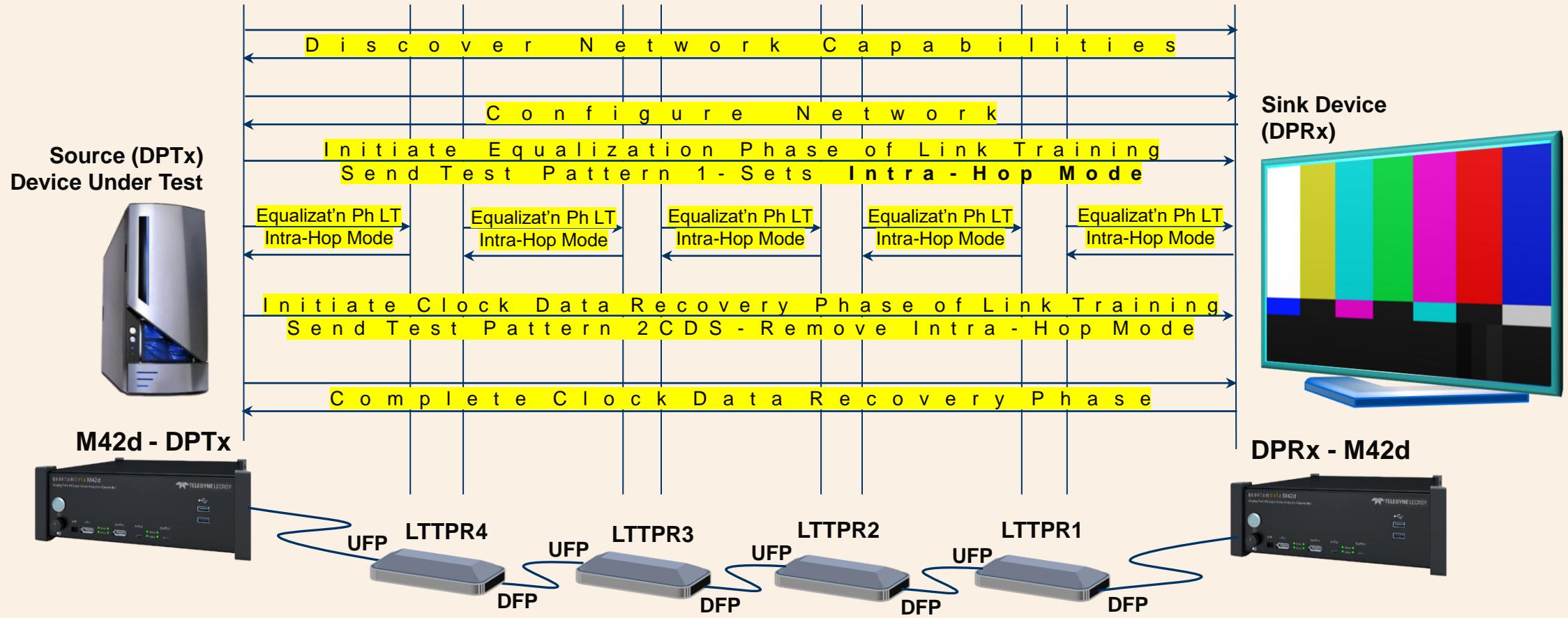
128b/132b Link Training Equalization Phase

Link Training – Start Link Training – Send Training Pattern 1



- ◆ The purpose of the new Link Training for DP 2.0 is to ensure that link training can be completed in a reasonable amount of time (650 msecs) with a network of up to eight (8) LTTPR devices.
- ◆ Source (DPTx) initiates link training by transmitting Training Pattern 1 (TPS1) for pre-charging the capacitors.
- ◆ The TPS1 is retransmitted down through the LTTPR network.
- ◆ Transmitting TPS1 puts the LTTPR devices into “Intra-Hop” Aux Transaction mode in preparation for the Equalization Phase of Link Training.
- ◆ In the Intra-Hop transaction mode, each adjacent device (LTTPR, DPTx or DPRx) conducts link training with its adjacent device(s).

128b/132b Non-Transparent Mode Link Training



Link Training – Equalization Phase – Check Read (Polling) Interval

The screenshot shows the ACA Data Viewer interface with the following details:

- Header:** ACA Data Viewer
- Menu Bar:** Open, Close, Export, Options, Filter, Find
- Toolbar:** A magnifying glass icon.
- Panel Title:** [20G LTTPR_AUX_LT_FFE5] Events: 522 (996)
- Message List:** A list of 159 messages. The first few messages are:
 - 126 DPLT DPUSBC-T11 +03:50:27.108810 > W:101 LANE_COUNT_SET L=1 84
 - 127 DPLT DPUSBC-T11 +03:50:27.108892 < ACK
 - 128 DPLT DPUSBC-T11 +03:50:27.108974 > W:102 TRAINING_PATTERN_SET: L=1 01
 - 129 DPLT DPUSBC-T11 +03:50:27.109255 < ACK
- Selected Message:** Message 143 (DPLT DPUSBC-T11 +03:50:27.114450) is selected. It has a yellow arrow pointing to its timestamp. The message details are as follows:
 - Start Time: +03:50:27.114723
 - Type: Native
 - Direction: Reply
 - Command: ACK
 - Reply to Read Request.
- Message Details:** A detailed view of the selected message shows the following:
 - 02216: 128b/132b_TRAINING_AUX_RD_INTERVAL
 - Bit Name Value Description
 - 6-0 128b/132b_TRAINING_AUX_RD_INTERVAL 5
 - 7-7 128b/132b_TRAINING_AUX_RD_INTERVAL_UNIT 1 1 msA yellow arrow points from the message list to this detailed view.
- Bottom Navigation:** Left and right arrows, page number 143, and a status message < ACK 85.

- ◆ Source (DPTx) reads setting from LTTPR or Sink (DPRx) for the “Read Interval.”
 - ◆ Read Interval determines how frequently Source (DPTx) (or downward facing port on an LTTPR) reads status (and adjusts FFE values) during the Equalization Phase.
 - ◆ Read Interval ensures Equalization Phase completes properly and within 450 msec.
 - ◆ “Unit[s]” are 1 (plus 1) in this case and setting is 6.
 - ◆ Here the Sink (DPRx) or LTTPR upward facing port is instructing the Source (DPTx) (or LTTPR downward facing port) to wait at least 6 msec before reading the status.

Link Training – Equalization Phase – Reads FFE Preset

ACA Data Viewer

Open Close Export Options Filter Find

[20G LTTPR_AUX_LT_FFE5] Events: 522 (996)

Index	Event Type	Event Description	Timestamp	
146	DPLT	DPUSBC-T11 +03:50:27.115741	> R:206 ADJUST_REQUEST_LANE0_1 L=2	+03:50:27.115741
147	DPLT	DPUSBC-T11 +03:50:27.116014	< DEFER	+03:50:27.116014
148	DPLT	DPUSBC-T11 +03:50:27.116574	> R:206 ADJUST_REQUEST_LANE0_1 L=2	+03:50:27.116574
149	DPLT	DPUSBC-T11 +03:50:27.116847	< DEFER	+03:50:27.116847
150	DPLT	DPUSBC-T11 +03:50:27.117401	> R:206 ADJUST_REQUEST_LANE0_1 L=2	+03:50:27.117401
151	DPLT	DPUSBC-T11 +03:50:27.117674	< DEFER	+03:50:27.117674
152	DPLT	DPUSBC-T11 +03:50:27.118234	> R:206 ADJUST_REQUEST_LANE0_1 L=2	+03:50:27.118234
153	DPLT	DPUSBC-T11 +03:50:27.118507	< DEFER	+03:50:27.118507
154	DPLT	DPUSBC-T11 +03:50:27.119103	> R:206 ADJUST_REQUEST_LANE0_1 L=2	+03:50:27.119103
155	DPLT	DPUSBC-T11 +03:50:27.119376	< DEFER	+03:50:27.119376
156	DPLT	DPUSBC-T11 +03:50:27.119990	> R:206 ADJUST_REQUEST_LANE0_1 L=2	+03:50:27.119990
157	DPLT	DPUSBC-T11 +03:50:27.120263	< ACK 00 00	+03:50:27.120263
158	DPLT	DPUSBC-T11 +03:50:27.120561	> W:102 TRAINING_PATTERN_SET: L=5 02 00 00 00 00	+03:50:27.120561
159	DPLT	DPUSBC-T11 +03:50:27.120675	< ACK	+03:50:27.120675
160	DPLT	DPUSBC-T11 +03:50:27.126893	> R:202 LANE0_1_STATUS: L=6	+03:50:27.126893
161	DPLT	DPUSBC-T11 +03:50:27.126967	< ACK 11 11 80 0B 11 11	+03:50:27.126967
162	DNAT	DPUSBC-T11 +03:50:27.127157	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1	+03:50:27.127157
163	DNAT	DPUSBC-T11 +03:50:27.127231	< ACK 85	+03:50:27.127231
164	DPLT	DPUSBC-T11 +03:50:27.127449	> W:103 TRAINING_LANE0_SET L=4 01 01 01 01	+03:50:27.127449
165	DPLT	DPUSBC-T11 +03:50:27.127555	< ACK	+03:50:27.127555
166	DPLT	DPUSBC-T11 +03:50:27.133713	> R:202 LANE0_1_STATUS: L=6	+03:50:27.133713
167	DPLT	DPUSBC-T11 +03:50:27.133787	< ACK 11 11 00 0B 22 22	+03:50:27.133787
168	DNAT	DPUSBC-T11 +03:50:27.133999	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1	+03:50:27.133999
169	DNAT	DPUSBC-T11 +03:50:27.134073	< ACK 85	+03:50:27.134073
170	DPLT	DPUSBC-T11 +03:50:27.134269	> W:103 TRAINING_LANE0_SET L=4 02 02 02 02	+03:50:27.134269
171	DPLT	DPUSBC-T11 +03:50:27.134375	< ACK	+03:50:27.134375
172	DPLT	DPUSBC-T11 +03:50:27.140566	> R:202 LANE0_1_STATUS: L=6	+03:50:27.140566
173	DPLT	DPUSBC-T11 +03:50:27.140640	< ACK 11 11 00 0B 33 33	+03:50:27.140640
174	DNAT	DPUSBC-T11 +03:50:27.140821	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1	+03:50:27.140821
175	DNAT	DPUSBC-T11 +03:50:27.140895	< ACK 85	+03:50:27.140895
176	DPLT	DPUSBC-T11 +03:50:27.141132	> W:103 TRAINING_LANE0_SET L=4 03 03 03 03	+03:50:27.141132
177	DPLT	DPUSBC-T11 +03:50:27.141238	< ACK	+03:50:27.141238
178	DPLT	DPUSBC-T11 +03:50:27.147468	> R:202 LANE0_1_STATUS: L=6	+03:50:27.147468
179	DPLT	DPUSBC-T11 +03:50:27.147542	< ACK 11 11 00 0B 44 44	+03:50:27.147542

Start Time: +03:50:27.120263
Type: Native
Direction: Reply
Command: ACK
Reply to Read Request.

00206: ADJUST_REQUEST_LANE0_1
8b/10b Link Layer

Bit	Name	Value	Description
1-0	VOLTAGE_SWING_LANE0	0	Level #
3-2	PRE-EMPHASIS_LANE0	0	Level #
5-4	VOLTAGE_SWING_LANE1	0	Level #
7-6	PRE-EMPHASIS_LANE1	0	Level #

128b/132b Link Layer

Bit	Name	Value	Description
3-0	TX_FFE_PRESET_VALUE_LANE0	0	
7-4	TX_FFE_PRESET_VALUE_LANE1	0	

00207: ADJUST_REQUEST_LANE2_3
8b/10b Link Layer

Bit	Name	Value	Description
1-0	VOLTAGE_SWING_LANE2	0	Level #
3-2	PRE-EMPHASIS_LANE2	0	Level #
5-4	VOLTAGE_SWING_LANE3	0	Level #
7-6	PRE-EMPHASIS_LANE3	0	Level #

128b/132b Link Layer

Bit	Name	Value	Description
3-0	TX_FFE_PRESET_VALUE_LANE2	0	
7-4	TX_FFE_PRESET_VALUE_LANE3	0	

[0000] [00 00 00 -- -- -- --] [...]

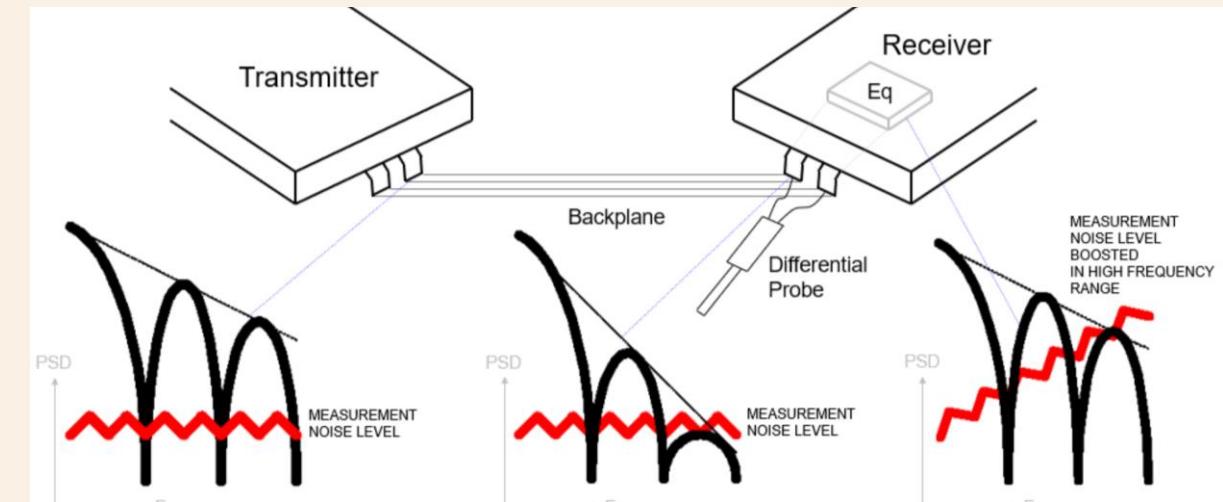
157: < ACK 00 00

- ◆ Source (DPTx) reads the FFE preset values at register 206-207 for all lanes.
 - ◆ This FFE preset value is the value a Source (DPTx) will use for Training Pattern 2 sequence.

Note: There are only 16 FFE values that can be specified throughout up to 20 loops.

What is FFE?

- Feed Forward Equalization is used for the higher DP 2.0 data rates.
- What are Feed Forward Equalizers (FFE)?
 - DisplayPort DPTx and LTTPRs use Feed Forward Equalization (FFE) when conducting link training with their adjacent nodes.
 - FFE is similar to pre-emphasis in that they apply a correction to the signal at the transmitter end.
 - FFEs can remove much of the distortion resulting from Inter-Symbol Interference (ISI).
 - FFEs invert a transmission channel's (of a cable or PCB board trace) frequency response which acts like a low pass filter.
 - FFEs modify the amplitude of transmitted bits to counter the distortion that the transmission channel exhibits. Effectively the transmission channel cancels out the pre-distortion in the FFE.



Link Training – Start Equalization Phase – Send Training Pattern 2 & Set FFE

ACA Data Viewer

Open Close Export Options Filter Find

[20G LTTPR_AUX_LT_FFE5] Events: 522 (996)

146	DPLT	DPUSBC-T11	+03:50:27.115741	> R:206 ADJUST_REQUEST_LANE0_1 L=2
147	DPLT	DPUSBC-T11	+03:50:27.116014	< DEFER
148	DPLT	DPUSBC-T11	+03:50:27.116574	> R:206 ADJUST_REQUEST_LANE0_1 L=2
149	DPLT	DPUSBC-T11	+03:50:27.116847	< DEFER
150	DPLT	DPUSBC-T11	+03:50:27.117401	> R:206 ADJUST_REQUEST_LANE0_1 L=2
151	DPLT	DPUSBC-T11	+03:50:27.117674	< DEFER
152	DPLT	DPUSBC-T11	+03:50:27.118234	> R:206 ADJUST_REQUEST_LANE0_1 L=2
153	DPLT	DPUSBC-T11	+03:50:27.118507	< DEFER
154	DPLT	DPUSBC-T11	+03:50:27.119103	> R:206 ADJUST_REQUEST_LANE0_1 L=2
155	DPLT	DPUSBC-T11	+03:50:27.119376	< DEFER
156	DPLT	DPUSBC-T11	+03:50:27.119990	> R:206 ADJUST_REQUEST_LANE0_1 L=2
157	DPLT	DPUSBC-T11	+03:50:27.120263	< ACK 00 00
158	DPLT	DPUSBC-T11	+03:50:27.120561	> W:102 TRAINING_PATTERN_SET: L=5 02 00 00 00 00
159	DPLT	DPUSBC-T11	+03:50:27.120675	< ACK
160	DPLT	DPUSBC-T11	+03:50:27.126893	> R:202 LANE0_1_STATUS: L=6
161	DPLT	DPUSBC-T11	+03:50:27.126967	< ACK 11 11 80 0B 11 11
162	DNAT	DPUSBC-T11	+03:50:27.127157	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
163	DNAT	DPUSBC-T11	+03:50:27.127231	< ACK 85
164	DPLT	DPUSBC-T11	+03:50:27.127449	> W:103 TRAINING_LANE0_SET L=4 01 01 01 01
165	DPLT	DPUSBC-T11	+03:50:27.127555	< ACK
166	DPLT	DPUSBC-T11	+03:50:27.133713	> R:202 LANE0_1_STATUS: L=6
167	DPLT	DPUSBC-T11	+03:50:27.133787	< ACK 11 11 00 0B 22 22
168	DNAT	DPUSBC-T11	+03:50:27.133999	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
169	DNAT	DPUSBC-T11	+03:50:27.134073	< ACK 85
170	DPLT	DPUSBC-T11	+03:50:27.134269	> W:103 TRAINING_LANE0_SET L=4 02 02 02 02
171	DPLT	DPUSBC-T11	+03:50:27.134375	< ACK
172	DPLT	DPUSBC-T11	+03:50:27.140566	> R:202 LANE0_1_STATUS: L=6
173	DPLT	DPUSBC-T11	+03:50:27.140640	< ACK 11 11 00 0B 33 33
174	DNAT	DPUSBC-T11	+03:50:27.140821	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
175	DNAT	DPUSBC-T11	+03:50:27.140895	< ACK 85
176	DPLT	DPUSBC-T11	+03:50:27.141132	> W:103 TRAINING_LANE0_SET L=4 03 03 03 03
177	DPLT	DPUSBC-T11	+03:50:27.141238	< ACK
178	DPLT	DPUSBC-T11	+03:50:27.147468	> R:202 LANE0_1_STATUS: L=6
179	DPLT	DPUSBC-T11	+03:50:27.147542	< ACK 11 11 00 0B 44 44



Start Time: +03:50:27.120561
Type: Native
Direction: Request
Command: Write
Address: 0x00102 (TRAINING_PATTERN_SET:)

Length: 5

00102: TRAINING_PATTERN_SET:
8b/10b Link Layer

Bit	Name	Value	Description
3-0	TRAINING_PATTERN_SELECT	2	Pattern 2
4	RECOVERED_CLOCK_OUT_EN	N(0)	
5	SCRAMBLING_DISABLE	N(0)	
7-6	SYMBOL_ERROR_COUNT_SEL	0	Disparity and Symbol error

128b/132b Link Layer

Bit	Name	Value	Description
3-0	TRAINING_PATTERN_SELECT	2	128b/132b TPS2
4	SCRAMBLING_DISABLE	N(0)	Reserved
6		0	Reserved
7		0	Reserved

00103: TRAINING_LANE0_SET
8b/10b Link Layer

Bit	Name	Value	Description
1-0	VOLTAGE_SWING_SET	0	Level #
2	MAX_SWING_REACHED	N(0)	
4-3	PRE-EMPHASIS_SET	0	Level #
5	MAX_PRE-EMPHASIS_REACHED	N(0)	
6		0	Reserved
7		0	Reserved

128b/132b Link Layer

158: > W:102 TRAINING_PATTERN_SET: L=5 02 00 00 00 00

- ◆ Source (DPTx) begins transmitting Training Pattern 2 down the LTTPR network to initiate Equalization Phase.
- ◆ Equalization Phase time budget is 450 msecs:
 - ◆ 400 msecs for upward facing side (cumulative).
 - ◆ 50 msecs for downward facing side (cumulative).
- ◆ Equalization Phase takes place concurrently within each hop:
 - ◆ DPTx-LTTPR UFP
 - ◆ LTTPR DFP-LTTPR-UFP
 - ◆ LTTPR DFP-DPRx
 - ◆ DPTx-DPRx.
- ◆ Source (DPTx) writes TPS2 and FFE values in a **single Aux write** for registers 102 to 106 (see next slide).

Link Training – Equalization Phase – Send Training Pattern 2 & Set FFE

ACA Data Viewer			
		Open	Close
		Export	Options
		Filter	Find
[20G LTTPR_AUX_LT_FFEs] Events: 522 (996)			
146	DPLT DPUSBC-T11 +03:50:27.115741	> R:206 ADJUST_REQUEST_LANE0_1 L=2	
147	DPLT DPUSBC-T11 +03:50:27.116014	< DEFER	
148	DPLT DPUSBC-T11 +03:50:27.116574	> R:206 ADJUST_REQUEST_LANE0_1 L=2	
149	DPLT DPUSBC-T11 +03:50:27.116847	< DEFER	
150	DPLT DPUSBC-T11 +03:50:27.117401	> R:206 ADJUST_REQUEST_LANE0_1 L=2	
151	DPLT DPUSBC-T11 +03:50:27.117674	< DEFER	
152	DPLT DPUSBC-T11 +03:50:27.118234	> R:206 ADJUST_REQUEST_LANE0_1 L=2	
153	DPLT DPUSBC-T11 +03:50:27.118507	< DEFER	
154	DPLT DPUSBC-T11 +03:50:27.119103	> R:206 ADJUST_REQUEST_LANE0_1 L=2	
155	DPLT DPUSBC-T11 +03:50:27.119376	< DEFER	
156	DPLT DPUSBC-T11 +03:50:27.119990	> R:206 ADJUST_REQUEST_LANE0_1 L=2	
157	DPLT DPUSBC-T11 +03:50:27.120263	< ACK 00 00	
158	DPLT DPUSBC-T11 +03:50:27.120675	> W:102 TRAINING_PATTERN_SET: L=5 02 00 00 00 00	
159	DPLT DPUSBC-T11 +03:50:27.120675	< ACK	
160	DPLT DPUSBC-T11 +03:50:27.126893	> R:202 LANE0_1_STATUS: L=6	
161	DPLT DPUSBC-T11 +03:50:27.126967	< ACK 11 11 80 0B 11 11	
162	DNAT DPUSBC-T11 +03:50:27.127157	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1	
163	DNAT DPUSBC-T11 +03:50:27.127231	< ACK 85	
164	DPLT DPUSBC-T11 +03:50:27.127449	> W:103 TRAINING_LANE0_SET L=4 01 01 01 01	
165	DPLT DPUSBC-T11 +03:50:27.127555	< ACK	
166	DPLT DPUSBC-T11 +03:50:27.133713	> R:202 LANE0_1_STATUS: L=6	
167	DPLT DPUSBC-T11 +03:50:27.133787	< ACK 11 11 00 0B 22 22	
168	DNAT DPUSBC-T11 +03:50:27.133999	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1	
169	DNAT DPUSBC-T11 +03:50:27.134073	< ACK 85	
170	DPLT DPUSBC-T11 +03:50:27.134269	> W:103 TRAINING_LANE0_SET L=4 02 02 02 02	
171	DPLT DPUSBC-T11 +03:50:27.134375	< ACK	
172	DPLT DPUSBC-T11 +03:50:27.140566	> R:202 LANE0_1_STATUS: L=6	
173	DPLT DPUSBC-T11 +03:50:27.140640	< ACK 11 11 00 0B 33 33	
174	DNAT DPUSBC-T11 +03:50:27.140821	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1	
175	DNAT DPUSBC-T11 +03:50:27.140895	< ACK 85	
176	DPLT DPUSBC-T11 +03:50:27.141132	> W:103 TRAINING_LANE0_SET L=4 03 03 03 03	
177	DPLT DPUSBC-T11 +03:50:27.141238	< ACK	
178	DPLT DPUSBC-T11 +03:50:27.147468	> R:202 LANE0_1_STATUS: L=6	
179	DPLT DPUSBC-T11 +03:50:27.147542	< ACK 11 11 00 0B 44 44	

- Source (DPTx) writes TPS2 and FFE values in a single Aux write for registers 102 to 106 (see next slide).
- Source (DPTx) iterates up to 20 times with 16 different FFE values (0-15) to achieve Equalization.

Link Training – Equalization Phase – Check Equalization Done

ACA Data Viewer

Open Close Export Options Filter Find

[20G LTTPR_AUX_LT_FFE5] Events: 522 (996)

150	DPLT	DPUSBC-T11	+03:50:27.117401	> R:206 ADJUST_REQUEST_LANE0_1 L=2
151	DPLT	DPUSBC-T11	+03:50:27.117674	< DEFER
152	DPLT	DPUSBC-T11	+03:50:27.118234	> R:206 ADJUST_REQUEST_LANE0_1 L=2
153	DPLT	DPUSBC-T11	+03:50:27.118507	< DEFER
154	DPLT	DPUSBC-T11	+03:50:27.119103	> R:206 ADJUST_REQUEST_LANE0_1 L=2
155	DPLT	DPUSBC-T11	+03:50:27.119376	< DEFER
156	DPLT	DPUSBC-T11	+03:50:27.119990	> R:206 ADJUST_REQUEST_LANE0_1 L=2
157	DPLT	DPUSBC-T11	+03:50:27.120263	< ACK 00 00
158	DPLT	DPUSBC-T11	+03:50:27.120561	> W:102 TRAINING_PATTERN_SET: L=5 02 00 00 00 00
159	DPLT	DPUSBC-T11	+03:50:27.120675	< ACK
160	DPLT	DPUSBC-T11	+03:50:27.126893	> R:202 LANE0_1_STATUS: L=6
161	DPLT	DPUSBC-T11	+03:50:27.126967	< ACK 11 11 80 0B 11 11
162	DNAT	DPUSBC-T11	+03:50:27.127157	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
163	DNAT	DPUSBC-T11	+03:50:27.127231	< ACK 85
164	DPLT	DPUSBC-T11	+03:50:27.127449	> W:103 TRAINING_LANE0_SET L=4 01 01 01 01
165	DPLT	DPUSBC-T11	+03:50:27.127555	< ACK
166	DPLT	DPUSBC-T11	+03:50:27.133713	> R:202 LANE0_1_STATUS: L=6
167	DPLT	DPUSBC-T11	+03:50:27.133787	< ACK 11 11 00 0B 22 22
168	DNAT	DPUSBC-T11	+03:50:27.133999	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
169	DNAT	DPUSBC-T11	+03:50:27.134073	< ACK 85
170	DPLT	DPUSBC-T11	+03:50:27.134269	> W:103 TRAINING_LANE0_SET L=4 02 02 02 02
171	DPLT	DPUSBC-T11	+03:50:27.134375	< ACK
172	DPLT	DPUSBC-T11	+03:50:27.140566	> R:202 LANE0_1_STATUS: L=6
173	DPLT	DPUSBC-T11	+03:50:27.140640	< ACK 11 11 00 0B 33 33
174	DNAT	DPUSBC-T11	+03:50:27.140821	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
175	DNAT	DPUSBC-T11	+03:50:27.140895	< ACK 85
176	DPLT	DPUSBC-T11	+03:50:27.141132	> W:103 TRAINING_LANE0_SET L=4 03 03 03 03
177	DPLT	DPUSBC-T11	+03:50:27.141238	< ACK
178	DPLT	DPUSBC-T11	+03:50:27.147468	> R:202 LANE0_1_STATUS: L=6
179	DPLT	DPUSBC-T11	+03:50:27.147542	< ACK 11 11 00 0B 44 44
180	DNAT	DPUSBC-T11	+03:50:27.147781	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
181	DNAT	DPUSBC-T11	+03:50:27.147855	< ACK 85
182	DPLT	DPUSBC-T11	+03:50:27.148187	> W:103 TRAINING_LANE0_SET L=4 04 04 04 04
183	DPLT	DPUSBC-T11	+03:50:27.148293	< ACK
184	DPLT	DPUSBC-T11	+03:50:27.154478	> R:202 LANE0_1_STATUS: L=6

Start Time: +03:50:27.126967
Type: Native
Direction: Reply
Command: ACK
Reply to Read Request.

00202: LANE0_1_STATUS:

Bit	Name	Value	Description
3	LANE0_CR_DONE	Y(1)	
4	LANE0_CHANNEL_EQ_DONE	N(0)	
5	LANE0_SYMBOL_LOCKED	N(0)	
6		0	Reserved
7	LANE1_CR_DONE	Y(1)	
8	LANE1_CHANNEL_EQ_DONE	N(0)	
9	LANE1_SYMBOL_LOCKED	N(0)	
10		0	Reserved

00203: LANE2_3_STATUS

Bit	Name	Value	Description
3	LANE2_CR_DONE	Y(1)	
4	LANE2_CHANNEL_EQ_DONE	N(0)	
5	LANE2_SYMBOL_LOCKED	N(0)	
6		0	Reserved
7	LANE3_CR_DONE	Y(1)	
8	LANE3_CHANNEL_EQ_DONE	N(0)	
9	LANE3_SYMBOL_LOCKED	N(0)	
10		0	Reserved

00204: LANE_ALIGN_STATUS_UPDATED

Bit	Name	Value	Description
0	INTERLANE_ALIGN_DONE	N(0)	
1	POST_LT_ADJ_REQ_IN_PROGRESS	N(0)	
2	128b/132b_DPRX_EQ_INTERLANE_ALIGN_DONE	N(0)	
3	128b/132b_DPRX_CDS_INTERLANE_ALIGN_DONE	N(0)	
4	128b/132b_LT_FAILED	N(0)	
5		0	Reserved
6	DOWNSTREAM_PORT_STATUS_CHANGED	N(0)	
7	LINK_STATUS_UPDATED	Y(1)	

161: < ACK 11 11 80 0B 11 11

- Source (DPTx) reads registers 202-206 to check if the Equalization Phase is done.
- In this example the Equalization Phase is not done (Channel EQ Done is not set).
- Note: We are watching the aux transactions between the source DPTx and the adjacent LTTPR.

LT – Equalization Phase – Check Equalization Done & Show Intra-Hop Status

ACA Data Viewer

Open Close Export Options Filter Find [20G LTTPR_AUX_LT_FFE5] Events: 522 (996)

154	DPLT	DPUSBC-T11	+03:50:27.119103	> R:206 ADJUST_REQUEST_LANE0_1 L=2
155	DPLT	DPUSBC-T11	+03:50:27.119376	< DEFER
156	DPLT	DPUSBC-T11	+03:50:27.119990	> R:206 ADJUST_REQUEST_LANE0_1 L=2
157	DPLT	DPUSBC-T11	+03:50:27.120263	< ACK 00 00
158	DPLT	DPUSBC-T11	+03:50:27.120561	> W:102 TRAINING_PATTERN_SET: L=5 02 00 00 00 00
159	DPLT	DPUSBC-T11	+03:50:27.120675	< ACK
160	DPLT	DPUSBC-T11	+03:50:27.126893	> R:202 LANE0_1_STATUS: L=6
161	DPLT	DPUSBC-T11	+03:50:27.126967	< ACK 11 11 80 0B 11 11
162	DNAT	DPUSBC-T11	+03:50:27.127157	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
163	DNAT	DPUSBC-T11	+03:50:27.127231	< ACK 85
164	DPLT	DPUSBC-T11	+03:50:27.127449	> W:103 TRAINING_LANE0_SET L=4 01 01 01 01
165	DPLT	DPUSBC-T11	+03:50:27.127555	< ACK
166	DPLT	DPUSBC-T11	+03:50:27.133713	> R:202 LANE0_1_STATUS: L=6
167	DPLT	DPUSBC-T11	+03:50:27.133787	< ACK 11 11 00 0B 22 22
168	DNAT	DPUSBC-T11	+03:50:27.133999	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
169	DNAT	DPUSBC-T11	+03:50:27.134073	< ACK 85
170	DPLT	DPUSBC-T11	+03:50:27.134269	> W:103 TRAINING_LANE0_SET L=4 02 02 02 02
171	DPLT	DPUSBC-T11	+03:50:27.134375	< ACK
172	DPLT	DPUSBC-T11	+03:50:27.140566	> R:202 LANE0_1_STATUS: L=6
173	DPLT	DPUSBC-T11	+03:50:27.140640	< ACK 11 11 00 0B 33 33
174	DNAT	DPUSBC-T11	+03:50:27.140821	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
175	DNAT	DPUSBC-T11	+03:50:27.140895	< ACK 85
176	DPLT	DPUSBC-T11	+03:50:27.141132	> W:103 TRAINING_LANE0_SET L=4 03 03 03 03
177	DPLT	DPUSBC-T11	+03:50:27.141238	< ACK
178	DPLT	DPUSBC-T11	+03:50:27.147468	> R:202 LANE0_1_STATUS: L=6
179	DPLT	DPUSBC-T11	+03:50:27.147542	< ACK 11 11 00 0B 44 44
180	DNAT	DPUSBC-T11	+03:50:27.147781	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
181	DNAT	DPUSBC-T11	+03:50:27.147855	< ACK 85
182	DPLT	DPUSBC-T11	+03:50:27.148187	> W:103 TRAINING_LANE0_SET L=4 04 04 04 04
183	DPLT	DPUSBC-T11	+03:50:27.148293	< ACK
184	DPLT	DPUSBC-T11	+03:50:27.154478	> R:202 LANE0_1_STATUS: L=6
185	DPLT	DPUSBC-T11	+03:50:27.154552	< ACK 11 11 00 0B 55 55
186	DNAT	DPUSBC-T11	+03:50:27.154752	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
187	DNAT	DPUSBC-T11	+03:50:27.154826	< ACK 85
188	DPLT	DPUSBC-T11	+03:50:27.155018	> W:103 TRAINING_LANE0_SET L=4 05 05 05 05

- ◆ **Note 1:** LTTPRs are still in the Intra-Hop Aux Transaction mode which means the reply is coming from the LTTPR device that is adjacent to the Source (DPTx).
- ◆ **Note 2:** Intra-Hop Transaction mode is exited when Clock Data Switch (CDS) Phase begins.

Link Training – Equalization Phase – Read FFE Value from Downstream

ACA Data Viewer

Open Close Export Options Filter Find

[20G_LTTPR_AUX_LT_FFE5] Events: 522 (996)

Line	Event Type	Source	Timestamp	Message
151	DPLT	DPUSBC-T11	+03:50:27.117674	< DEFER
152	DPLT	DPUSBC-T11	+03:50:27.118234	> R:206 ADJUST_REQUEST_LANE0_1 L=2
153	DPLT	DPUSBC-T11	+03:50:27.118507	< DEFER
154	DPLT	DPUSBC-T11	+03:50:27.119103	> R:206 ADJUST_REQUEST_LANE0_1 L=2
155	DPLT	DPUSBC-T11	+03:50:27.119376	< DEFER
156	DPLT	DPUSBC-T11	+03:50:27.119990	> R:206 ADJUST_REQUEST_LANE0_1 L=2
157	DPLT	DPUSBC-T11	+03:50:27.120263	< ACK 00 00
158	DPLT	DPUSBC-T11	+03:50:27.120561	> W:102 TRAINING_PATTERN_SET: L=5 02 00 00 00 00
159	DPLT	DPUSBC-T11	+03:50:27.120675	< ACK
160	DPLT	DPUSBC-T11	+03:50:27.120883	> R:202 LANE0_1_STATUS: L=6
161	DPLT	DPUSBC-T11	+03:50:27.121111	< ACK 11 11 80 0B 11 11
162	DNAT	DPUSBC-T11	+03:50:27.1217157	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
163	DNAT	DPUSBC-T11	+03:50:27.122321	< ACK 85
164	DPLT	DPUSBC-T11	+03:50:27.127449	> W:103 TRAINING_LANE0_SET L=4 01 01 01 01
165	DPLT	DPUSBC-T11	+03:50:27.127555	< ACK
166	DPLT	DPUSBC-T11	+03:50:27.133713	> R:202 LANE0_1_STATUS: L=6
167	DPLT	DPUSBC-T11	+03:50:27.133787	< ACK 11 11 00 0B 22 22
168	DNAT	DPUSBC-T11	+03:50:27.133999	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
169	DNAT	DPUSBC-T11	+03:50:27.134073	< ACK 85
170	DPLT	DPUSBC-T11	+03:50:27.134269	> W:103 TRAINING_LANE0_SET L=4 02 02 02 02
171	DPLT	DPUSBC-T11	+03:50:27.134375	< ACK
172	DPLT	DPUSBC-T11	+03:50:27.140566	> R:202 LANE0_1_STATUS: L=6
173	DPLT	DPUSBC-T11	+03:50:27.140640	< ACK 11 11 00 0B 33 33
174	DNAT	DPUSBC-T11	+03:50:27.140821	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
175	DNAT	DPUSBC-T11	+03:50:27.140895	< ACK 85
176	DPLT	DPUSBC-T11	+03:50:27.141132	> W:103 TRAINING_LANE0_SET L=4 03 03 03 03
177	DPLT	DPUSBC-T11	+03:50:27.141238	< ACK
178	DPLT	DPUSBC-T11	+03:50:27.147468	> R:202 LANE0_1_STATUS: L=6
179	DPLT	DPUSBC-T11	+03:50:27.147542	< ACK 11 11 00 0B 44 44
180	DNAT	DPUSBC-T11	+03:50:27.147781	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
181	DNAT	DPUSBC-T11	+03:50:27.147855	< ACK 85
182	DPLT	DPUSBC-T11	+03:50:27.148187	> W:103 TRAINING_LANE0_SET L=4 04 04 04 04
183	DPLT	DPUSBC-T11	+03:50:27.148293	< ACK
184	DPLT	DPUSBC-T11	+03:50:27.154478	> R:202 LANE0_1_STATUS: L=6
185	DPLT	DPUSBC-T11	+03:50:27.154552	< ACK 11 11 00 0B 55 55

00206: ADJUST_REQUEST_LANE0_1
8b/10b Link Layer

Bit	Name	Value	Description
1-0	VOLTAGE_SWING_LANE0	1	Level #
3-2	PRE-EMPHASIS_LANE0	0	Level #
5-4	VOLTAGE_SWING_LANE1	1	Level #
7-6	PRE-EMPHASIS_LANE1	0	Level #

128b/132b Link Layer

Bit	Name	Value	Description
3-0	TX_FFE_PRESET_VALUE_LANE0	1	
7-4	TX_FFE_PRESET_VALUE_LANE1	1	

00207: ADJUST_REQUEST_LANE2_3
8b/10b Link Layer

Bit	Name	Value	Description
1-0	VOLTAGE_SWING_LANE2	1	Level #
3-2	PRE-EMPHASIS_LANE2	0	Level #
5-4	VOLTAGE_SWING_LANE3	1	Level #
7-6	PRE-EMPHASIS_LANE3	0	Level #

128b/132b Link Layer

Bit	Name	Value	Description
3-0	TX_FFE_PRESET_VALUE_LANE2	1	
7-4	TX_FFE_PRESET_VALUE_LANE3	1	

[0000] [00 11 11 80 0B 11 11 --] [.....]

161: < ACK 11 11 80 0B 11 11

- ♦ Sink Equalization did not complete, the Source (DPTx) reads register 206 and 207 to determine what FFE value to use next.
- ♦ In this example the FFE value requested from the downstream device is 1.
- ♦ Note that the Source (DPTx) in this case is receiving the request for an FFE setting from the adjacent downstream UFP (upward facing port) which in this example is LTTPR 8.

Link Training – Equalization Phase – Write FFE Value

ACA Data Viewer

Open Close Export Options Filter Find

[20G LTTPR_AUX_LT_FFE5] Events: 522 (996)

151	DPLT	DPUSBC-T11	+03:50:27.117674	< DEFER
152	DPLT	DPUSBC-T11	+03:50:27.118234	> R:206 ADJUST_REQUEST_LANE0_1 L=2
153	DPLT	DPUSBC-T11	+03:50:27.118507	< DEFER
154	DPLT	DPUSBC-T11	+03:50:27.119103	> R:206 ADJUST_REQUEST_LANE0_1 L=2
155	DPLT	DPUSBC-T11	+03:50:27.119376	< DEFER
156	DPLT	DPUSBC-T11	+03:50:27.119990	> R:206 ADJUST_REQUEST_LANE0_1 L=2
157	DPLT	DPUSBC-T11	+03:50:27.120263	< ACK 00 00
158	DPLT	DPUSBC-T11	+03:50:27.120561	> W:102 TRAINING_PATTERN_SET: L=5 02 00 00 00 00
159	DPLT	DPUSBC-T11	+03:50:27.120675	< ACK
160	DPLT	DPUSBC-T11	+03:50:27.126893	> R:202 LANE0_1_STATUS: L=6
161	DPLT	DPUSBC-T11	+03:50:27.126967	< ACK 11 11 80 0B 11 11
162	DNAT	DPUSBC-T11	+03:50:27.127157	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
163	DNAT	DPUSBC-T11	+03:50:27.127231	< ACK 85
164	DPLT	DPUSBC-T11	+03:50:27.127449	> W:103 TRAINING_LANE0_SET L=4 01 01 01 01
165	DPLT	DPUSBC-T11	+03:50:27.127555	< ACK
166	DPLT	DPUSBC-T11	+03:50:27.133713	> R:202 LANE0_1_STATUS: L=6
167	DPLT	DPUSBC-T11	+03:50:27.133787	< ACK 11 11 00 0B 22 22
168	DNAT	DPUSBC-T11	+03:50:27.133999	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
169	DNAT	DPUSBC-T11	+03:50:27.134073	< ACK 85
170	DPLT	DPUSBC-T11	+03:50:27.134269	> W:103 TRAINING_LANE0_SET L=4 02 02 02 02
171	DPLT	DPUSBC-T11	+03:50:27.134375	< ACK
172	DPLT	DPUSBC-T11	+03:50:27.140566	> R:202 LANE0_1_STATUS: L=6
173	DPLT	DPUSBC-T11	+03:50:27.140640	< ACK 11 11 00 0B 33 33
174	DNAT	DPUSBC-T11	+03:50:27.140821	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
175	DNAT	DPUSBC-T11	+03:50:27.140895	< ACK 85
176	DPLT	DPUSBC-T11	+03:50:27.141132	> W:103 TRAINING_LANE0_SET L=4 03 03 03 03
177	DPLT	DPUSBC-T11	+03:50:27.141238	< ACK
178	DPLT	DPUSBC-T11	+03:50:27.147468	> R:202 LANE0_1_STATUS: L=6
179	DPLT	DPUSBC-T11	+03:50:27.147542	< ACK 11 11 00 0B 44 44
180	DNAT	DPUSBC-T11	+03:50:27.147781	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
181	DNAT	DPUSBC-T11	+03:50:27.147855	< ACK 85
182	DPLT	DPUSBC-T11	+03:50:27.148187	> W:103 TRAINING_LANE0_SET L=4 04 04 04 04
183	DPLT	DPUSBC-T11	+03:50:27.148293	< ACK
184	DPLT	DPUSBC-T11	+03:50:27.154478	> R:202 LANE0_1_STATUS: L=6
185	DPLT	DPUSBC-T11	+03:50:27.154552	< ACK 11 11 00 0B 55 55

00105: TRAINING_LANE2_SET
8b/10b Link Layer

Bit	Name	Value	Description
1-0	VOLTAGE_SWING_SET	1	Level #
2	MAX_SWING_REACHED	N(0)	
4-3	PRE-EMPHASIS_SET	0	Level #
5	MAX_PRE-EMPHASIS_REACHED	N(0)	
6		0	Reserved
7		0	Reserved

128b/132b Link Layer

Bit	Name	Value	Description
3-0	TX_FFE_PRESET_VALUE	1	
4		0	Reserved
5		0	Reserved
6		0	Reserved
7		0	Reserved

00106: TRAINING_LANE3_SET
8b/10b Link Layer

Bit	Name	Value	Description
1-0	VOLTAGE_SWING_SET	1	Level #
2	MAX_SWING_REACHED	N(0)	
4-3	PRE-EMPHASIS_SET	0	Level #
5	MAX_PRE-EMPHASIS_REACHED	N(0)	
6		0	Reserved
7		0	Reserved

128b/132b Link Layer

Bit	Name	Value	Description
164: > W:103 TRAINING_LANE0_SET L=4 01 01 01 01			

- Source (DPTx) adjusts FFE value based on the request from the downstream device.
 - In this example the FFE value is set to 1 by writing to registers 103 through 106 for Lanes 0-3.
- Note:** Not all FFE adjustment iterations will be depicted in the screen examples that follow.

Link Training – Equalization Phase - Check if Equalization Done

ACA Data Viewer

Open Close Export Options Filter Find

[20G LTTPR_AUX_LT_FFE5] Events: 522 (996)

151	DPLT	DPUSBC-T11	+03:50:27.117674	< DEFER
152	DPLT	DPUSBC-T11	+03:50:27.118234	> R:206 ADJUST_REQUEST_LANE0_1 L=2
153	DPLT	DPUSBC-T11	+03:50:27.118507	< DEFER
154	DPLT	DPUSBC-T11	+03:50:27.119103	> R:206 ADJUST_REQUEST_LANE0_1 L=2
155	DPLT	DPUSBC-T11	+03:50:27.119376	< DEFER
156	DPLT	DPUSBC-T11	+03:50:27.119990	> R:206 ADJUST_REQUEST_LANE0_1 L=2
157	DPLT	DPUSBC-T11	+03:50:27.120263	< ACK 00 00
158	DPLT	DPUSBC-T11	+03:50:27.120561	> W:102 TRAINING_PATTERN_SET: L=5 02 00 00 00 00
159	DPLT	DPUSBC-T11	+03:50:27.120675	< ACK
160	DPLT	DPUSBC-T11	+03:50:27.126893	> R:202 LANE0_1_STATUS: L=6
161	DPLT	DPUSBC-T11	+03:50:27.126967	< ACK 11 11 0B 11 11
162	DNAT	DPUSBC-T11	+03:50:27.127157	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
163	DNAT	DPUSBC-T11	+03:50:27.127231	< ACK 85
164	DPLT	DPUSBC-T11	+03:50:27.127449	> W:103 TRAINING_LANE0_SET L=4 01 01 01 01
165	DPLT	DPUSBC-T11	+03:50:27.127555	< ACK
166	DPLT	DPUSBC-T11	+03:50:27.133713	> R:202 LANE0_1_STATUS: L=6
167	DPLT	DPUSBC-T11	+03:50:27.133787	< ACK 11 11 00 0B 22 22
168	DNAT	DPUSBC-T11	+03:50:27.133999	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
169	DNAT	DPUSBC-T11	+03:50:27.134073	< ACK 85
170	DPLT	DPUSBC-T11	+03:50:27.134269	> W:103 TRAINING_LANE0_SET L=4 02 02 02 02
171	DPLT	DPUSBC-T11	+03:50:27.134375	< ACK
172	DPLT	DPUSBC-T11	+03:50:27.140566	> R:202 LANE0_1_STATUS: L=6
173	DPLT	DPUSBC-T11	+03:50:27.140640	< ACK 11 11 00 0B 33 33
174	DNAT	DPUSBC-T11	+03:50:27.140821	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
175	DNAT	DPUSBC-T11	+03:50:27.140895	< ACK 85
176	DPLT	DPUSBC-T11	+03:50:27.141132	> W:103 TRAINING_LANE0_SET L=4 03 03 03 03
177	DPLT	DPUSBC-T11	+03:50:27.141238	< ACK
178	DPLT	DPUSBC-T11	+03:50:27.147468	> R:202 LANE0_1_STATUS: L=6
179	DPLT	DPUSBC-T11	+03:50:27.147542	< ACK 11 11 00 0B 44 44
180	DNAT	DPUSBC-T11	+03:50:27.147781	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
181	DNAT	DPUSBC-T11	+03:50:27.147855	< ACK 85
182	DPLT	DPUSBC-T11	+03:50:27.148187	> W:103 TRAINING_LANE0_SET L=4 04 04 04 04
183	DPLT	DPUSBC-T11	+03:50:27.148293	< ACK
184	DPLT	DPUSBC-T11	+03:50:27.154478	> R:202 LANE0_1_STATUS: L=6
185	DPLT	DPUSBC-T11	+03:50:27.154552	< ACK 11 11 00 0B 55 55

Start Time: +03:50:27.133787
Type: Native
Direction: Reply
Command: ACK
Reply to Read Request.

00202: LANE0_1_STATUS:

Bit	Name	Value Description
0	LANE0_CR_DONE	Y(1)
1	LANE0_CHANNEL_EQ_DONE	N(0)
2	LANE0_SYMBOL_LOCKED	N(0)
3		0 Reserved
4	LANE1_CR_DONE	Y(1)
5	LANE1_CHANNEL_EQ_DONE	N(0)
6	LANE1_SYMBOL_LOCKED	N(0)
7		0 Reserved

00203: LANE2_3_STATUS

Bit	Name	Value Description
0	LANE2_CR_DONE	Y(1)
1	LANE2_CHANNEL_EQ_DONE	N(0)
2	LANE2_SYMBOL_LOCKED	N(0)
3		0 Reserved
4	LANE3_CR_DONE	Y(1)
5	LANE3_CHANNEL_EQ_DONE	N(0)
6	LANE3_SYMBOL_LOCKED	N(0)
7		0 Reserved

00204: LANE_ALIGN_STATUS_UPDATED

Bit	Name	Value Description
0	INTERLANE_ALIGN_DONE	N(0)
1	POST_LT_ADJ_REQ_IN_PROGRESS	N(0)
2	128b/132b_DPRX_EQ_INTERLANE_ALIGN_DONE	N(0)
3	128b/132b_DPRX_CDS_INTERLANE_ALIGN_DONE	N(0)
4	128b/132b_LT_FAILED	N(0)
5		0 Reserved
6	DOWNSTREAM_PORT_STATUS_CHANGED	N(0)
7	LINK_STATUS_UPDATED	N(0)

167: < ACK 11 11 00 0B 22 22

- Source (DPTx) again reads register 202 and 203 to check if Equalization Phase is done.
- In this example Channel Equalization is still not done so more adjustments to FFE will be made as depicted in the examples in the following slides.
- We continue iterating through that FFE 20 setting loop.

Link Training – Equalization Phase – Read FFE Value from Downstream

ACU Data Viewer						
			Open	Close	Export	Options
			Filter	Find		
[20G_LTTPR_AUX_LT_FFE5] Events: 522 (996)						
162	DNAT	DPUSBC-T11	+03:50:27.127157	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1		
163	DNAT	DPUSBC-T11	+03:50:27.127231	< ACK 85		
164	DPLT	DPUSBC-T11	+03:50:27.127449	> W:103 TRAINING_LANE0_SET L=4 01 01 01 01		
165	DPLT	DPUSBC-T11	+03:50:27.127555	< ACK		
166	DPLT	DPUSBC-T11	+03:50:27.133713	> R:202 LANE0_1_STATUS: L=6		
167	DPLT	DPUSBC-T11	+03:50:27.133787	< ACK 11 11 00 OB 22 22		
168	DNAT	DPUSBC-T11	+03:50:27.133999	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1		
169	DNAT	DPUSBC-T11	+03:50:27.134073	< ACK 85		
170	DPLT	DPUSBC-T11	+03:50:27.134269	> W:103 TRAINING_LANE0_SET L=4 02 02 02 02		
171	DPLT	DPUSBC-T11	+03:50:27.134375	< ACK		
172	DPLT	DPUSBC-T11	+03:50:27.140566	> R:202 LANE0_1_STATUS: L=6		
173	DPLT	DPUSBC-T11	+03:50:27.140640	< ACK 11 11 00 OB 33 33		
174	DNAT	DPUSBC-T11	+03:50:27.140821	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1		
175	DNAT	DPUSBC-T11	+03:50:27.140895	< ACK 85		
176	DPLT	DPUSBC-T11	+03:50:27.141132	> W:103 TRAINING_LANE0_SET L=4 03 03 03 03		
177	DPLT	DPUSBC-T11	+03:50:27.141238	< ACK		
178	DPLT	DPUSBC-T11	+03:50:27.147468	> R:202 LANE0_1_STATUS: L=6		
179	DPLT	DPUSBC-T11	+03:50:27.147542	< ACK 11 11 00 OB 44 44		
180	DNAT	DPUSBC-T11	+03:50:27.147781	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1		
181	DNAT	DPUSBC-T11	+03:50:27.147855	< ACK 85		
182	DPLT	DPUSBC-T11	+03:50:27.148187	> W:103 TRAINING_LANE0_SET L=4 04 04 04 04		
183	DPLT	DPUSBC-T11	+03:50:27.148293	< ACK		
184	DPLT	DPUSBC-T11	+03:50:27.154478	> R:202 LANE0_1_STATUS: L=6		
185	DPLT	DPUSBC-T11	+03:50:27.15	< ACK 11 11 00 OB 55 55		
186	DNAT	DPUSBC-T11	+03:50:27.154752	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1		
187	DNAT	DPUSBC-T11	+03:50:27.154826	< ACK 85		
188	DPLT	DPUSBC-T11	+03:50:27.155018	> W:103 TRAINING_LANE0_SET L=4 05 05 05 05		
189	DPLT	DPUSBC-T11	+03:50:27.155124	< ACK		
190	DPLT	DPUSBC-T11	+03:50:27.161274	> R:202 LANE0_1_STATUS: L=6		
191	DPLT	DPUSBC-T11	+03:50:27.161348	< ACK 77 77 85 OB 66 66		
192	DNAT	DPUSBC-T11	+03:50:27.161548	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1		
193	DNAT	DPUSBC-T11	+03:50:27.161622	< ACK 85		
194	DPLT	DPUSBC-T11	+03:50:27.161744	> R:202 LANE0_1_STATUS: L=4		
195	DPLT	DPUSBC-T11	+03:50:27.161818	< ACK 77 77 05 OB		
196	DNAT	DPUSBC-T11	+03:50:27.161922	> R:F0008 EQ done per LTTPR L=1		

- ◆ Because Equalization Phase was not completed, the sink (DPRx) requests a new FFE value.
- ◆ Source (DPTx) again reads registers 206 and 207 to determine what FFE value to use.
- ◆ In this example the FFE value requested from the downstream device is 5. **Note:** It is possible that the lanes could specify different values for FFE or some lanes could complete Equalization sooner than others and not specify a new value of FFE.

Link Training – Equalization Phase – Write FFE Value

ACA Data Viewer

Open Close Export Options Filter Find [20G_LTTPR_AUX_LT_FFE5] Events: 522 (996)

162	DNAT	DPUSBC-T11	+03:50:27.127157	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
163	DNAT	DPUSBC-T11	+03:50:27.127231	< ACK 85
164	DPLT	DPUSBC-T11	+03:50:27.127449	> W:103 TRAINING_LANE0_SET L=4 01 01 01 01
165	DPLT	DPUSBC-T11	+03:50:27.127555	< ACK
166	DPLT	DPUSBC-T11	+03:50:27.133713	> R:202 LANE0_1_STATUS: L=6
167	DPLT	DPUSBC-T11	+03:50:27.133787	< ACK 11 11 00 0B 22 22
168	DNAT	DPUSBC-T11	+03:50:27.133999	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
169	DNAT	DPUSBC-T11	+03:50:27.134073	< ACK 85
170	DPLT	DPUSBC-T11	+03:50:27.134269	> W:103 TRAINING_LANE0_SET L=4 02 02 02 02
171	DPLT	DPUSBC-T11	+03:50:27.134375	< ACK
172	DPLT	DPUSBC-T11	+03:50:27.140566	> R:202 LANE0_1_STATUS: L=6
173	DPLT	DPUSBC-T11	+03:50:27.140640	< ACK 11 11 00 0B 33 33
174	DNAT	DPUSBC-T11	+03:50:27.140821	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
175	DNAT	DPUSBC-T11	+03:50:27.140895	< ACK 85
176	DPLT	DPUSBC-T11	+03:50:27.141132	> W:103 TRAINING_LANE0_SET L=4 03 03 03 03
177	DPLT	DPUSBC-T11	+03:50:27.141238	< ACK
178	DPLT	DPUSBC-T11	+03:50:27.147468	> R:202 LANE0_1_STATUS: L=6
179	DPLT	DPUSBC-T11	+03:50:27.147542	< ACK 11 11 00 0B 44 44
180	DNAT	DPUSBC-T11	+03:50:27.147781	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
181	DNAT	DPUSBC-T11	+03:50:27.147855	< ACK 85
182	DPLT	DPUSBC-T11	+03:50:27.148187	> W:103 TRAINING_LANE0_SET L=4 04 04 04 04
183	DPLT	DPUSBC-T11	+03:50:27.148293	< ACK
184	DPLT	DPUSBC-T11	+03:50:27.154478	> R:202 LANE0_1_STATUS: L=6
185	DPLT	DPUSBC-T11	+03:50:27.154552	< ACK 11 11 00 0B 55 55
186	DNAT	DPUSBC-T11	+03:50:27.154752	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
187	DNAT	DPUSBC-T11	+03:50:27.154826	< ACK 85
188	DPLT	DPUSBC-T11	+03:50:27.155124	> W:103 TRAINING_LANE0_SET L=4 05 05 05 05
189	DPLT	DPUSBC-T11	+03:50:27.155124	< ACK
190	DPLT	DPUSBC-T11	+03:50:27.161274	> R:202 LANE0_1_STATUS: L=6
191	DPLT	DPUSBC-T11	+03:50:27.161348	< ACK 77 77 85 0B 66 66
192	DNAT	DPUSBC-T11	+03:50:27.161548	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
193	DNAT	DPUSBC-T11	+03:50:27.161622	< ACK 85
194	DPLT	DPUSBC-T11	+03:50:27.161744	> R:202 LANE0_1_STATUS: L=4
195	DPLT	DPUSBC-T11	+03:50:27.161818	< ACK 77 77 05 0B
196	DNAT	DPUSBC-T11	+03:50:27.161922	> R:F0008 EQ done per LTTPR L=1

- The Source (DPTx) adjusts the FFE value to 5 by writing to registers 103 through 106 for Lanes 0-3.
- In this example the FFE value is set to 5 as shown in accordance with the request from the downstream device.

Link Training – Equalization Phase - Check Equal'n Inter-Lane Align Done

ACA Data Viewer

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[20G_LTTPR_AUX_LT_FFE5] Events: 522 (996)

173	DPLT	DPUSBC-T11	+03:50:27.140640	< ACK 11 11 00 0B 33 33
174	DNAT	DPUSBC-T11	+03:50:27.140821	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
175	DNAT	DPUSBC-T11	+03:50:27.140895	< ACK 85
176	DPLT	DPUSBC-T11	+03:50:27.141132	> W:103 TRAINING_LANE0_SET L=4 03 03 03 03
177	DPLT	DPUSBC-T11	+03:50:27.141238	< ACK
178	DPLT	DPUSBC-T11	+03:50:27.147468	> R:202 LANE0_1_STATUS: L=6
179	DPLT	DPUSBC-T11	+03:50:27.147542	< ACK 11 11 00 0B 44 44
180	DNAT	DPUSBC-T11	+03:50:27.147781	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
181	DNAT	DPUSBC-T11	+03:50:27.147855	< ACK 85
182	DPLT	DPUSBC-T11	+03:50:27.148187	> W:103 TRAINING_LANE0_SET L=4 04 04 04 04
183	DPLT	DPUSBC-T11	+03:50:27.148293	< ACK
184	DPLT	DPUSBC-T11	+03:50:27.154478	> R:202 LANE0_1_STATUS: L=6
185	DPLT	DPUSBC-T11	+03:50:27.154552	< ACK 11 11 00 0B 55 55
186	DNAT	DPUSBC-T11	+03:50:27.154752	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
187	DNAT	DPUSBC-T11	+03:50:27.154826	< ACK 85
188	DPLT	DPUSBC-T11	+03:50:27.155018	> W:103 TRAINING_LANE0_SET L=4 05 05 05 05
189	DPLT	DPUSBC-T11	+03:50:27.155124	< ACK
190	DPLT	DPUSBC-T11	+03:50:27.161274	> R:202 LANE0_1_STATUS: L=6
191	DPLT	DPUSBC-T11	+03:50:27.161348	< ACK 77 77 85 0B 66 66
192	DNAT	DPUSBC-T11	+03:50:27.161548	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
193	DNAT	DPUSBC-T11	+03:50:27.161622	< ACK 85
194	DPLT	DPUSBC-T11	+03:50:27.161744	> R:202 LANE0_1_STATUS: L=4
195	DPLT	DPUSBC-T11	+03:50:27.161818	< ACK 77 77 05 0B
196	DNAT	DPUSBC-T11	+03:50:27.161922	> R:F0008 EQ done per LTTPR L=1
197	DNAT	DPUSBC-T11	+03:50:27.161996	< ACK FF
198	DPLT	DPUSBC-T11	+03:50:27.162127	> W:102 TRAINING_PATTERN_SET: L=1 03
199	DPLT	DPUSBC-T11	+03:50:27.162209	< ACK
200	DPLT	DPUSBC-T11	+03:50:27.163378	> R:202 LANE0_1_STATUS: L=4
201	DPLT	DPUSBC-T11	+03:50:27.163452	< ACK 77 77 85 03
202	DPLT	DPUSBC-T11	+03:50:27.164715	> R:202 LANE0_1_STATUS: L=4
203	DPLT	DPUSBC-T11	+03:50:27.164789	< ACK 77 77 05 03
204	DPLT	DPUSBC-T11	+03:50:27.166083	> R:202 LANE0_1_STATUS: L=4
205	DPLT	DPUSBC-T11	+03:50:27.166157	< ACK 77 77 05 03
206	DPLT	DPUSBC-T11	+03:50:27.167481	> R:202 LANE0_1_STATUS: L=4
207	DPLT	DPUSBC-T11	+03:50:27.167555	< ACK 77 77 0D 03

Start Time: +03:50:27.161348
Type: Native
Direction: Reply
Command: ACK
Reply to Read Request.

00202: LANE0_1_STATUS:

Bit	Name	Value	Description
0	LANE0_CR_DONE	Y(1)	
1	LANE0_CHANNEL_EQ_DONE	Y(1)	
2	LANE0_SYMBOL_LOCKED	Y(1)	
3		0	Reserved
4	LANE1_CR_DONE	Y(1)	
5	LANE1_CHANNEL_EQ_DONE	Y(1)	
6	LANE1_SYMBOL_LOCKED	Y(1)	
7		0	Reserved

00203: LANE2_3_STATUS

Bit	Name	Value	Description
0	LANE2_CR_DONE	Y(1)	
1	LANE2_CHANNEL_EQ_DONE	Y(1)	
2	LANE2_SYMBOL_LOCKED	Y(1)	
3		0	Reserved
4	LANE3_CR_DONE	Y(1)	
5	LANE3_CHANNEL_EQ_DONE	Y(1)	
6	LANE3_SYMBOL_LOCKED	Y(1)	
7		0	Reserved

00204: LANE_ALIGN_STATUS_UPDATED

Bit	Name	Value	Description
0	INTERLANE_ALIGN_DONE	Y(1)	
1	POST_LT_ADJ_REQ_IN_PROGRESS	N(0)	
2	128b/132b_DPRX_EQ_INTERLANE_ALIGN_DONE	Y(1)	
3	128b/132b_DPRX_CDS_INTERLANE_ALIGN_DONE	N(0)	
4	128b/132b_LT_FAILED	N(0)	
5		0	Reserved
6	DOWNSTREAM_PORT_STATUS_CHANGED	N(0)	
7	LINK_STATUS_UPDATED	Y(1)	

191: < ACK 77 77 85 0B 66 66

- Source (DPTx) again reads registers 202-205 to check if Channel Equalization is done.

- In this example Channel Equalization is done on all four (4) lanes.

- Equalization Inter-Lane align is also successfully completed.

Note: Sometimes Channel Equalization is completed but Inter-Lane alignment is not done. In that case there is no need to continue adjusting FFE preset values. The Source (DPTx) will continue to read registers 202-205 only for Equalization Inter-Lane alignment done status.

Link Training – Equalization Phase - Check Equalization Done for LTTPRs

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[20G_LTTPR_AUX_LT_non_transparent] Events: 492 (936)

Line Number	Source	Destination	Time	Message
158	DPLT	DPUSBC-T11	+00:49:01.668881	> W:102 TRAINING_PATTERN_SET: L=5 02 00 00 00 00 00
159	DPLT	DPUSBC-T11	+00:49:01.668995	< ACK
160	DPLT	DPUSBC-T11	+00:49:01.675161	> R:202 LANE0_1_STATUS: L=6
161	DPLT	DPUSBC-T11	+00:49:01.675235	< ACK 77 77 85 0B 11 11
162	DNAT	DPUSBC-T11	+00:49:01.675415	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
163	DNAT	DPUSBC-T11	+00:49:01.675489	< ACK 85
164	DPLT	DPUSBC-T11	+00:49:01.675624	> R:202 LANE0_1_STATUS: L=4
165	DPLT	DPUSBC-T11	+00:49:01.675698	< ACK 77 77 05 0B
166	DNAT	DPUSBC-T11	+00:49:01.675802	> R:F0008 EQ done per LTTPR L=1
167	DNAT	DPUSBC-T11	+00:49:01.676123	< ACK FF
168	DPLT	DPUSBC-T11	+00:49:01.676123	> W:102 TRAINING_PATTERN_SET: L=1 03
169	DPLT	DPUSBC-T11	+00:49:01.676205	< ACK
170	DPLT	DPUSBC-T11	+00:49:01.677386	> R:202 LANE0_1_STATUS: L=4
171	DPLT	DPUSBC-T11	+00:49:01.677460	< ACK 77 77 85 03
172	DPLT	DPUSBC-T11	+00:49:01.678750	> R:202 LANE0_1_STATUS: L=4
173	DPLT	DPUSBC-T11	+00:49:01.678824	< ACK 77 77 05 03
174	DPLT	DPUSBC-T11	+00:49:01.680097	> R:202 LANE0_1_STATUS: L=4
175	DPLT	DPUSBC-T11	+00:49:01.680171	< ACK 77 77 05 03
176	DPLT	DPUSBC-T11	+00:49:01.681425	> R:202 LANE0_1_STATUS: L=4
177	DPLT	DPUSBC-T11	+00:49:01.681499	< ACK 77 77 0D 03
178	DPLT	DPUSBC-T11	+00:49:01.681705	> W:102 TRAINING_PATTERN_SET: L=1 00
179	DPLT	DPUSBC-T11	+00:49:01.681787	< ACK
180	DNAT	DPUSBC-T11	+00:49:01.681870	> R:200 SINK_COUNT L=6
181	DNAT	DPUSBC-T11	+00:49:01.681945	< ACK 41 00 77 77 0D 02
182	DPLT	DPUSBC-T11	+00:49:01.682232	> R:100 LINK_BW_SET L=9
183	DPLT	DPUSBC-T11	+00:49:01.682307	< ACK 02 84 00 00 00 00 00 00 02
184	DNAT	DPUSBC-T11	+00:49:01.682484	> R:200 SINK_COUNT L=8
185	DNAT	DPUSBC-T11	+00:49:01.682559	< ACK 41 00 77 77 0D 02 11 11
186	DPLT	DPUSBC-T11	+00:49:01.684486	> R:100 LINK_BW_SET L=9
187	DPLT	DPUSBC-T11	+00:49:01.684561	< ACK 02 84 00 00 00 00 00 00 02
188	DPLT	DPUSBC-T11	+00:49:01.688715	> R:100 LINK_BW_SET L=9
189	DPLT	DPUSBC-T11	+00:49:01.688790	< ACK 02 84 00 00 00 00 00 00 02
190	DPLT	DPUSBC-T11	+00:49:02.154440	> R:100 LINK_BW_SET L=9

Start Time: +00:49:01.675876
Type: Native
Direction: Reply
Command: ACK
Reply to Read Request.

F0008: EQ done per LTTPR

Bit	Name	Value Description
0	LTTPR1 DFP EQ Done	Y(1)
1	LTTPR2 DFP EQ Done	Y(1)
2	LTTPR3 DFP EQ Done	Y(1)
3	LTTPR4 DFP EQ Done	Y(1)
4	LTTPR5 DFP EQ Done	Y(1)
5	LTTPR6 DFP EQ Done	Y(1)
6	LTTPR7 DFP EQ Done	Y(1)
7	LTTPR8 DFP EQ Done	Y(1)

[0000] [00 FF -- -- -- -- -- --] [...]

167: < ACK FF

- After the Source (DPTx) determines that the channels are equalized, it then verifies that the LTTPR devices downstream have also completed the Equalization Phase by reading register F0008.
- In this example all eight (8) LTTPRs have completed Equalization.

Link Training – Equalization Phase - Time Duration of Equalization Phase

ACA Data Viewer

Open Close Export Options Filter Find

[20G LTTPR_AUX_LT_FFE5] Events: 522 (996)

Event ID	Device	Timestamp	Message	
151	DPLT	DPUSBC-T11	-00:00:00.002887	< DEFER
152	DPLT	DPUSBC-T11	-00:00:00.002327	> R:206 ADJUST_REQUEST_LANE0_1 L=2
153	DPLT	DPUSBC-T11	-00:00:00.002054	< DEFER
154	DPLT	DPUSBC-T11	-00:00:00.001458	> R:206 ADJUST_REQUEST_LANE0_1 L=2
155	DPLT	DPUSBC-T11	-00:00:00.001185	< DEFER
156	DPLT	DPUSBC-T11	-00:00:00.000571	> R:206 ADJUST_REQUEST_LANE0_1 L=2
157	DPLT	DPUSBC-T11	-00:00:00.000298	< ACK 00 00
158	DPLT	DPUSBC-T11	+00:00:00.000000	> W:102 TRAINING_PATTERN_SET: L=5 02 00 00 00 00 00
159	DPLT	DPUSBC-T11	+00:00:00.000114	< ACK
160	DPLT	DPUSBC-T11	+00:00:00.006332	> R:202 LANE0_1_STATUS: L=6
161	DPLT	DPUSBC-T11	+00:00:00.006406	< ACK 11 11 80 0B 11 11
162	DNAT	DPUSBC-T11	+00:00:00.006596	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
163	DNAT	DPUSBC-T11	+00:00:00.006670	< ACK 85
164	DPLT	DPUSBC-T11	+00:00:00.006888	> W:103 TRAINING_LANE0_SET L=4 01 01 01 01
165	DPLT	DPUSBC-T11	+00:00:00.006994	< ACK
166	DPLT	DPUSBC-T11	+00:00:00.013152	> R:202 LANE0_1_STATUS: L=6
167	DPLT	DPUSBC-T11	+00:00:00.013226	< ACK 11 11 00 0B 22 22
168	DNAT	DPUSBC-T11	+00:00:00.013438	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
169	DNAT	DPUSBC-T11	+00:00:00.013512	< ACK 85
170	DPLT	DPUSBC-T11	+00:00:00.013708	> W:103 TRAINING_LANE0_SET L=4 02 02 02 02
171	DPLT	DPUSBC-T11	+00:00:00.013814	< ACK
172	DPLT	DPUSBC-T11	+00:00:00.020005	> R:202 LANE0_1_STATUS: L=6
173	DPLT	DPUSBC-T11	+00:00:00.020079	< ACK 11 11 00 0B 33 33
174	DNAT	DPUSBC-T11	+00:00:00.020260	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
175	DNAT	DPUSBC-T11	+00:00:00.020334	< ACK 85
176	DPLT	DPUSBC-T11	+00:00:00.020571	> W:103 TRAINING_LANE0_SET L=4 03 03 03 03
177	DPLT	DPUSBC-T11	+00:00:00.020677	< ACK
178	DPLT	DPUSBC-T11	+00:00:00.026907	> R:202 LANE0_1_STATUS: L=6
179	DPLT	DPUSBC-T11	+00:00:00.026981	< ACK 11 11 00 0B 44 44
180	DNAT	DPUSBC-T11	+00:00:00.027220	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
181	DNAT	DPUSBC-T11	+00:00:00.027294	< ACK 85
182	DPLT	DPUSBC-T11	+00:00:00.027626	> W:103 TRAINING_LANE0_SET L=4 04 04 04 04
183	DPLT	DPUSBC-T11	+00:00:00.027732	< ACK
184	DPLT	DPUSBC-T11	+00:00:00.033917	> R:202 LANE0_1_STATUS: L=6
185	DPLT	DPUSBC-T11	+00:00:00.033991	< ACK 11 11 00 0B 55 55

Start Time: +03:50:27.120561
Type: Native
Direction: Request
Command: Write
Address: 0x00102 (TRAINING_PATTERN_SET:)
Length: 5

00102: TRAINING_PATTERN_SET:
8b/10b Link Layer

Bit	Name	Value	Description
3-0	TRAINING_PATTERN_SELECT	2	Pattern 2
4	RECOVERED_CLOCK_OUT_EN	N(0)	
5	SCRAMBLING_DISABLE	N(0)	
7-6	SYMBOL_ERROR_COUNT_SEL	0	Disparity and Symbol

128b/132b Link Layer

Bit	Name	Value	Description
3-0	TRAINING_PATTERN_SELECT	2	128b/132b TPS2
4	RECOVERED_CLOCK_OUT_EN	0	Reserved
5	SCRAMBLING_DISABLE	N(0)	
6	RESERVED	0	Reserved
7	RESERVED	0	Reserved

00103: TRAINING_LANE0_SET
8b/10b Link Layer

Bit	Name	Value	Description
1-0	VOLTAGE_SWING_SET	0	Level #
2	MAX_SWING_REACHED	N(0)	
4-3	PRE-EMPHASIS_SET	0	Level #
5	MAX_PRE-EMPHASIS_REACHED	N(0)	
6	RESERVED	0	Reserved
7	RESERVED	0	Reserved

128b/132b Link Layer

158: > W:102 TRAINING_PATTERN_SET: L=5 02 00 00 00 00 00

- ◆ Equalization Phase needs to complete in 450 msec. Each hop has 400 msec to complete.
- ◆ The devices in each and all hops conduct Equalization concurrently.
- ◆ Elapsed time is depicted in the screen examples (here and next slide).
- ◆ Example shows the baseline time reset to zero at the beginning of link training when Training Pattern 2 is transmitted.
- ◆ Equalization Phase concludes when the downstream network of LTTPR devices and the sink (DPRx) reports that the Equalization Phase is completed (next slide).

Link Training – Equalization Phase - Time Duration of Equalization Phase

ACA Data Viewer

Open Close Export Options Filter Find

[20G LTTPR_AUX_LT_FFE5] Events: 522 (996)

168	DNAT	DPUSBC-T11	+00:00:00.013438	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
169	DNAT	DPUSBC-T11	+00:00:00.013512	< ACK 85
170	DPLT	DPUSBC-T11	+00:00:00.013708	> W:103 TRAINING_LANE0_SET L=4 02 02 02 02
171	DPLT	DPUSBC-T11	+00:00:00.013814	< ACK
172	DPLT	DPUSBC-T11	+00:00:00.020005	> R:202 LANE0_1_STATUS: L=6
173	DPLT	DPUSBC-T11	+00:00:00.020079	< ACK 11 11 00 0B 33 33
174	DNAT	DPUSBC-T11	+00:00:00.020260	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
175	DNAT	DPUSBC-T11	+00:00:00.020334	< ACK 85
176	DPLT	DPUSBC-T11	+00:00:00.020571	> W:103 TRAINING_LANE0_SET L=4 03 03 03 03
177	DPLT	DPUSBC-T11	+00:00:00.020677	< ACK
178	DPLT	DPUSBC-T11	+00:00:00.026907	> R:202 LANE0_1_STATUS: L=6
179	DPLT	DPUSBC-T11	+00:00:00.026981	< ACK 11 11 00 0B 44 44
180	DNAT	DPUSBC-T11	+00:00:00.027220	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
181	DNAT	DPUSBC-T11	+00:00:00.027294	< ACK 85
182	DPLT	DPUSBC-T11	+00:00:00.027626	> W:103 TRAINING_LANE0_SET L=4 04 04 04 04
183	DPLT	DPUSBC-T11	+00:00:00.027732	< ACK
184	DPLT	DPUSBC-T11	+00:00:00.033917	> R:202 LANE0_1_STATUS: L=6
185	DPLT	DPUSBC-T11	+00:00:00.033991	< ACK 11 11 00 0B 55 55
186	DNAT	DPUSBC-T11	+00:00:00.034191	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
187	DNAT	DPUSBC-T11	+00:00:00.034265	< ACK 85
188	DPLT	DPUSBC-T11	+00:00:00.034457	> W:103 TRAINING_LANE0_SET L=4 05 05 05 05
189	DPLT	DPUSBC-T11	+00:00:00.034563	< ACK
190	DPLT	DPUSBC-T11	+00:00:00.040713	> R:202 LANE0_1_STATUS: L=6
191	DPLT	DPUSBC-T11	+00:00:00.040787	< ACK 77 77 85 0B 66 66
192	DNAT	DPUSBC-T11	+00:00:00.040987	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
193	DNAT	DPUSBC-T11	+00:00:00.041061	< ACK 85
194	DPLT	DPUSBC-T11	+00:00:00.041183	> R:202 LANE0_1_STATUS: L=4
195	DPLT	DPUSBC-T11	+00:00:00.041257	< ACK 77 77 05 0B
196	DNAT	DPUSBC-T11	+00:00:00.041361	> R:F0008 EQ done per LTTPR L=1
197	DNAT	DPUSBC-T11	+00:00:00.041435	< ACK FF
198	DPLT	DPUSBC-T11	+00:00:00.041566	> W:102 TRAINING_PATTERN_SET: L=1 03
199	DPLT	DPUSBC-T11	+00:00:00.041648	< ACK
200	DPLT	DPUSBC-T11	+00:00:00.042817	> R:202 LANE0_1_STATUS: L=4
201	DPLT	DPUSBC-T11	+00:00:00.042891	< ACK 77 77 85 03
202	DPLT	DPUSBC-T11	+00:00:00.044154	> R:202 LANE0_1_STATUS: L=4

Start Time: +00:00:00.040787
Type: Native
Direction: Reply
Command: ACK
Reply to Read Request.

00202: LANE0_1_STATUS:

Bit	Name	Value Description
0	LANE0_CR_DONE	Y(1)
1	LANE0_CHANNEL_EQ_DONE	Y(1)
2	LANE0_SYMBOL_LOCKED	Y(1)
3		0 Reserved
4	LANE1_CR_DONE	Y(1)
5	LANE1_CHANNEL_EQ_DONE	Y(1)
6	LANE1_SYMBOL_LOCKED	Y(1)
7		0 Reserved

00203: LANE2_3_STATUS

Bit	Name	Value Description
0	LANE2_CR_DONE	Y(1)
1	LANE2_CHANNEL_EQ_DONE	Y(1)
2	LANE2_SYMBOL_LOCKED	Y(1)
3		0 Reserved
4	LANE3_CR_DONE	Y(1)
5	LANE3_CHANNEL_EQ_DONE	Y(1)
6	LANE3_SYMBOL_LOCKED	Y(1)
7		0 Reserved

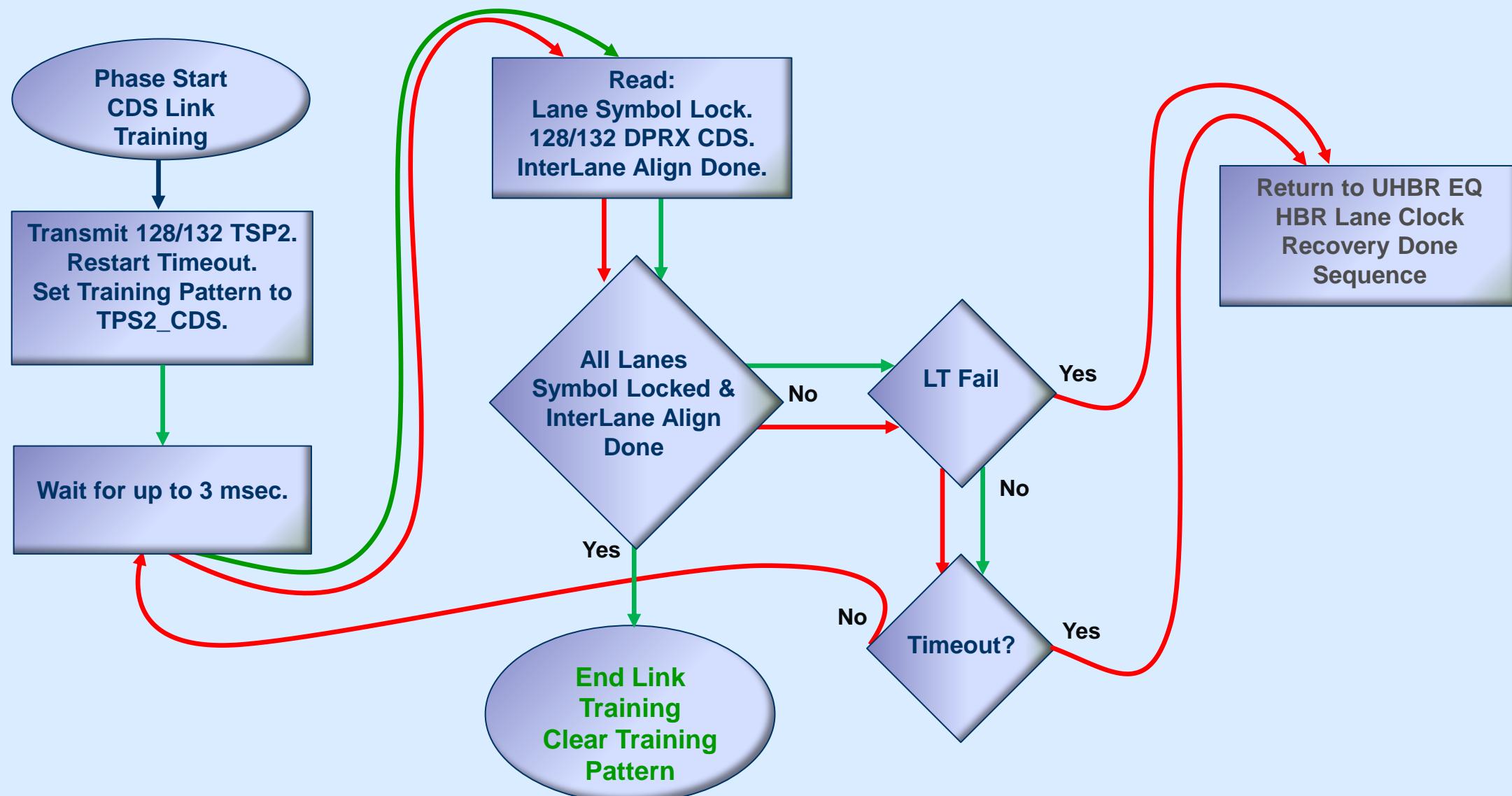
00204: LANE_ALIGN_STATUS_UPDATED

Bit	Name	Value Description
0	INTERLANE_ALIGN_DONE	Y(1)
1	POST_LT_ADJ_REQ_IN_PROGRESS	N(0)
2	128b/132b_DPRX_EQ_INTERLANE_ALIGN_DONE	Y(1)
3	128b/132b_DPRX_CDS_INTERLANE_ALIGN_DONE	N(0)
4	128b/132b_LT_FAILED	N(0)
5		0 Reserved
6	DOWNSTREAM_PORT_STATUS_CHANGED	N(0)
7	LINK_STATUS_UPDATED	Y(1)

- In this example the Equalization Phase completes in 40 msecs.

128b/132b Link Training Begin Clock Data Switch Phase

Link Training – Clock Data Switch Phase Flow Diagram (Simplified)



Link Training – Start Clock Data Switch (CDS) Phase

The screenshot shows the ACA Data Viewer interface with the following details:

- File Menu:** Open, Close, Export, Options.
- Search Bar:** Filter, Find.
- Log View:** [20G_LTTPR_AUX_LT_FFE5] Events: 522 (996). The log lists various frames, mostly ACKs and R:202 LANEO_1_STATUS frames, indicating the initial link training phase.
- Selected Frame (Frame 198):**
 - Details:** Start Time: +00:00:00.041566, Type: Native, Direction: Request, Command: Write, Address: 0x00102 (TRAINING_PATTERN_SET:).
 - Length:** 1
 - Content:** 00102: TRAINING_PATTERN_SET:
8b/10b Link Layer

Bit	Name	Value	Description
3-0	TRAINING_PATTERN_SELECT	3	Pattern 3
4	RECOVERED_CLOCK_OUT_EN	N(0)	
5	SCRAMBLING_DISABLE	N(0)	
7-6	SYMBOL_ERROR_COUNT_SEL	0	Disparity and Symbol error

128b/132b Link Layer

Bit	Name	Value	Description
3-0	TRAINING_PATTERN_SELECT	3	128b/132b TPS2_CDS (Clock and Data Switch)
4	RECOVERED_CLOCK_OUT_EN	0	Reserved
5	SCRAMBLING_DISABLE	N(0)	
6	SYMBOL_ERROR_COUNT_SEL	0	Reserved
7	SYMBOL_ERROR_COUNT_SEL	0	Reserved

[0000][80 01 02 00 03 -- -- --] [.....]
- Bottom Status:** 198: > W:102 TRAINING_PATTERN_SET: L=1 03

- With Equalization Phase completed, the second phase of Link Training (Clock Data Switch) Phase begins.
- Source (DPTx) transmits Training Pattern 2_CDS to cause each LTTPR device to **retransmit the DPTx Training Pattern 2 via its recovered clock (recovered from upstream DPTx)**.
- Source (DPTx) sets a timer for the completion of the Clock Data Switch Phase: 20 msec * the number of LTTPRs + 20 msec.

Link Training – Start Clock Data Switch (CDS) Phase

ACA Data Viewer

Open Close Export Options Filter Find

[20G_LTTPR_AUX_LT_FFEs] Events: 522 (996)

189	DPLT	DPUSBC-T11	+00:00:00.034563	< ACK
190	DPLT	DPUSBC-T11	+00:00:00.040713	> R:202 LANEO_1_STATUS: L=6
191	DPLT	DPUSBC-T11	+00:00:00.040787	< ACK 77 77 85 0B 66 66
192	DNAT	DPUSBC-T11	+00:00:00.040987	> R:2216 128b/132b_TRAINING_AUX_RD_...
193	DNAT	DPUSBC-T11	+00:00:00.041061	< ACK 85
194	DPLT	DPUSBC-T11	+00:00:00.041183	> R:202 LANEO_1_STATUS: L=4
195	DPLT	DPUSBC-T11	+00:00:00.041257	< ACK 77 77 05 0B
196	DNAT	DPUSBC-T11	+00:00:00.041361	> R:F0008 EQ done per LTTPR L=1
197	DNAT	DPUSBC-T11	+00:00:00.041435	< ACK FF
198	DPLT	DPUSBC-T11	+00:00:00.041566	> W:102 TRAINING_PATTERN_SET: L=1 03
199	DPLT	DPUSBC-T11	+00:00:00.041648	< ACK
200	DPLT	DPUSBC-T11	+00:00:00.042817	> R:202 LANEO_1_STATUS: L=4
201	DPLT	DPUSBC-T11	+00:00:00.042891	< ACK 77 77 85 03
202	DPLT	DPUSBC-T11	+00:00:00.044154	> R:202 LANEO_1_STATUS: L=4
203	DPLT	DPUSBC-T11	+00:00:00.044228	< ACK 77 77 05 03
204	DPLT	DPUSBC-T11	+00:00:00.045522	> R:202 LANEO_1_STATUS: L=4
205	DPLT	DPUSBC-T11	+00:00:00.045596	< ACK 77 77 05 03
206	DPLT	DPUSBC-T11	+00:00:00.046920	> R:202 LANEO_1_STATUS: L=4
207	DPLT	DPUSBC-T11	+00:00:00.046994	< ACK 77 77 0D 03
208	DPLT	DPUSBC-T11	+00:00:00.047229	> W:102 TRAINING_PATTERN_SET: L=1 00
209	DPLT	DPUSBC-T11	+00:00:00.047311	< ACK
210	DNAT	DPUSBC-T11	+00:00:00.047486	> R:200 SINK_COUNT L=6
211	DNAT	DPUSBC-T11	+00:00:00.047560	< ACK 41 00 77 77 0D 02
212	DPLT	DPUSBC-T11	+00:00:00.047859	> R:100 LINK_BW_SET L=9
213	DPLT	DPUSBC-T11	+00:00:00.047933	< ACK 02 84 00 05 05 05 05 00 02
214	DNAT	DPUSBC-T11	+00:00:00.048129	> R:200 SINK_COUNT L=8
215	DNAT	DPUSBC-T11	+00:00:00.048203	< ACK 41 00 77 77 0D 03 66 66
216	DPLT	DPUSBC-T11	+00:00:00.050187	> R:100 LINK_BW_SET L=9
217	DPLT	DPUSBC-T11	+00:00:00.050261	< ACK 02 84 00 05 05 05 05 00 02
218	DPLT	DPUSBC-T11	+00:00:00.054403	> R:100 LINK_BW_SET L=9
219	DPLT	DPUSBC-T11	+00:00:00.054477	< ACK 02 84 00 05 05 05 05 00 02
220	DPLT	DPUSBC-T11	+00:00:00.520460	> R:100 LINK_BW_SET L=9
221	DPLT	DPUSBC-T11	+00:00:00.520534	< ACK 02 84 00 05 05 05 05 00 02
222	DPLT	DPUSBC-T11	+00:00:00.520682	> R:100 LINK_BW_SET L=9
223	DPLT	DPUSBC-T11	+00:00:00.520756	< ACK 02 84 00 05 05 05 05 00 02

Start Time: +00:00:00.041566
Type: Native
Direction: Request
Command: Write
Address: 0x00102 (TRAINING_PATTERN_SET:)

Length: 1

00102: TRAINING_PATTERN_SET:
8b/10b Link Layer

Bit	Name	Value	Description
3-0	TRAINING_PATTERN_SELECT	3	Pattern 3
4	RECOVERED_CLOCK_OUT_EN	N(0)	
5	SCRAMBLING_DISABLE	N(0)	
7-6	SYMBOL_ERROR_COUNT_SEL	0	Disparity and Symbol error

128b/132b Link Layer

Bit	Name	Value	Description
3-0	TRAINING_PATTERN_SELECT	3	128b/132b TPS2_CDS (Clock and Data Switch)
4		0	Reserved
5	SCRAMBLING_DISABLE	N(0)	
6		0	Reserved
7		0	Reserved

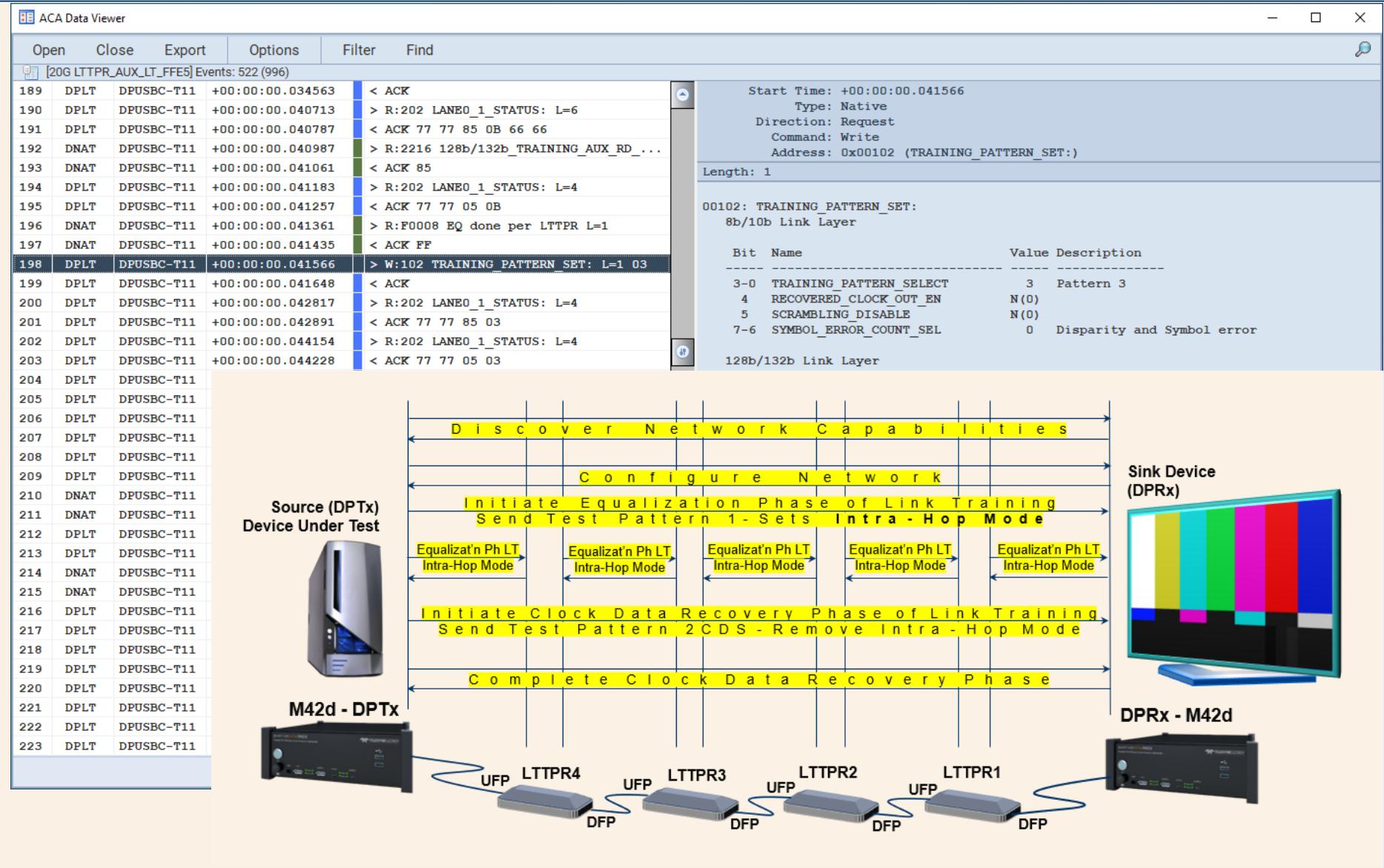
[0000][80 01 02 00 03 -- -- --] [.....]

198: > W:102 TRAINING_PATTERN_SET: L=1 03



- With Equalization Phase completed, the second phase of Link Training (Clock Data Switch) Phase begins.
- Source (DPTx) transmits Training Pattern 2_CDS to cause each LTTPR device to **retransmit the DPTx Training Pattern 2 via its recovered clock (recovered from upstream DPTx)**.
- Source (DPTx) sets a timer for the completion of the Clock Data Switch Phase: 20 msecs * the number of LTTPRs + 20 msecs.

Link Training – Start Clock Data Switch (CDS) Phase



- With Equalization Phase completed, the second phase of Link Training (Clock Data Switch) Phase begins.
- Source (DPTx) transmits Training Pattern 2_CDS to cause each LTTPR device to **retransmit the DPTx Training Pattern 2 via its recovered clock (recovered from upstream DPTx)**.
- Source (DPTx) sets a timer for the completion of the Clock Data Switch Phase: 20 msec * the number of LTTPRs + 20 msec.

Link Training – Clock Data Switch Phase – Check if Symbol Lock Done

ACA Data Viewer					
			Open	Close	Export
			Options	Filter	Find
[20G_LTTPR_AUX_LT_FFE5] Events: 522 (996)					
189	DPLT	DPUSBC-T11	+00:00:00.034563	< ACK	
190	DPLT	DPUSBC-T11	+00:00:00.040713	> R:202 LANE0_1_STATUS: L=6	
191	DPLT	DPUSBC-T11	+00:00:00.040787	< ACK 77 77 85 0B 66 66	
192	DNAT	DPUSBC-T11	+00:00:00.040987	> R:2216 128b/132b_TRAINING_AUX_RD...	
193	DNAT	DPUSBC-T11	+00:00:00.041061	< ACK 85	
194	DPLT	DPUSBC-T11	+00:00:00.041183	> R:202 LANE0_1_STATUS: L=4	
195	DPLT	DPUSBC-T11	+00:00:00.041257	< ACK 77 77 05 0B	
196	DNAT	DPUSBC-T11	+00:00:00.041361	> R:F0008 EQ done per LTTPR L=1	
197	DNAT	DPUSBC-T11	+00:00:00.041435	< ACK FF	
198	DPLT	DPUSBC-T11	+00:00:00.041566	> W:102 TRAINING_PATTERN_SET: L=1 03	
199	DPLT	DPUSBC-T11	+00:00:00.041648	< ACK	
200	DPLT	DPUSBC-T11	+00:00:00.042817	> R:202 LANE0_1_STATUS: L=4	
201	DPLT	DPUSBC-T11	+00:00:00.042891	< ACK 77 77 85 03	
202	DPLT	DPUSBC-T11	+00:00:00.044154	> R:202 LANE0_1_STATUS: L=4	
203	DPLT	DPUSBC-T11	+00:00:00.044228	< ACK 77 77 05 03	
204	DPLT	DPUSBC-T11	+00:00:00.045522	> R:202 LANE0_1_STATUS: L=4	
205	DPLT	DPUSBC-T11	+00:00:00.045596	< ACK 77 77 05 03	
206	DPLT	DPUSBC-T11	+00:00:00.046920	> R:202 LANE0_1_STATUS: L=4	
207	DPLT	DPUSBC-T11	+00:00:00.046994	< ACK 77 77 0D 03	
208	DPLT	DPUSBC-T11	+00:00:00.047229	> W:102 TRAINING_PATTERN_SET: L=1 00	
209	DPLT	DPUSBC-T11	+00:00:00.047311	< ACK	
210	DNAT	DPUSBC-T11	+00:00:00.047486	> R:200 SINK_COUNT L=6	
211	DNAT	DPUSBC-T11	+00:00:00.047560	< ACK 41 00 77 77 0D 02	
212	DPLT	DPUSBC-T11	+00:00:00.047859	> R:100 LINK_BW_SET L=9	
213	DPLT	DPUSBC-T11	+00:00:00.047933	< ACK 02 84 00 05 05 05 00 02	
214	DNAT	DPUSBC-T11	+00:00:00.048129	> R:200 SINK_COUNT L=8	
215	DNAT	DPUSBC-T11	+00:00:00.048203	< ACK 41 00 77 77 0D 03 66 66	
216	DPLT	DPUSBC-T11	+00:00:00.050187	> R:100 LINK_BW_SET L=9	
217	DPLT	DPUSBC-T11	+00:00:00.050261	< ACK 02 84 00 05 05 05 00 02	
218	DPLT	DPUSBC-T11	+00:00:00.054403	> R:100 LINK_BW_SET L=9	
219	DPLT	DPUSBC-T11	+00:00:00.054477	< ACK 02 84 00 05 05 05 00 02	
220	DPLT	DPUSBC-T11	+00:00:00.520460	> R:100 LINK_BW_SET L=9	
221	DPLT	DPUSBC-T11	+00:00:00.520534	< ACK 02 84 00 05 05 05 00 02	
222	DPLT	DPUSBC-T11	+00:00:00.520682	> R:100 LINK_BW_SET L=9	
223	DPLT	DPUSBC-T11	+00:00:00.520756	< ACK 02 84 00 05 05 05 00 02	

- Source (DPTx) checks if the Symbol Lock and Clock Data Switch (CDS) Inter-Lane Alignment are done.

- The screen example shows that the Symbol Lock is completed but the CDS Inter-Lane alignment is not completed.

Note: The LTTPR network has transitioned out of the Intra-Hop Aux Transaction mode.

Link Training – Clock Data Switch Phase – Check if Inter-Lane Align Done

ACA Data Viewer

Open Close Export Options Filter Find

[20G LTPP_AUX_LT_FFE5] Events: 522 (996)

189	DPLT	DPUSBC-T11	+00:00:00.034563	< ACK
190	DPLT	DPUSBC-T11	+00:00:00.040713	> R:202 LANEO_1_STATUS: L=6
191	DPLT	DPUSBC-T11	+00:00:00.040787	< ACK 77 77 85 0B 66 66
192	DNAT	DPUSBC-T11	+00:00:00.040987	> R:2216 128b/132b_TRAINING_AUX_RD...
193	DNAT	DPUSBC-T11	+00:00:00.041061	< ACK 85
194	DPLT	DPUSBC-T11	+00:00:00.041183	> R:202 LANEO_1_STATUS: L=4
195	DPLT	DPUSBC-T11	+00:00:00.041257	< ACK 77 77 05 0B
196	DNAT	DPUSBC-T11	+00:00:00.041361	> R:F0008 EQ done per LTPP L=1
197	DNAT	DPUSBC-T11	+00:00:00.041435	< ACK FF
198	DPLT	DPUSBC-T11	+00:00:00.041566	> W:102 TRAINING_PATTERN_SET: L=1 03
199	DPLT	DPUSBC-T11	+00:00:00.041648	< ACK
200	DPLT	DPUSBC-T11	+00:00:00.042817	> R:202 LANEO_1_STATUS: L=4
201	DPLT	DPUSBC-T11	+00:00:00.042891	< ACK 77 77 85 03
202	DPLT	DPUSBC-T11	+00:00:00.044154	> R:202 LANEO_1_STATUS: L=4
203	DPLT	DPUSBC-T11	+00:00:00.044228	< ACK 77 77 05 03
204	DPLT	DPUSBC-T11	+00:00:00.045522	> R:202 LANEO_1_STATUS: L=4
205	DPLT	DPUSBC-T11	+00:00:00.045596	< ACK 77 77 05 03
206	DPLT	DPUSBC-T11	+00:00:00.046920	> R:202 LANEO_1_STATUS: L=4
207	DPLT	DPUSBC-T11	+00:00:00.046994	< ACK 77 77 0D 03
208	DPLT	DPUSBC-T11	+00:00:00.047229	> W:102 TRAINING_PATTERN_SET: L=1 00
209	DPLT	DPUSBC-T11	+00:00:00.047311	< ACK
210	DNAT	DPUSBC-T11	+00:00:00.047486	> R:200 SINK_COUNT L=6
211	DNAT	DPUSBC-T11	+00:00:00.047560	< ACK 41 00 77 77 0D 02
212	DPLT	DPUSBC-T11	+00:00:00.047859	> R:100 LINK_BW_SET L=9
213	DPLT	DPUSBC-T11	+00:00:00.047933	< ACK 02 84 00 05 05 05 05 00 02
214	DNAT	DPUSBC-T11	+00:00:00.048129	> R:200 SINK_COUNT L=8
215	DNAT	DPUSBC-T11	+00:00:00.048203	< ACK 41 00 77 77 0D 03 66 66
216	DPLT	DPUSBC-T11	+00:00:00.050187	> R:100 LINK_BW_SET L=9
217	DPLT	DPUSBC-T11	+00:00:00.050261	< ACK 02 84 00 05 05 05 05 00 02
218	DPLT	DPUSBC-T11	+00:00:00.054403	> R:100 LINK_BW_SET L=9
219	DPLT	DPUSBC-T11	+00:00:00.054477	< ACK 02 84 00 05 05 05 05 00 02
220	DPLT	DPUSBC-T11	+00:00:00.520460	> R:100 LINK_BW_SET L=9
221	DPLT	DPUSBC-T11	+00:00:00.520534	< ACK 02 84 00 05 05 05 05 00 02
222	DPLT	DPUSBC-T11	+00:00:00.520682	> R:100 LINK_BW_SET L=9
223	DPLT	DPUSBC-T11	+00:00:00.520756	< ACK 02 84 00 05 05 05 05 00 02

Start Time: +00:00:00.046994
Type: Native
Direction: Reply
Command: ACK
Reply to Read Request.

00202: LANEO_1_STATUS:

Bit	Name	Value Description
0	LANEO_CR_DONE	Y(1)
1	LANEO_CHANNEL_EQ_DONE	Y(1)
2	LANEO_SYMBOL_LOCKED	Y(1)
3		0 Reserved
4	LANE1_CR_DONE	Y(1)
5	LANE1_CHANNEL_EQ_DONE	Y(1)
6	LANE1_SYMBOL_LOCKED	Y(1)
7		0 Reserved

00203: LANE2_3_STATUS

Bit	Name	Value Description
0	LANE2_CR_DONE	Y(1)
1	LANE2_CHANNEL_EQ_DONE	Y(1)
2	LANE2_SYMBOL_LOCKED	Y(1)
3		0 Reserved
4	LANE3_CR_DONE	Y(1)
5	LANE3_CHANNEL_EQ_DONE	Y(1)
6	LANE3_SYMBOL_LOCKED	Y(1)
7		0 Reserved

00204: LANE_ALIGN_STATUS_UPDATED

Bit	Name	Value Description
0	INTERLANE_ALIGN_DONE	Y(1)
1	POST_LT_ADJ_REQ_IN_PROGRESS	N(0)
2	128b/132b DPRX_EQ_INTERLANE_ALIGN_DONE	Y(1)
3	128b/132b DPRX CDS_INTERLANE_ALIGN_DONE	Y(1)
4	128b/132b_LT_FAILED	N(0)
5		0 Reserved
6	DOWNSTREAM_PORT_STATUS_CHANGED	N(0)
7	LINK_STATUS_UPDATED	N(0)



207: < ACK 77 77 0D 03

- Source (DPTx) checks if the Clock Data Switch (CDS) Inter-Lane Alignment is done.
- The screen example shows that CDS Phase is completed. Symbol Lock has been achieved as well.

Link Training – Clock Data Switch Phase (CDS) Done

ACA Data Viewer

Open Close Export Options Filter Find

[20G LTPR_AUX_LT_FFE5] Events: 522 (996)

189	DPLT	DPUSBC-T11	+00:00:00.034563	< ACK
190	DPLT	DPUSBC-T11	+00:00:00.040713	> R:202 LANE0_1_STATUS: L=6
191	DPLT	DPUSBC-T11	+00:00:00.040787	< ACK 77 77 85 0B 66 66
192	DNAT	DPUSBC-T11	+00:00:00.040987	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL...
193	DNAT	DPUSBC-T11	+00:00:00.041061	< ACK 85
194	DPLT	DPUSBC-T11	+00:00:00.041183	> R:202 LANE0_1_STATUS: L=4
195	DPLT	DPUSBC-T11	+00:00:00.041257	< ACK 77 77 05 0B
196	DNAT	DPUSBC-T11	+00:00:00.041361	> R:F0008 EQ done per LTPR L=1
197	DNAT	DPUSBC-T11	+00:00:00.041435	< ACK FF
198	DPLT	DPUSBC-T11	+00:00:00.041566	> W:102 TRAINING_PATTERN_SET: L=1 03
199	DPLT	DPUSBC-T11	+00:00:00.041648	< ACK
200	DPLT	DPUSBC-T11	+00:00:00.042817	> R:202 LANE0_1_STATUS: L=4
201	DPLT	DPUSBC-T11	+00:00:00.042891	< ACK 77 77 85 03
202	DPLT	DPUSBC-T11	+00:00:00.044154	> R:202 LANE0_1_STATUS: L=4
203	DPLT	DPUSBC-T11	+00:00:00.044228	< ACK 77 77 05 03
204	DPLT	DPUSBC-T11	+00:00:00.045522	> R:202 LANE0_1_STATUS: L=4
205	DPLT	DPUSBC-T11	+00:00:00.045596	< ACK 77 77 05 03
206	DPLT	DPUSBC-T11	+00:00:00.046920	> R:202 LANE0_1_STATUS: L=4
207	DPLT	DPUSBC-T11	+00:00:00.046994	< ACK 77 77 0D 03
208	DPLT	DPUSBC-T11	+00:00:00.047229	> W:102 TRAINING_PATTERN_SET: L=1 00
209	DPLT	DPUSBC-T11	+00:00:00.047311	< ACK
210	DNAT	DPUSBC-T11	+00:00:00.047486	> R:200 SINK_COUNT L=6
211	DNAT	DPUSBC-T11	+00:00:00.047560	< ACK 41 00 77 77 0D 02
212	DPLT	DPUSBC-T11	+00:00:00.047859	> R:100 LINK_BW_SET L=9
213	DPLT	DPUSBC-T11	+00:00:00.047933	< ACK 02 84 00 05 05 05 05 00 02
214	DNAT	DPUSBC-T11	+00:00:00.048129	> R:200 SINK_COUNT L=8
215	DNAT	DPUSBC-T11	+00:00:00.048203	< ACK 41 00 77 77 0D 03 66 66
216	DPLT	DPUSBC-T11	+00:00:00.050187	> R:100 LINK_BW_SET L=9
217	DPLT	DPUSBC-T11	+00:00:00.050261	< ACK 02 84 00 05 05 05 05 00 02
218	DPLT	DPUSBC-T11	+00:00:00.054403	> R:100 LINK_BW_SET L=9
219	DPLT	DPUSBC-T11	+00:00:00.054477	< ACK 02 84 00 05 05 05 05 00 02
220	DPLT	DPUSBC-T11	+00:00:00.520460	> R:100 LINK_BW_SET L=9
221	DPLT	DPUSBC-T11	+00:00:00.520534	< ACK 02 84 00 05 05 05 05 00 02
222	DPLT	DPUSBC-T11	+00:00:00.520682	> R:100 LINK_BW_SET L=9
223	DPLT	DPUSBC-T11	+00:00:00.520756	< ACK 02 84 00 05 05 05 05 00 02

Start Time: +00:00:00.047229
Type: Native
Direction: Request
Command: Write
Address: 0x00102 (TRAINING_PATTERN_SET:)

Length: 1

00102: TRAINING_PATTERN_SET:
8b/10b Link Layer

Bit	Name	Value	Description
3-0	TRAINING_PATTERN_SELECT	0	None
4	RECOVERED_CLOCK_OUT_EN	N(0)	
5	SCRAMBLING_DISABLE	N(0)	
7-6	SYMBOL_ERROR_COUNT_SEL	0	Disparity and Symbol error

128b/132b Link Layer

Bit	Name	Value	Description
3-0	TRAINING_PATTERN_SELECT	0	None
4	RECOVERED_CLOCK_OUT_EN	0	Reserved
5	SCRAMBLING_DISABLE	N(0)	
6	SYMBOL_ERROR_COUNT_SEL	0	Reserved
7	SYMBOL_ERROR_COUNT_SEL	0	Reserved

[0000][80 01 02 00 00 -- -- --][.....]

208: > W:102 TRAINING_PATTERN_SET: L=1 00

- ◆ With both Link Training phases completed, there is no longer a need to send a Training Pattern.
- ◆ The Source (DPTx) writes 0 to register 102 to halt the transmission of a Training Pattern. The screen example depicts this.
- ◆ This marks the end of Link Training.

Link Training – Link Training Duration

ACA Data Viewer

Open Close Export Options Filter Find

[20G LTTPR_AUX_LT_FFE5] Events: 522 (996)

113	DPLT	DPUSBC-T11	-00:00:00.001859	< ACK
114	DNAT	DPUSBC-T11	-00:00:00.001718	> W:600 SINK_SET_POWER L=1 01
115	DNAT	DPUSBC-T11	-00:00:00.001636	< ACK
116	DNAT	DPUSBC-T11	-00:00:00.001564	> R:E TRAINING_AUX_RD_INTERVAL L=1
117	DNAT	DPUSBC-T11	-00:00:00.001490	< ACK 81
118	DPLT	DPUSBC-T11	-00:00:00.001362	> W:102 TRAINING_PATTERN_SET: L=1 00
119	DPLT	DPUSBC-T11	-00:00:00.001280	< ACK
120	DPLT	DPUSBC-T11	-00:00:00.001219	> R:205 SINK_STATUS L=1
121	DPLT	DPUSBC-T11	-00:00:00.001145	< ACK 03
122	DPLT	DPUSBC-T11	-00:00:00.000509	> W:108 MAIN_LINK_CHANNEL_CODING_SET L=1 02
123	DPLT	DPUSBC-T11	-00:00:00.000427	< ACK
124	DPLT	DPUSBC-T11	-00:00:00.000362	> W:100 LINK_BW_SET L=1 02
125	DPLT	DPUSBC-T11	-00:00:00.000280	< ACK
126	DPLT	DPUSBC-T11	-00:00:00.000164	> W:101 LANE_COUNT_SET L=1 84
127	DPLT	DPUSBC-T11	-00:00:00.000082	< ACK
128	DPLT	DPUSBC-T11	+00:00:00.000000	> W:102 TRAINING_PATTERN_SET: L=1 01
129	DPLT	DPUSBC-T11	+00:00:00.000281	< ACK
130	DNAT	DPUSBC-T11	+00:00:00.000355	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
131	DNAT	DPUSBC-T11	+00:00:00.000628	< DEFER
132	DNAT	DPUSBC-T11	+00:00:00.001194	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
133	DNAT	DPUSBC-T11	+00:00:00.001467	< DEFER
134	DNAT	DPUSBC-T11	+00:00:00.002041	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
135	DNAT	DPUSBC-T11	+00:00:00.002314	< DEFER
136	DNAT	DPUSBC-T11	+00:00:00.002901	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
137	DNAT	DPUSBC-T11	+00:00:00.003174	< DEFER
138	DNAT	DPUSBC-T11	+00:00:00.003745	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
139	DNAT	DPUSBC-T11	+00:00:00.004018	< DEFER
140	DNAT	DPUSBC-T11	+00:00:00.004588	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
141	DNAT	DPUSBC-T11	+00:00:00.004861	< DEFER
142	DNAT	DPUSBC-T11	+00:00:00.005476	> R:2216 128b/132b_TRAINING_AUX_RD_INTERVAL L=1
143	DNAT	DPUSBC-T11	+00:00:00.005749	< ACK 85
144	DPLT	DPUSBC-T11	+00:00:00.005894	> R:206 ADJUST_REQUEST_LANE0_1 L=2
145	DPLT	DPUSBC-T11	+00:00:00.006167	< DEFER
146	DPLT	DPUSBC-T11	+00:00:00.006767	> R:206 ADJUST_REQUEST_LANE0_1 L=2
147	DPLT	DPUSBC-T11	+00:00:00.007040	< DEFER

Start Time: +00:00:00.000000
Type: Native
Direction: Request
Command: Write
Address: 0x00102 (TRAINING_PATTERN_SET:)

Length: 1

00102: TRAINING_PATTERN_SET:
8b/10b Link Layer

Bit	Name	Value	Description
3-0	TRAINING_PATTERN_SELECT	1	Pattern 1
4	RECOVERED_CLOCK_OUT_EN	N(0)	
5	SCRAMBLING_DISABLE	N(0)	
7-6	SYMBOL_ERROR_COUNT_SEL	0	Disparity and Symbol error

128b/132b Link Layer

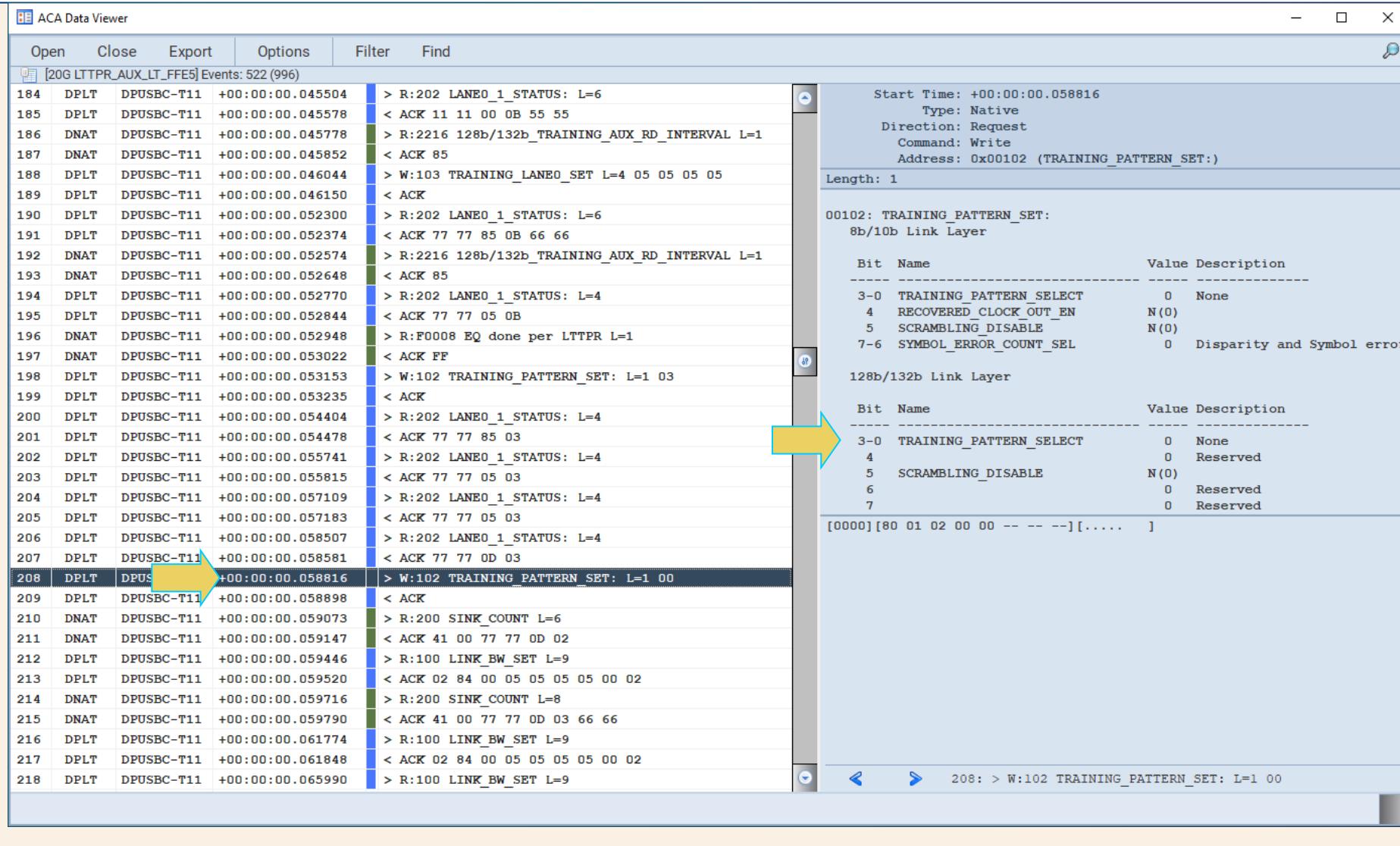
Bit	Name	Value	Description
3-0	TRAINING_PATTERN_SELECT	1	128b/132b TPS1
4	SCRAMBLING_DISABLE	0	Reserved
5	SCRAMBLING_DISABLE	N(0)	
6	SCRAMBLING_DISABLE	0	Reserved
7	SCRAMBLING_DISABLE	0	Reserved

[0000] [80 01 02 00 01 -- --] [.....]

128: > W:102 TRAINING_PATTERN_SET: L=1 01

- The entire Link Training process needs to complete in 650 msec or less.
- This is depicted on the two screen examples (this slide and next slide).
- In this case the Link Training completed in 59 msec from the time when Training Pattern 1 is transmitted to the time when the downstream network of LTTPRs and the sink (DPRx) report that they have exited out of the Clock Data Switch (CDS) Phase (next slide).

Link Training – Link Training Duration



- ◆ The Link Training completed in about 59 msec from the time when Training Pattern 1 is transmitted to the time when the downstream network of LTTPRs and the sink (DPRx) report that they have exited out of the Clock Data Switch (CDS) Phase and the Source DPTx writes Training Pattern 0 to register 102.

Link Layer Link Training – DP 2.0 Source Compliance – Link Training

DP 2.0 Source CT Core R1.0

Instrument: MyM41h [10.30.196.198] Connect Cards

CDF Entry Test Selection Test Options / Preview

Open Save Select All Categories Deselect All Categories

Category Tests Select All Clear All

Category	Tests	Select All	Clear All
AUX Rd. after HPD	<input type="checkbox"/> 4.3.1.10: [Same as DP1.4]Unsuccessful Link Training (Failure in Channel Equalization) ⓘ		
EDID and DPCD Rd.	<input type="checkbox"/> 4.3.1.11: [Same as DP1.4]Successful Link Training (Simultaneous Request for Diff. Voltage Swing/Pre-emphasis) ⓘ		
Link Training	<input type="checkbox"/> 4.3.1.12: [Same as DP1.4]Source Device Link Training CR Fallback Test ⓘ		
Link Maint.	<input type="checkbox"/> 4.3.1.13: [Same as DP1.4]Source Device Link Training EQ Fallback Test ⓘ		
Video	<input type="checkbox"/> 4.3.1.14: [DP2.0]Successful Link Training at All Supported Lane Counts and UHBR Link Speeds ⓘ		
Power Management	<input type="checkbox"/> 4.3.1.15: [DP2.0]Successful Link Training Upon HPD Plug Event for UHBR speed ⓘ		
Audio	<input type="checkbox"/> 4.3.1.16: [DP2.0]Successful Link Training when EQ done at 20th loop during channel EQ phase ⓘ		
Fec	<input type="checkbox"/> 4.3.1.17: [DP2.0]Successful Link Training to a Lower Bandwidth, when CHANNEL_EQ_DONE bits not set in 20 loops during channel EQ phase. ⓘ		
Dsc	<input type="checkbox"/> 4.3.1.18: [DP2.0]Successful Link Training to a Lower Bandwidth. When LT Failed received in middle of 20 loop (random value 1 to 19) during channel EQ Done. ⓘ		
	<input type="checkbox"/> 4.3.1.19: [DP2.0]Successful Link Training to a Lower Bandwidth. When LT Failed received at 20th loop during channel EQ Done. ⓘ		
	<input type="checkbox"/> 4.3.1.20: [DP2.0]Successful Link Training to a Lower Bandwidth. When LT Failed received at after EQ done. ⓘ		
	<input type="checkbox"/> 4.3.1.21: [DP2.0]Successful Link Training to a Lower Bandwidth. When EQ_INTERLANE_ALIGN_DONE bit not set during EQ phase. ⓘ		
	<input type="checkbox"/> 4.3.1.22: [DP2.0]Successful Link Training to a Lower Bandwidth. When Symbols not locked during CDS phase. ⓘ		
	<input type="checkbox"/> 4.3.1.23: [DP2.0]Successful Link Training to a Lower Bandwidth. When CDS_INTERLANE_ALIGN_DONE bit not set during CDS phase. ⓘ		

CLOSE

- ◆ List of currently defined compliance tests for DP 2.0 source devices for Link Training.

Link Layer Link Training – DP 2.0 Source Compliance – Link Training

Compliance Test Results Viewer

DP 2.0 Source (Core R1.0) Compliance Test Results

HTML Report Instrument: MyM41h [10.30.196.198]

Results Name: UHBR_DP20_Source_CTS_12tests_6_7_20201

Date Tested: June 7, 2021 9:44 AM

Overall Status: CTS Core R1.0 - Pass

Manufacturer: Model Name: Port Tested: 1

CONTINUE TEST EXECUTION

4.2.2.11: [DP2.0]Various UHBR AUX read interval verification in first EQ loop.

Iter 01: PASS

4.2.2.12: [DP2.0]UHBR Link Status/Adjust different FFE Request, different AUX read interval for 10 EQ loop

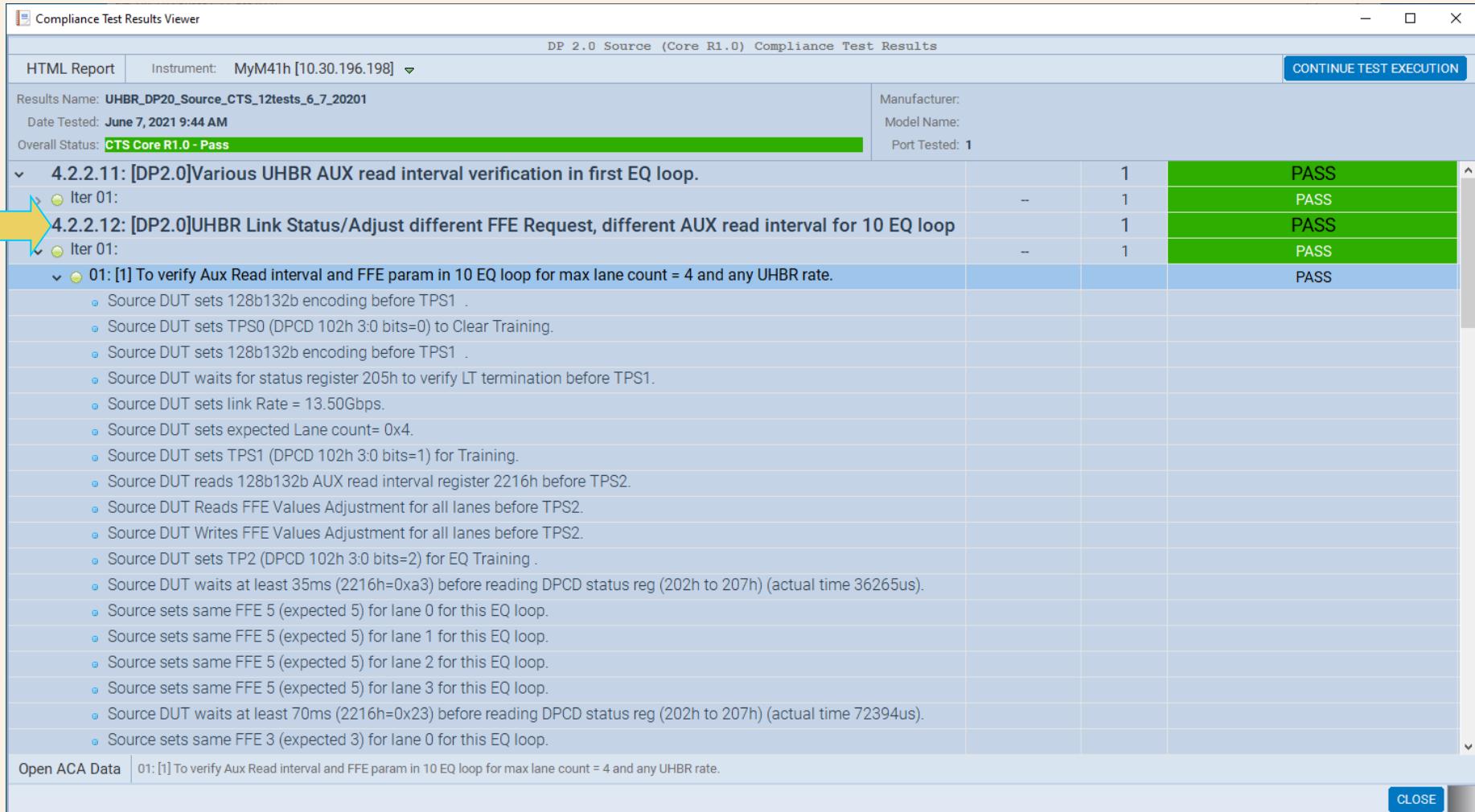
Iter 01: PASS

01: [1] To verify Aux Read interval and FFE param in 10 EQ loop for max lane count = 4 and any UHBR rate.

- Source DUT sets 128b132b encoding before TPS1 .
- Source DUT sets TPS0 (DPCD 102h 3:0 bits=0) to Clear Training.
- Source DUT sets 128b132b encoding before TPS1 .
- Source DUT waits for status register 205h to verify LT termination before TPS1.
- Source DUT sets link Rate = 13.50Gbps.
- Source DUT sets expected Lane count= 0x4.
- Source DUT sets TPS1 (DPCD 102h 3:0 bits=1) for Training.
- Source DUT reads 128b132b AUX read interval register 2216h before TPS2.
- Source DUT Reads FFE Values Adjustment for all lanes before TPS2.
- Source DUT Writes FFE Values Adjustment for all lanes before TPS2.
- Source DUT sets TP2 (DPCD 102h 3:0 bits=2) for EQ Training .
- Source DUT waits at least 35ms (2216h=0xa3) before reading DPCD status reg (202h to 207h) (actual time 36265us).
- Source sets same FFE 5 (expected 5) for lane 0 for this EQ loop.
- Source sets same FFE 5 (expected 5) for lane 1 for this EQ loop.
- Source sets same FFE 5 (expected 5) for lane 2 for this EQ loop.
- Source sets same FFE 5 (expected 5) for lane 3 for this EQ loop.
- Source DUT waits at least 70ms (2216h=0x23) before reading DPCD status reg (202h to 207h) (actual time 72394us).
- Source sets same FFE 3 (expected 3) for lane 0 for this EQ loop.

Open ACA Data 01: [1] To verify Aux Read interval and FFE param in 10 EQ loop for max lane count = 4 and any UHBR rate.

CLOSE



- ◆ List of currently defined compliance tests for DP 2.0 source devices for Link Training.

Link Layer Link Training – DP 2.0 Source Compliance – Link Training

Compliance Test Results Viewer

DP 2.0 Source (Core R1.0) Compliance Test Results

HTML Report Instrument: MyM41h [10.30.196.198] CONTINUE TEST EXECUTION

Results Name: UHBR_DP20_Source_CTS_12tests_6_7_20201
Date Tested: June 7, 2021 9:44 AM
Overall Status: CTS Core R1.0 - Pass

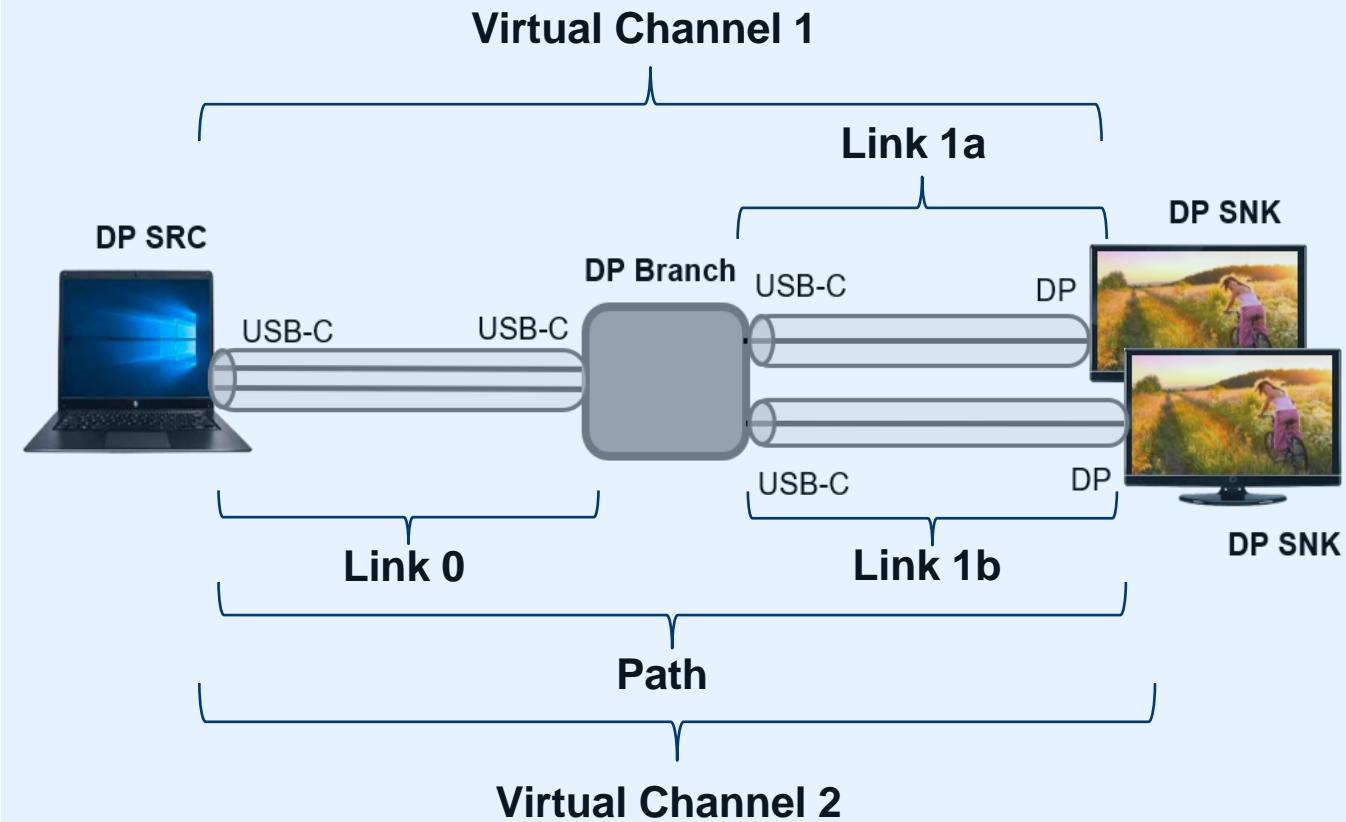
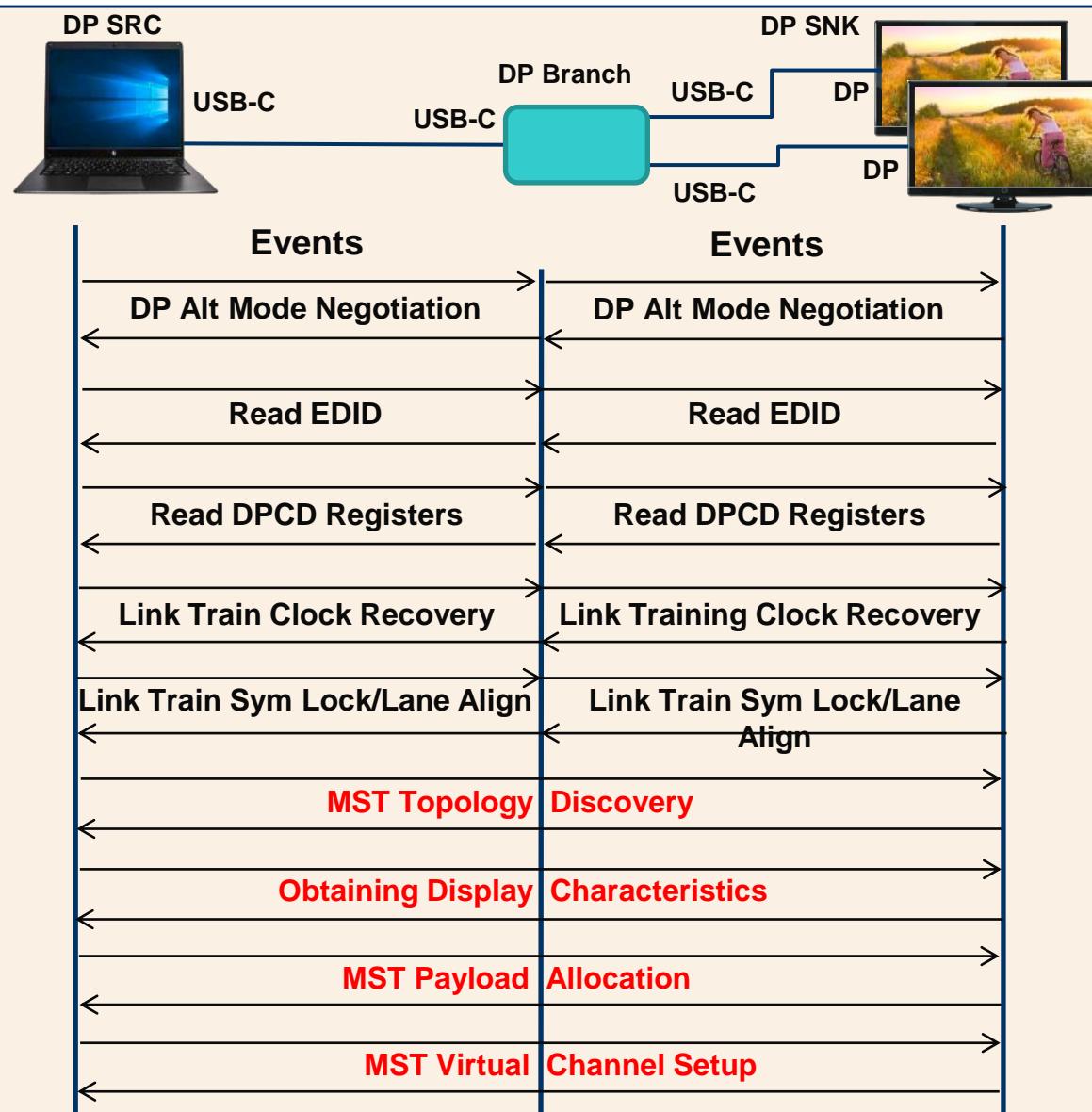
Manufacturer:
Model Name:
Port Tested: 1

4.2.2.11: [DP2.0]Various UHBR AUX read interval verification in first EQ loop. Iter 01:	1	PASS
4.2.2.12: [DP2.0]UHBR Link Status/Adjust different FFE Request, different AUX read interval for 10 EQ loop Iter 01: 01: [1] To verify Aux Read interval and FFE param in 10 EQ loop for max lane count = 4 and any UHBR rate.	1	PASS
4.3.1.14: [DP2.0]Successful Link Training at All Supported Lane Counts and UHBR Link Speeds	1	PASS
4.3.1.15: [DP2.0]Successful Link Training Upon HPD Plug Event for UHBR speed	1	PASS
4.3.1.16: [DP2.0]Successful Link Training when EQ done at 20th loop during channel EQ phase Iter 01: 01: [1] Link Training test for lane count = 4 and lane_rate = 10.00 02: [2] Link Training test for lane count = 4 and lane_rate = 13.50 Source DUT sets 128b132b encoding before TPS1 . Source DUT sets TPS0 (DPCD 102h 3:0 bits=0) to Clear Training. Source DUT sets 128b132b encoding before TPS1 . Source DUT waits for status register 205h to verify LT termination before TPS1. Source DUT sets expected Link Rate= 13.50Gbps. Source DUT sets expected Lane count= 0x4. Source DUT sets TPS1 (DPCD 102h 3:0 bits=1) for Training. Source DUT reads 128b132b AUX read interval register 2216h before TPS2. Source DUT Reads FFE Values Adjustment for all lanes before TPS2. Source DUT Writes FFE Values Adjustment for all lanes before TPS2. Source DUT sets TP2 (DPCD 102h 3:0 bits=2) for EQ Training . Source DUT does 20 loop for Channel EQ lock.	1	PASS
Open ACA Data	01: [1] To verify Aux Read interval and FFE param in 10 EQ loop for max lane count = 4 and any UHBR rate.	CLOSE

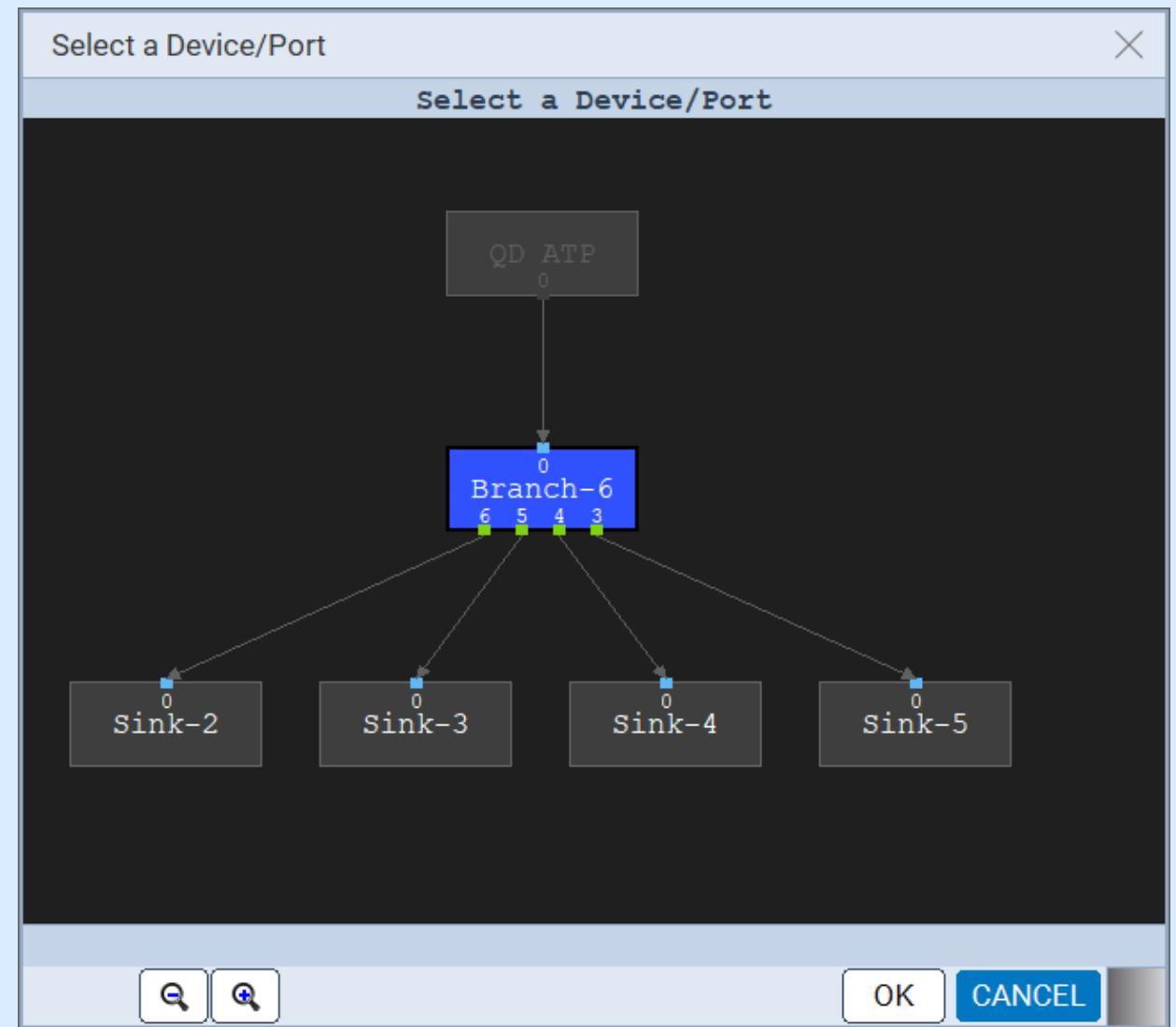
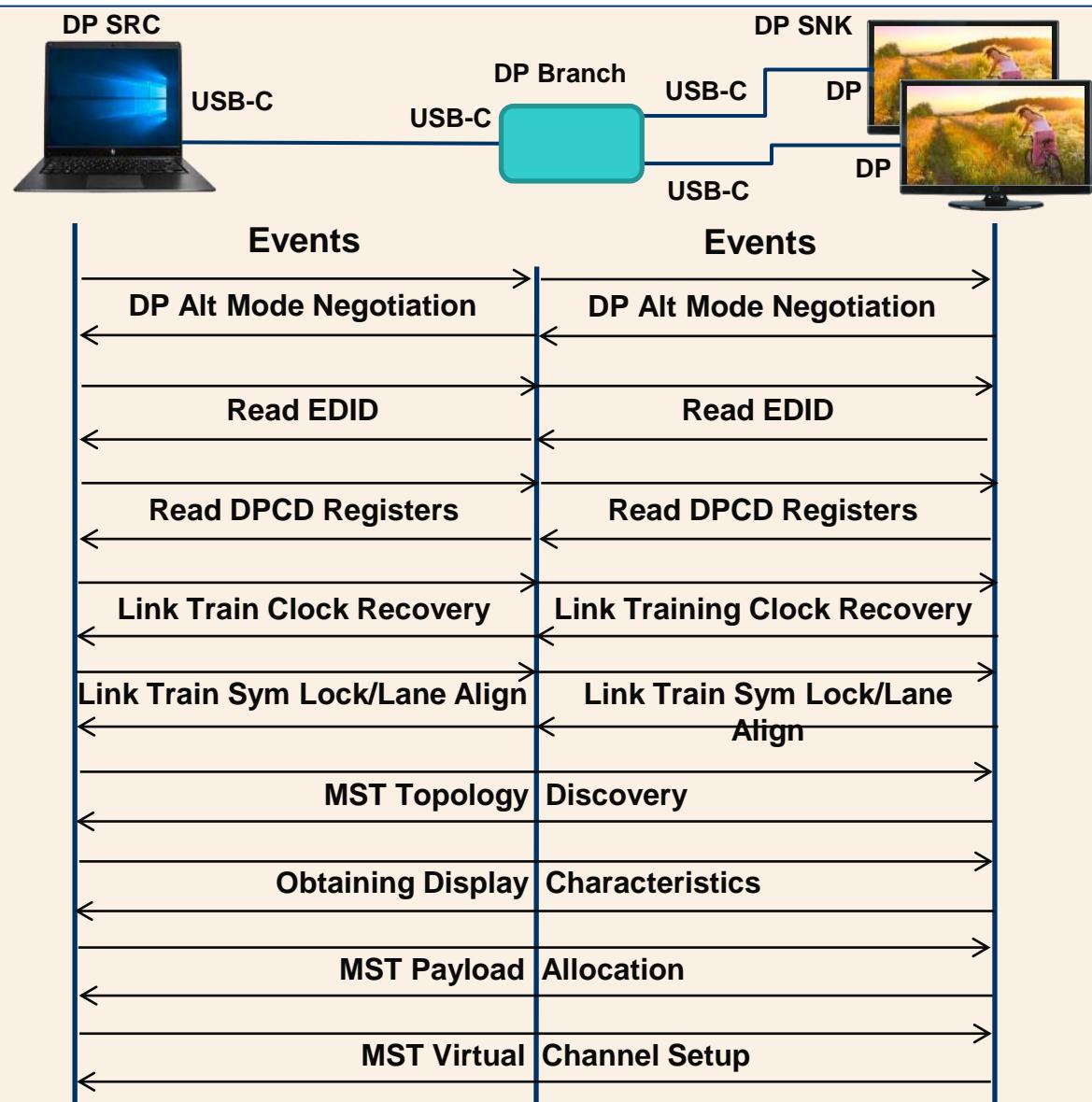
- Sample Link Layer compliance test results for DP 2.0 link training.

View Multi-Stream Transport Transactions

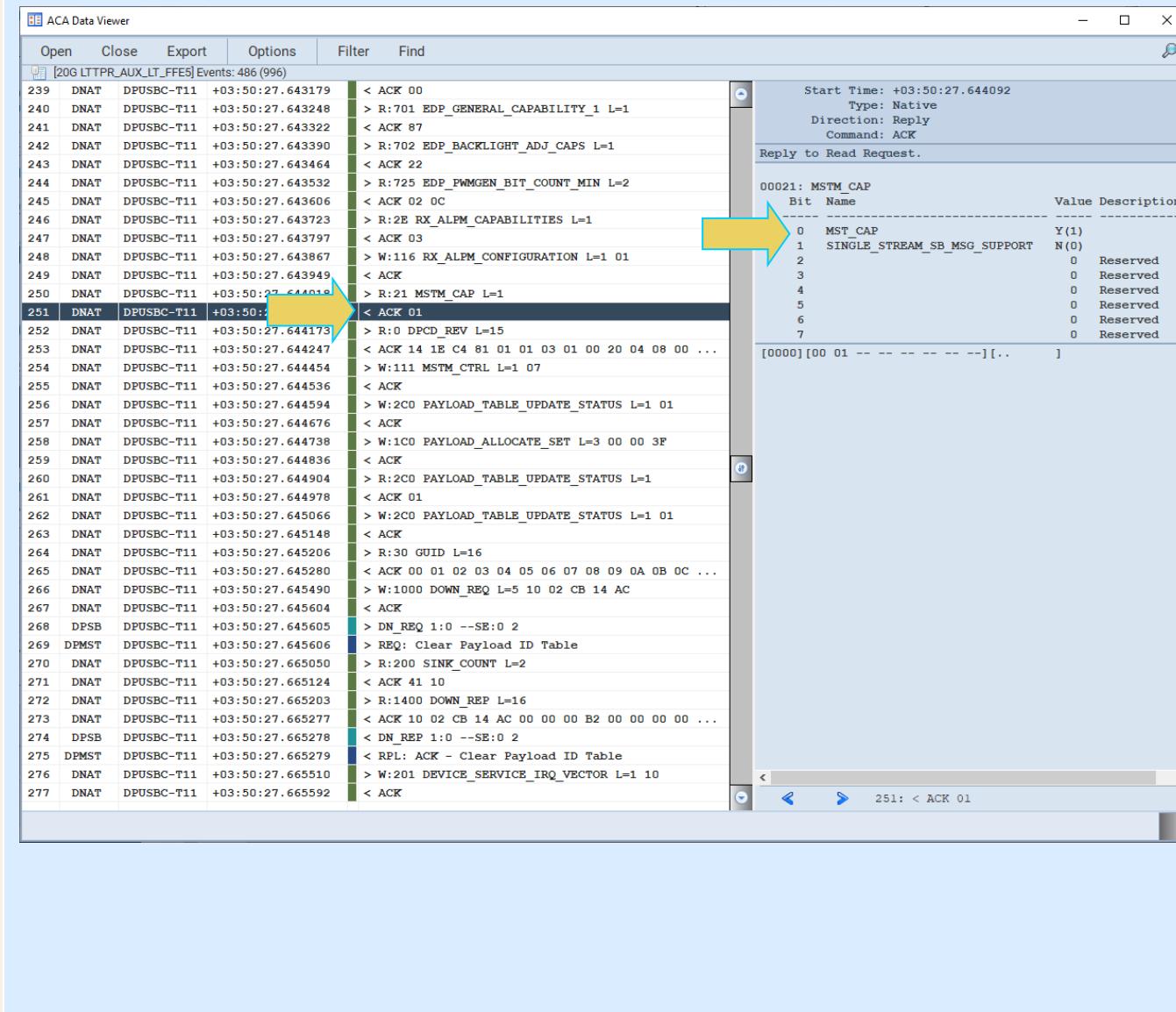
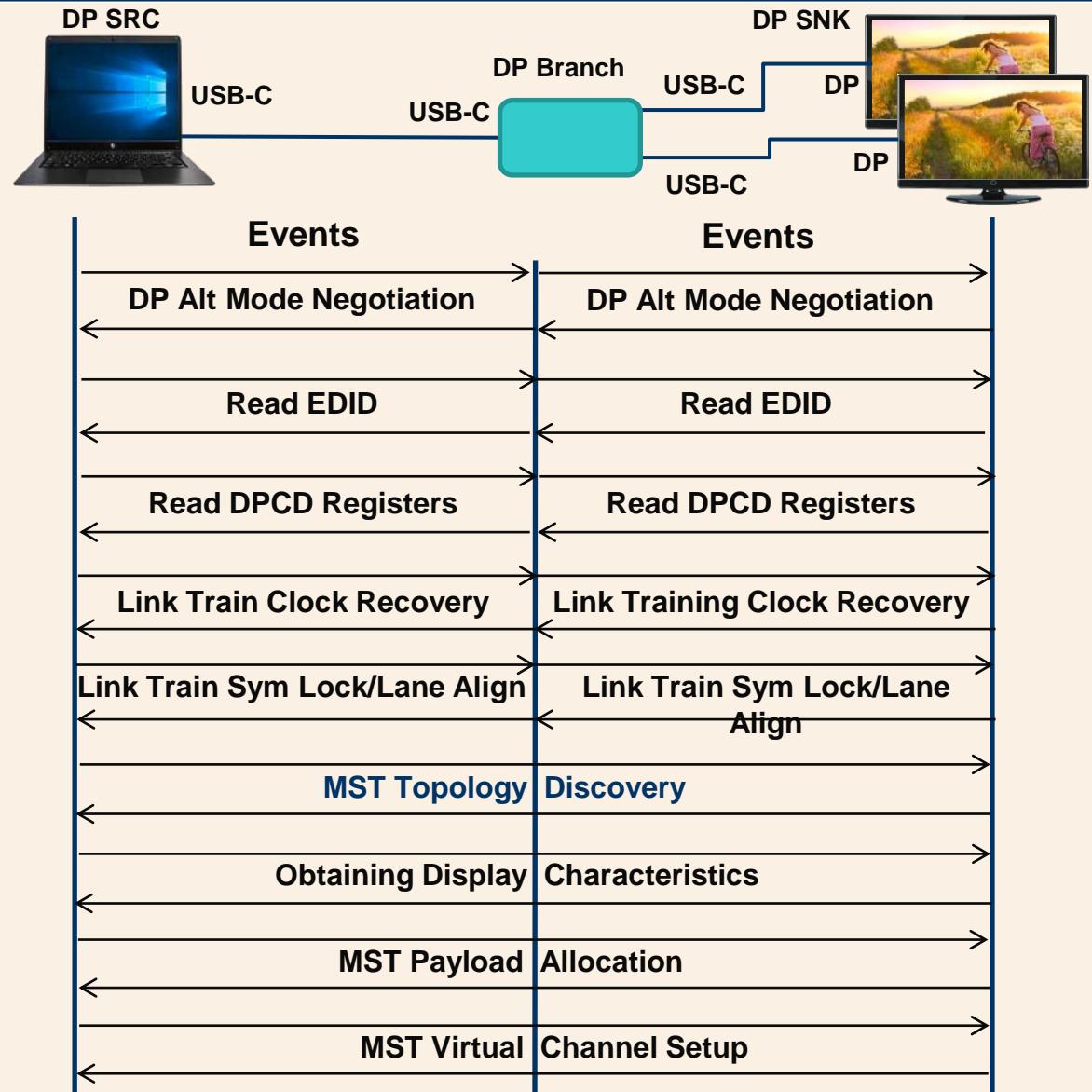
Multi-Stream Transport (MST) Architecture



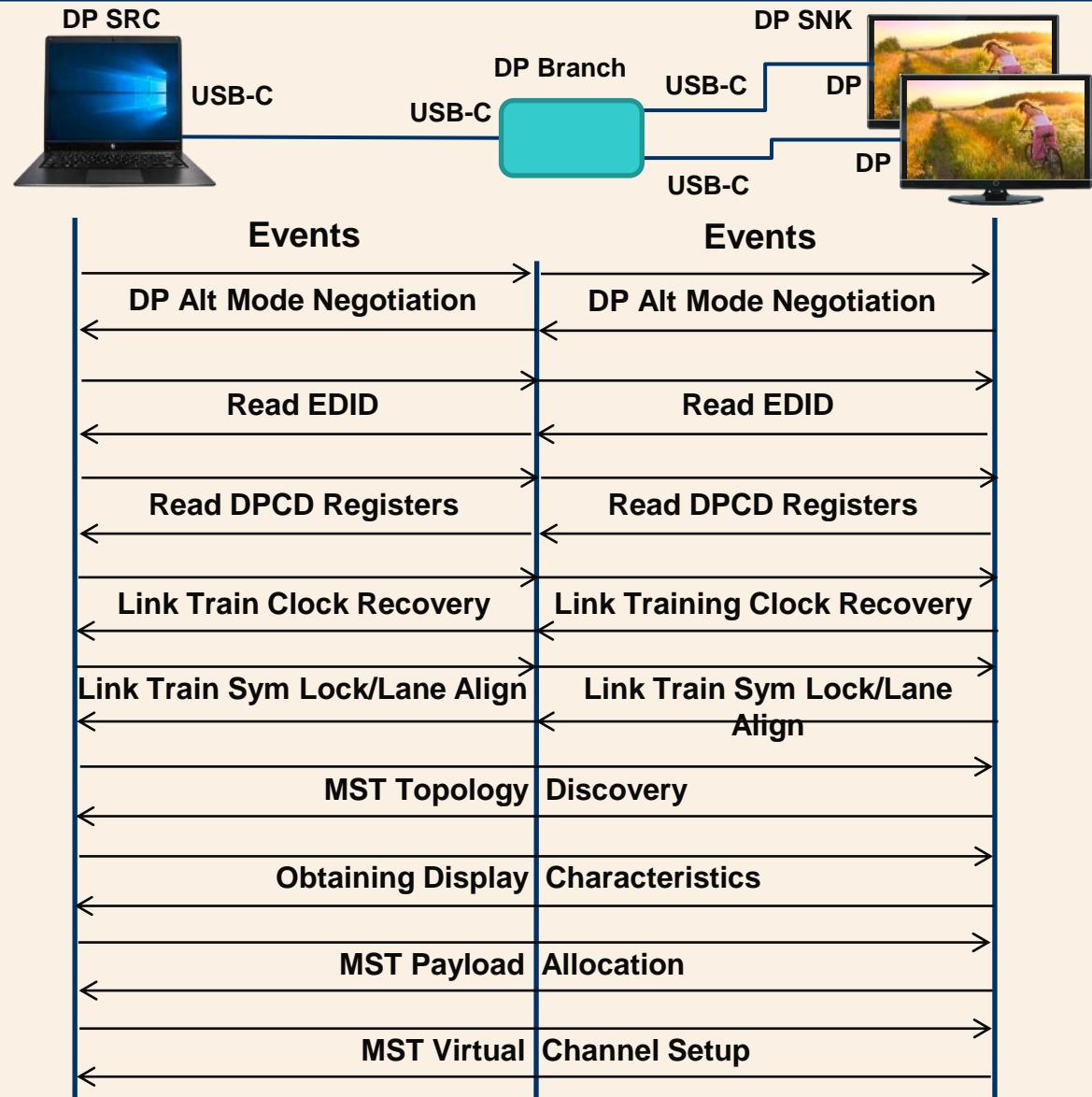
Multi-Stream Transport (MST) Architecture



Multi-Stream Configuration – Source Verifies Branch MST Capabilities



Multi-Stream Configuration – Source Sets MST Enable to Instruct Branch to use MST



ACA Data Viewer

Open Close Export Options Filter Find

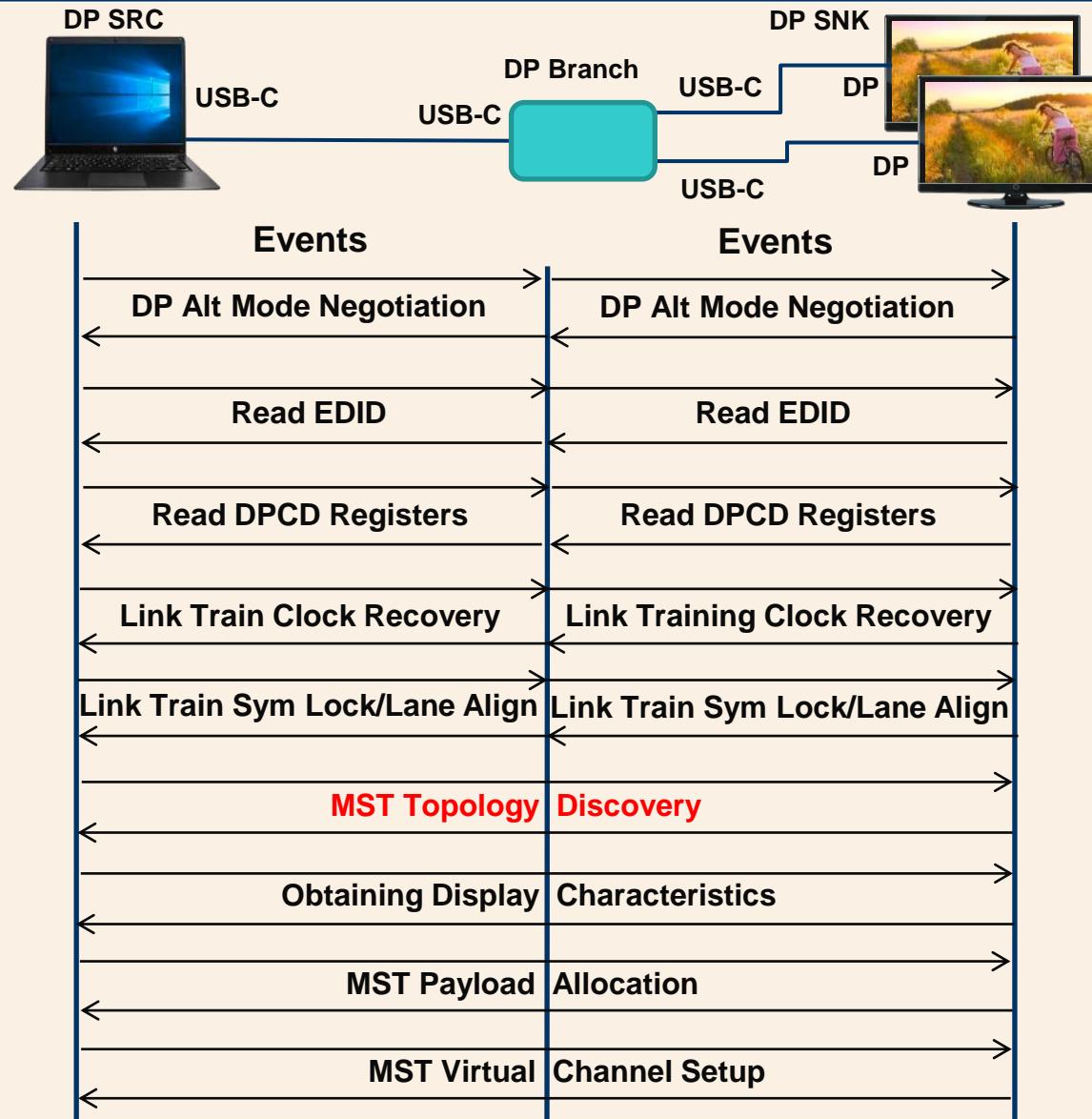
[20G_LTTPR_AUX_LT_FFE5] Events: 486 (996)

Start Time	Type	Direction	Command	Address	Length
+03:50:27.644454	Native	Request	Write	0x00111 (MSTM_CTRL)	1
00111: MSTM_CTRL					
Bit Name	Value Description				
0 MST_EN	Y(1)	1 UP_REQ_EN	Y(1)	2 UPSTREAM_IS_SRC	Y(1)
3	0 Reserved	4	0 Reserved	5	0 Reserved
6	0 Reserved	7	0 Reserved		
[0000][80 01 11 00 07 -- -- --][.....]					

239 DNAT DPUSBC-T11 +03:50:27.643179 < ACK 00
240 DNAT DPUSBC-T11 +03:50:27.643248 > R:701 EDP_GENERAL_CAPABILITY_1 L=1
241 DNAT DPUSBC-T11 +03:50:27.643322 < ACK 87
242 DNAT DPUSBC-T11 +03:50:27.643390 > R:702 EDP_BACKLIGHT_ADJ_CAPS L=1
243 DNAT DPUSBC-T11 +03:50:27.643464 < ACK 22
244 DNAT DPUSBC-T11 +03:50:27.643532 > R:725 EDP_PWMGEN_BIT_COUNT_MIN L=2
245 DNAT DPUSBC-T11 +03:50:27.643606 < ACK 02 OC
246 DNAT DPUSBC-T11 +03:50:27.643723 > R:28 RX_ALPM_CAPABILITIES L=1
247 DNAT DPUSBC-T11 +03:50:27.643797 < ACK 03
248 DNAT DPUSBC-T11 +03:50:27.643867 > W:116 RX_ALPM_CONFIGURATION L=1 01
249 DNAT DPUSBC-T11 +03:50:27.643949 < ACK
250 DNAT DPUSBC-T11 +03:50:27.644018 > R:21 MSTM_CAP L=1
251 DNAT DPUSBC-T11 +03:50:27.644092 < ACK 01
252 DNAT DPUSBC-T11 +03:50:27.644173 > R:0 DPCD_REV L=15
253 DNAT DPUSBC-T11 +03:50:27.644247 < ACK 14 1E C4 81 01 01 03 01 00 20 04 08 00 ...
254 DNAT DPUSBC-T11 +03:50:27.644350 > W:111 MSTM_CTRL L=1 07
255 DNAT DPUSBC-T11 +03:50:27.644356 < ACK
256 DNAT DPUSBC-T11 +03:50:27.644594 > W:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1 01
257 DNAT DPUSBC-T11 +03:50:27.644676 < ACK
258 DNAT DPUSBC-T11 +03:50:27.644738 > W:1C0 PAYLOAD_ALLOCATE_SET L=3 00 00 3F
259 DNAT DPUSBC-T11 +03:50:27.644836 < ACK
260 DNAT DPUSBC-T11 +03:50:27.644904 > R:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1
261 DNAT DPUSBC-T11 +03:50:27.644978 < ACK 01
262 DNAT DPUSBC-T11 +03:50:27.645066 > W:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1 01
263 DNAT DPUSBC-T11 +03:50:27.645148 < ACK
264 DNAT DPUSBC-T11 +03:50:27.645206 > R:30 GUID L=16
265 DNAT DPUSBC-T11 +03:50:27.645280 < ACK 00 01 02 03 04 05 06 07 08 09 0A 0B 0C ...
266 DNAT DPUSBC-T11 +03:50:27.645490 > W:1000 DOWN_REQ L=5 10 02 CB 14 AC
267 DNAT DPUSBC-T11 +03:50:27.645604 < ACK
268 DPSB DPUSBC-T11 +03:50:27.645605 > DN_REQ 1:0 --SE:0 2
269 DPMST DPUSBC-T11 +03:50:27.645606 > REQ: Clear Payload ID Table
270 DNAT DPUSBC-T11 +03:50:27.665050 > R:200 SINK_COUNT L=2
271 DNAT DPUSBC-T11 +03:50:27.665124 < ACK 41 10
272 DNAT DPUSBC-T11 +03:50:27.665203 > R:1400 DOWN REP L=16
273 DNAT DPUSBC-T11 +03:50:27.665277 < ACK 10 02 CB 14 AC 00 00 00 B2 00 00 00 00 ...
274 DPSB DPUSBC-T11 +03:50:27.665278 < DN_REQ 1:0 --SE:0 2
275 DPMST DPUSBC-T11 +03:50:27.665279 < RPL: ACK - Clear Payload ID Table
276 DNAT DPUSBC-T11 +03:50:27.665510 > W:201 DEVICE_SERVICE_IRQ_VECTOR L=1 10
277 DNAT DPUSBC-T11 +03:50:27.665592 < ACK

Topology Discovery

Multi-Stream Configuration – Read Branch Global Unique Identifier (GUID)



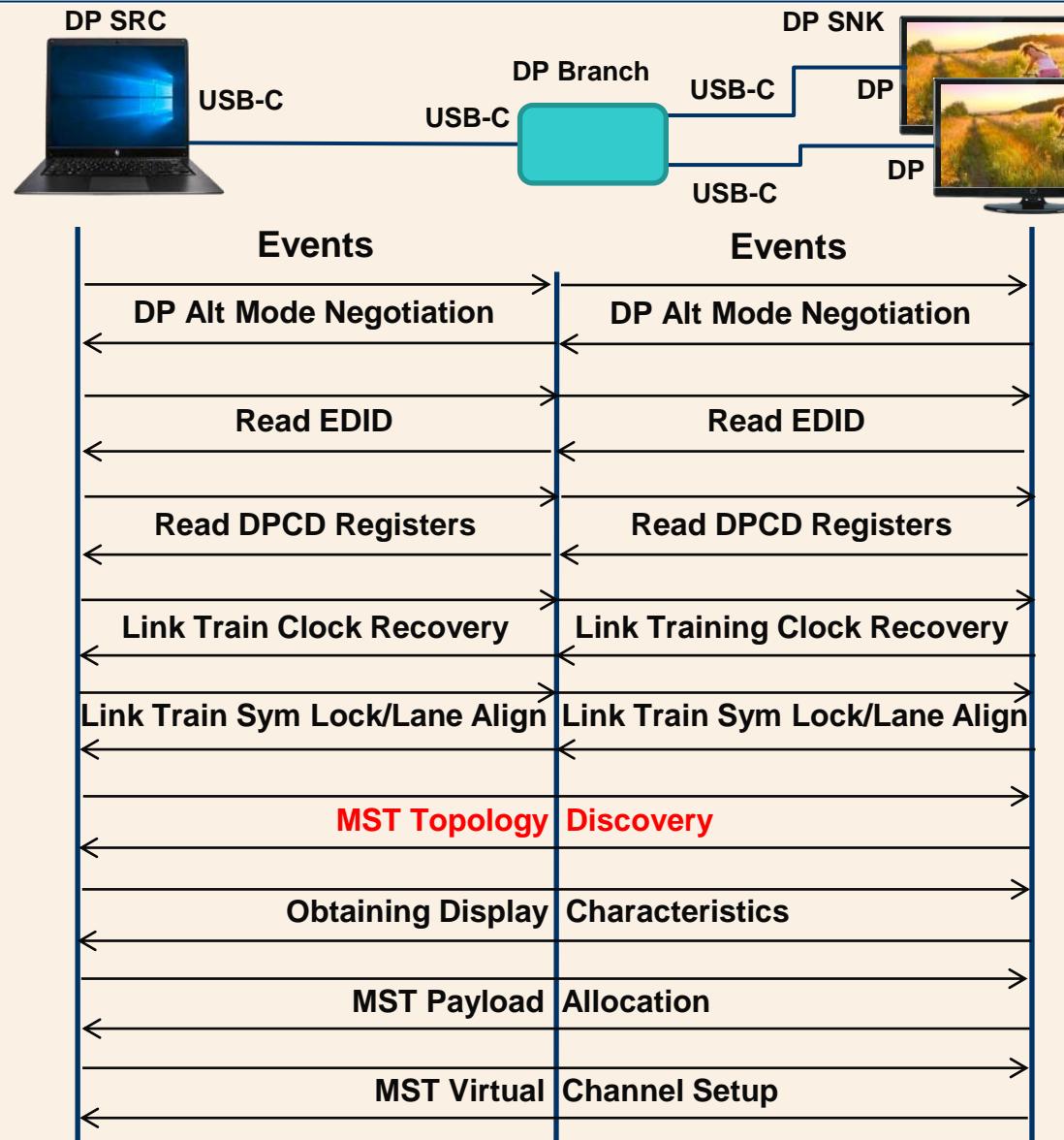
ACD Data Viewer

	Open	Close	Export	Options	Filter	Find
[20G_LTTPR_AUX_LT_FFE5] Events: 486 (996)						
239 DNAT DPUSBC-T11 +03:50:27.643179	< ACK 00					
240 DNAT DPUSBC-T11 +03:50:27.643248	> R:701 EDP_GENERAL_CAPABILITY_1 L=1					
241 DNAT DPUSBC-T11 +03:50:27.643322	< ACK 87					
242 DNAT DPUSBC-T11 +03:50:27.643390	> R:702 EDP_BACKLIGHT_ADJ_CAPS L=1					
243 DNAT DPUSBC-T11 +03:50:27.643464	< ACK 22					
244 DNAT DPUSBC-T11 +03:50:27.643532	> R:725 EDP_PWMGEN_BIT_COUNT_MIN L=2					
245 DNAT DPUSBC-T11 +03:50:27.643606	< ACK 02 OC					
246 DNAT DPUSBC-T11 +03:50:27.643723	> R:2E RX_ALPM_CAPABILITIES L=1					
247 DNAT DPUSBC-T11 +03:50:27.643797	< ACK 03					
248 DNAT DPUSBC-T11 +03:50:27.643867	> W:116 RX_ALPM_CONFIGURATION L=1 01					
249 DNAT DPUSBC-T11 +03:50:27.643949	< ACK					
250 DNAT DPUSBC-T11 +03:50:27.644018	> R:21 MSTN_CAP L=1					
251 DNAT DPUSBC-T11 +03:50:27.644092	< ACK 01					
252 DNAT DPUSBC-T11 +03:50:27.644173	> R:0 DPDC_REV L=15					
253 DNAT DPUSBC-T11 +03:50:27.644247	< ACK 14 1E C4 81 01 01 03 01 00 20 04 08 00 00 81					
254 DNAT DPUSBC-T11 +03:50:27.644454	> W:111 MSTN_CTRL L=1 07					
255 DNAT DPUSBC-T11 +03:50:27.644536	< ACK					
256 DNAT DPUSBC-T11 +03:50:27.644594	> W:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1 01					
257 DNAT DPUSBC-T11 +03:50:27.644676	< ACK					
258 DNAT DPUSBC-T11 +03:50:27.644738	> W:1C0 PAYLOAD_ALLOCATE_SET L=3 00 00 3F					
259 DNAT DPUSBC-T11 +03:50:27.644836	< ACK					
260 DNAT DPUSBC-T11 +03:50:27.644904	> R:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1					
261 DNAT DPUSBC-T11 +03:50:27.644978	< ACK 01					
262 DNAT DPUSBC-T11 +03:50:27.645066	> W:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1 01					
263 DNAT DPUSBC-T11 +03:50:27.645148	< ACK					
264 DNAT DPUSBC-T11 +03:50:27.645160	> R:30 GUID L=16					
265 DNAT DPUSBC-T11 +03:50:27.645490	< ACK 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0...					
266 DNAT DPUSBC-T11 +03:50:27.645604	> W:1000 DOWN_REQ L=5 10 02 CB 14 AC					
267 DNAT DPUSBC-T11 +03:50:27.645604	< ACK					
268 DPSB DPUSBC-T11 +03:50:27.645605	> DN_REQ 1:0 --SE:0 2					
269 DPMST DPUSBC-T11 +03:50:27.645606	> REQ: Clear Payload ID Table					
270 DNAT DPUSBC-T11 +03:50:27.665050	> R:200 SINK_COUNT L=2					
271 DNAT DPUSBC-T11 +03:50:27.665124	< ACK 41 10					
272 DNAT DPUSBC-T11 +03:50:27.665203	> R:1400 DOWN_REQ L=16					
273 DNAT DPUSBC-T11 +03:50:27.665277	< ACK 10 02 CB 14 AC 00 00 00 B2 00 00 00 00 3...					
274 DPSB DPUSBC-T11 +03:50:27.665278	< DN_REQ 1:0 --SE:0 2					
275 DPMST DPUSBC-T11 +03:50:27.665279	< RPL: ACK - Clear Payload ID Table					
276 DNAT DPUSBC-T11 +03:50:27.665510	> W:201 DEVICE_SERVICE_IRQ_VECTOR L=1 10					
277 DNAT DPUSBC-T11 +03:50:27.665592	< ACK					

Start Time: +03:50:27.645280
Type: Native
Direction: Reply
Command: ACK
Reply to Read Request.

00030: GUID
Offset: 0 to 15
Bytes: 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F
[0000][00 01 02 03 04 05 06].....
[0008][07 08 09 0A 0B 0C 0D 0E].....
[0010][OF -----]..

Multi-Stream Configuration – Topology Discovery, Sideband Message Header



ACA Data Viewer window showing the log of events:

Log Content:

```

[20G_LTTPR_AUX_LT_FFE5] Events: 486 (996)
244 DNAT DPUSBC-T11 +03:50:27.643532 > R:725 EDP_PWMGEN_BIT_COUNT_MIN L=2
245 DNAT DPUSBC-T11 +03:50:27.643606 < ACK 02 0C
246 DNAT DPUSBC-T11 +03:50:27.643723 > R:2E RX_ALPM_CAPABILITIES L=1
247 DNAT DPUSBC-T11 +03:50:27.643797 < ACK 03
248 DNAT DPUSBC-T11 +03:50:27.643867 > W:116 RX_ALPM_CONFIGURATION L=1 01
249 DNAT DPUSBC-T11 +03:50:27.643949 < ACK
250 DNAT DPUSBC-T11 +03:50:27.644018 > R:21 MSTM_CAP L=1
251 DNAT DPUSBC-T11 +03:50:27.644092 < ACK 01
252 DNAT DPUSBC-T11 +03:50:27.644173 > R:0 DPCD_REV L=15
253 DNAT DPUSBC-T11 +03:50:27.644247 < ACK 14 1E C4 81 01 01 03 01 00 20 04 08 00 00 81
254 DNAT DPUSBC-T11 +03:50:27.644454 > W:111 MSTM_CTRL L=1 07
255 DNAT DPUSBC-T11 +03:50:27.644536 < ACK
256 DNAT DPUSBC-T11 +03:50:27.644594 > W:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1 01
257 DNAT DPUSBC-T11 +03:50:27.644676 < ACK
258 DNAT DPUSBC-T11 +03:50:27.644738 > W:1C0 PAYLOAD_ALLOCATE_SET L=3 00 00 3F
259 DNAT DPUSBC-T11 +03:50:27.644836 < ACK
260 DNAT DPUSBC-T11 +03:50:27.644904 > R:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1
261 DNAT DPUSBC-T11 +03:50:27.644976 < ACK 01
262 DNAT DPUSBC-T11 +03:50:27.645066 > W:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1 01
263 DNAT DPUSBC-T11 +03:50:27.645148 < ACK
264 DNAT DPUSBC-T11 +03:50:27.645206 > R:30 GUID L=16
265 DNAT DPUSBC-T11 +03:50:27.645280 < ACK 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D ...
266 DNAT DPUSBC-T11 +03:50:27.645490 > W:1000 DOWN_REQ L=5 10 02 CB 14 AC
267 DNAT DPUSBC-T11 +03:50:27.645644 < ACK
268 DPSB DPUSBC-T11 +03:50:27.645666 > DN_REQ 1:0 --SE:0 2
269 DPMST DPUSBC-T11 +03:50:27.645676 > REQ: Clear Payload ID Table
270 DNAT DPUSBC-T11 +03:50:27.665050 > R:200 SINK_COUNT L=2
271 DNAT DPUSBC-T11 +03:50:27.665124 < ACK 41 10
272 DNAT DPUSBC-T11 +03:50:27.665203 > R:1400 DOWN REP L=16
273 DNAT DPUSBC-T11 +03:50:27.665277 < ACK 10 02 CB 14 AC 00 00 B2 00 00 00 00 00 ...
274 DPSB DPUSBC-T11 +03:50:27.665278 < DN_REQ 1:0 --SE:0 2
275 DPMST DPUSBC-T11 +03:50:27.665279 < RPL: ACK - Clear Payload ID Table
276 DNAT DPUSBC-T11 +03:50:27.665510 > W:201 DEVICE_SERVICE_IRQ_VECTOR L=1 10
277 DNAT DPUSBC-T11 +03:50:27.665592 < ACK
278 DNAT DPUSBC-T11 +03:50:27.666253 > W:1000 DOWN_REQ L=5 10 02 D8 01 D5
279 DNAT DPUSBC-T11 +03:50:27.666368 < ACK
280 DPSB DPUSBC-T11 +03:50:27.666369 > DN_REQ 1:0 --SE:1 2
281 DPMST DPUSBC-T11 +03:50:27.666370 > REQ: Link Address
282 DNAT DPUSBC-T11 +03:50:27.686188 > R:200 SINK_COUNT L=2

```

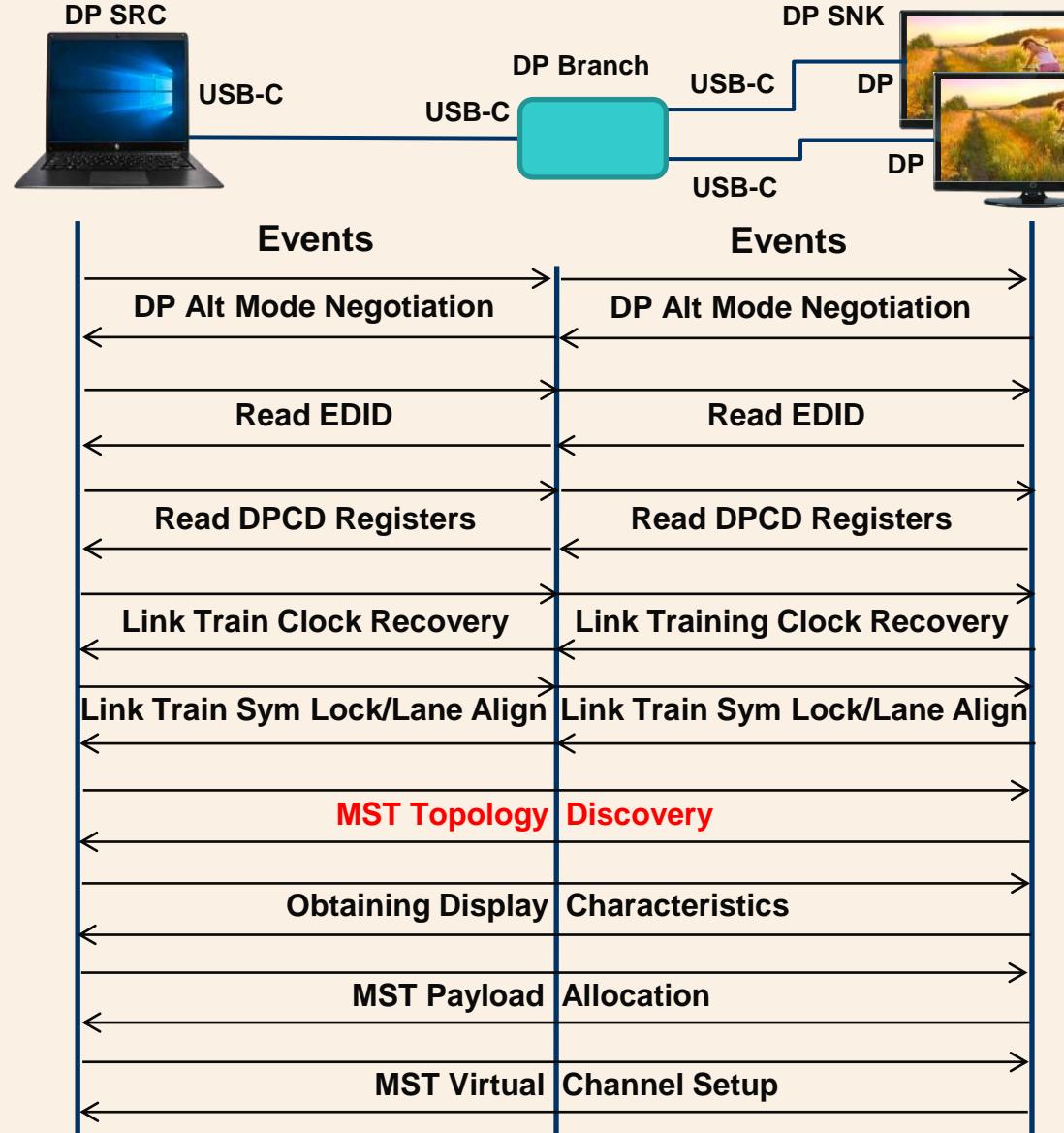
Details Panel:

- Start Time: +03:50:27.645605
- Type: Down Request
- Header CRC: OK
- Body CRC: OK
- Link_Count_Total: 1
- Link_Count_Remaining: 0
- Relative_Address: Broadcast_Message: false Path_Message: false
- Start_Of_Message_Transaction: true
- End_Of_Message_Transaction: true
- Message_Sequence_No: 0
- Sideband_MSG_Header_CRC: Bh
- Sideband_MSG_Body_Length: 2
- Sideband_MSG_Data_CRC: ACh
- Sideband_MSG_Data:

Raw Data:

```
[0000][14 --- --- --- ---]....]
```

Multi-Stream Configuration – Topology Discovery, Clear Payload ID Table



ACA Data Viewer

Open Close Export Options Filter Find

20G_LTTPR_AUX_LT_FFE5 Events: 486 (996)

```

252 DNAT DPUSBC-T11 +03:50:27.644173 > R:0 DPDC_REV L=15
253 DNAT DPUSBC-T11 +03:50:27.644247 < ACK 14 1E C4 81 01 01 03 01 00 20 04 08 00 00 81
254 DNAT DPUSBC-T11 +03:50:27.644454 > W:111 MSTM_CTRL L=1 07
255 DNAT DPUSBC-T11 +03:50:27.644536 < ACK
256 DNAT DPUSBC-T11 +03:50:27.644594 > W:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1 01
257 DNAT DPUSBC-T11 +03:50:27.644676 < ACK
258 DNAT DPUSBC-T11 +03:50:27.644738 > W:1C0 PAYLOAD_ALLOCATE_SET L=3 00 00 3F
259 DNAT DPUSBC-T11 +03:50:27.644836 < ACK
260 DNAT DPUSBC-T11 +03:50:27.644904 > R:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1
261 DNAT DPUSBC-T11 +03:50:27.644978 < ACK 01
262 DNAT DPUSBC-T11 +03:50:27.645066 > W:2C0 PAYLOAD_TABLE_UPDATE_STATUS L=1 01
263 DNAT DPUSBC-T11 +03:50:27.645148 < ACK
264 DNAT DPUSBC-T11 +03:50:27.645206 > R:30 GUID L=16
265 DNAT DPUSBC-T11 +03:50:27.645280 < ACK 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D ...
266 DNAT DPUSBC-T11 +03:50:27.645490 > W:1000 DOWN_REQ L=5 10 02 CB 14 AC
267 DNAT DPUSBC-T11 +03:50:27.645604 < ACK
268 DPSB DPUSBC-T11 +03:50:27.645605 > DN_REQ 1:0 --SE:0 2
269 DPMST DPUSBC-T11 +03:50:27.645605 > REQ: Clear Payload ID Table
270 DNAT DPUSBC-T11 +03:50:27.665050 < R:200 SINK_COUNT L=2
271 DNAT DPUSBC-T11 +03:50:27.665124 < ACK 41 10
272 DNAT DPUSBC-T11 +03:50:27.665203 > R:1400 DOWN REP L=16
273 DNAT DPUSBC-T11 +03:50:27.665277 < ACK 10 02 CB 14 AC 00 00 00 B2 00 00 00 00 00 ...
274 DPSB DPUSBC-T11 +03:50:27.665278 < DN_REQ 1:0 --SE:0 2
275 DPMST DPUSBC-T11 +03:50:27.665279 < RPL: ACK - Clear Payload ID Table
276 DNAT DPUSBC-T11 +03:50:27.665510 > W:201 DEVICE_SERVICE_IRQ_VECTOR L=1 10
277 DNAT DPUSBC-T11 +03:50:27.665592 < ACK
278 DNAT DPUSBC-T11 +03:50:27.666253 > W:1000 DOWN_REQ L=5 10 02 D8 01 D5
279 DNAT DPUSBC-T11 +03:50:27.666368 < ACK
280 DPSB DPUSBC-T11 +03:50:27.666369 > DN_REQ 1:0 --SE:1 2
281 DPMST DPUSBC-T11 +03:50:27.666370 > REQ: Link Address
282 DNAT DPUSBC-T11 +03:50:27.666188 > R:200 SINK_COUNT L=2
283 DNAT DPUSBC-T11 +03:50:27.666263 < ACK 41 10
284 DNAT DPUSBC-T11 +03:50:27.666348 > R:1400 DOWN REP L=16
285 DNAT DPUSBC-T11 +03:50:27.666423 < ACK 10 11 94 01 32 DC C6 CB 77 00 00 00 31 DC ...
286 DNAT DPUSBC-T11 +03:50:27.666647 > R:1410 DOWN REP(16) L=4
287 DNAT DPUSBC-T11 +03:50:27.666722 < ACK 77 00 00 19
288 DPSB DPUSBC-T11 +03:50:27.666723 < DN_REQ 1:0 --S:1 17
289 DNAT DPUSBC-T11 +03:50:27.666828 > W:201 DEVICE_SERVICE_IRQ_VECTOR L=1 10
290 DNAT DPUSBC-T11 +03:50:27.666911 < ACK

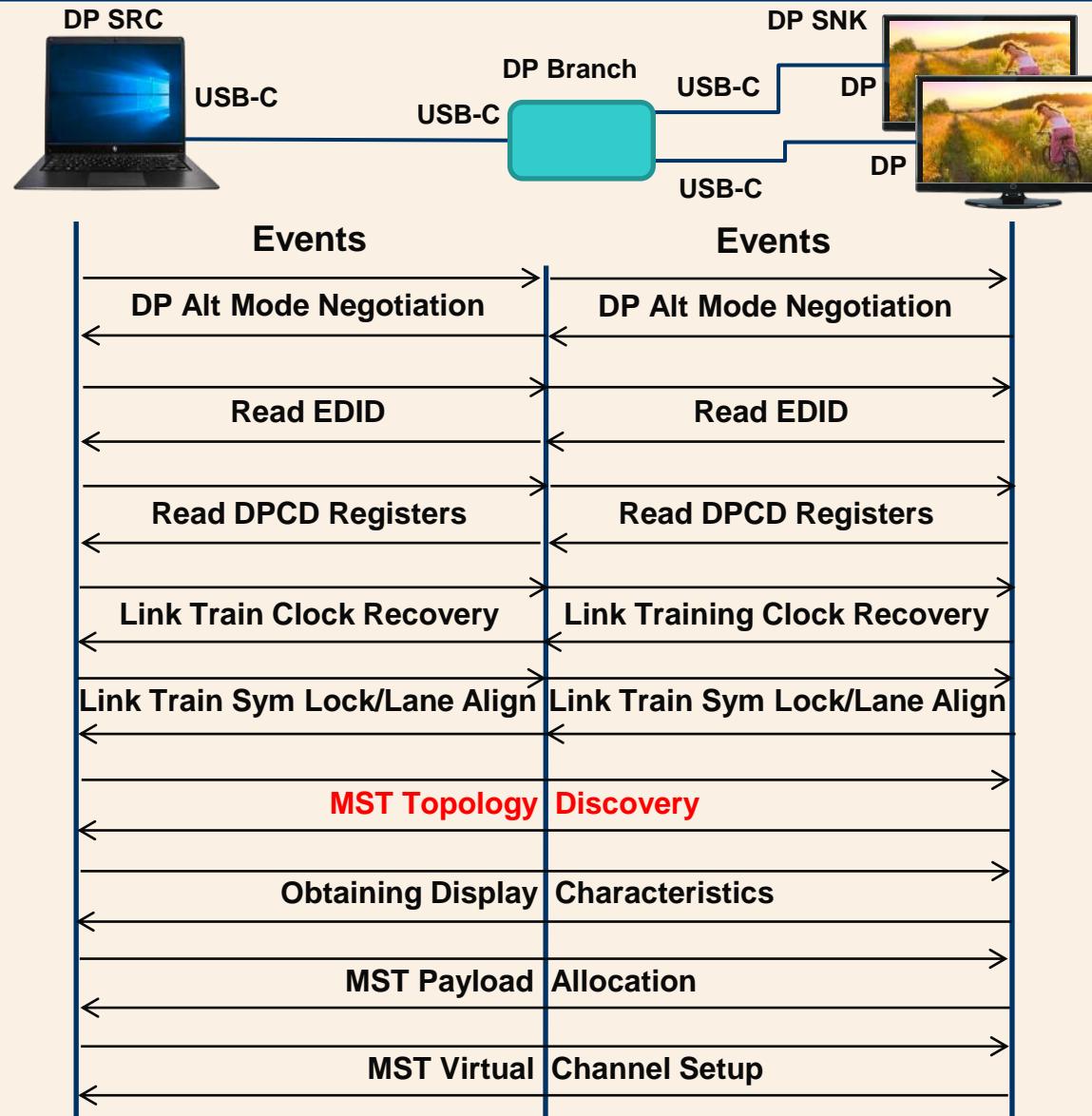
```

Start Time: +03:50:27.645606
Type: Clear Payload ID Table
Source: Down Request
Sequence No: 0

Raw Data:

```
[0000][14 --- --- --- --- ---] [..]
```

Multi-Stream Configuration – Topology Discovery - Link Address Message Header



ACA Data Viewer

20G LTTPR_AUX_LT_FFE5 Events: 132 (996)

78	DPLT	DPUSBC-T11	+03:50:27.641021
79	DPLT	DPUSBC-T11	+03:50:27.641095
80	DPLT	DPUSBC-T11	+03:50:27.641243
81	DPLT	DPUSBC-T11	+03:50:27.641317
82	DPSB	DPUSBC-T11	+03:50:27.645605
83	DPMST	DPUSBC-T11	+03:50:27.645606
84	DPSB	DPUSBC-T11	+03:50:27.665278
85	DPMST	DPUSBC-T11	+03:50:27.665279
86	DPSB	DPUSBC-T11	+03:50:27.666370
87	DPMST	DPUSBC-T11	+03:50:27.666370
88	DPSB	DPUSBC-T11	+03:50:27.686723
89	DPSB	DPUSBC-T11	+03:50:27.707684
90	DPSB	DPUSBC-T11	+03:50:27.727502
91	DPSB	DPUSBC-T11	+03:50:27.746904
92	DPSB	DPUSBC-T11	+03:50:27.766974
93	DPSB	DPUSBC-T11	+03:50:27.786886
94	DPSB	DPUSBC-T11	+03:50:27.806568
95	DPMST	DPUSBC-T11	+03:50:27.806569
96	DPSB	DPUSBC-T11	+03:50:27.807100
97	DPMST	DPUSBC-T11	+03:50:27.807101
98	DPSB	DPUSBC-T11	+03:50:27.827602
99	DPMST	DPUSBC-T11	+03:50:27.827603
100	DPSB	DPUSBC-T11	+03:50:27.828307
101	DPMST	DPUSBC-T11	+03:50:27.828308
102	DPSB	DPUSBC-T11	+03:50:27.848573
103	DPMST	DPUSBC-T11	+03:50:27.848574
104	DPSB	DPUSBC-T11	+03:50:27.849383
105	DPMST	DPUSBC-T11	+03:50:27.849384
106	DPSB	DPUSBC-T11	+03:50:27.868963
107	DPMST	DPUSBC-T11	+03:50:27.868964
108	DPSB	DPUSBC-T11	+03:50:27.869751
109	DPMST	DPUSBC-T11	+03:50:27.869752
110	DPSB	DPUSBC-T11	+03:50:27.889965
111	DPMST	DPUSBC-T11	+03:50:27.889966
112	DPSB	DPUSBC-T11	+03:50:27.891215
113	DPMST	DPUSBC-T11	+03:50:27.891216
114	DPSB	DPUSBC-T11	+03:50:27.911900
115	DPMST	DPUSBC-T11	+03:50:27.911901

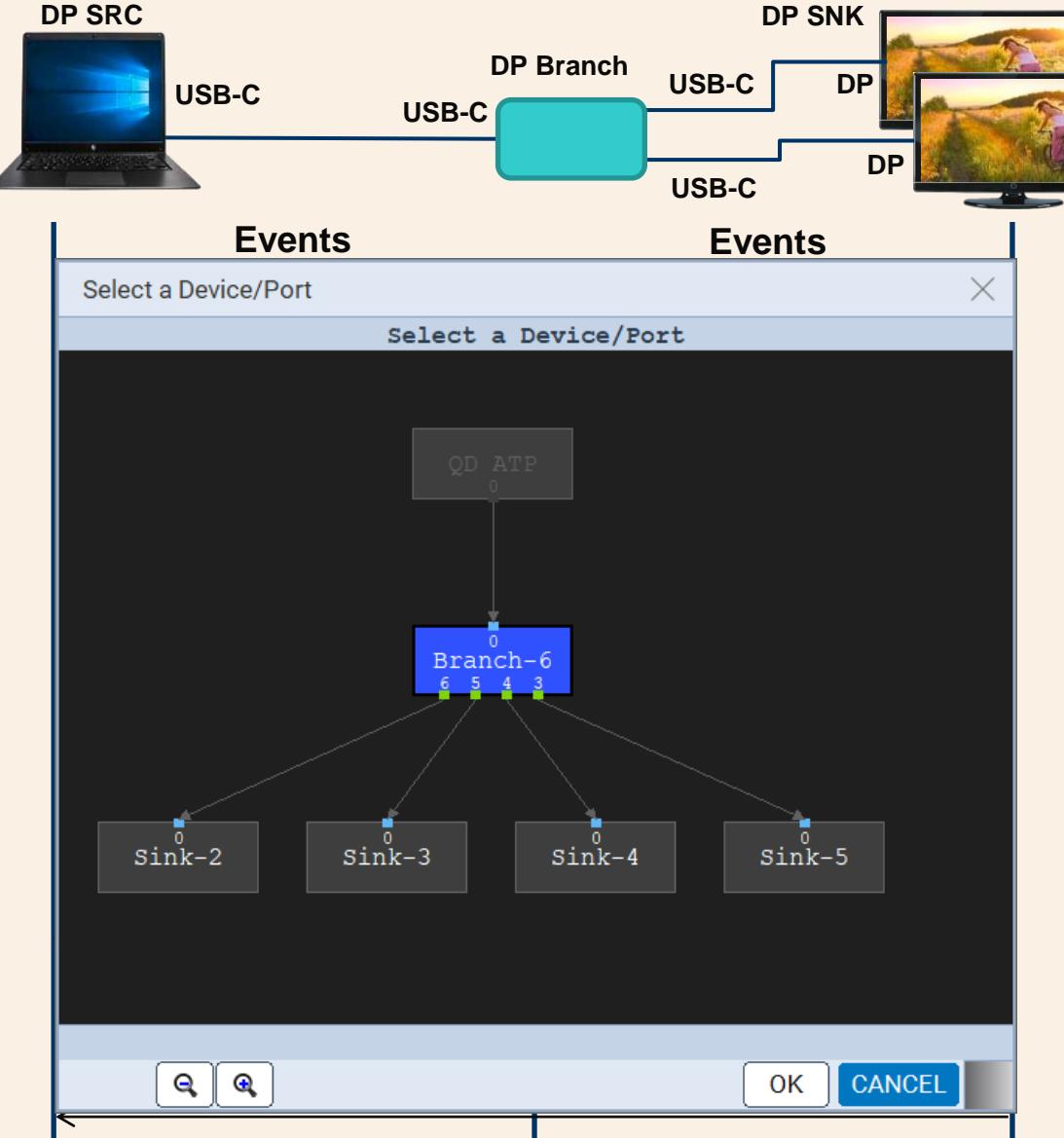
Start Time: +03:50:27.666369
Type: Down Request
Header CRC: OK
Body CRC: OK

Link_Count_Total: 1
Link_Count_Remaining: 0
Relative_Address:
Broadcast_Message: false
Path_Message: false
Start_Of_Message_Transaction: true
End_Of_Message_Transaction: true
Message_Sequence_No: 1
Sideband_MSG_Header_CRC: 8h

Sideband_MSG_Body_Length: 2
Sideband_MSG_Data_CRC: D5h
Sideband_MSG_Data:
[0000][01-----][. . .]

Raw Data:
[0000][10 02 D8 01 D5 -----][. . .]

Multi-Stream Configuration – Topology Discovery - Link Address Message



ACA Data Viewer

Open Close Export Options Filter Find

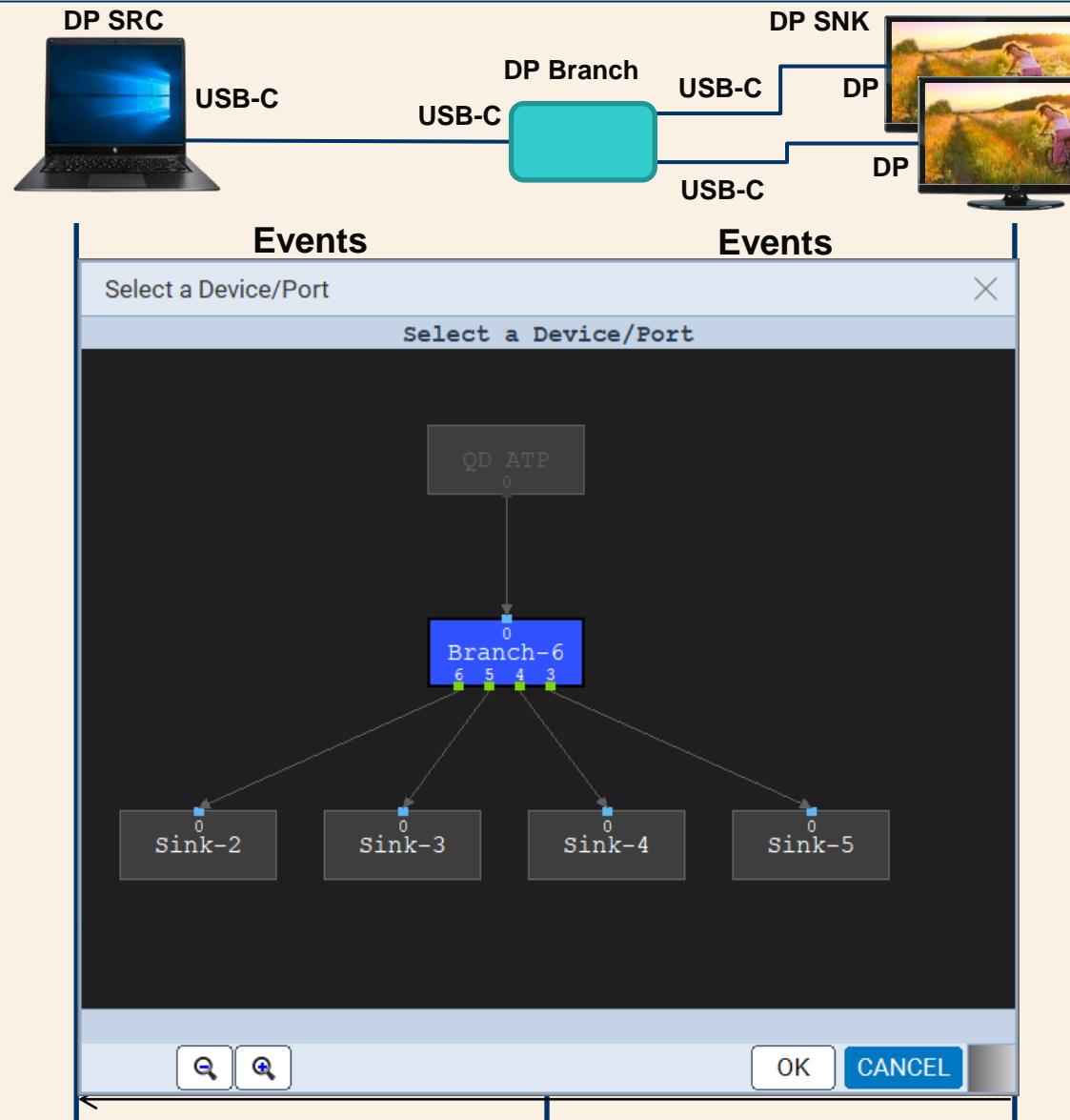
[20G LTTPR_AUX_LT_FFE5] Events: 132 (996)

78 DPLT DPUSBC-T11 +03:50:27.641021	> R:100 LINK_BW_SET L=9
79 DPLT DPUSBC-T11 +03:50:27.641095	< ACK 02 84 00 05 05 05 05 00 02
80 DPLT DPUSBC-T11 +03:50:27.641243	> R:100 LINK_BW_SET L=9
81 DPLT DPUSBC-T11 +03:50:27.641317	< ACK 02 84 00 05 05 05 05 00 02
82 DPSB DPUSBC-T11 +03:50:27.645605	> DN_REQ 1:0 --SE:0 2
83 DPMST DPUSBC-T11 +03:50:27.645606	> REQ: Clear Payload ID Table
84 DPSB DPUSBC-T11 +03:50:27.665278	< DN REP 1:0 --SE:0 2
85 DPMST DPUSBC-T11 +03:50:27.665279	< RPL: ACK - Clear Payload II
86 DPSB DPUSBC-T11 +03:50:27.666369	> DN_REQ 1:0 --SE:1 2
87 DPMST DPUSBC-T11 +03:50:27.666370	> REQ: Link Address
88 DPSB DPUSBC-T11 +03:50:27.686723	< DN REP 1:0 --S:1 17
89 DPSB DPUSBC-T11 +03:50:27.707684	< DN REP 1:0 -----:1 17
90 DPSB DPUSBC-T11 +03:50:27.727502	< DN REP 1:0 -----:1 17
91 DPSB DPUSBC-T11 +03:50:27.746904	< DN REP 1:0 -----:1 17
92 DPSB DPUSBC-T11 +03:50:27.766974	< DN REP 1:0 -----:1 17
93 DPSB DPUSBC-T11 +03:50:27.786886	< DN REP 1:0 -----:1 17
94 DPSB DPUSBC-T11 +03:50:27.80656	< DN REP 1:0 -----:1 5
95 DPMST DPUSBC-T11 +03:50:27.80671	< RPL: ACK - Link Address
96 DPSB DPUSBC-T11 +03:50:27.807101	> DN_REQ 1:0 --PSE:0 3
97 DPMST DPUSBC-T11 +03:50:27.827602	> REQ: Enum Path Resources
98 DPSB DPUSBC-T11 +03:50:27.827603	< DN REP 1:0 --PSE:0 7
99 DPMST DPUSBC-T11 +03:50:27.827603	< RPL: ACK - Enum Path Resources
100 DPSB DPUSBC-T11 +03:50:27.828307	> DN_REQ 1:0 --PSE:1 3
101 DPMST DPUSBC-T11 +03:50:27.828308	> REQ: Enum Path Resources
102 DPSB DPUSBC-T11 +03:50:27.848573	< DN REP 1:0 --PSE:1 7
103 DPMST DPUSBC-T11 +03:50:27.848574	< RPL: ACK - Enum Path Resources
104 DPSB DPUSBC-T11 +03:50:27.849383	> DN_REQ 1:0 --PSE:0 3
105 DPMST DPUSBC-T11 +03:50:27.849384	> REQ: Enum Path Resources
106 DPSB DPUSBC-T11 +03:50:27.868963	< DN REP 1:0 --PSE:0 7
107 DPMST DPUSBC-T11 +03:50:27.868964	< RPL: ACK - Enum Path Resources
108 DPSB DPUSBC-T11 +03:50:27.869751	> DN_REQ 1:0 --PSE:1 3
109 DPMST DPUSBC-T11 +03:50:27.869752	> REQ: Enum Path Resources
110 DPSB DPUSBC-T11 +03:50:27.889965	< DN REP 1:0 --PSE:1 7
111 DPMST DPUSBC-T11 +03:50:27.889966	< RPL: ACK - Enum Path Resources

Start Time: +03:50:27.806569
Type: ACK - Link Address
Source: Down Reply
Sequence No: 1
Global_Unique_Identifier: 32 DC C6 CB 77 00 00 00 31 DC C6 CB 77 00 00 00
Number_Of_Ports: 5
Port 0 Description --
Input_Port: 1 (RX)
Peer_Device_Type: 1
- Source device or SST Branch device connected to an upstream port.
Port_Number: 0
Messaging_Capability_Status: 1
DisplayPort_Device_Plug_Status: 1 Connected & Initialized
-- Port 1 Description --
Input_Port: 0 (TX)
Peer_Device_Type: 3
- SST Sink device or stream Sink in an MST Sink/Composite device.
Port_Number: 3
Messaging_Capability_Status: 0
DisplayPort_Device_Plug_Status: 1 Connected & Initialized
Legacy_Device_Plug_Status: 0
DPID Revision: 14h
Peer_Global_Unique_Identifier: 31 DC C6 CB 77 00 00 00 31 DC C6 CB 77 00 00 00
Number_SD_Sreams: 1
Number_SD_Sream_Sinks: 2
Port 2 Description --
Input_Port: 0 (TX)
Peer_Device_Type: 3
- SST Sink device or stream Sink in an MST Sink/Composite device.
Port_Number: 4
Messaging_Capability_Status: 0
DisplayPort_Device_Plug_Status: 1 Connected & Initialized
Legacy_Device_Plug_Status: 0
DPID Revision: 14h
Peer_Global_Unique_Identifier: 33 DC C6 CB 77 00 00 00 31 DC C6 CB 77 00 00 00
Number_SD_Sreams: 1
Number_SD_Sream_Sinks: 2

95: < RPL: ACK - Link Address

Multi-Stream Configuration – Topology Discovery - Link Address Message



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[20G LTTPR_AUX_LT_FFS] Events: 132 (996)

78	DPLT	DPUSBC-T11	+03:50:27.641021	> R:100 LINK_BW_SET L=9
79	DPLT	DPUSBC-T11	+03:50:27.641095	< ACK 02 84 00 05 05 05 05 00 02
80	DPLT	DPUSBC-T11	+03:50:27.641243	> R:100 LINK_BW_SET L=9
81	DPLT	DPUSBC-T11	+03:50:27.641317	< ACK 02 84 00 05 05 05 05 00 02
82	DPSB	DPUSBC-T11	+03:50:27.645605	> DN_REQ 1:0 --SE:0 2
83	DPMST	DPUSBC-T11	+03:50:27.645606	< REQ: Clear Payload ID Table
84	DPSB	DPUSBC-T11	+03:50:27.665278	< DN_REQ 1:0 --SE:0 2
85	DPMST	DPUSBC-T11	+03:50:27.665279	< RPL: ACK - Clear Payload ID ...
86	DPSB	DPUSBC-T11	+03:50:27.666369	> DN_REQ 1:0 --SE:1 2
87	DPMST	DPUSBC-T11	+03:50:27.666370	> REQ: Link Address
88	DPSB	DPUSBC-T11	+03:50:27.686723	< DN_REQ 1:0 --S:1 17
89	DPSB	DPUSBC-T11	+03:50:27.707684	< DN_REQ 1:0 ----:1 17
90	DPSB	DPUSBC-T11	+03:50:27.727502	< DN_REQ 1:0 ----:1 17
91	DPSB	DPUSBC-T11	+03:50:27.746904	< DN_REQ 1:0 ----:1 17
92	DPSB	DPUSBC-T11	+03:50:27.766974	< DN_REQ 1:0 ----:1 17
93	DPSB	DPUSBC-T11	+03:50:27.786886	< DN_REQ 1:0 ----:1 17
94	DPSB	DPUSBC-T11	+03:50:27.806568	< DN_REQ 1:0 ----:E:1 5
95	DPMST	DPUSBC-T11	+03:50:27.807100	< RPL: ACK - Link Address
96	DPSB	DPUSBC-T11	+03:50:27.807100	> DN_REQ 1:0 -PSE:0 3
97	DPMST	DPUSBC-T11	+03:50:27.807101	> REQ: Enum Path Resources
98	DPSB	DPUSBC-T11	+03:50:27.827602	< DN_REQ 1:0 -PSE:0 7
99	DPMST	DPUSBC-T11	+03:50:27.827603	< RPL: ACK - Enum Path Reso
100	DPSB	DPUSBC-T11	+03:50:27.828307	> DN_REQ 1:0 -PSE:1 3
101	DPMST	DPUSBC-T11	+03:50:27.828308	> REQ: Enum Path Resources
102	DPSB	DPUSBC-T11	+03:50:27.848573	< DN_REQ 1:0 -PSE:1 7
103	DPMST	DPUSBC-T11	+03:50:27.848574	< RPL: ACK - Enum Path Resources
104	DPSB	DPUSBC-T11	+03:50:27.849383	> DN_REQ 1:0 -PSE:0 3
105	DPMST	DPUSBC-T11	+03:50:27.849384	> REQ: Enum Path Resources
106	DPSB	DPUSBC-T11	+03:50:27.868963	< DN_REQ 1:0 -PSE:0 7
107	DPMST	DPUSBC-T11	+03:50:27.868964	< RPL: ACK - Enum Path Resources
108	DPSB	DPUSBC-T11	+03:50:27.869751	> DN_REQ 1:0 -PSE:1 3
109	DPMST	DPUSBC-T11	+03:50:27.869752	> REQ: Enum Path Resources
110	DPSB	DPUSBC-T11	+03:50:27.889965	< DN_REQ 1:0 -PSE:1 7
111	DPMST	DPUSBC-T11	+03:50:27.889966	< RPL: ACK - Enum Path Resources

Port 2 Description --
Input_Port: 0 (TX)
Peer_Device_Type: 3
- SST Sink device or stream Sink in an MST Sink/Composite device.
Port Number: 4
DisplayPort_Device_Plug_Status: 1 Connected & Initialized
Legacy_Device_Plug_Status: 0
DPID_Revision: 14h
Peer_Global_Unique_Identifier: 33 DC C6 CB 77 00 00 00 31 DC C6 CB 77 00 00 00
Number_SD_PStreams: 1
Number_SD_Stream_Sinks: 2

Port 3 Description --
Input_Port: 0 (TX)
Peer_Device_Type: 3
- SST Sink device or stream Sink in an MST Sink/Composite device.
Port Number: 5
Messaging_Capability_Status: 0
DisplayPort_Device_Plug_Status: 1 Connected & Initialized
Legacy_Device_Plug_Status: 0
DPID Revision: 14h
Peer_Global_Unique_Identifier: 34 DC C6 CB 77 00 00 00 31 DC C6 CB 77 00 00 00
Number_SD_PStreams: 1
Number_SD_Stream_Sinks: 2

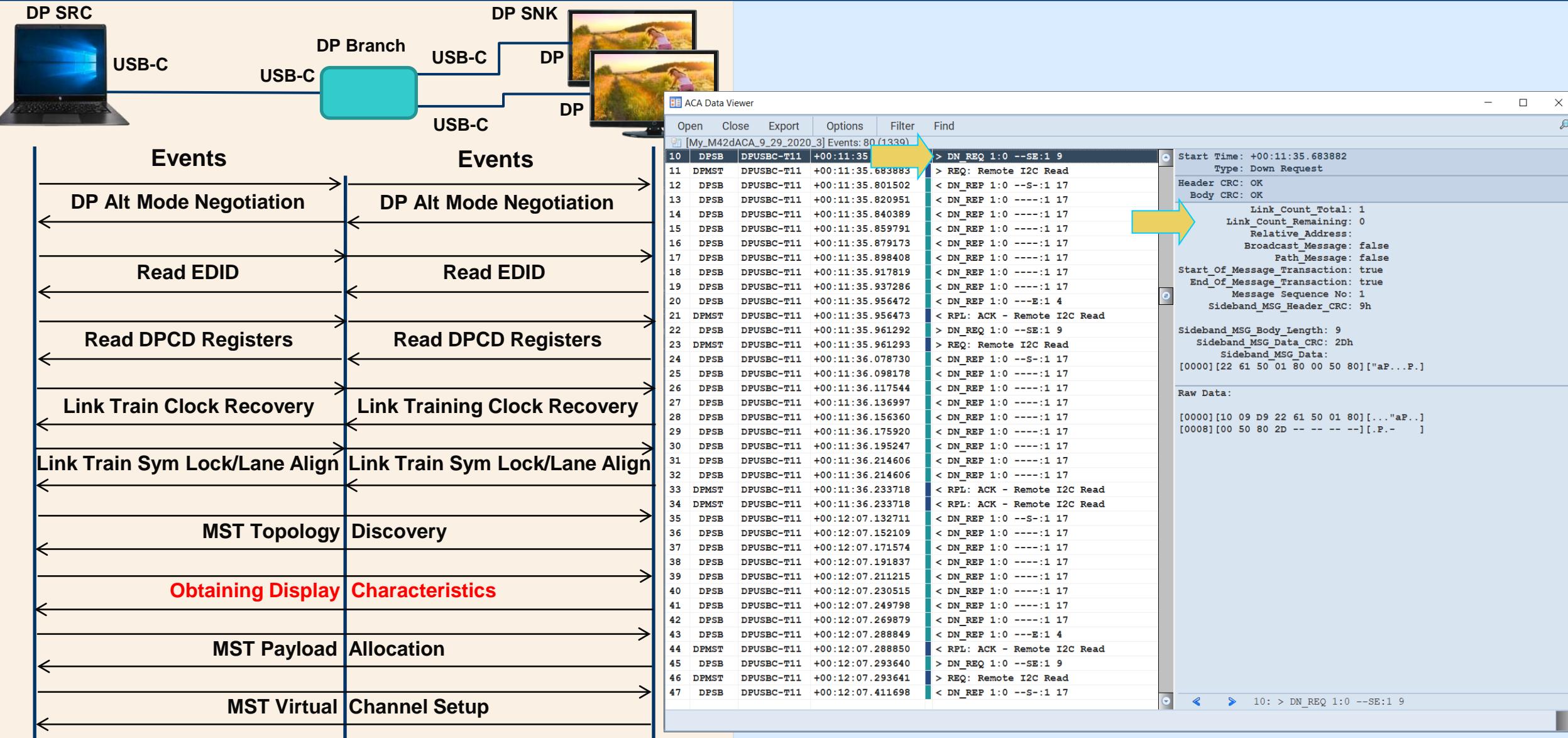
Port 4 Description --
Input_Port: 0 (TX)
Peer_Device_Type: 3
- SST Sink device or stream Sink in an MST Sink/Composite device.
Port Number: 6
Messaging_Capability_Status: 0
DisplayPort_Device_Plug_Status: 1 Connected & Initialized
Legacy_Device_Plug_Status: 0
DPID Revision: 14h
Peer_Global_Unique_Identifier: 35 DC C6 CB 77 00 00 00 31 DC C6 CB 77 00 00 00
Number_SD_PStreams: 1
Number_SD_Stream_Sinks: 2

Raw Data:

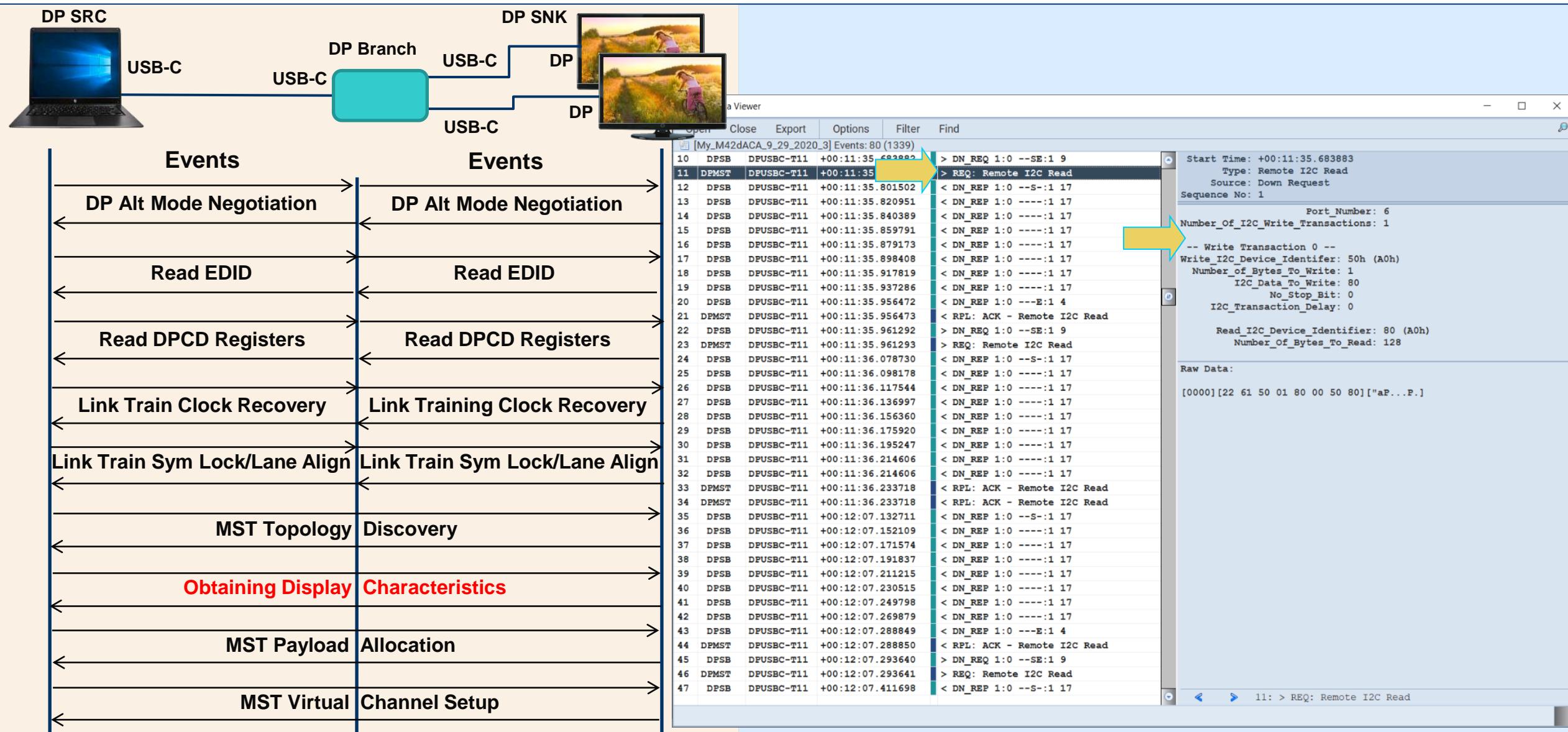
95: < RPL: ACK - Link Address

Read EDID of Remote Sinks

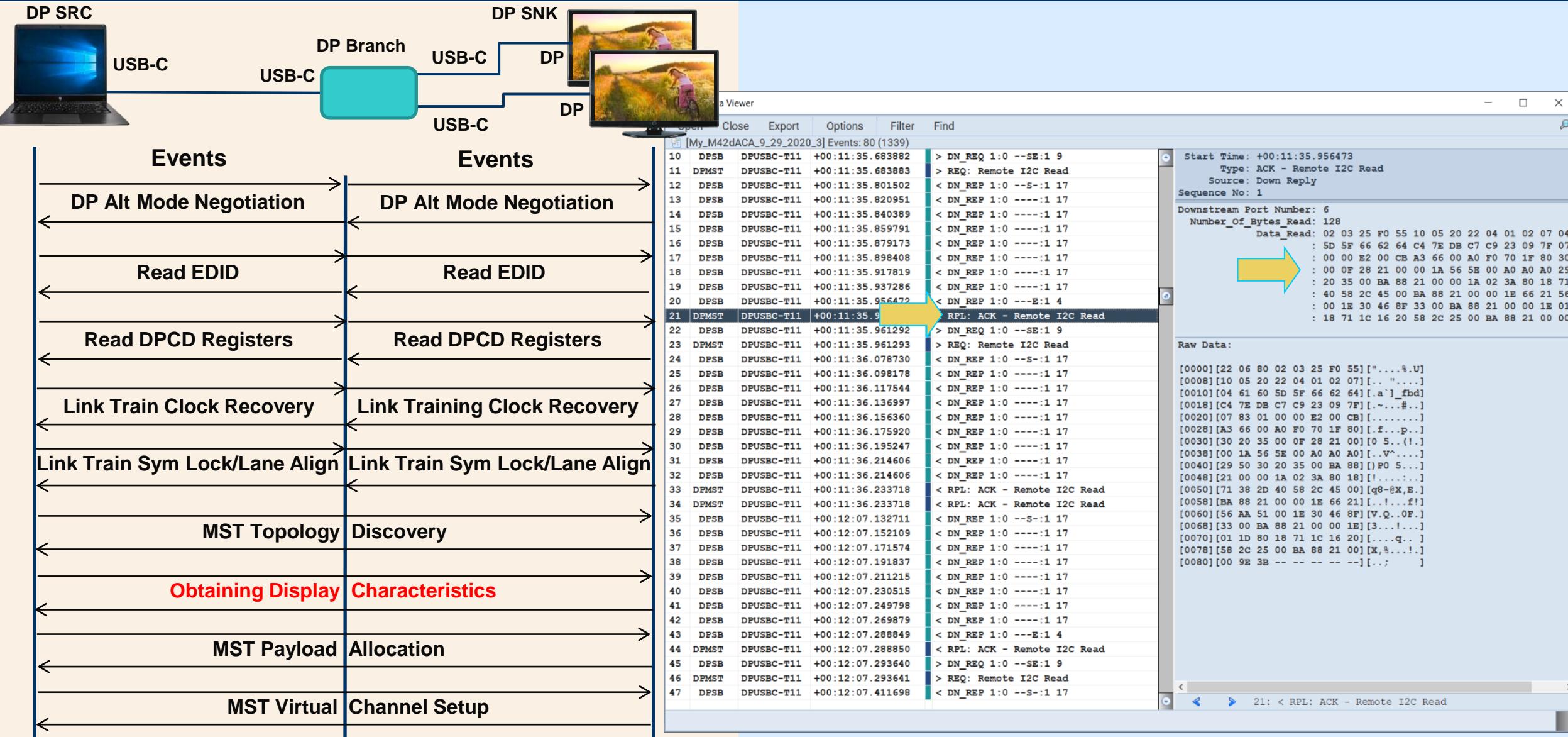
Multi-Stream Configuration – Read EDID of Remote Sinks – Sideband Message Header



Multi-Stream Configuration – Read EDID of Remote Sinks

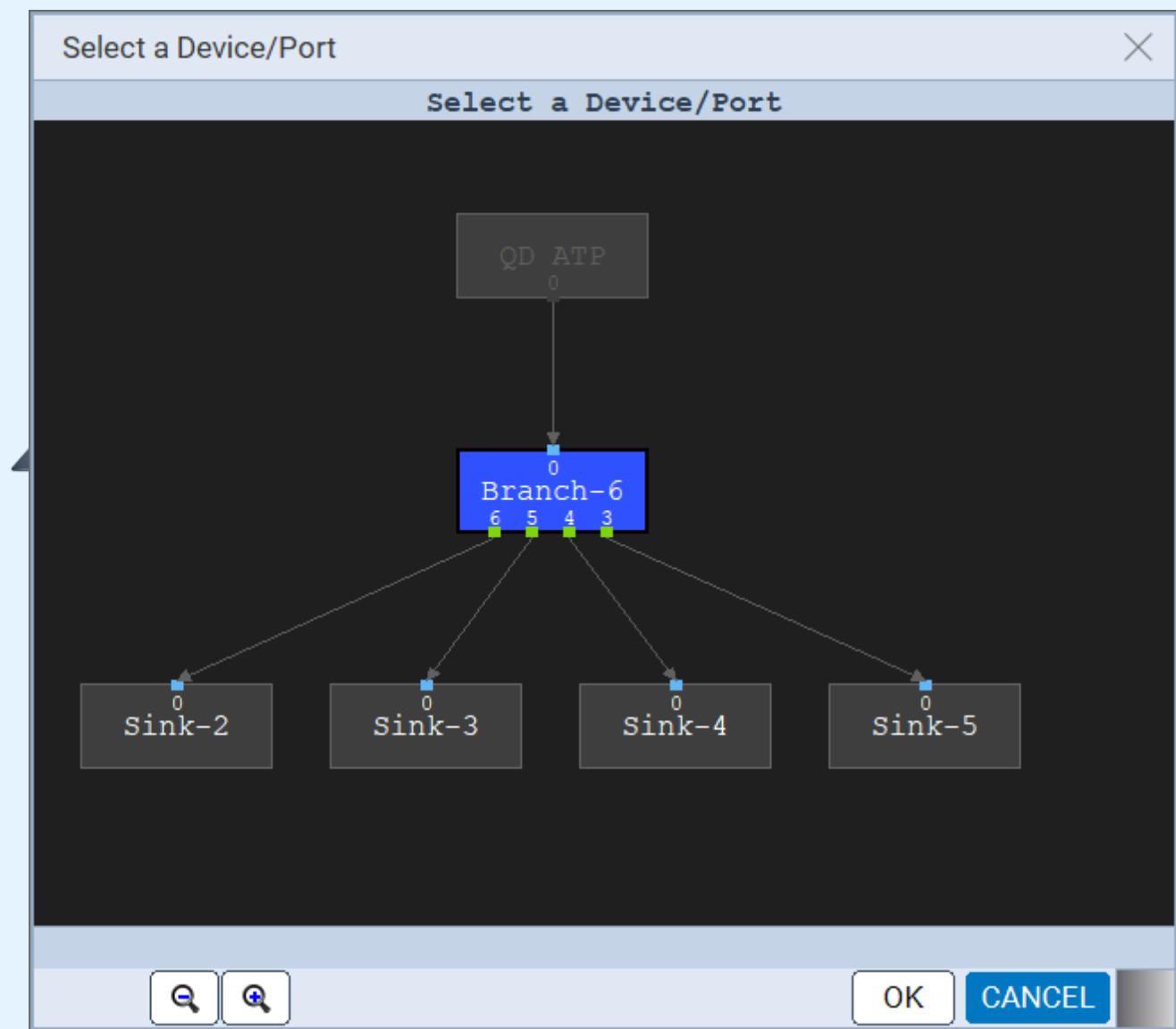
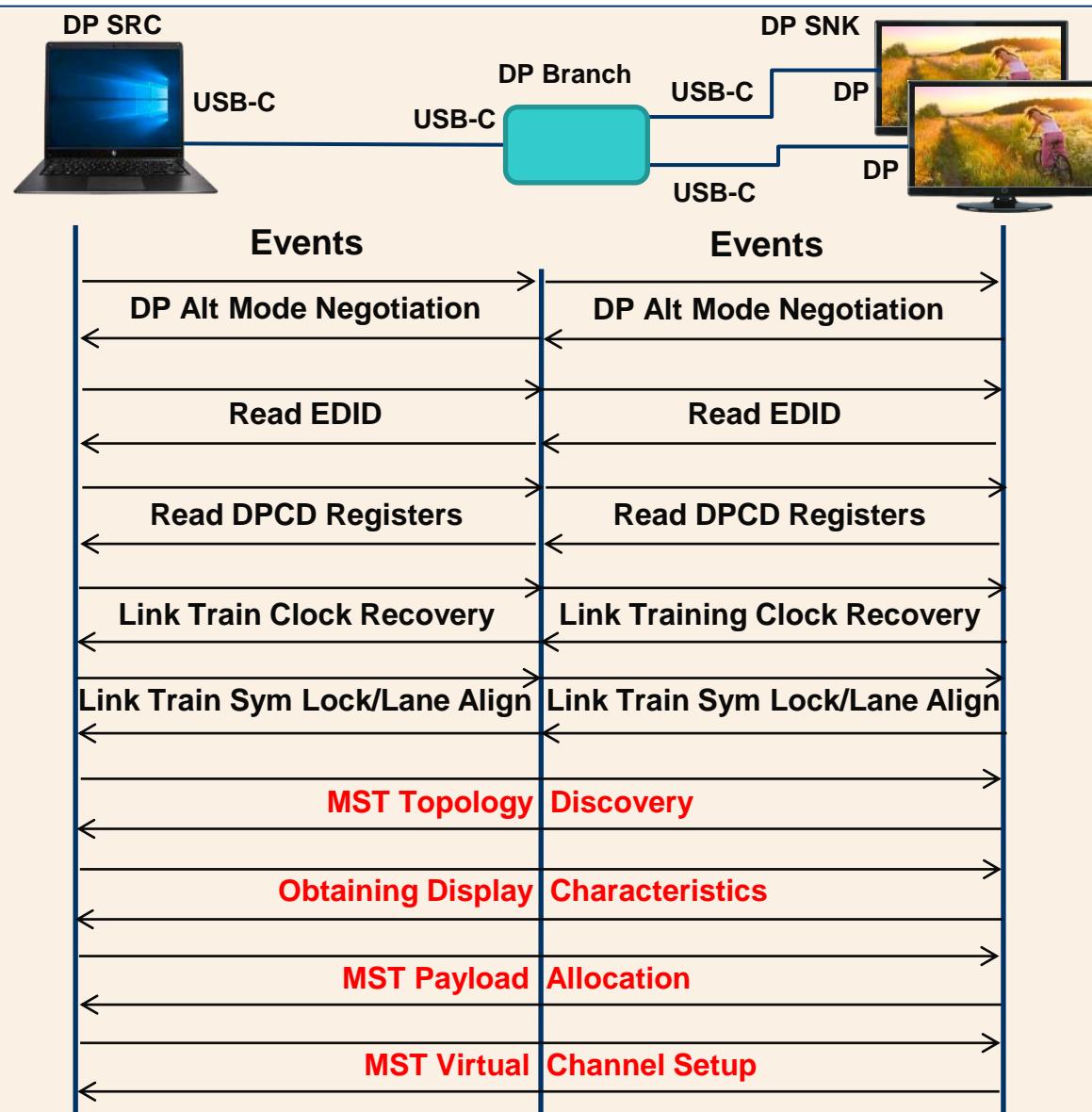


Multi-Stream Configuration – Read EDID of Remote Sinks

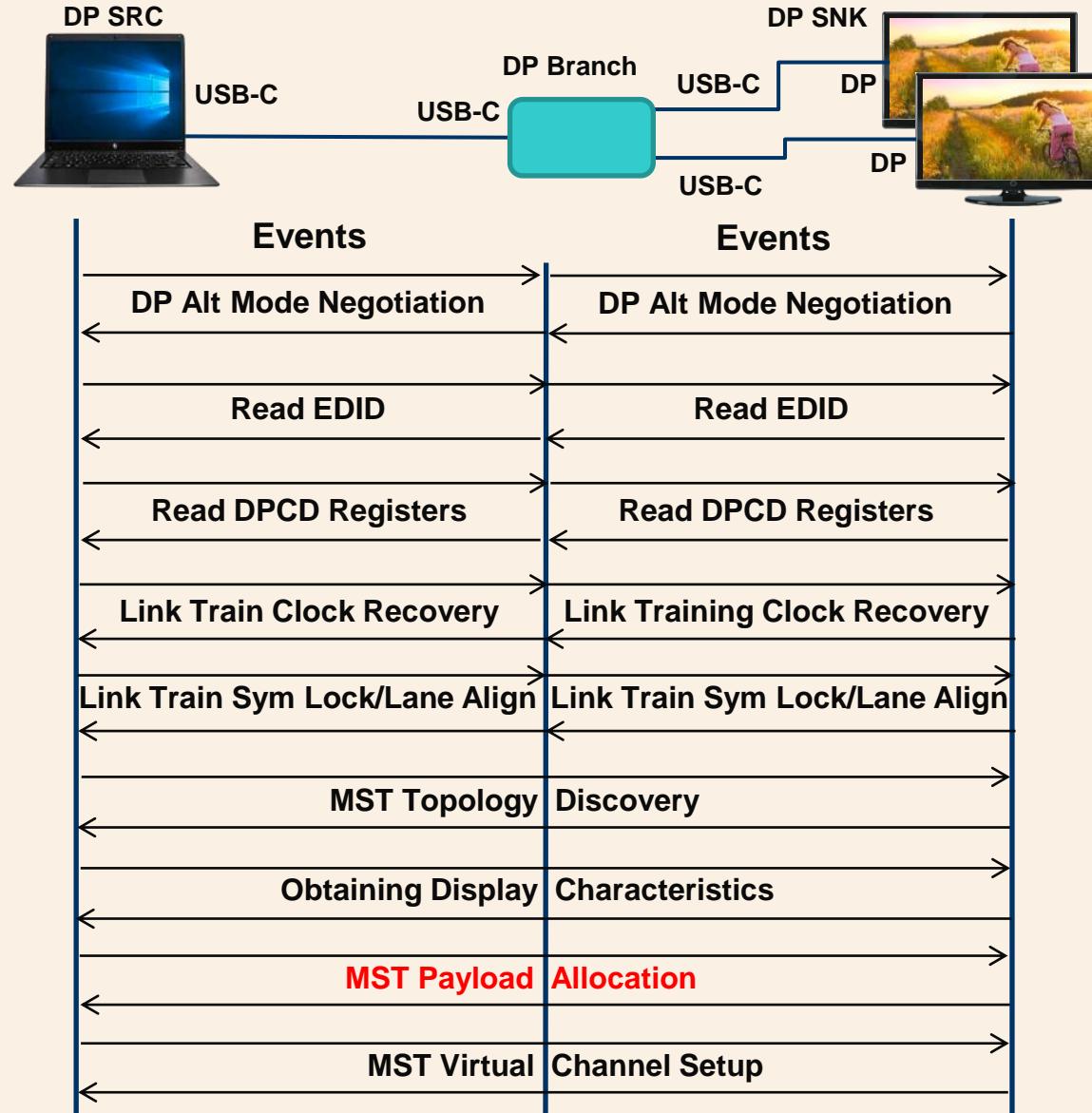


MST Path Enumeration / Path Allocation

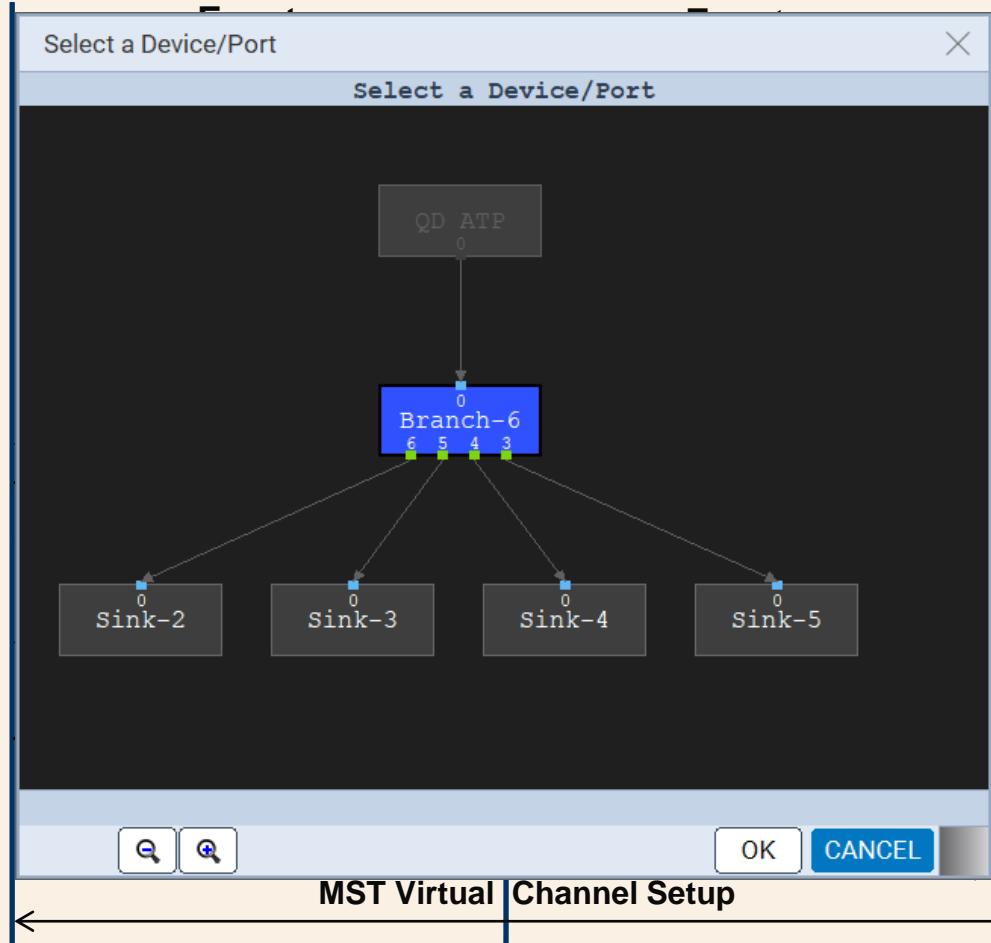
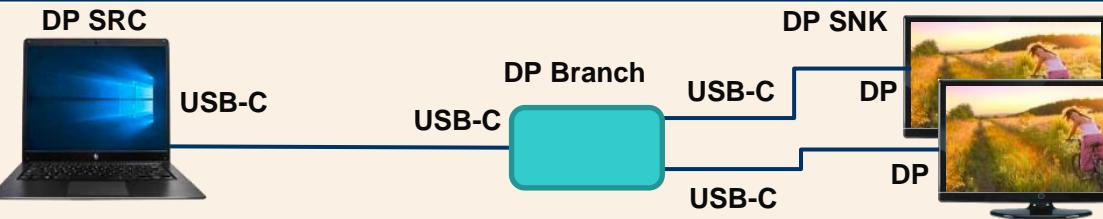
Multi-Stream Transport (MST) – Path Enumeration



Multi-Stream Configuration – Path Enumeration – Branch Port e.g. 3



Multi-Stream Configuration – Path Enumeration Response - Branch e.g. Port 3



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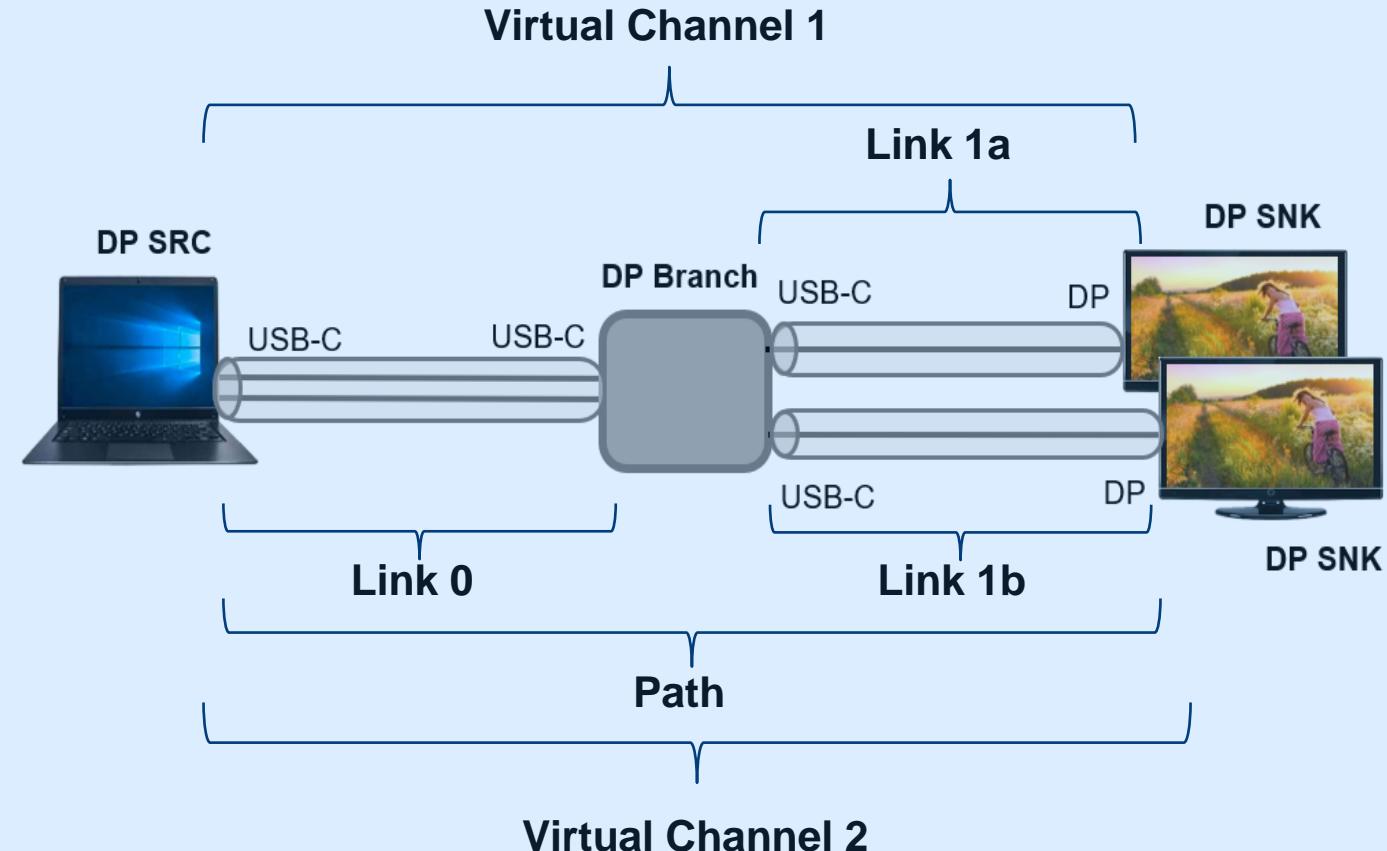
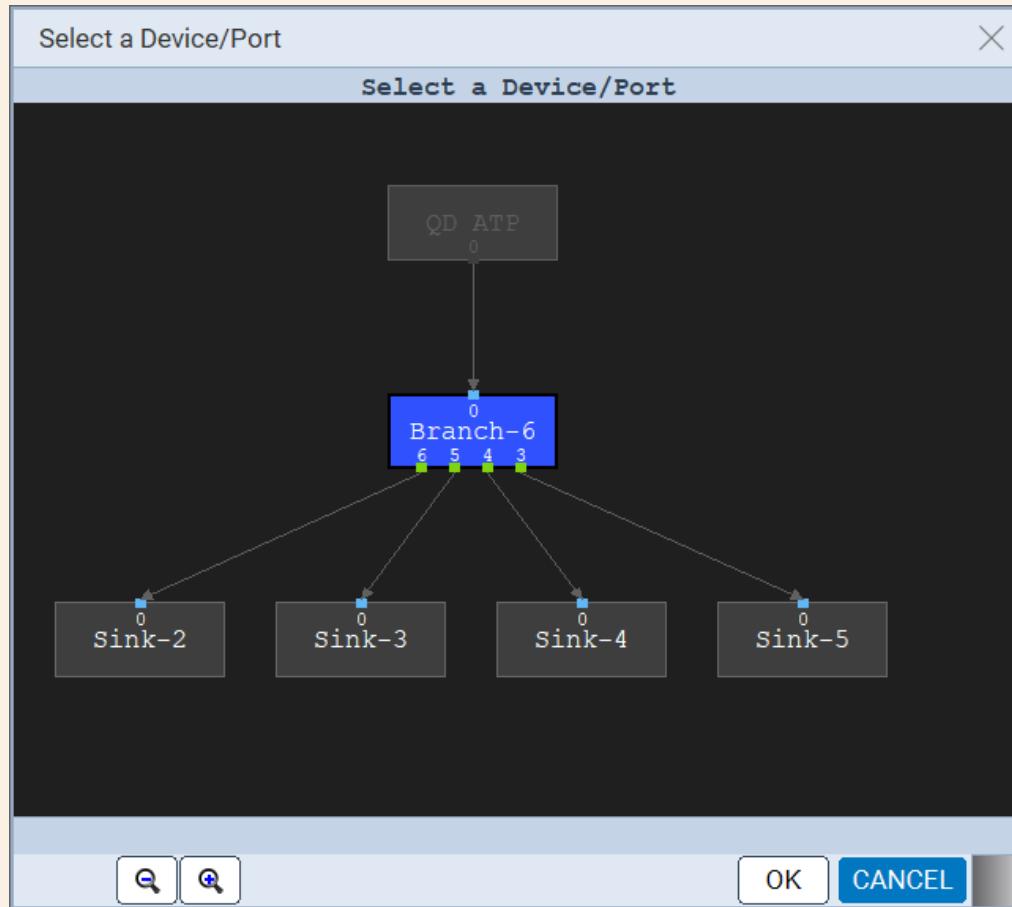
[20G LTPR_AUX_LT_FFE5] Events: 132 (996)

79	DPLT	DPUSBC-T11	+03:50:27.641095
80	DPLT	DPUSBC-T11	+03:50:27.641243
81	DPLT	DPUSBC-T11	+03:50:27.641317
82	DPSB	DPUSBC-T11	+03:50:27.645605
83	DPMST	DPUSBC-T11	+03:50:27.645606
84	DPSB	DPUSBC-T11	+03:50:27.665278
85	DPMST	DPUSBC-T11	+03:50:27.665279
86	DPSB	DPUSBC-T11	+03:50:27.666369
87	DPMST	DPUSBC-T11	+03:50:27.666370
88	DPSB	DPUSBC-T11	+03:50:27.686723
89	DPSB	DPUSBC-T11	+03:50:27.707684
90	DPSB	DPUSBC-T11	+03:50:27.727502
91	DPSB	DPUSBC-T11	+03:50:27.746904
92	DPSB	DPUSBC-T11	+03:50:27.766974
93	DPSB	DPUSBC-T11	+03:50:27.786886
94	DPSB	DPUSBC-T11	+03:50:27.806568
95	DPMST	DPUSBC-T11	+03:50:27.806569
96	DPSB	DPUSBC-T11	+03:50:27.807100
97	DPMST	DPUSBC-T11	+03:50:27.807101
98	DPSB	DPUSBC-T11	+03:50:27.827602
99	DPMST	DPUSBC-T11	+03:50:27.827603
100	DPSB	DPUSBC-T11	+03:50:27.828307
101	DPMST	DPUSBC-T11	+03:50:27.828308
102	DPSB	DPUSBC-T11	+03:50:27.848571
103	DPMST	DPUSBC-T11	+03:50:27.849384
104	DPSB	DPUSBC-T11	+03:50:27.849384
105	DPMST	DPUSBC-T11	+03:50:27.849384
106	DPSB	DPUSBC-T11	+03:50:27.868963
107	DPMST	DPUSBC-T11	+03:50:27.868964
108	DPSB	DPUSBC-T11	+03:50:27.869751
109	DPMST	DPUSBC-T11	+03:50:27.869752
110	DPSB	DPUSBC-T11	+03:50:27.889965
111	DPMST	DPUSBC-T11	+03:50:27.889966
112	DPSB	DPUSBC-T11	+03:50:27.891215
113	DPMST	DPUSBC-T11	+03:50:27.891216
114	DPSB	DPUSBC-T11	+03:50:27.911900
115	DPMST	DPUSBC-T11	+03:50:27.911901
116	DPSB	DPUSBC-T11	+03:50:29.115248
117	DPMST	DPUSBC-T11	+03:50:29.115249

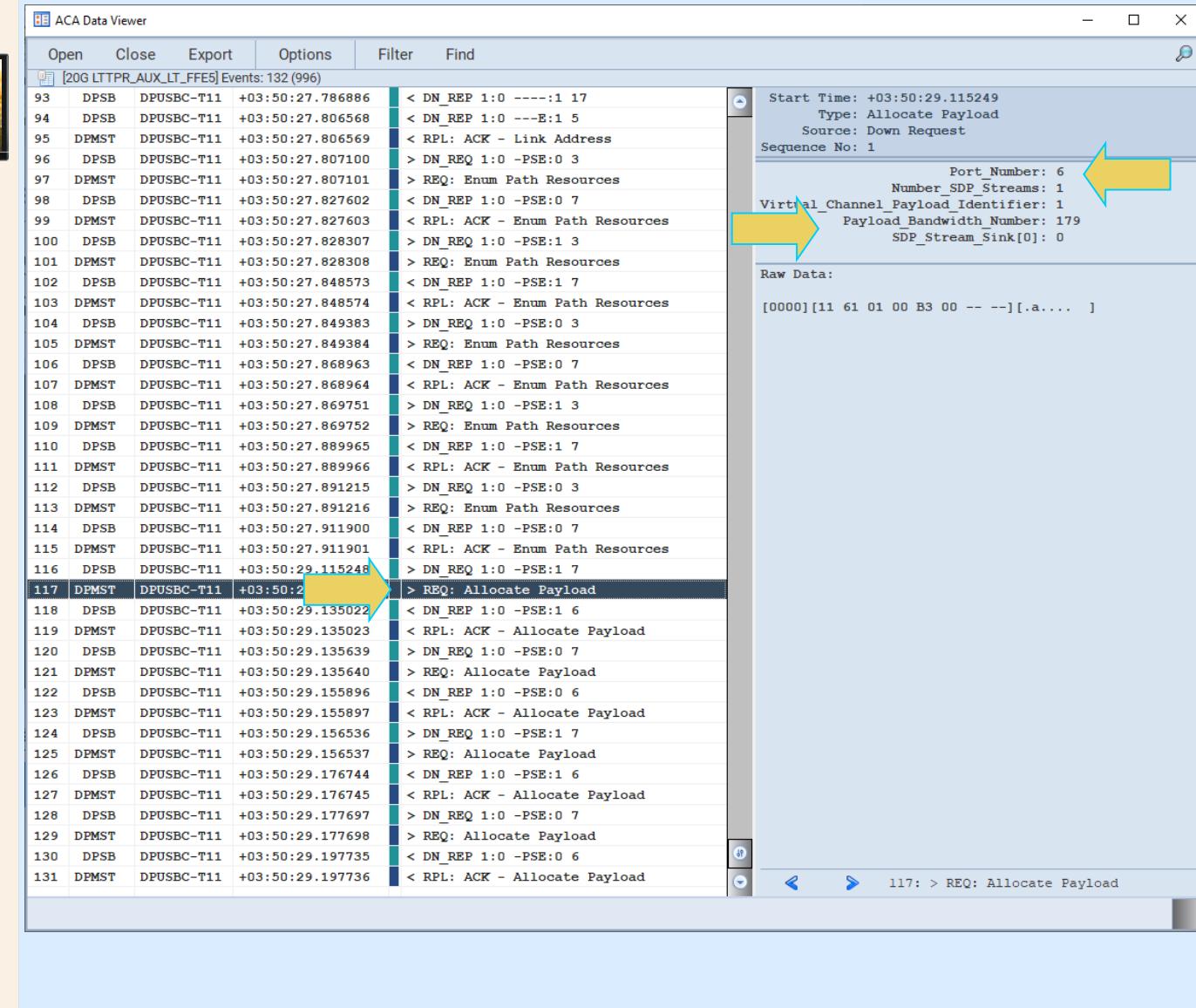
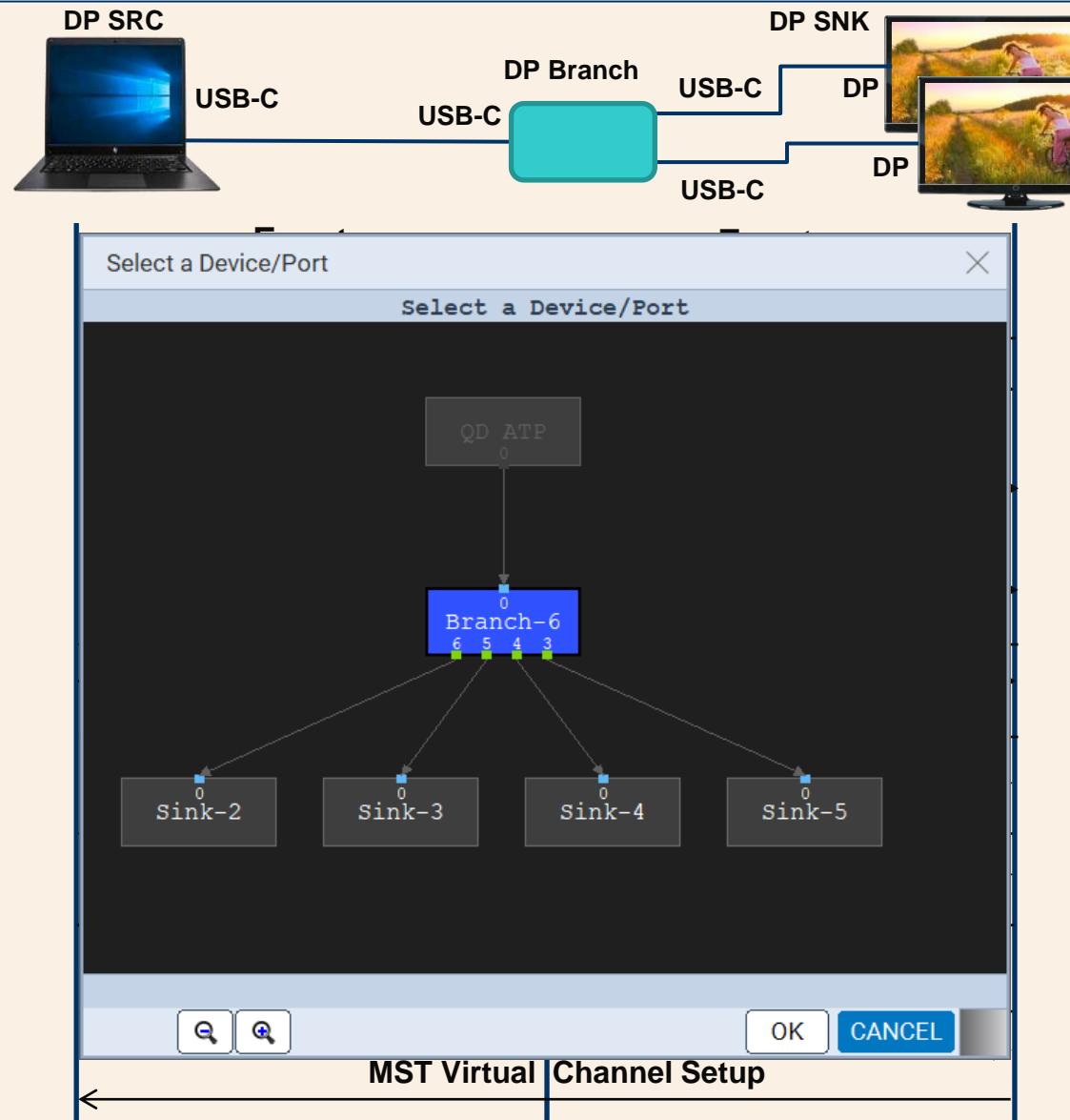
Start Time: +03:50:27.848574
Type: ACK - Enum Path Resources
Source: Down Reply
Sequence No: 1
Port_Number: 3
FEC_Capability: 1
Full_Payload_Bandwidth_Number: 3840
Available_Payload_Bandwidth_Number: 3840
Raw Data:
[0000][10 31 OF 00 OF 00 -- --].[.1....]

103: < RPL: ACK - Enum Path Resources

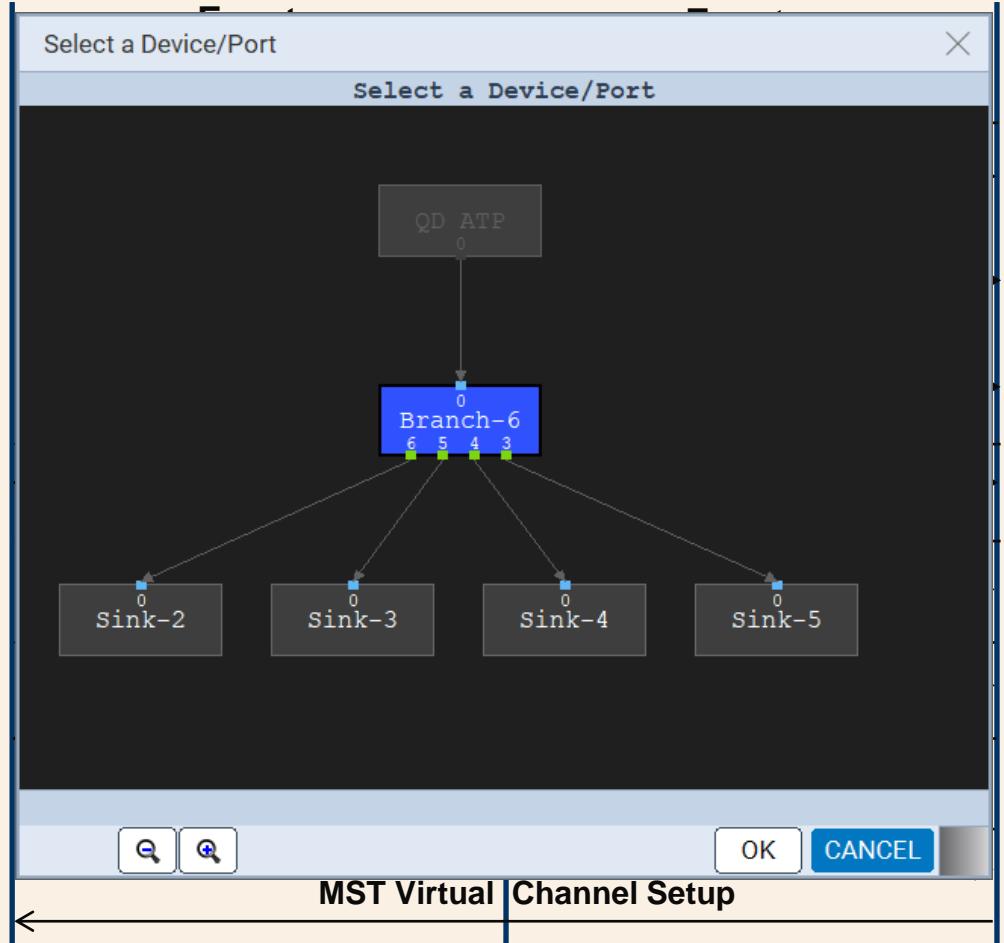
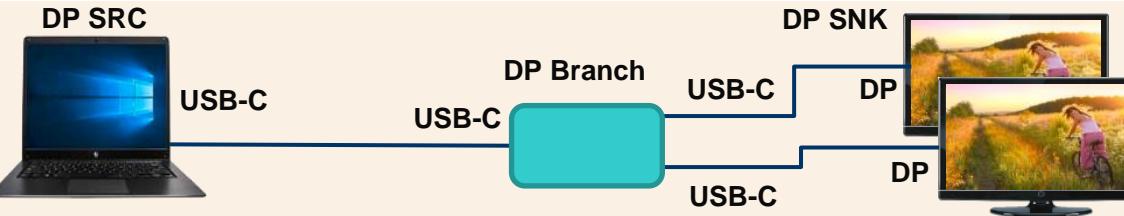
Multi-Stream Transport (MST) – Create Virtual Channels with Allocate Payload



Multi-Stream Configuration – Allocate Payload for Each Port, e.g. Port 6, Stream 1



Multi-Stream Configuration – Allocate Payload for Each Port, e.g. Port 6, Stream 1



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20G LTTPR_AUX_LT_FFE5 Events: 132 (996)

93	DPSB	DPUSBC-T11	+03:50:27.786886	< DN_REQ 1:0 ----:1 17
94	DPSB	DPUSBC-T11	+03:50:27.806568	< DN_REQ 1:0 ---E:1 5
95	DPMST	DPUSBC-T11	+03:50:27.806569	< RPL: ACK - Link Address
96	DPSB	DPUSBC-T11	+03:50:27.807100	> DN_REQ 1:0 -PSE:0 3
97	DPMST	DPUSBC-T11	+03:50:27.807101	> REQ: Enum Path Resources
98	DPSB	DPUSBC-T11	+03:50:27.827602	< DN_REQ 1:0 -PSE:0 7
99	DPMST	DPUSBC-T11	+03:50:27.827603	< RPL: ACK - Enum Path Resources
100	DPSB	DPUSBC-T11	+03:50:27.828307	> DN_REQ 1:0 -PSE:1 3
101	DPMST	DPUSBC-T11	+03:50:27.828308	> REQ: Enum Path Resources
102	DPSB	DPUSBC-T11	+03:50:27.848573	< DN_REQ 1:0 -PSE:1 7
103	DPMST	DPUSBC-T11	+03:50:27.848574	< RPL: ACK - Enum Path Resources
104	DPSB	DPUSBC-T11	+03:50:27.849383	> DN_REQ 1:0 -PSE:0 3
105	DPMST	DPUSBC-T11	+03:50:27.849384	> REQ: Enum Path Resources
106	DPSB	DPUSBC-T11	+03:50:27.868963	< DN_REQ 1:0 -PSE:0 7
107	DPMST	DPUSBC-T11	+03:50:27.868964	< RPL: ACK - Enum Path Resources
108	DPSB	DPUSBC-T11	+03:50:27.869751	> DN_REQ 1:0 -PSE:1 3
109	DPMST	DPUSBC-T11	+03:50:27.869752	> REQ: Enum Path Resources
110	DPSB	DPUSBC-T11	+03:50:27.889965	< DN_REQ 1:0 -PSE:1 7
111	DPMST	DPUSBC-T11	+03:50:27.889966	< RPL: ACK - Enum Path Resources
112	DPSB	DPUSBC-T11	+03:50:27.891215	> DN_REQ 1:0 -PSE:0 3
113	DPMST	DPUSBC-T11	+03:50:27.891216	> REQ: Enum Path Resources
114	DPSB	DPUSBC-T11	+03:50:27.911900	< DN_REQ 1:0 -PSE:0 7
115	DPMST	DPUSBC-T11	+03:50:27.911901	< RPL: ACK - Enum Path Resources
116	DPSB	DPUSBC-T11	+03:50:29.115248	> DN_REQ 1:0 -PSE:1 7
117	DPMST	DPUSBC-T11	+03:50:29.115249	> REQ: Allocate Payload
118	DPSB	DPUSBC-T11	+03:50:29.135652	< DN_REQ 1:0 -PSE:1 6
119	DPMST	DPUSBC-T11	+03:50:29.135653	< RPL: ACK - Allocate Payload
120	DPSB	DPUSBC-T11	+03:50:29.135659	> DN_REQ 1:0 -PSE:0 7
121	DPMST	DPUSBC-T11	+03:50:29.135640	> REQ: Allocate Payload
122	DPSB	DPUSBC-T11	+03:50:29.155896	< DN_REQ 1:0 -PSE:0 6
123	DPMST	DPUSBC-T11	+03:50:29.155897	< RPL: ACK - Allocate Payload
124	DPSB	DPUSBC-T11	+03:50:29.156536	> DN_REQ 1:0 -PSE:1 7
125	DPMST	DPUSBC-T11	+03:50:29.156537	> REQ: Allocate Payload
126	DPSB	DPUSBC-T11	+03:50:29.176744	< DN_REQ 1:0 -PSE:1 6
127	DPMST	DPUSBC-T11	+03:50:29.176745	< RPL: ACK - Allocate Payload
128	DPSB	DPUSBC-T11	+03:50:29.177697	> DN_REQ 1:0 -PSE:0 7
129	DPMST	DPUSBC-T11	+03:50:29.177698	> REQ: Allocate Payload
130	DPSB	DPUSBC-T11	+03:50:29.197735	< DN_REQ 1:0 -PSE:0 6
131	DPMST	DPUSBC-T11	+03:50:29.197736	< RPL: ACK - Allocate Payload

Start Time: +03:50:29.135023
Type: ACK - Allocate Payload
Source: Down Reply
Sequence No: 1

Port_Number: 6
Virtual_Channel_Payload_Identifier: 1
Allocated_Payload_Bandwidth_Number: 179

Raw Data:

```
[0000][11 60 01 00 B3 -- -- --][. ....]
```

119: < RPL: ACK - Allocate Payload

Thank you for your Attention

Please contact me, Neal Kendall at:

neal.kendall@teledyne.com

If you have any questions.

M42d 80G Video Analyzer/Generator



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