

DisplayPort Compliance Testing

Part 1: DisplayPort PHY testing



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About the Presenter



- 20+ years working in high speed serial data testing
- Joined Teledyne LeCroy in 2018
- BSEE in Electronic Design from Montana State University - Bozeman

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About Teledyne LeCroy



Teledyne LeCroy Factory
Chestnut Ridge, New York



- Teledyne LeCroy is an American company founded in 1964 in New York by Alabama native, Walter LeCroy
- Origins are high speed digitizers for particle physics research
- Teledyne LeCroy is the only oscilloscope vendor in the world who makes oscilloscopes in the USA
- Teledyne LeCroy corporate headquarters is located in Chestnut Ridge, New York
- Teledyne LeCroy is the oscilloscope technology leader, with realtime bandwidths to 100 GHz, and sample rates to 240 GS/s
- In 2004 and 2006, Teledyne LeCroy acquired the two largest protocol analyzer companies (CATC and Catalyst) merging them into a protocol analyzer division became the #1 protocol analyzer in the world. **And more recently acquired Quantum Data for video technologies**
- In 2012, LeCroy Corporation was acquired by Teledyne Technologies, and became Teledyne LeCroy

This is Part 1 of a 2-part webinar

Part 1: DP 1.4 PHY (Physical) Layer Compliance Testing

- DisplayPort Basics
- Test Tools for DisplayPort PHY testing
- Main link PHY tests
- Aux channel PHY tests
- Sink & Active Cable PHY tests
- USB-C Power Delivery Debug
- DisplayPort 2.0 PHY Preview

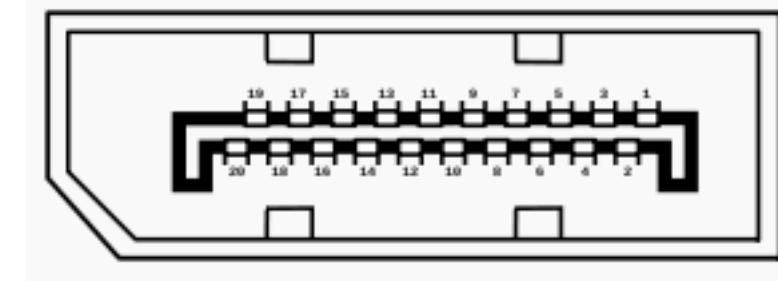
Part 2: DP 1.4 Link Layer Compliance Testing

- General protocols
- Link Layer compliance
- FEC and FEC compliance
- Display Stream Compression (DSC) and DSC compliance
- HDCP and HDCP compliance

*Visit DP1.4 Teledyne LeCroy Test Suites at upcoming
VESA PlugTest Burlingame, CA Embassy Suites Sept. 30th – Oct. 4th*

What is DisplayPort?

- DisplayPort (DP) is developed and maintained by VESA: **V**ideo **E**lectronics **S**tandards **A**sociation
- A modern interface for connecting PC to video monitor
 - Forward-looking replacement for DVI, VGA
 - Competes with HDMI – HDMI is more prevalent in home media & consumer electronics
- Single cable carries video and audio



DisplayPort Signaling Standards

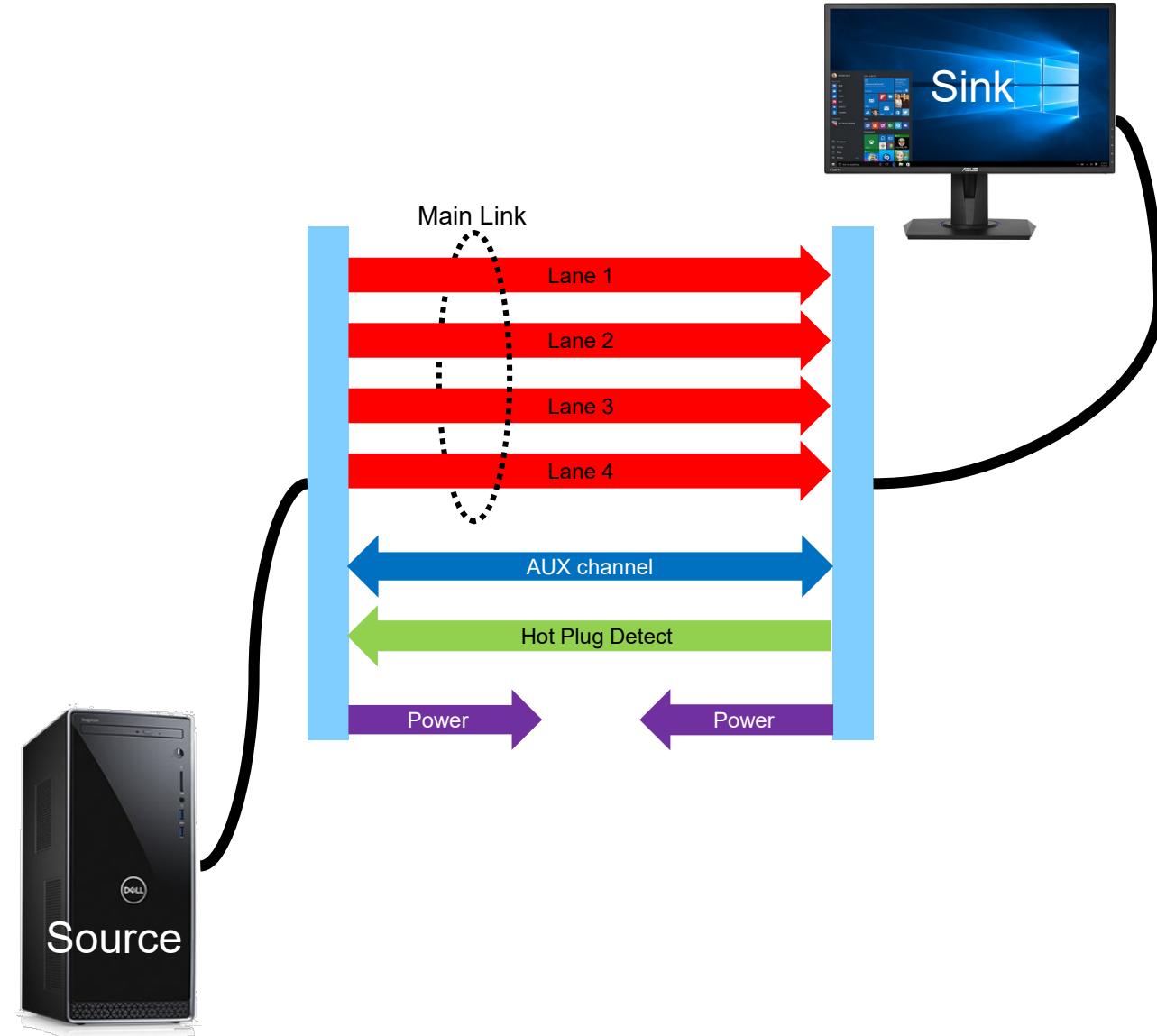
Deployed

Standard	Raw Bandwidth (4 Lanes)	Effective Bandwidth (4 Lanes)	Target Monitor Resolutions
DP 1.0/1.1 (HBR1)	10.8 Gbps	8.64 Gbps	1440p@60Hz
DP 1.2 (HBR 2)	21.6 Gbps	17.28 Gbps	4K@60Hz
DP 1.3/1.4 (HBR3)	32.4 Gbps	25.92 Gbps	4K@120Hz 8K@60Hz (w/DSC)
DP 2.0 (UHBR 20)	80 Gbps	77.37 Gbps	8K@60hz HDR >8K@60Hz SDR 4K@144Hz HDR 2x 5K@60Hz

Image Source: <https://www.anandtech.com/show/14590/vesa-announces-displayport-20-standard-bandwidth-for-8k-monitors-beyond>

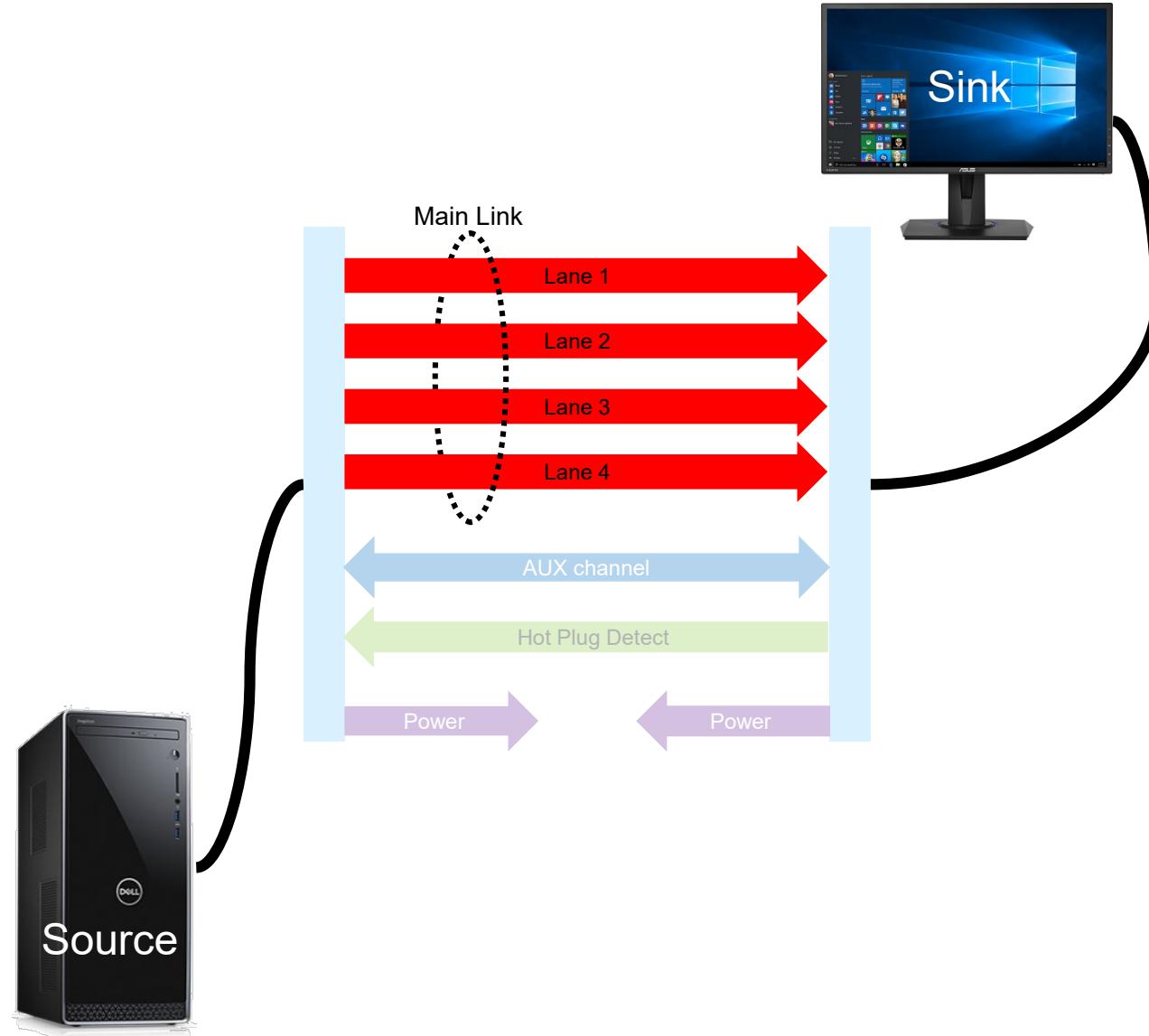
DisplayPort basics

- DisplayPort connects a video **source** (transmitter) such as a PC to a **sink** (receiver) such as a monitor
- DisplayPort link contains:
 - **Main Link:** 1, 2 or 4 high-speed data lanes
 - **AUX channel:** Auxiliary channel, a low-speed interface for source and sink to communicate
 - Hot plug detect



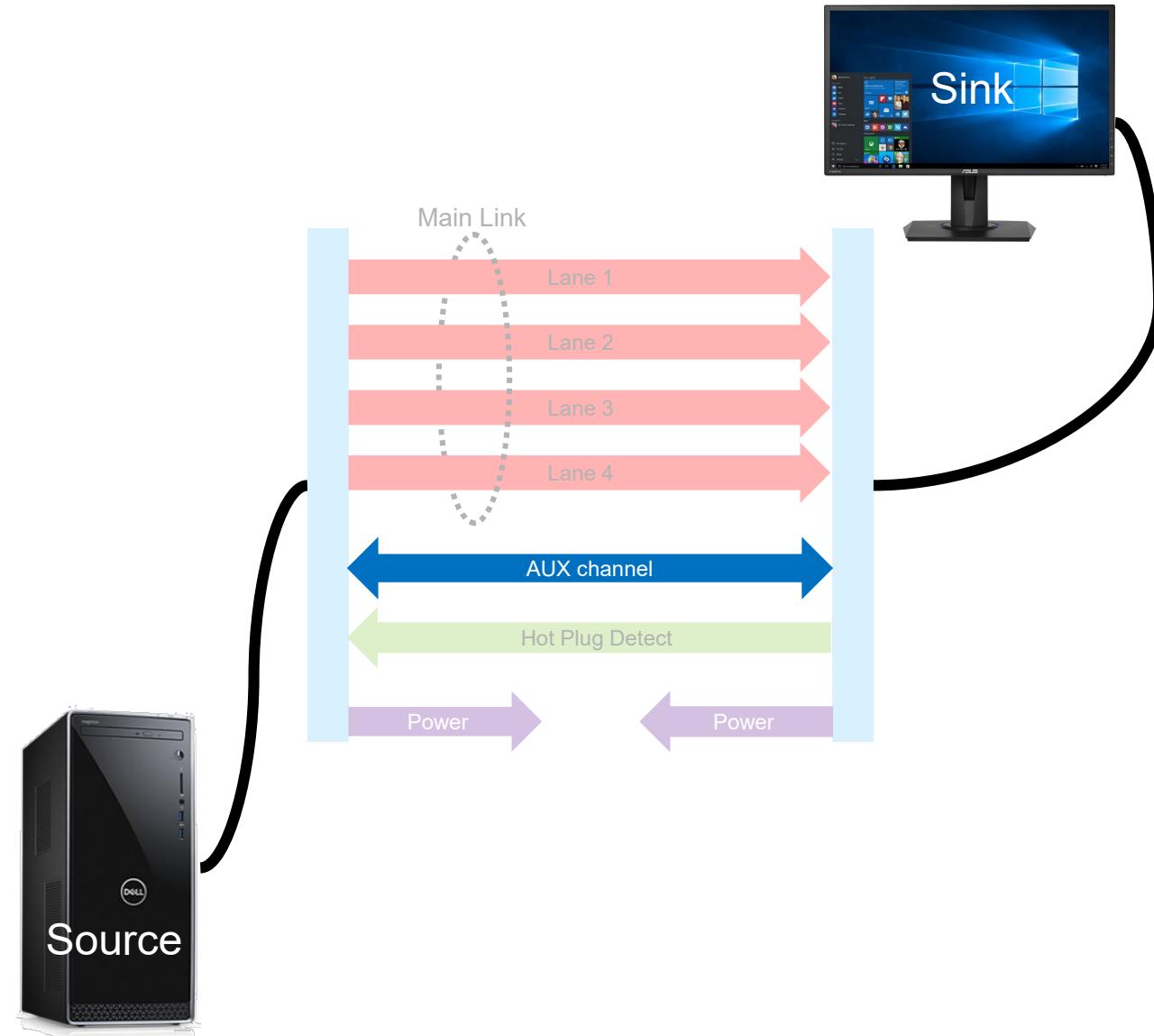
DisplayPort basics – Main Link

- Data transmitted on 1, 2 or 4 lanes, each with either:
 - 1.62 Gb/s (“RBR” = reduced bit rate)
 - 2.7 Gb/s (“HBR” = high bit rate)
 - 5.4 Gb/s (“HBR2” = higher bit rate 2, DisplayPort 1.2b)
 - 8.1 Gb/s (“HBR3” = highest bit rate 3, DisplayPort 1.4)
- Swing & Pre-emphasis negotiated at Link Up over AUX Channel
 - Swing Levels 400, 600, 800, 1200mV
 - Pre-Emphasis 0, 3.5, 6, 9.5dB
- 8b/10b encoding



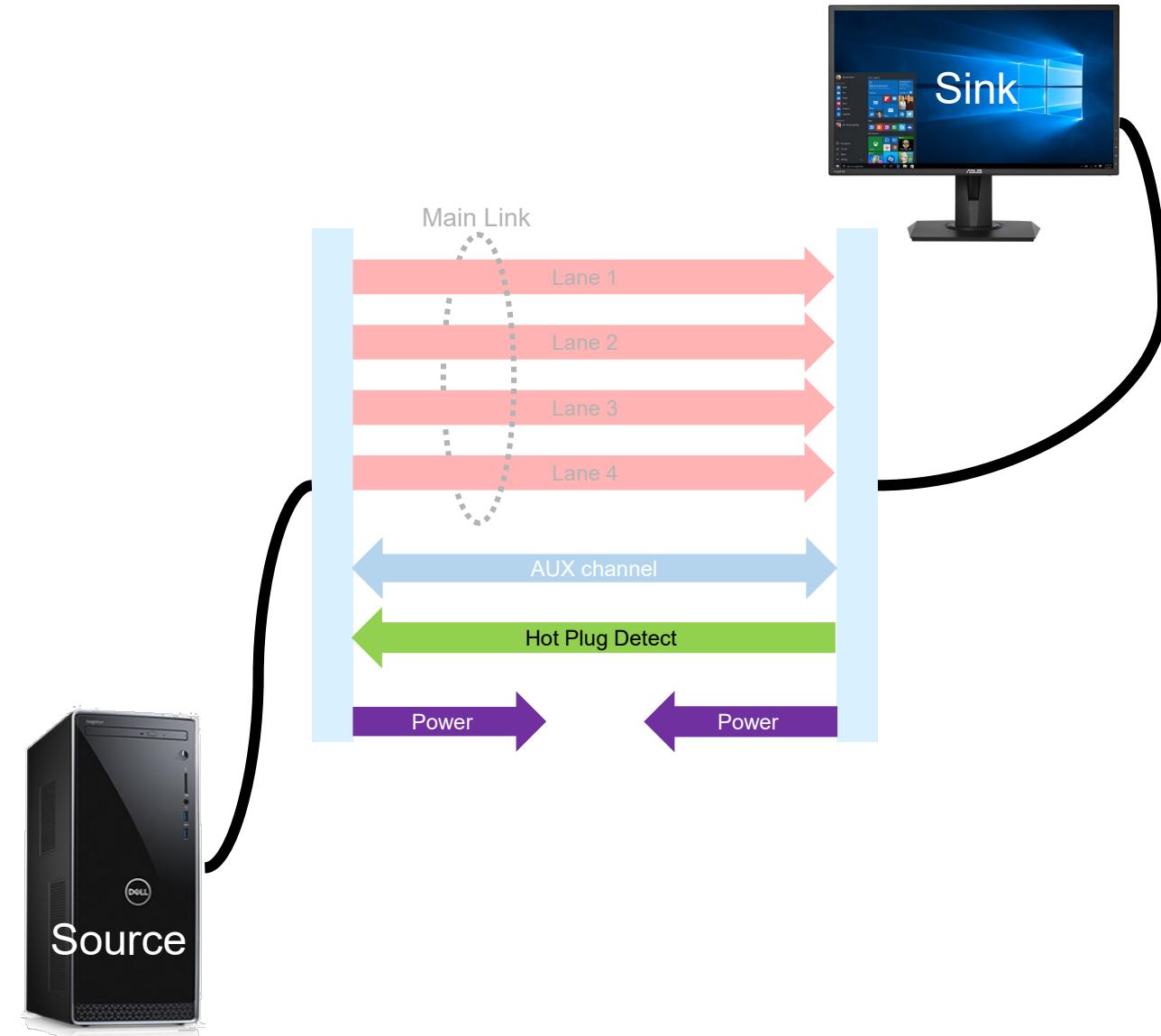
DisplayPort basics – Auxiliary Channel

- Used for communications between sink and source
 - Notification of main link data corruption
 - Transmission of audio or other data
 - Control of display settings
 - Control of source configuration
 - And more...
- 1V pk-pk
- Default: Manchester encoded data:1Mbps



DisplayPort basics – HPD & Power Delivery

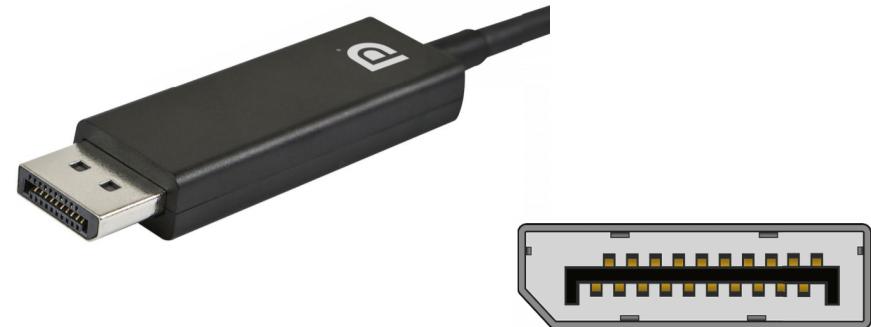
- Legacy Connectors
 - HDP – Hardwired Electrical Connection
 - DP Power for Active Cables and Adapters
- USB-C™ Connector
 - Uses USB-PD specification
 - HPD – Embedded in PD Messaging (After Power Contract)
 - V_{BUS} (up to 100W) for charging
 - V_{CONN} to power active cables and adapters



DisplayPort Connectors: Legacy connectors

- “Legacy” DisplayPort connectors come in two form factors:
 - **Full Size** DisplayPort connectors are used in desktop PC's, televisions, monitors etc
 - **Mini** DisplayPort connectors are used in laptop PC's
- Both form factors are functionally similar
 - Same number of pins
 - Up to 4 Main Link lanes
 - AUX and hot-plug detect
- Tested identically (except for test fixture)

Full Size DisplayPort connectors



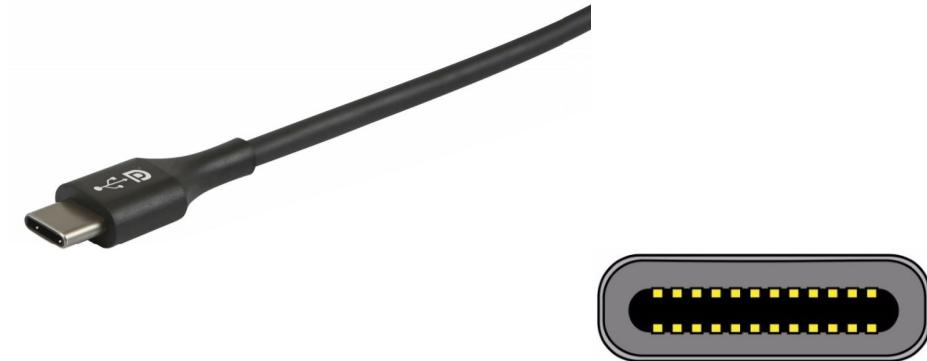
Mini DisplayPort connectors



DisplayPort Connectors: USB Type-C connectors

- DisplayPort can be carried over a USB-C connector as an “alt mode”
 - Alt mode means the device switches to a different PHY transmitter
- Can use all 4 high-speed pairs to transmit DisplayPort main link, or retain 2 lanes for superspeed USB
- AUX transmitted over SBU Pins

Type-C connectors



Type-C Pin Assignment E: 4 Lanes DP:

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	ML0TX+	ML0TX-	Vbus	AUX+	D1-	D1+	CC	Vbus	ML2TX-	ML2TX+	GND
GND	ML1TX+	ML1TX-	Vbus	Vconn	D2+	D2-	AUX-	Vbus	ML3TX-	ML3TX+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

USB-C Pin Assignment F: 2 Lanes DP, SS USB Tx/Rx:

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	ML0TX+	ML0TX-	Vbus	AUX+	D1-	D1+	CC	Vbus	TX1-	TX1+	GND
GND	ML1TX+	ML1TX-	Vbus	Vconn	D2+	D2-	AUX-	Vbus	RX1-	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

DisplayPort: History

- **DP Specifications (only the current version is active):**
 - **Version 1.0:** Original spec, 2006, RBR and HBR supported. Not known to be implemented.
 - **Version 1.1, 2007 1.1a, 2008:** First version to be implemented, with products available late 2007/early 2008.
 - **Version 1.2:** 2010, Introduced support for HBR2, MST.
 - **Version 1.3:** 2014, Introduced support for HBR3. Not known to be implemented.
 - **DP Alt Mode over USB Type-C 1.0a – Aug 2015**
 - Version 1.4: 2016.
 - **Version 1.4a:** 2018, Currently deployed version
- **DisplayPort Version 2.0:** June 2019; early development – UHBR Rates

DisplayPort test tools



TELEDYNE LECROY
Everywhereyoulook™

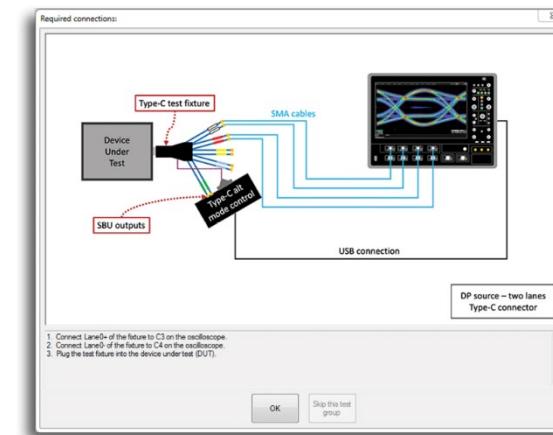
Required Oscilloscope for DisplayPort source testing

- Teledyne LeCroy SDA 816Zi-B
 - 16 GHz bandwidth is required for HBR3 (8.1 Gb/s) rates
- 4 channels of 16 GHz, 40 GS/s 50Ω high-bandwidth inputs
 - Also 1 MΩ inputs, allowing passive probes to be connected for AUX channel tests
- Eye diagram, jitter and noise analysis on up to 4 lanes simultaneously
- Eye Doctor software option for embedding cable models and emulating receiver equalization



QPHY-DisplayPort

- QualiPHY is designed to reduce the time, effort and specialized knowledge needed to perform compliance testing on high-speed serial buses.
 - Guides the user through each test setup
 - Performs each measurement in accordance with the relevant test procedure
 - Compares each measured value with the applicable specification limits
 - Fully documents all results
 - QualiPHY helps the user perform testing the right way—every time!



TELEDYNE LECROY **QualiPHY**

DisplayPort Test Report
Overall result: **Pass**

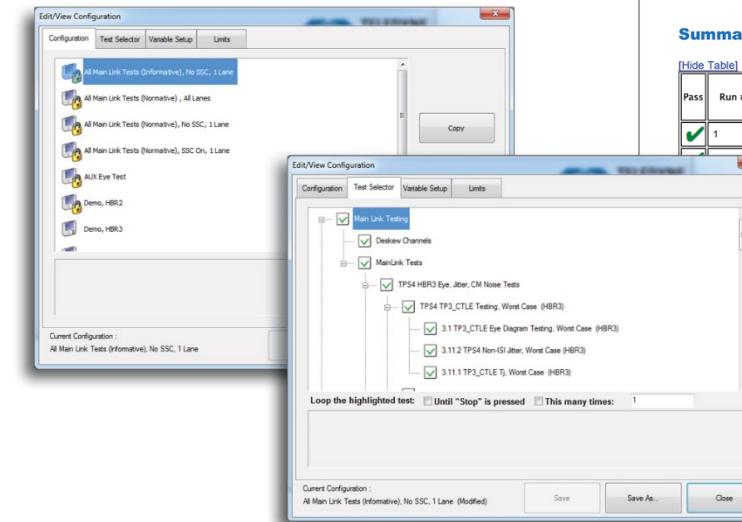
DUT:
Comment:
Time of session start:
Operator:
Temperature
Standard in use:

Run 1:
Time of run:
Configuration in use:
Limits in use:
Oscilloscope Name:
Oscilloscope Serial #:
Comments:
Oscilloscope firmware version:
QualiPHY core version:
QualiPHY script version:
Stylesheet version:

0.1.2.85
1.2.0.6

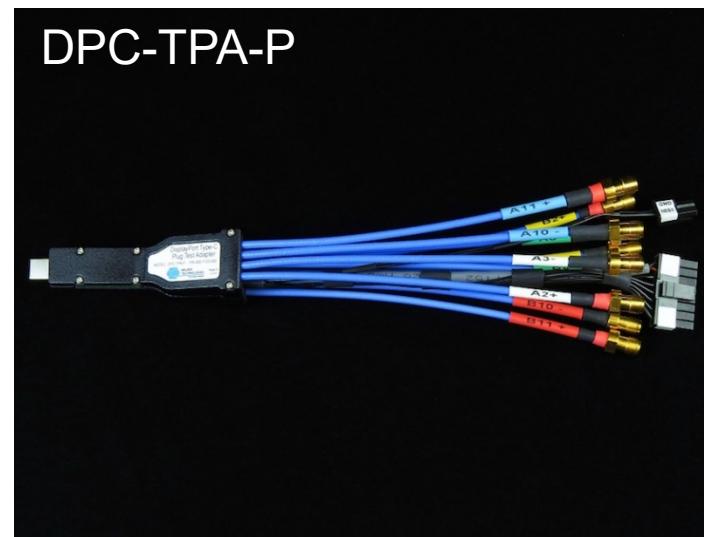
Summary Table

Pass	Run #	Test	Measurement	Lane	Speed	SSC	Nominal Output Level	Nominal Preemphasis	Current Value	Test Criteria
✓	1	3.1	Eye Mask HBR3	Lane0	2.7Gb/s	Disabled	800mV	0.0dB	0	x = 0
✓	1	3.1	Eye Mask HBR3	Lane1	2.7Gb/s	Disabled	800mV	0.0dB	0	x = 0
✓	1	3.1	Eye Mask HBR3	Lane0	1.62Gb/s	Disabled	800mV	0.0dB	0	x = 0
✓	1	3.1	Eye Mask HBR3	Lane1	1.62Gb/s	Disabled	800mV	0.0dB	0	x = 0



Test fixtures

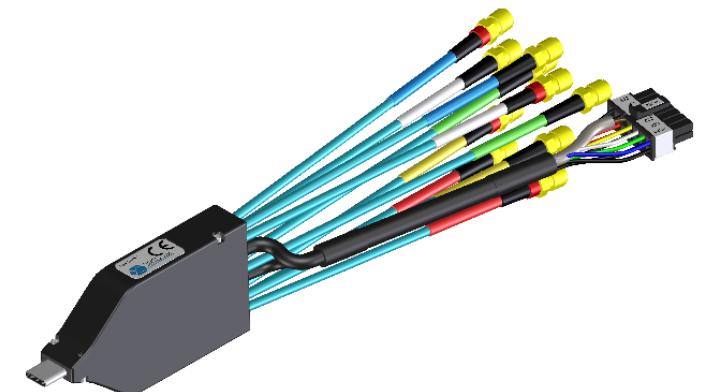
- Adapt DP source port to co-axial (SMA) connectors for direct input to oscilloscope channels
- Also break out AUX channel connectors
- Teledyne LeCroy recommends Wilder Technologies test fixtures
 - Legacy: DP-TPA-P
 - Type-C: DPC-TPA-P



Test fixtures

DUTC Test adapter & Type C TPA

- Supports Thunderbolt testing
 - Requires Thunderbolt Controller
 - Does not require SMP to SMA adapters
- Supports DisplayPort testing
 - Built in DP Receiver functionality
- Supports USB testing
 - Built in LFPS signaling

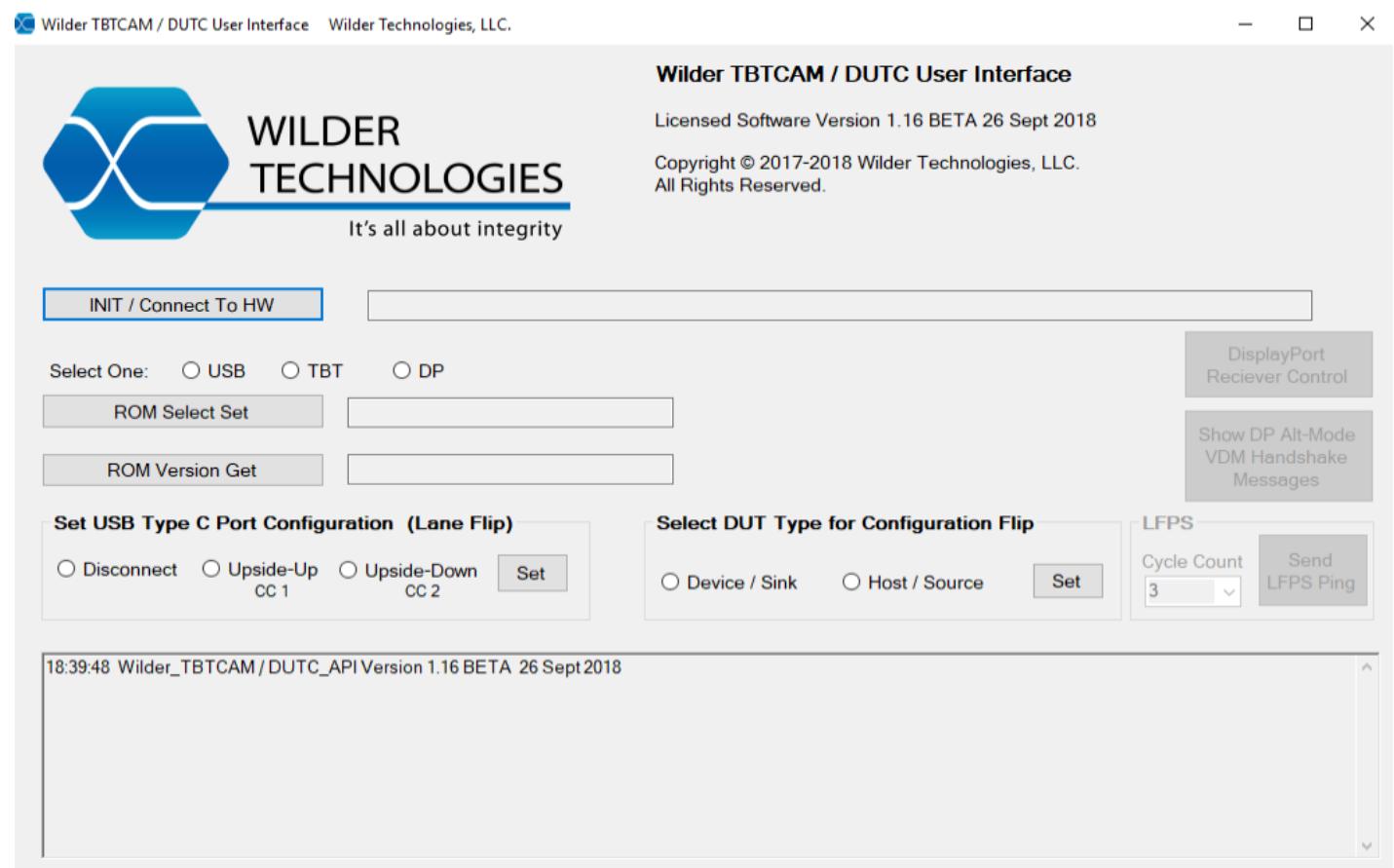


Contact www.wilder-tech.com for more information

Test fixtures

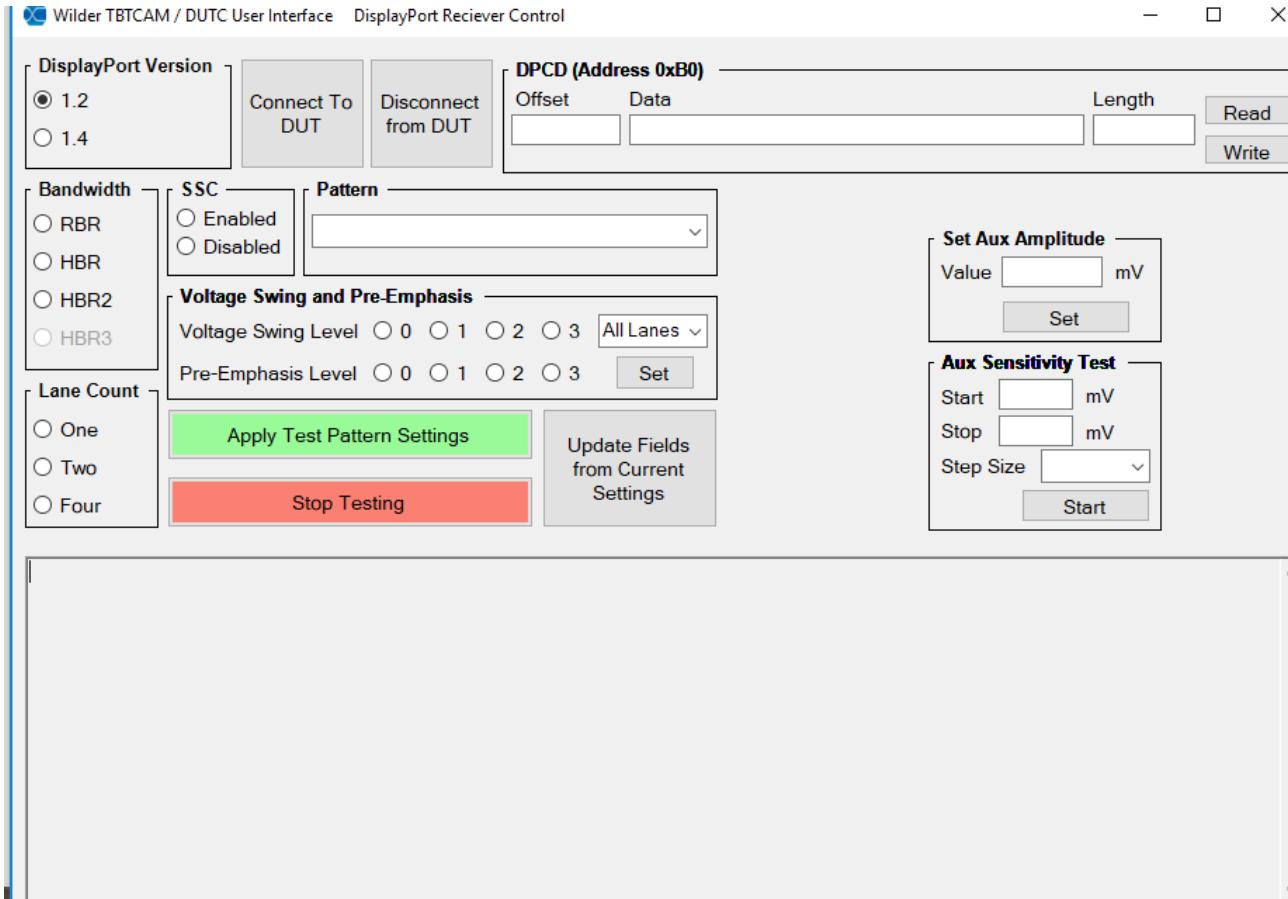
Control Software utility

- Simple operation
- Allow user to select with alt mode they want to operate in.
- Allows user to flip CC lines
- Provides feedback to user on the operations.



Test fixtures

DP Control Software Utility



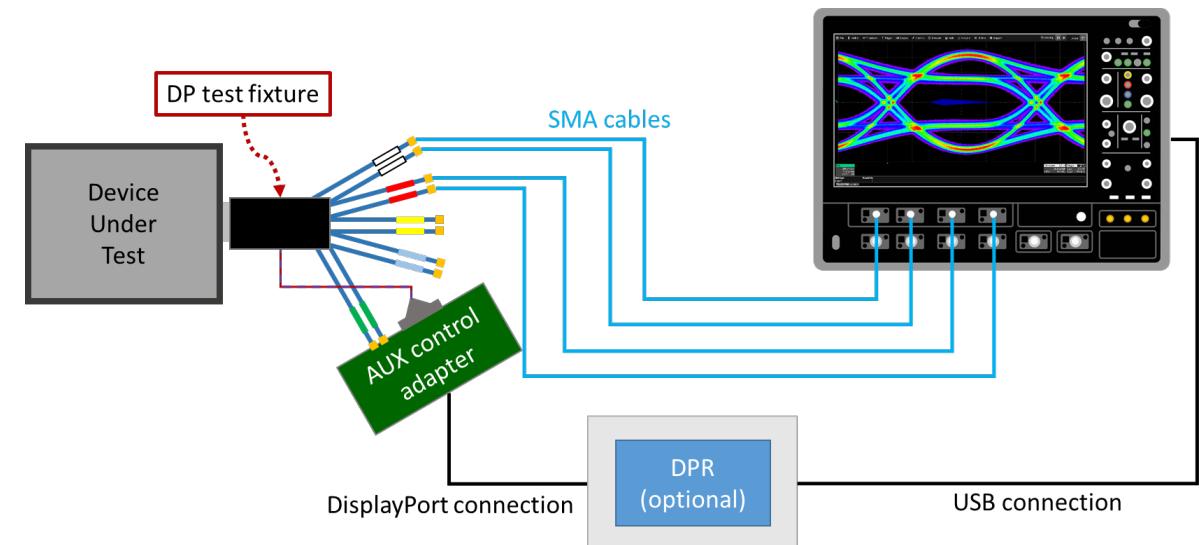
- Allows the user to configure the DUT to the parameters needed for any of the testing requirements.
- Allows for simple configuration changes
- Allows user to write or read registers
- Will test Aux Sensitivity per the specifications

DisplayPort 1.4 Physical layer compliance testing Main link tests



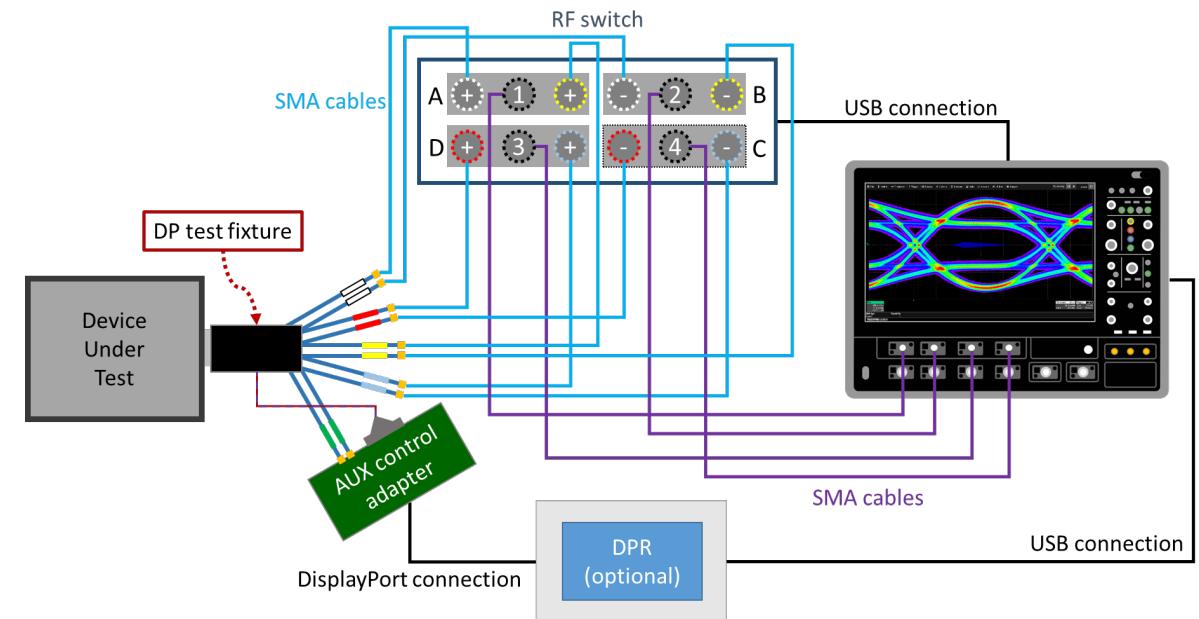
DisplayPort main link test connections – legacy connector

- Up to 2 main link lanes can be directly connected to the oscilloscope
- An AUX control adapter extracts the AUX channel from a connection to a DisplayPort sink
- Optionally, a programmable DisplayPort Reference Sink (DPR) can be used to automate DUT configuration through the AUX channel
 - QPHY-DisplayPort uses this to completely automate main link testing



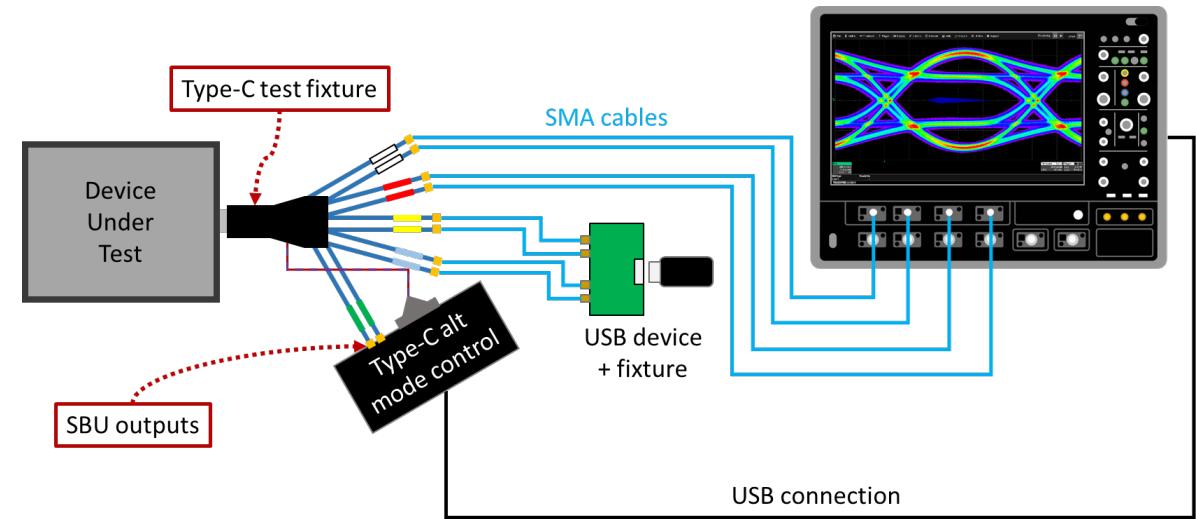
DisplayPort main link test connections – legacy connector

- All 4 main link lanes may be connected to the oscilloscope through an RF switch
- AUX control and DPR connections remain the same
- QPHY-DisplayPort also automates the switch control, for completely automated 4-lane testing



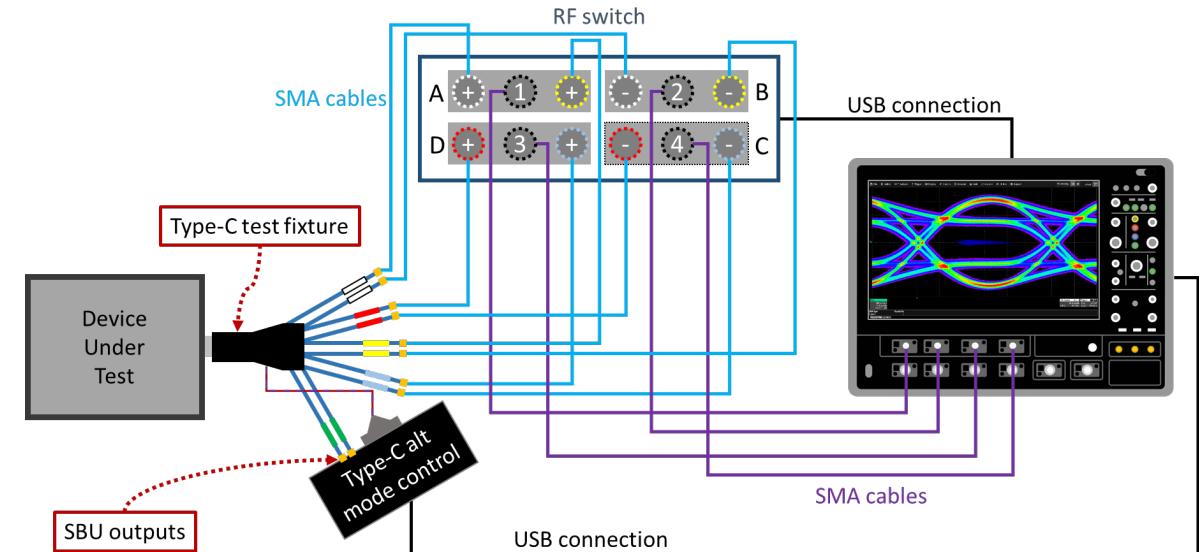
DisplayPort main link test connections – Type-C connector

- Up to 2 main link lanes can be directly connected to the oscilloscope
- A Type-C alt mode controller takes the place of the AUX control adapter
- The alt mode controller can be used to automate DUT configuration
 - QPHY-DisplayPort uses this to completely automate main link testing

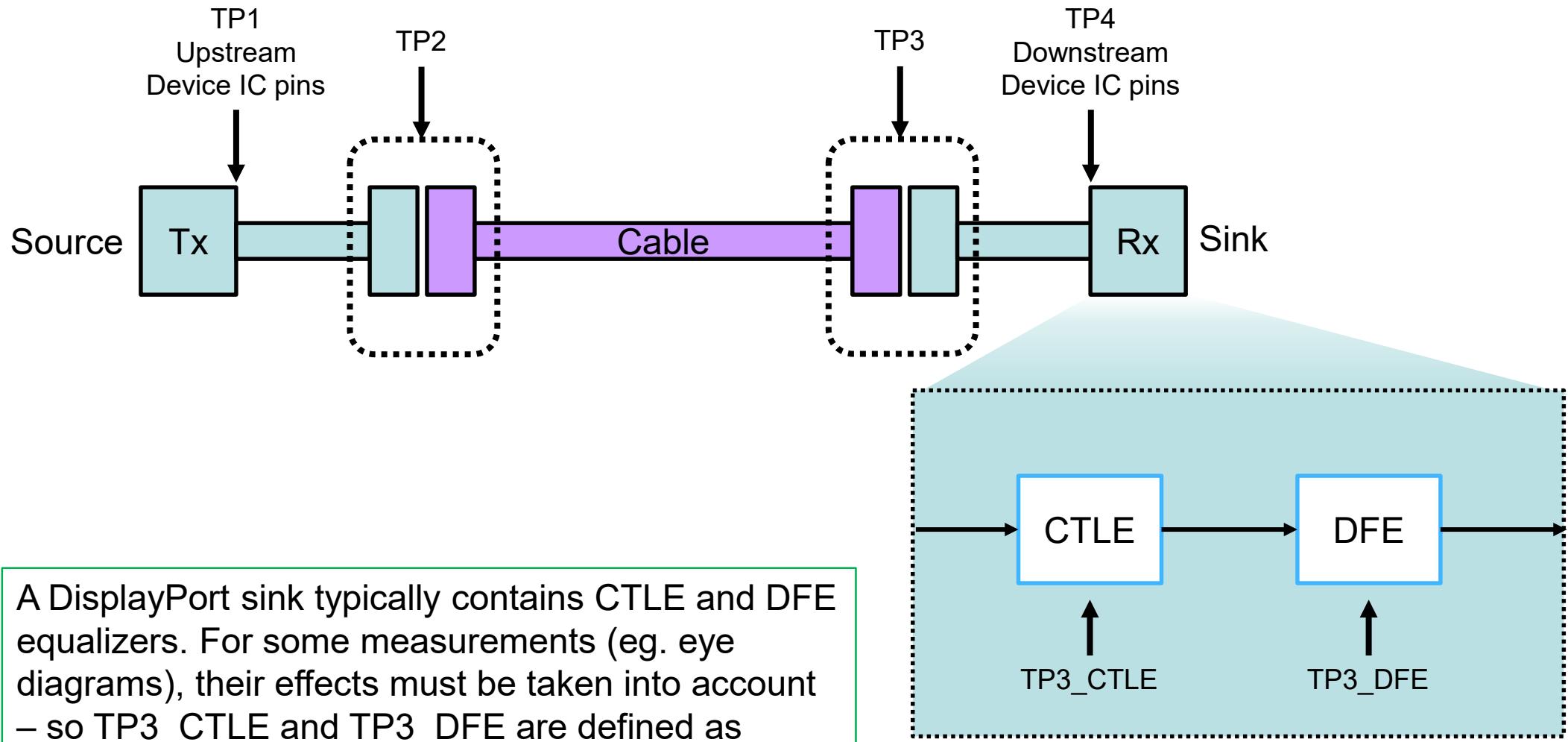


DisplayPort main link test connections – Type-C connector

- All 4 main link lanes may be connected to the oscilloscope through an RF switch
- Alt mode control connections remain the same
- QPHY-DisplayPort also automates the switch control, for completely automated 4-lane testing



DisplayPort measurement points

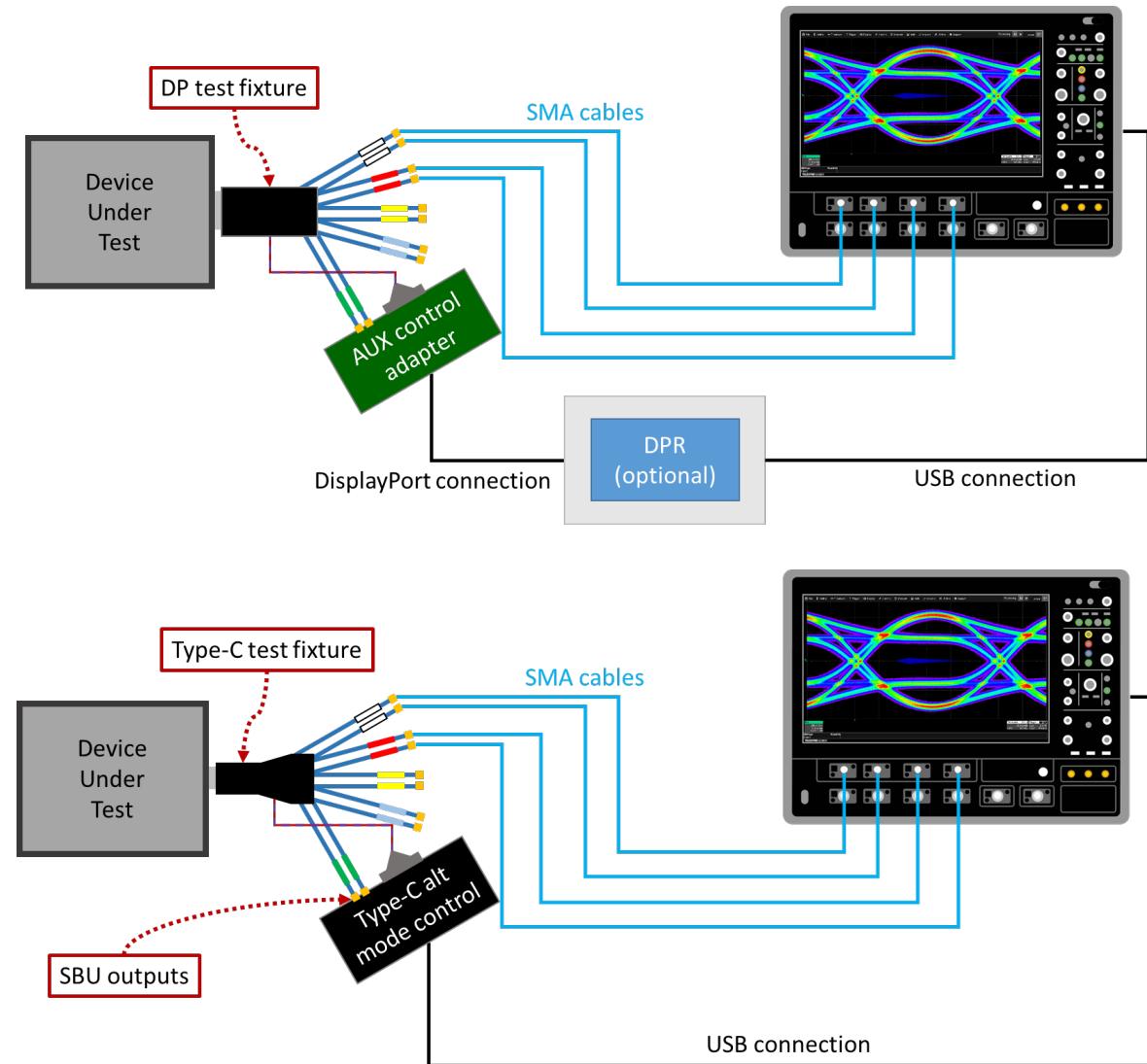
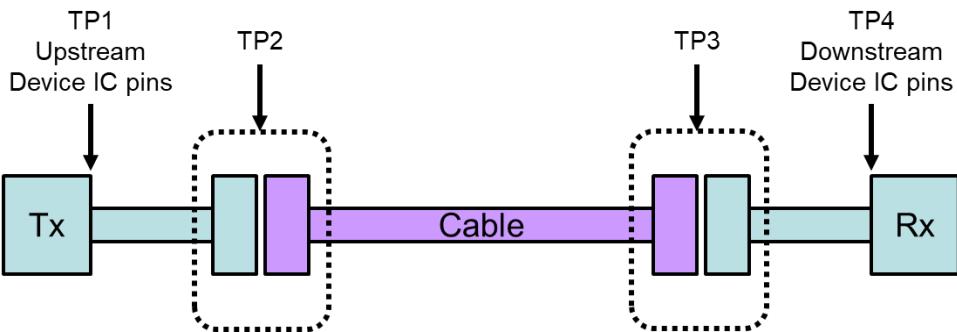


DP1.4 PHY CTS Source Tests and Test Patterns

Test	RBR	HBR	HBR2	HBR3
3.1 Eye Diagram Test (Normative)	PRBS7	PRBS7	CP2520	TPS4
3.2 Non-PE Level Verification Test (Normative)	PRBS7	PRBS7	N/A	N/A
3.3 PE Level Verification & Max Diff Pk-Pk (Normative)	PRBS7	PRBS7	N/A	N/A
3.4 PE Level and Equalization Verification Test (Normative)	N/A	N/A	PLTPAT	PLTPAT
3.5 VTX Pk-Pk Max (Normative)	N/A	N/A	PLTPAT	PLTPAT
3.6 Interpair Skew (Informative)	PRBS7	PRBS7	PRBS7	PRBS7
3.7 Intrapair Skew (Informative)	D10.2	D10.2	D10.2	D10.2
3.8 AC Common Mode Noise (Informative)	PRBS7	PRBS7	PRBS7	TPS4
3.9 Non-ISI Jitter Measurement (Normative)	PRBS7	PRBS7	N/A	TPS4
3.10 TX Differential Return Loss (Informative)	N/A	N/A	N/A	PRBS7
3.11 TJ/RJ/DJ (Normative) D10.2 Jitter (Normative)	PRBS7 N/A	PRBS7 N/A	CP2520 D10.2	TPS4 N/A
3.12 Main Link Frequency (Normative)	D10.2	D10.2	D10.2	D10.2
3.13 Spread Spectrum Modulation Frequency (Normative)	D10.2	D10.2	D10.2	D10.2
3.14 Spread Spectrum Modulation Deviation (Informative)	D10.2	D10.2	D10.2	D10.2
3.15 dF/dT Spread Spectrum Deviation HF Variation (Informative)	D10.2	D10.2	D10.2	D10.2

DisplayPort oscilloscope connections

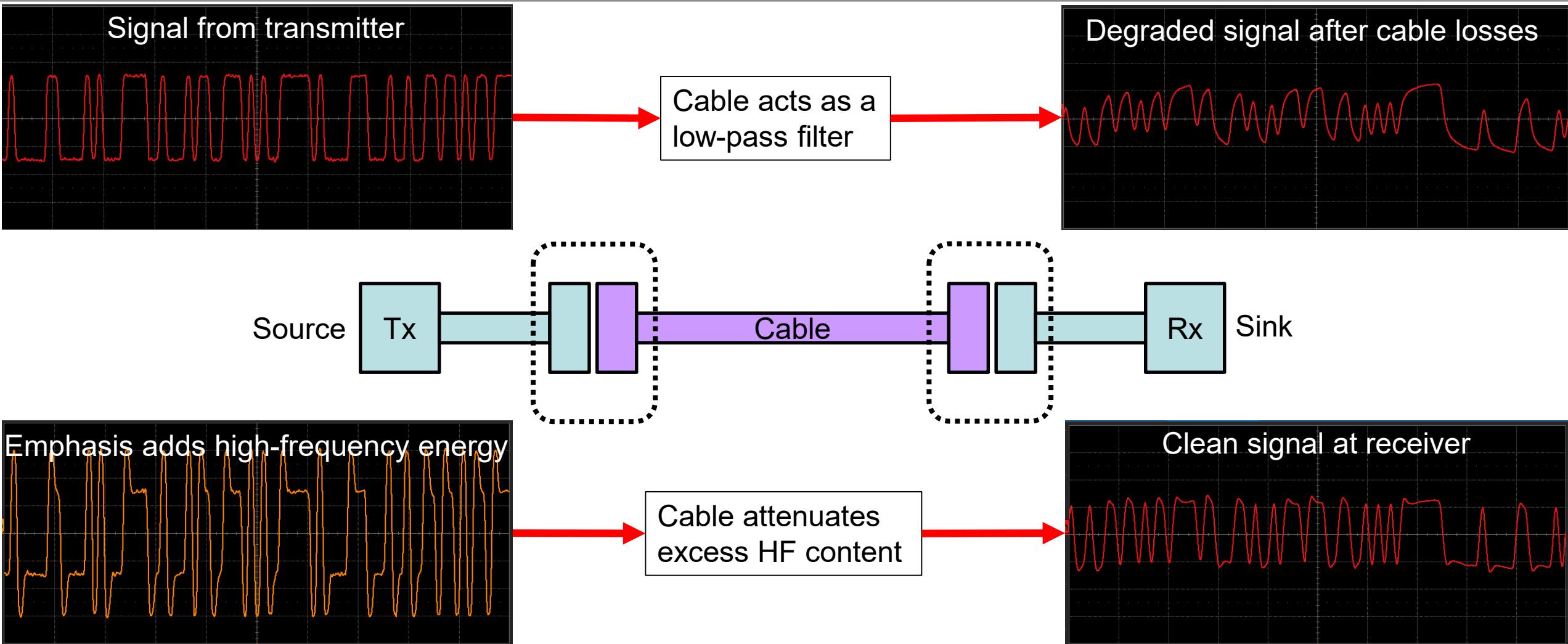
- In both legacy and Type-C test configurations, the oscilloscope is connected directly to the DP source output
- This is functionally equivalent to TP2:



Output Level Verification tests

- A DisplayPort source device must be able to produce multiple output swing and emphasis settings:
 - Differential swing settings: 400 mV, 600 mV, 800 mV, 1200 mV
 - Emphasis settings: 0 dB, 3.5 dB, 6 dB, 9 dB
 - Not all swing/emphasis combinations are valid (see next slide)
- Compliance tests measure:
 - Differential peak-to-peak voltage
 - Transmit emphasis levels
 - Non-transition voltage levels
- Ensure that the relationship between output swing/emphasis **settings** (and the actual **measured** output is monotonic.

What is pre-emphasis?



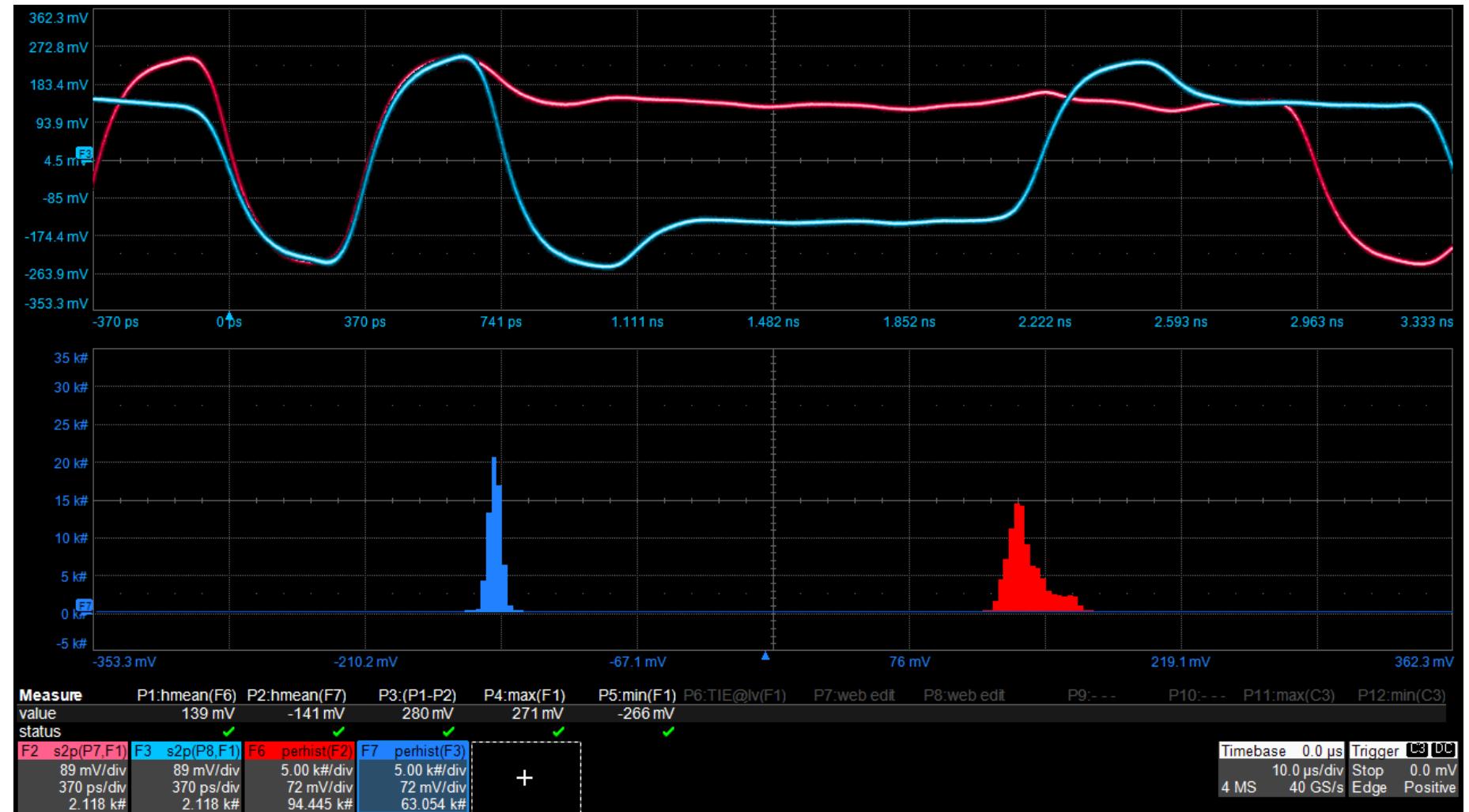
Output swing and emphasis combinations



	0 dB	3.5 dB	6 dB	9 dB
400 mV	Valid	Valid	Valid	Valid
600 mV	Valid	Valid	Valid	X
800 mV	Valid	Valid	X	X
1200 mV	Valid	X	X	X

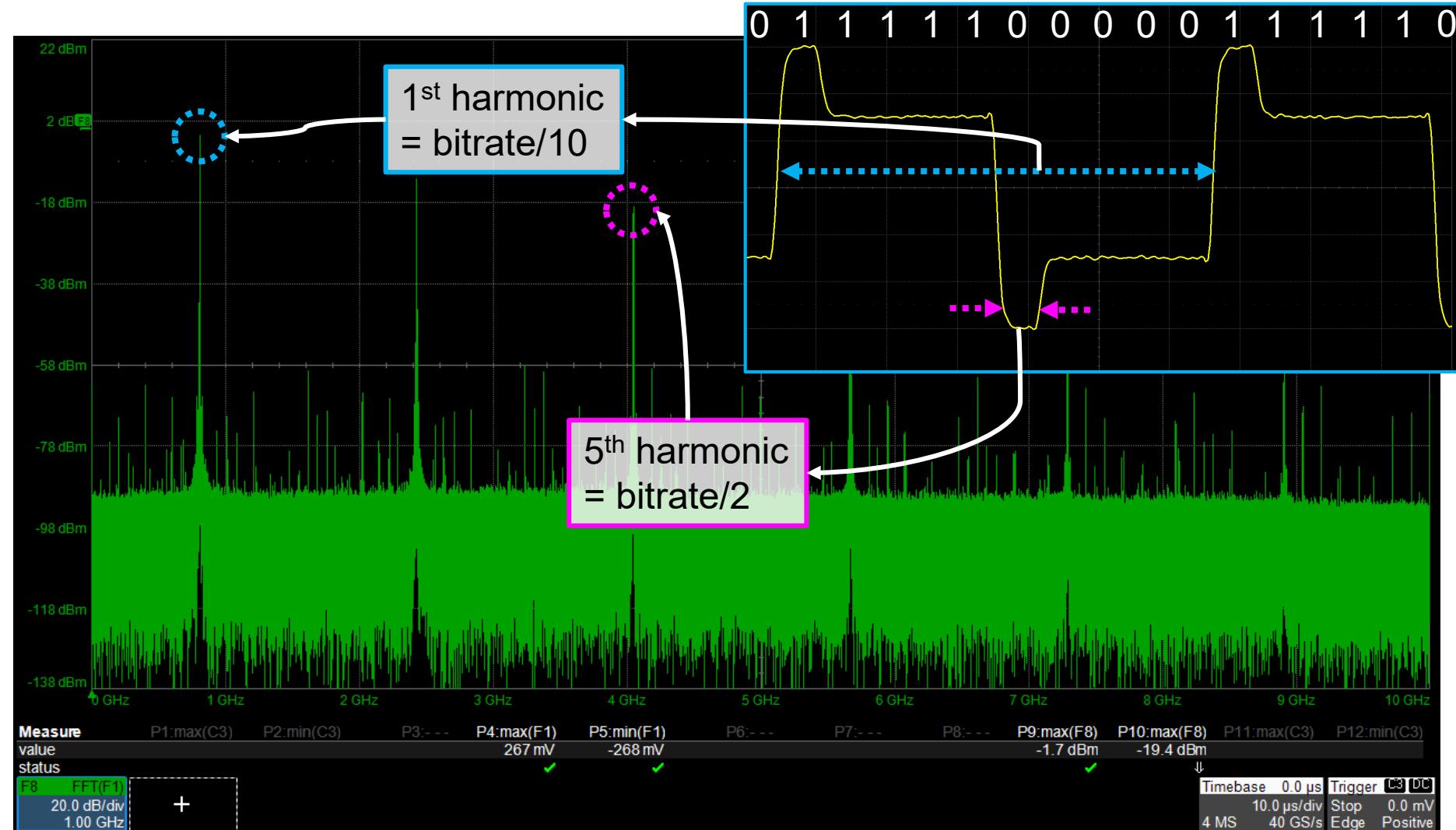
Level verification tests – RBR/HBR methodology

- Specific patterns are found in the transmitted waveform
- Histograms of the voltage levels at emphasized and non-emphasized points in the pattern are compiled
- Mean histogram values are used to calculate swing and emphasis levels



Level verification tests – HBR2/HBR3 methodology

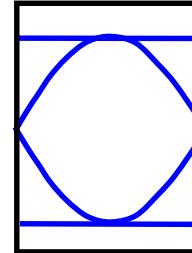
- PLTPAT (5 0's followed by 5 1's) is used
- Spectrum of signal is analyzed
- Relationship between 1st- and 5th- harmonic magnitude changes with emphasis level



How an eye diagram is created



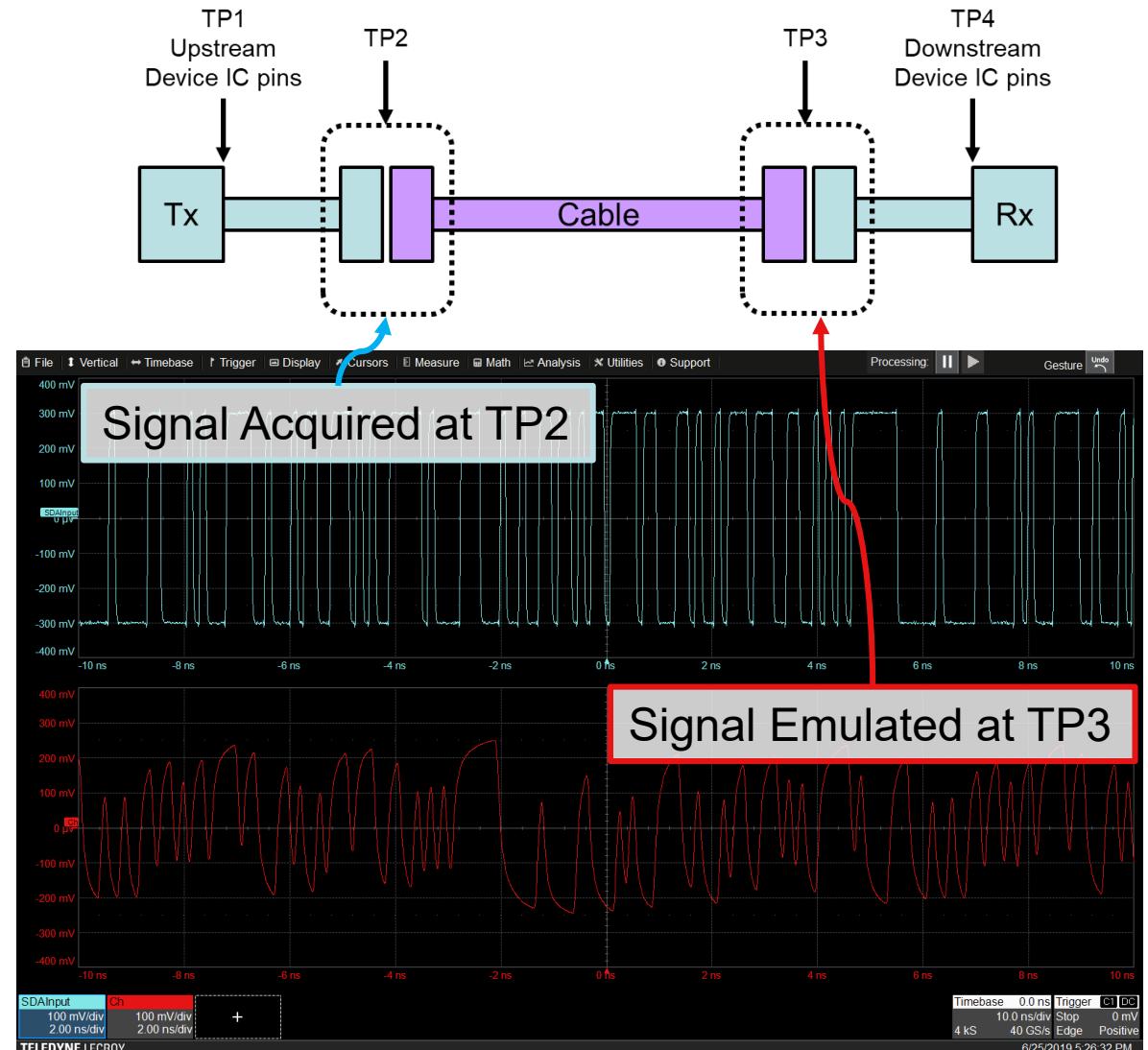
Slices are overlaid in a persisted fashion



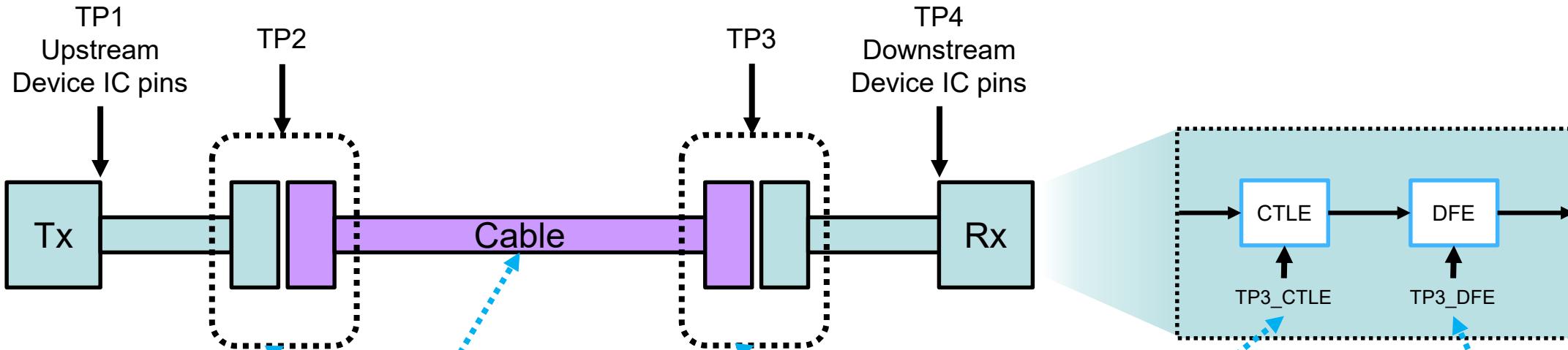
Eye Pattern Displayed

Eye Diagram test at HBR3

- Eye diagram testing for HBR3 is done at TP3 with equalization
- The signal is still captured by the oscilloscope at TP2
- A model of a worst-case compliant cable (provided by VESA as an S-parameter file) is embedded by the oscilloscope software to emulate the signal at TP3
 - We have content on S-parameters



Eye diagram test procedure overview



Step 1: Capture signal on oscilloscope at TP2

Step 3: Signal with emulated cable losses is what the signal looks like at TP3

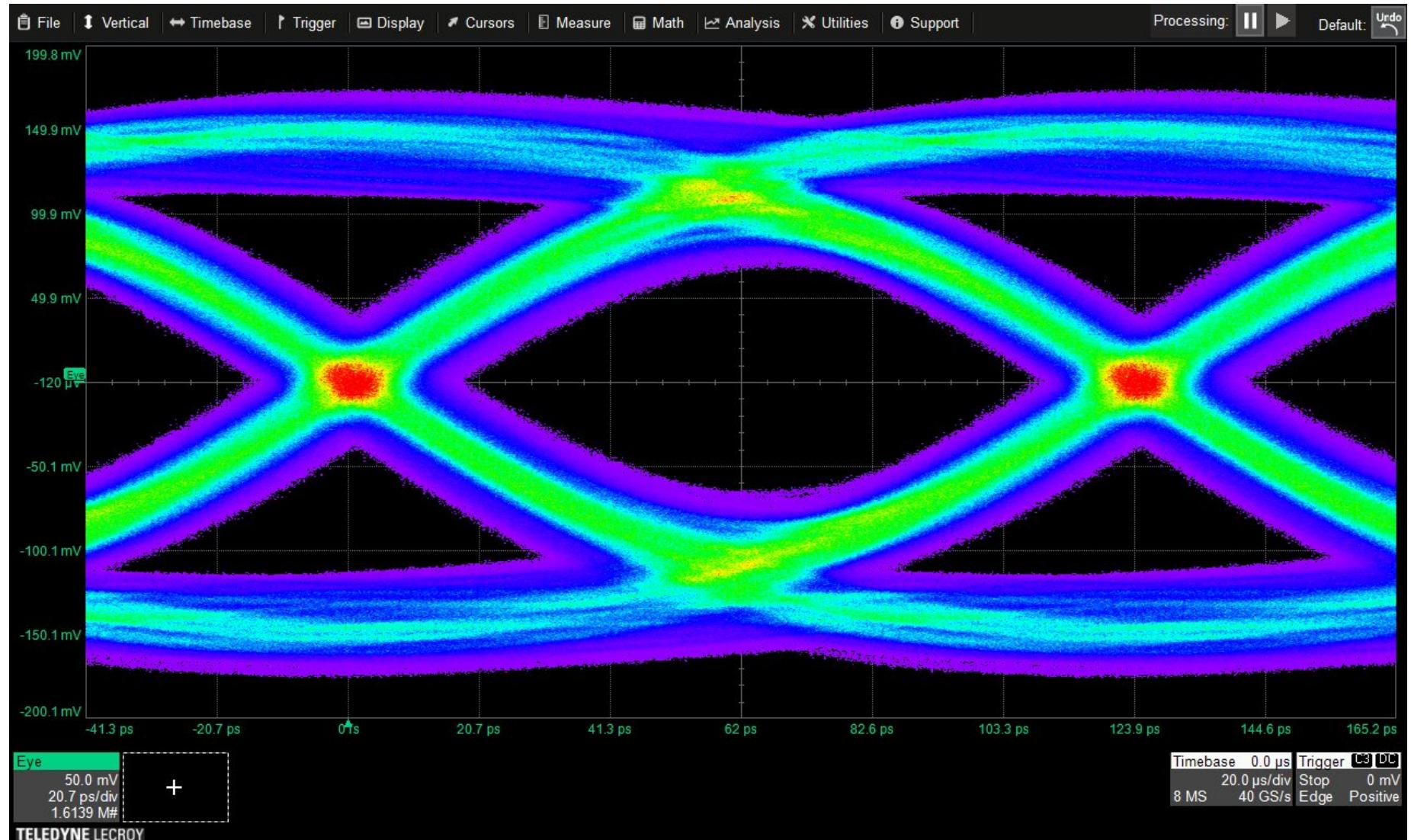
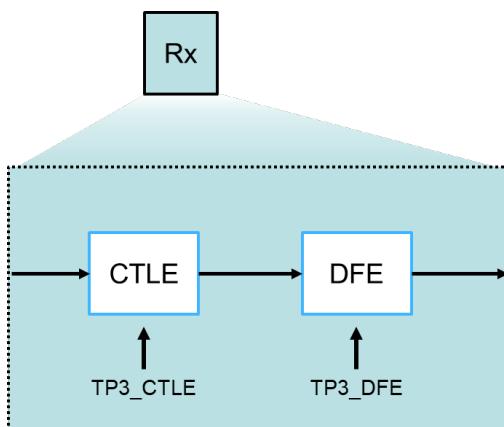
Step 2: Emulate cable losses using oscilloscope software

Step 4: Emulate various receiver CTLEs and create an eye diagram. If the eye passes the TP3_CTLE mask, the device passes

Step 5: If the device fails TP3_CTLE eye, use the VESA DFE tool to emulate TP3_DFE. If this eye passes, the device passes – otherwise it fails

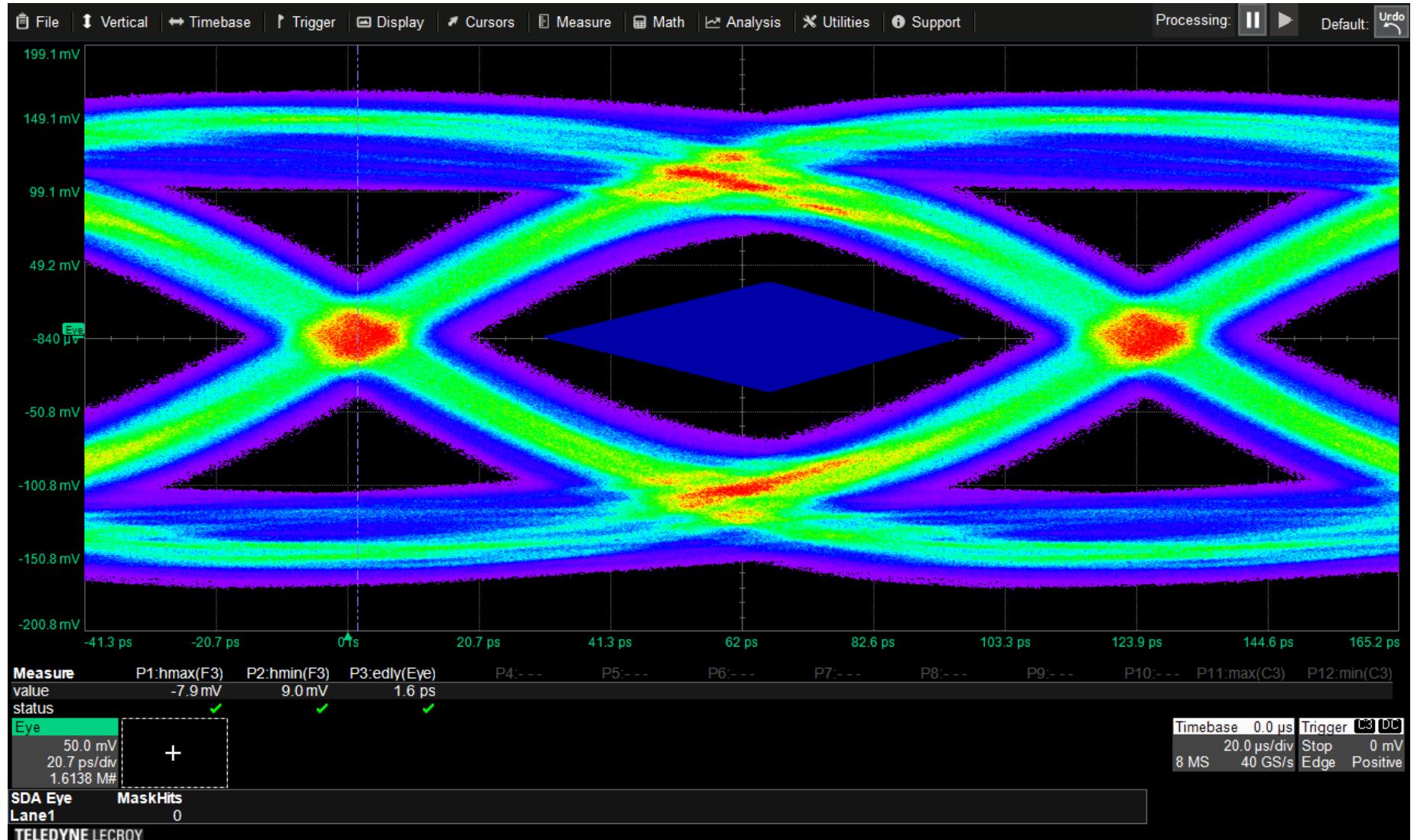
Eye Diagram test at TP3_CTELE

- To emulate the action of the receiver CTLE, the oscilloscope scans through multiple standard DP sink reference CTLEs (defined in the DP1.4 CTS)



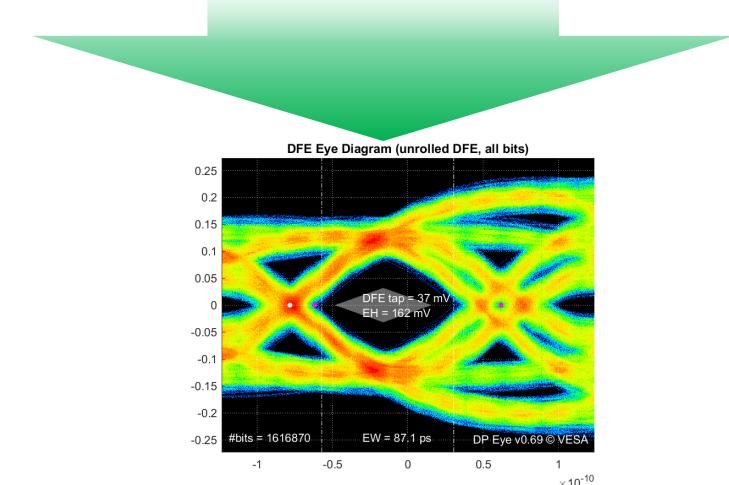
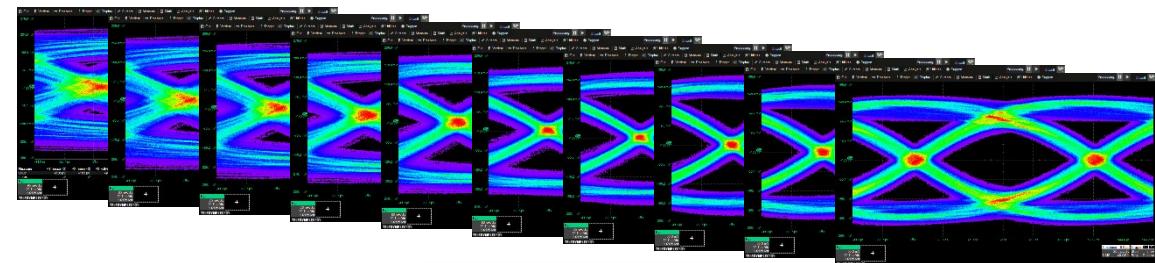
Eye Diagram test at TP3_CTE

- CTLE setting which gives the largest eye height is tested against a mask
 - Inner mask height = 65 mV
- If this mask test passes, the device **passes** the eye diagram test
- If it fails this mask, move on to the TP3_DFE test



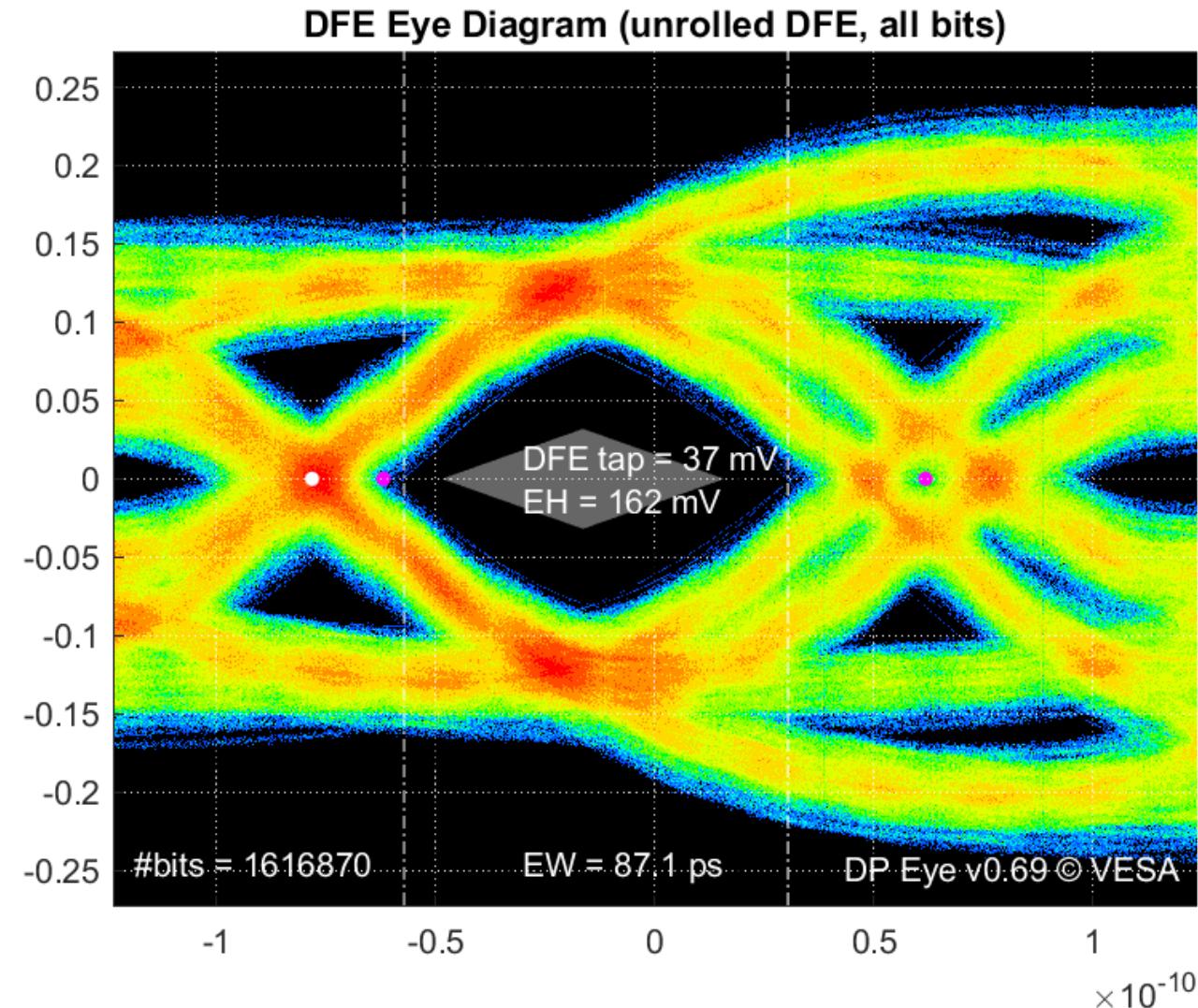
Eye Diagram test at TP3_DFE

- To ensure correlation among different test vendors, VESA has produced an external software tool to emulate the action of a reference DFE
- The oscilloscope software provides waveforms at TP3_CTE for **all** CTLE settings to the tool
 - Also provides a recovered clock waveform for each TP3_CTE signal
- The VESA DFE tool then processes all waveforms and selects the one with largest eye height



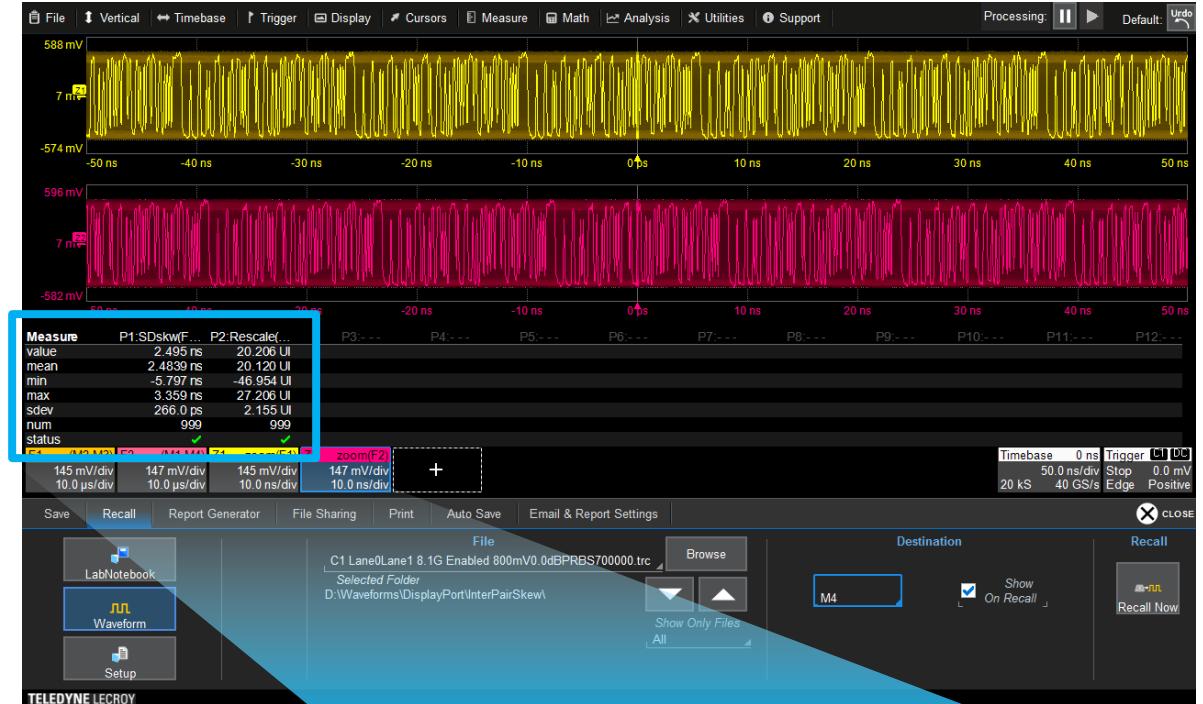
Eye Diagram test at TP3_DFE

- If the eye height at TP3_DFE is greater than 100mV:
PASS
- Otherwise:
FAIL



Inter-pair skew

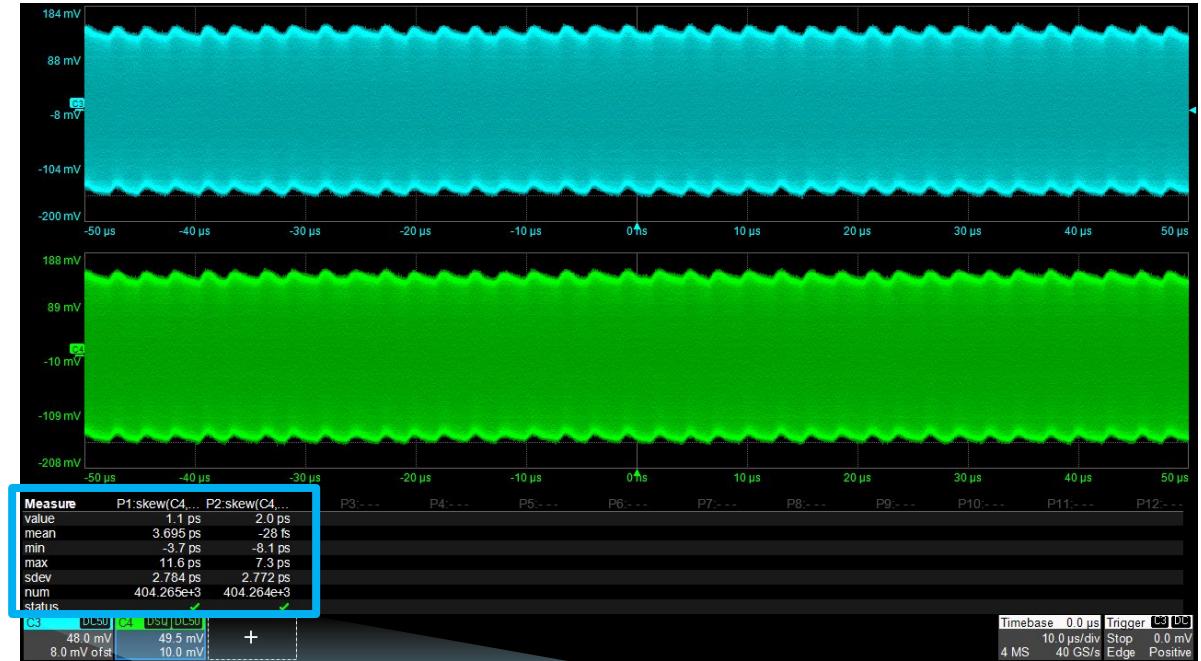
- Applies to DisplayPort transmitters with more than one main link data lane
- Verifies that the skew between any two differential pairs does not exceed the allowable skew
- The allowable skew depends on the lane rate and is specified in the CTS document.



Measure	P1:SDskw(F...)	P2:Rescale(...)
value	2.495 ns	20.206 UI
mean	2.4839 ns	20.120 UI
min	-5.797 ns	-46.954 UI
max	3.359 ns	27.206 UI
sdev	266.0 ps	2.155 UI
num	999	999
status	✓	✓

Intra-pair skew

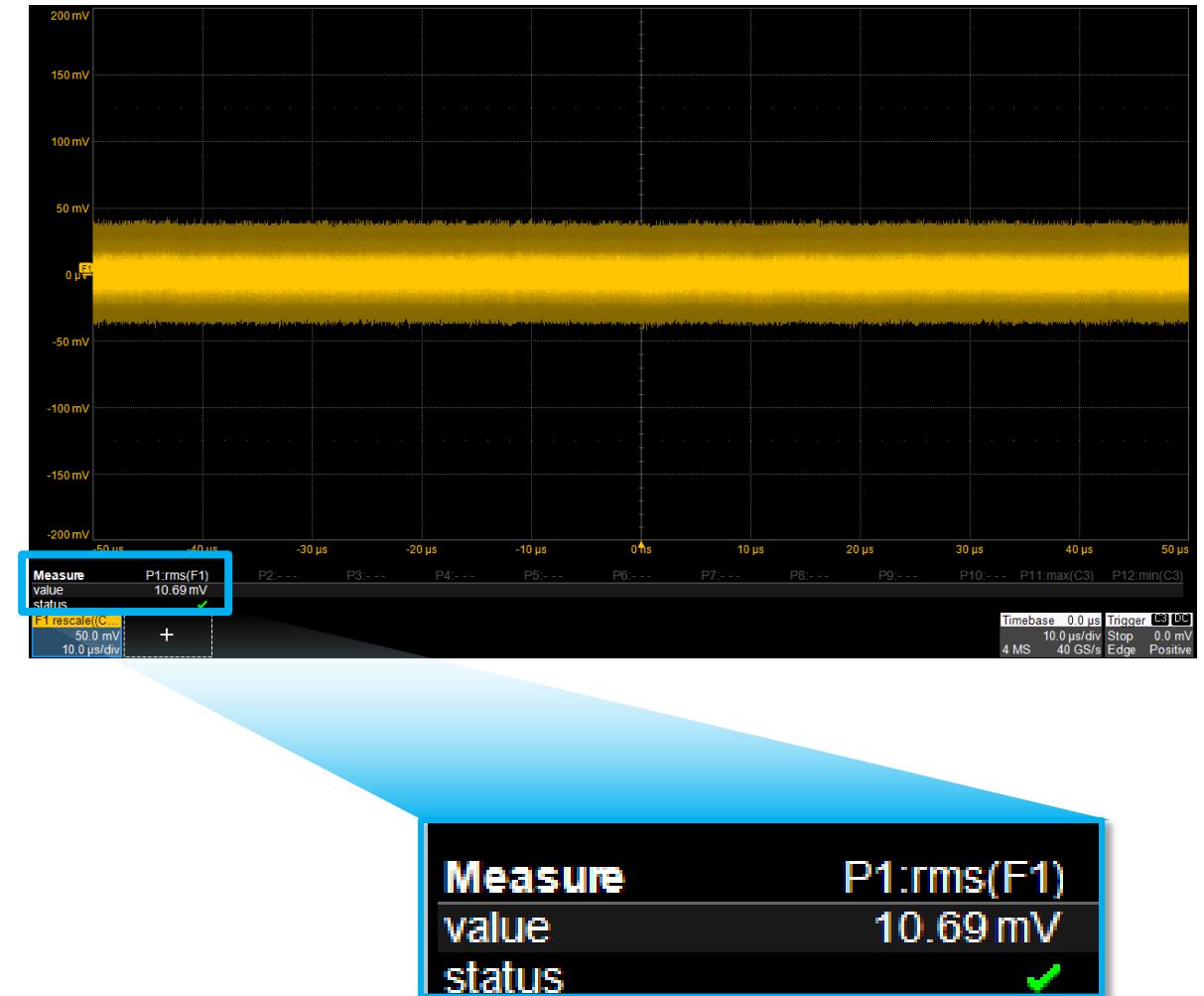
- Informative (non-normative) test
- Verifies whether the skew between the 2 opposing outputs of each differential pair is within the maximum allowable
- Excessive intra-pair skew can result in a degraded eye diagram and excessive bit errors.



Measure	P1:skew(C4,...)	P2:skew(C4,...)
value	1.1 ps	2.0 ps
mean	3.695 ps	-28 fs
min	-3.7 ps	-8.1 ps
max	11.6 ps	7.3 ps
sdev	2.784 ps	2.772 ps
num	404.265e+3	404.264e+3
status	✓ ✓	

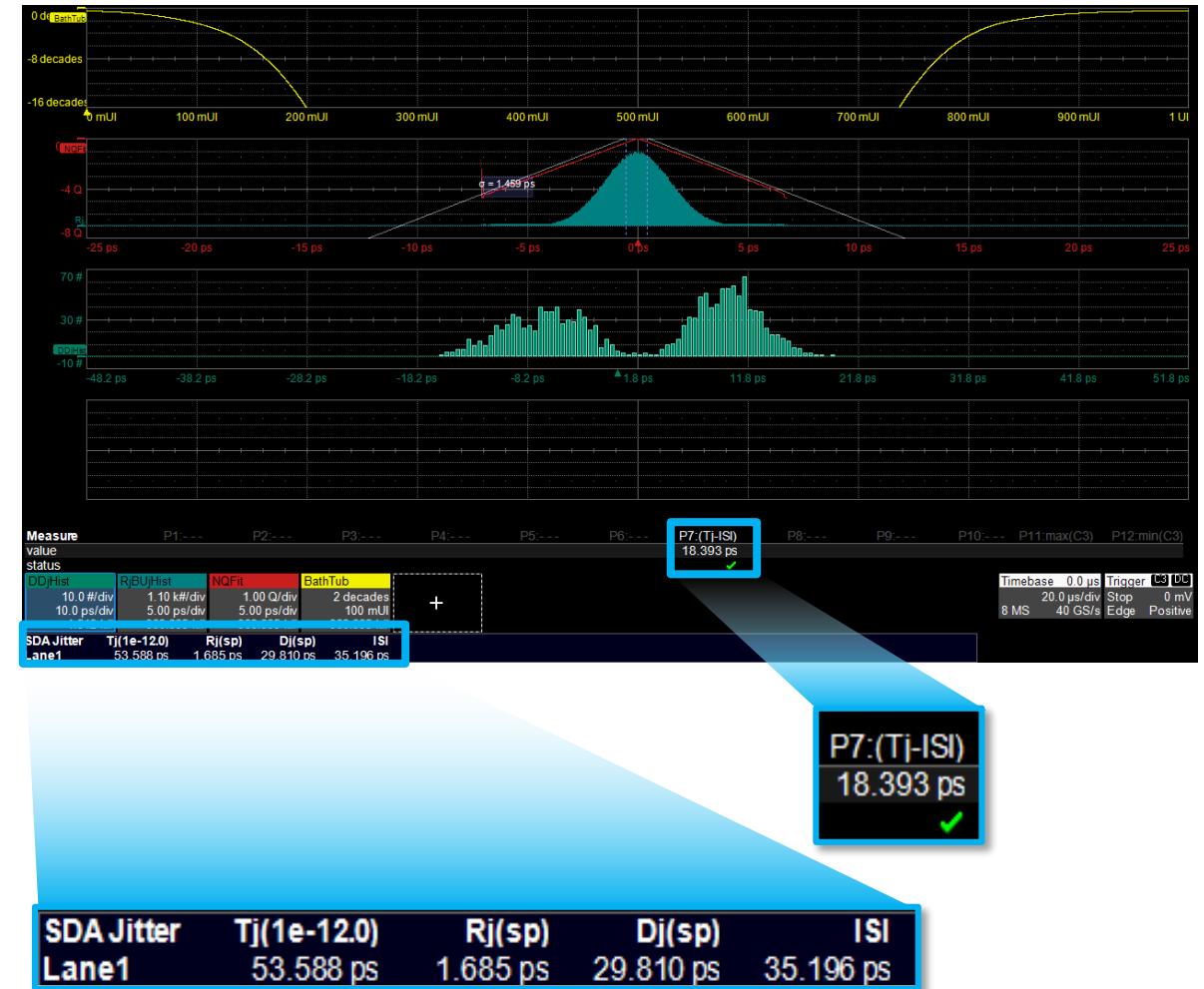
Common-mode noise

- Informative (non-normative) test
- Measures AC common-mode noise on each differential pair

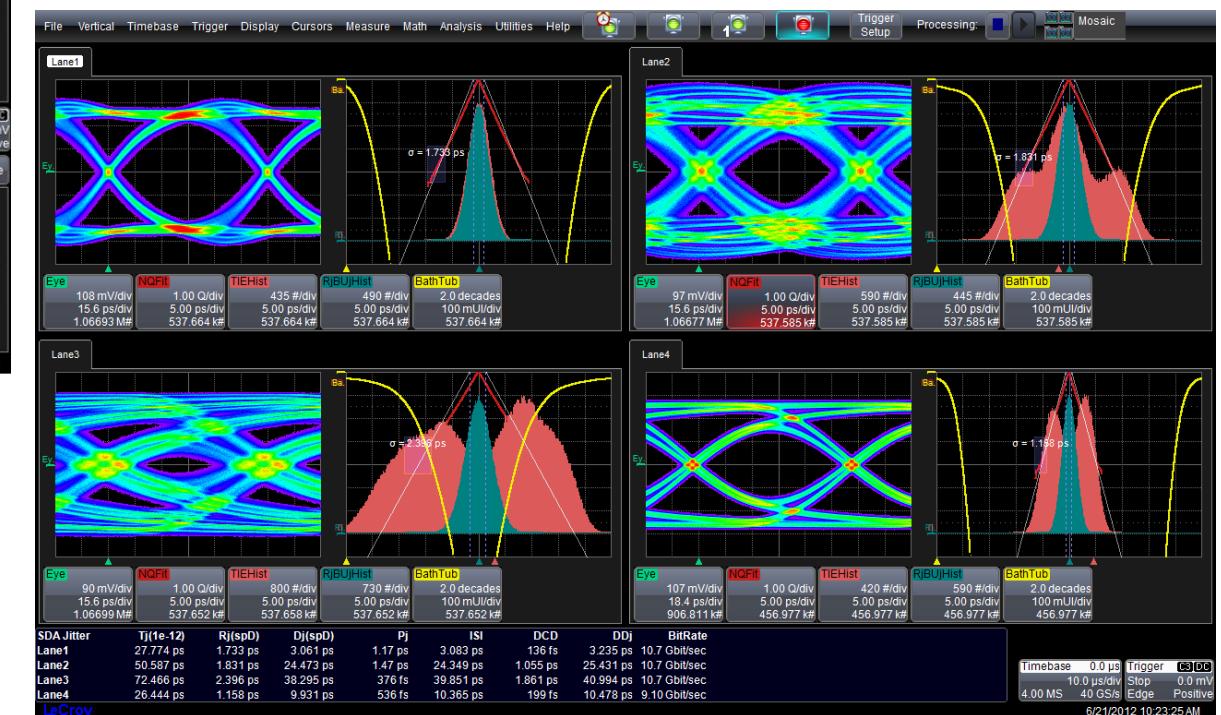
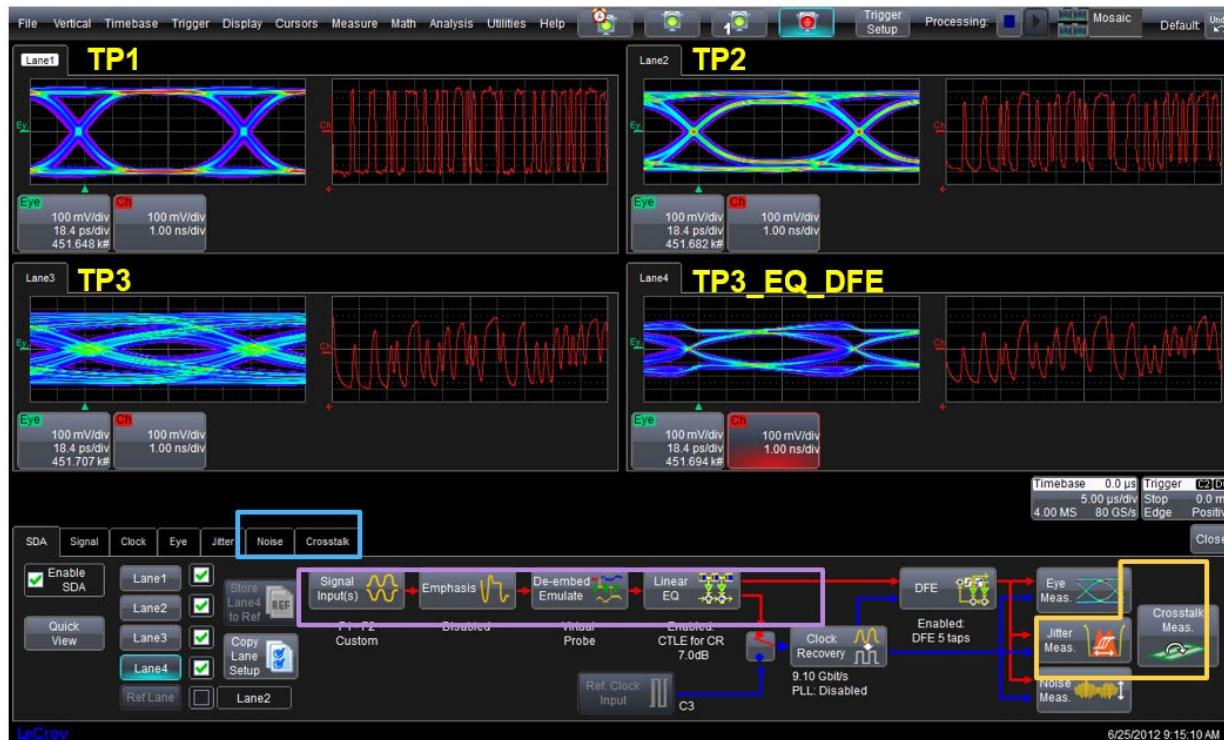


Jitter tests

- Normative test is carried out at TP2
- Non-ISI jitter limit at 1e-6 BER:
 - HBR3: 230 mUI (28.4 ps)
 - HBR2: Not specified/required
 - HBR: 276 mUI (102 ps)
 - RBR: 170 mUI (105 ps)



SDAIII-CompleteLinQ Solution: Multi-lane, Eye, Jitter, Noise and Crosstalk, EyeDrill, VirtualProbe

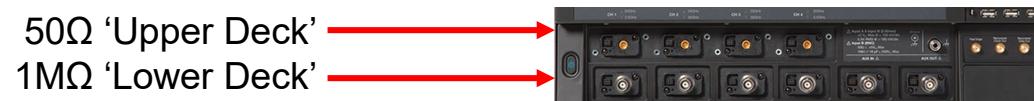
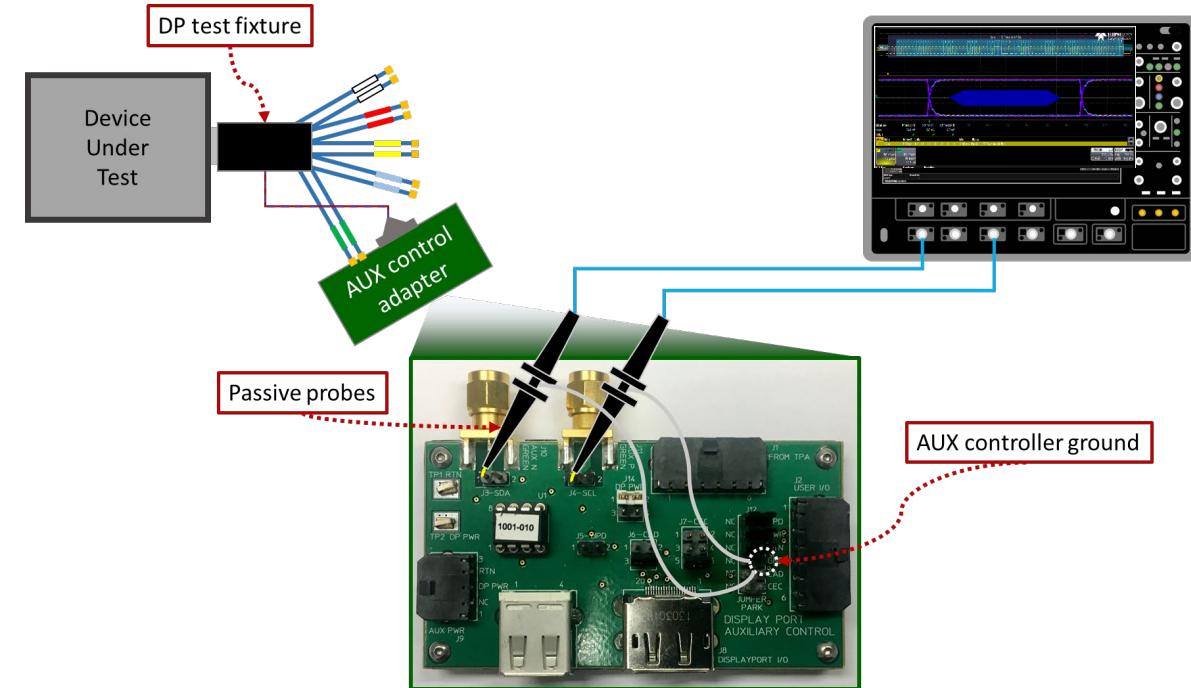


DisplayPort 1.4 Physical layer compliance testing AUX channel tests



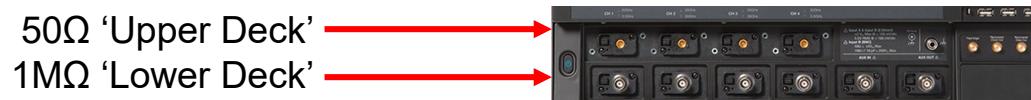
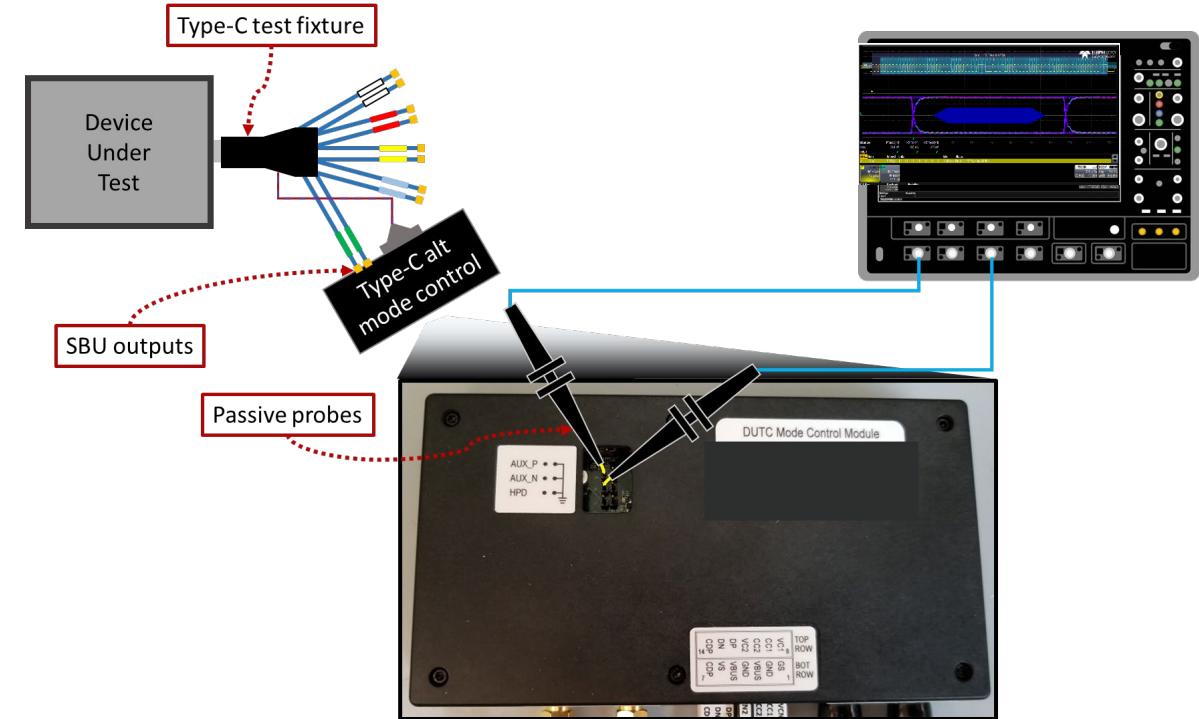
DisplayPort AUX channel test connections – legacy connector

- AUX channel is a low-speed interface
- AUX channel can be probed on the AUX control adapter using two passive probes
 - Teledyne LeCroy WaveMaster oscilloscopes have built-in $1\text{ M}\Omega$ inputs, allowing passive probes to be used without expensive, cumbersome adapters



DisplayPort AUX channel test connections – Type-C connector

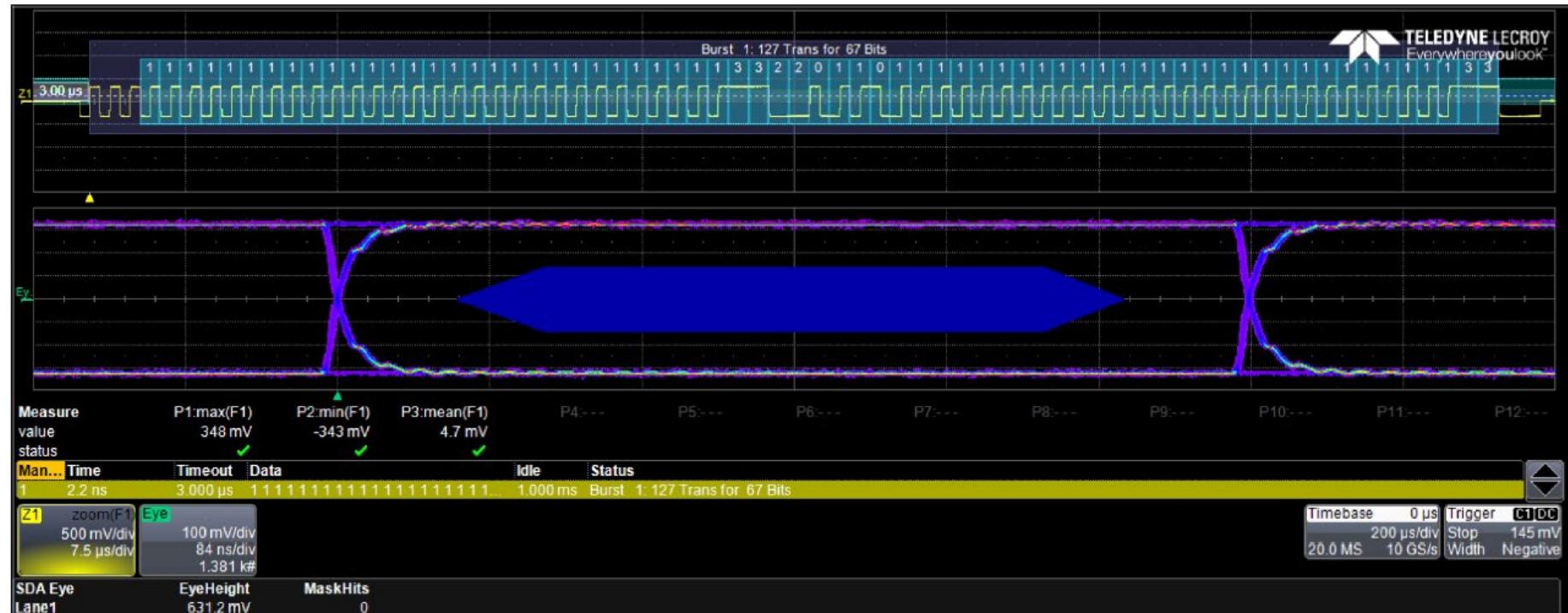
- AUX channel is a low-speed interface
- AUX channel can be probed on the alt mode controller using two passive probes
 - Teledyne LeCroy WaveMaster oscilloscopes have built-in $1\text{ M}\Omega$ inputs, allowing passive probes to be used without expensive, cumbersome adapters



AUX channel test: Eye diagram

- Eye diagram made from a specific section of an AUX signal packet

- Pass criteria:
 - Signal does not impinge on mask
 - Differential pk-pk level $\geq 290\text{mV}$



Test 8.1 - AUX Channel Eye Test

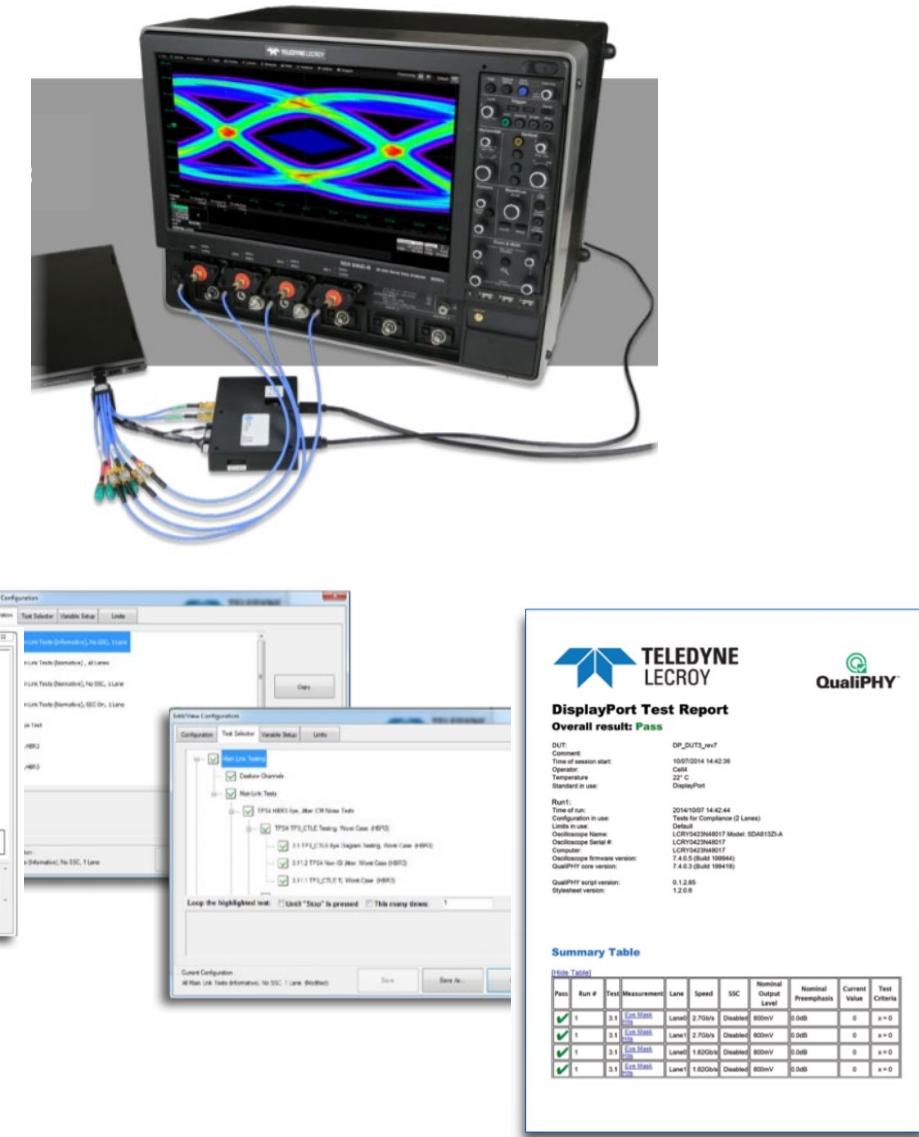
AUX channel test: Slew rate

- Tests that the AUX channel slew rate is not too fast
 - Fast edges on the AUX channel could induce noise on the main link
- Pass criterion:
slew rate < 375 mV/nS



DP1.4 - Required Test Equipment for DP Source PHY Testing

- Oscilloscope
 - WaveMaster 816Zi-B
(16 GHz or higher with 80 GS/s)
- Software
 - DisplayPort Compliance Software (QPHY-DisplayPort)
 - Automates Main Link & AUX PHY Tests
 - SDAIII, and EyeDrill
- Test Fixtures
 - Wilder Technologies



High-speed Interconnect Analyzer for S-parameter extraction

WavePulser-40iX-BUNDLE		
Frequency	Frequency Range	DC to 40 GHz
	S-parameters	Single-ended and Mixed-mode
	Calibration	Internal automatic and manual
	Dynamic Range	67 dB @40 GHz
Time	Spatial Resolution	< 1 mm
	Impedance Profile	Differential and Common Mode
	TDR/TDT	TDR/TDT
	Step/Impulse Rise Time	8.5 ps
Deep Toolbox	De-embedding	Yes, built-in
	Time-Gating	Yes, built-in
	Eye-Diagrams Emulation	Yes, built-in
	Jitter Analysis	Yes, built-in
US List Price		Less than 50 K\$



WavePulser 40iX

DisplayPort 1.4 Physical layer compliance testing Sink and Active Cable tests



DisplayPort PHY CTS Sink Compliance Testing

HS SSG



Variable ISI



RT Oscilloscope

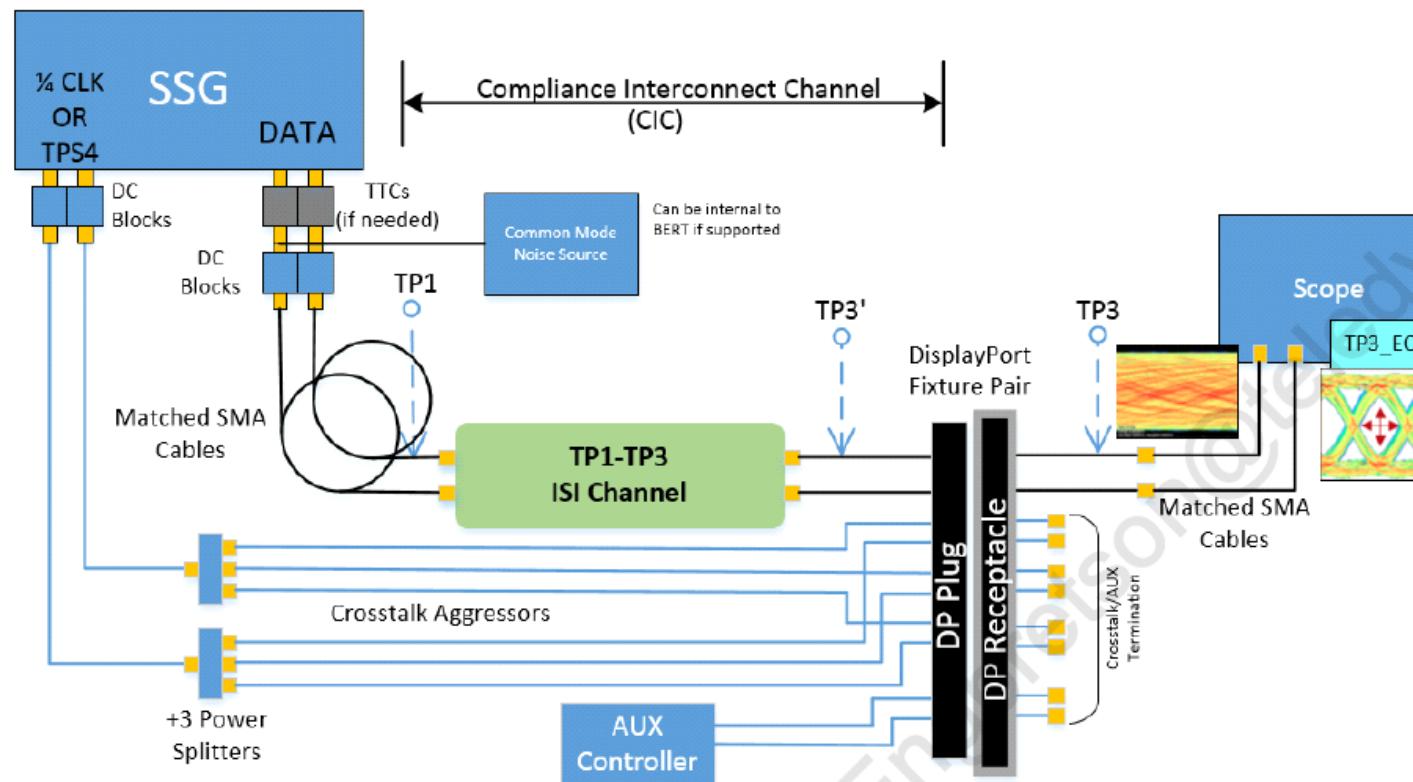
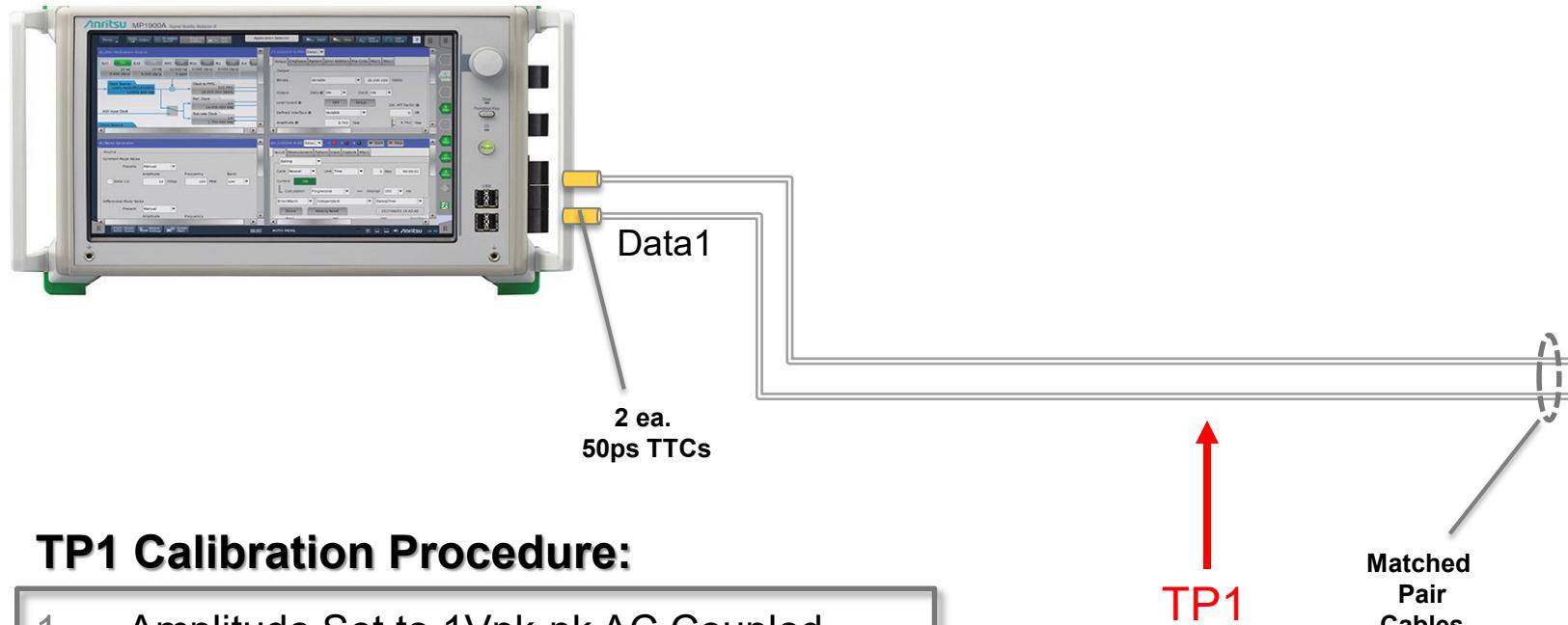


Figure 4-2: HBR3/HBR2/HBR JTOL Test Calibration Setup

DisplayPort PHY CTS Sink TP1 Calibration

SDA800Zi

Anritsu MP1900A



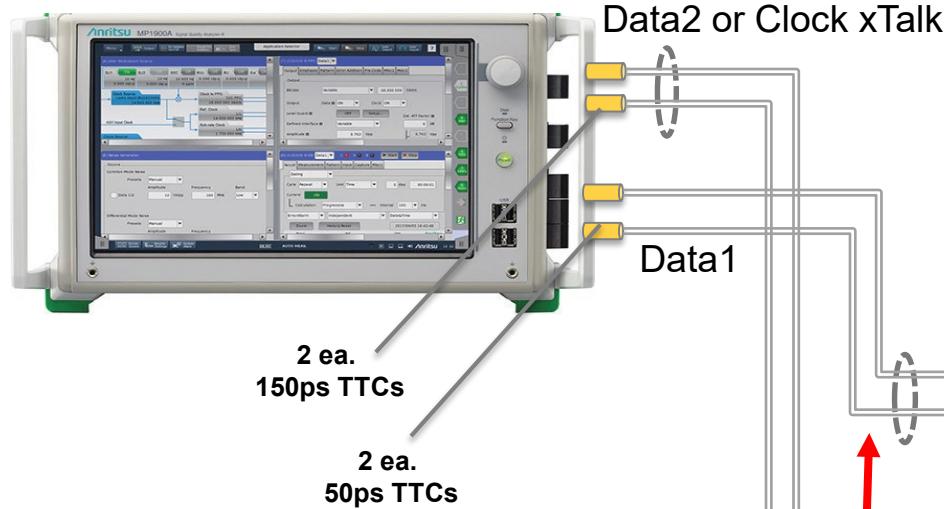
TP1 Calibration Procedure:

1. Amplitude Set to 1Vpk-pk AC Coupled
2. 50ps TTCs Connected to Data/#Data
3. Calibrate RJ_{rms} with D24.3 Pattern (1100)
4. Calibrate SJ_{FIXED} (HBR3 and HBR2) with D24.3 Pattern
5. Calibrate SJ_{SWEEP} at each frequency

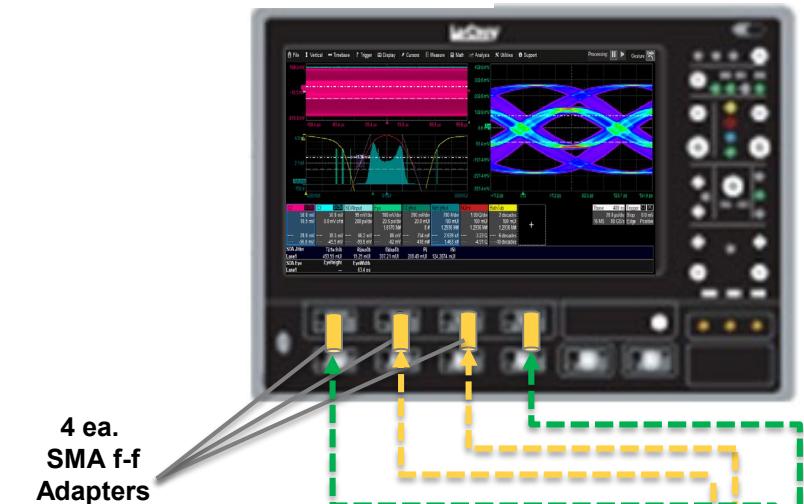
DisplayPort PHY CTS Sink TP2/TP3 Calibration

SDA800Zi

Anritsu MP1900A

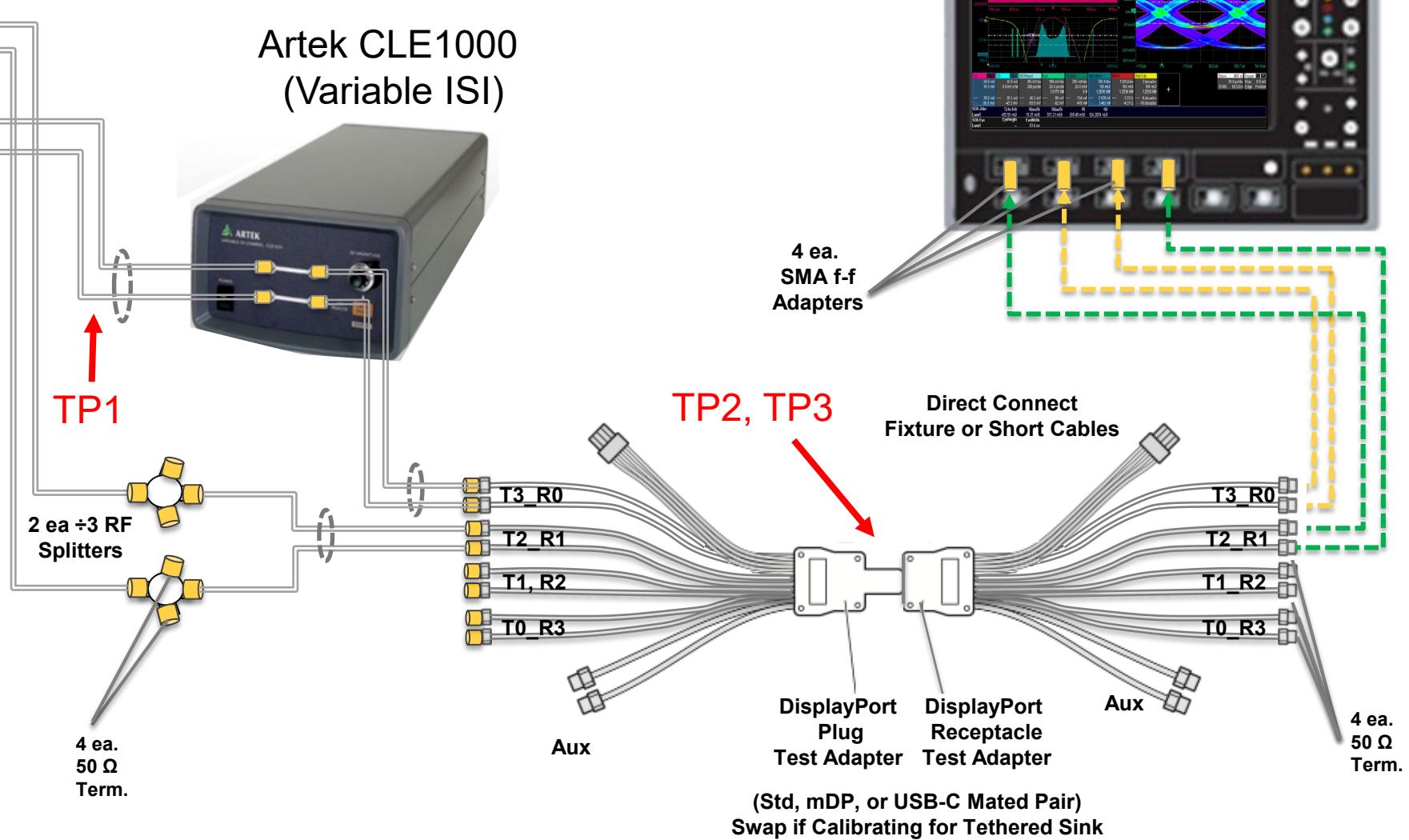


Artek CLE1000
(Variable ISI)



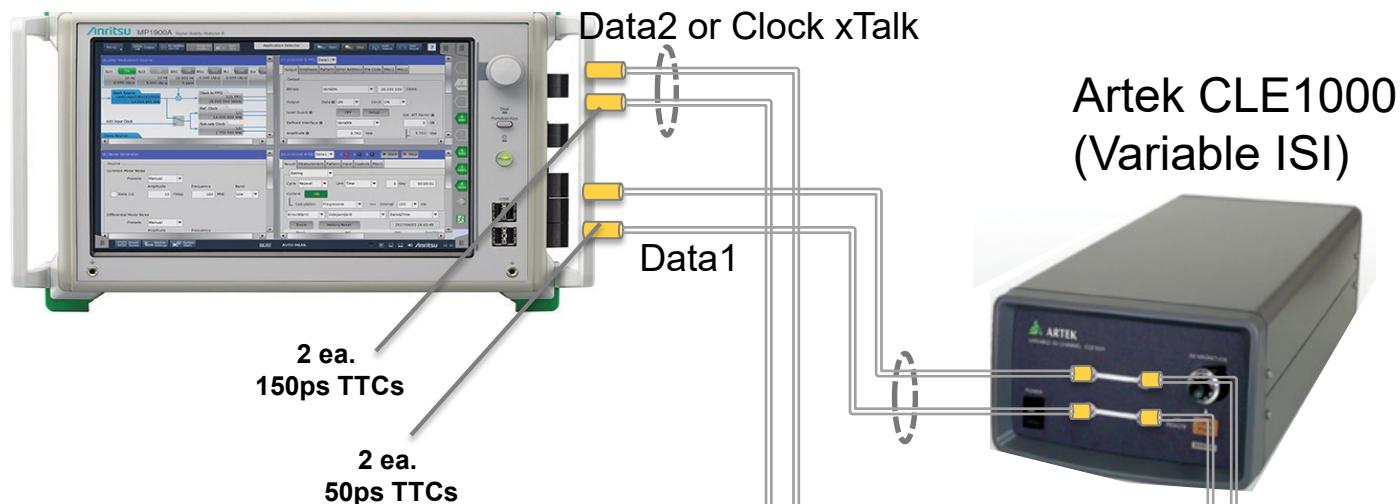
TP3 Calibration Procedure:

6. Turn on Compliance Pattern
7. Calibrate ISI at TP3_EQ with proper CDR Function
8. Turn On all Stressors
9. Calibrate Eye Height and Total Jitter
10. Calibrate xTalk (1/4 Rate Clock or 2nd Data Signal)
11. Disconnect Calibration Fixture and Connect to DUT



DisplayPort PHY CTS Sink Test

Anritsu MP1900A



Test Procedure:

1. Frequency Lock
2. Symbol Lock
3. Error Count Check
4. BER Test

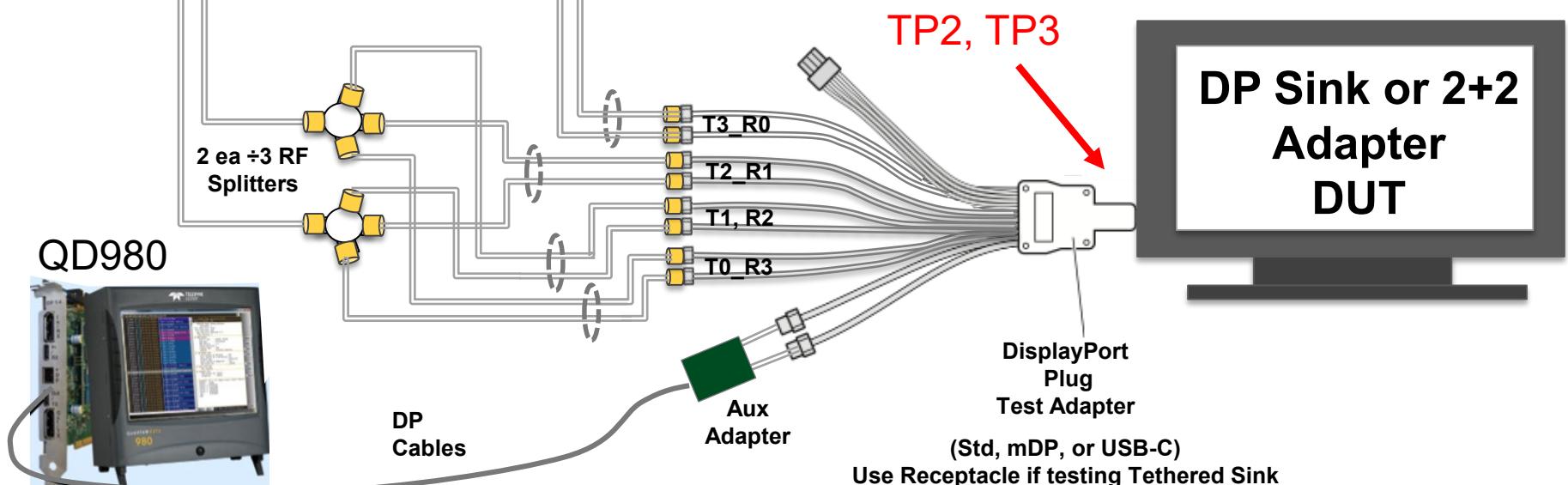


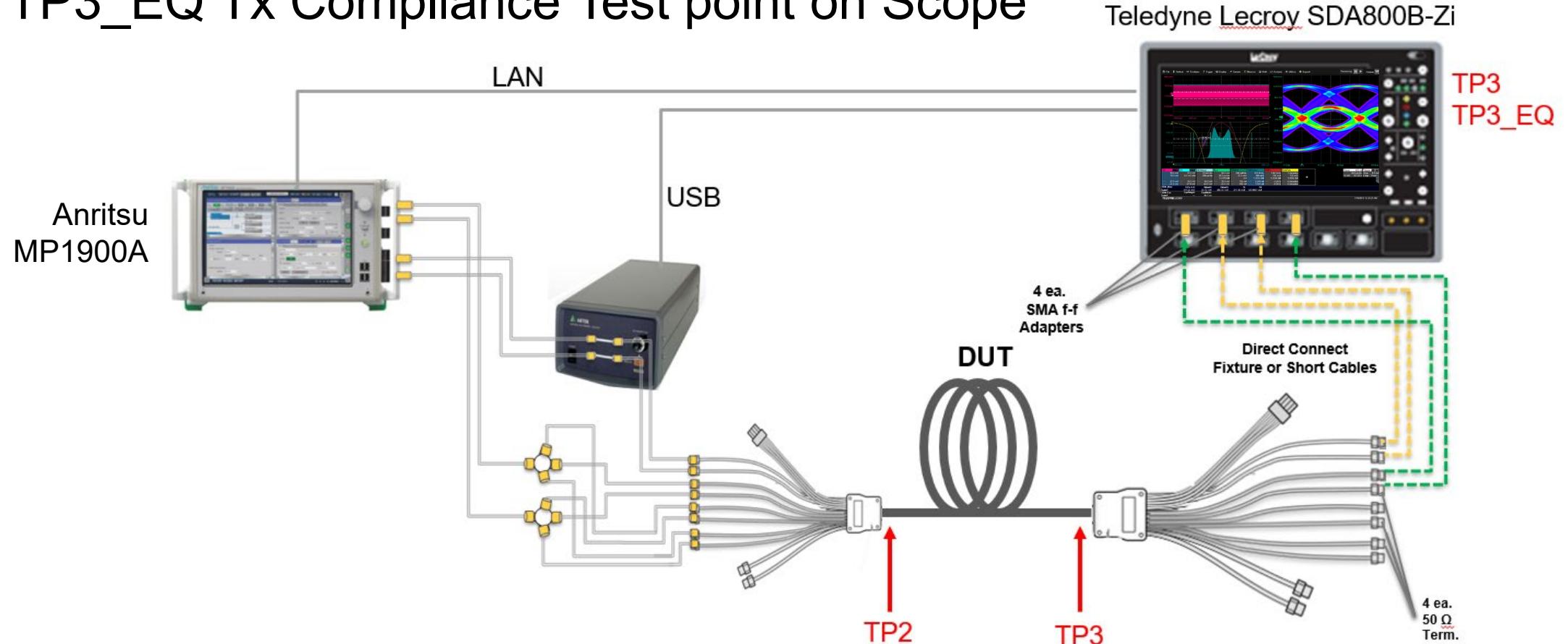
Table 4-3: BER Measurement Test Parameters

Jitter Frequency (MHz)	Number of Bits	Maximum Number of Allowable Bit Errors	Bit Rate	Observation Time (Seconds) ^a	Data Rate Offset
2	10^{12}	1000	HBR3	123	0
			HBR2	185	
			HBR	370	
			RBR	620	
10	10^{11}	100	HBR3	13	+350ppm
			HBR2	19	
			HBR	37	
			RBR	62	
20	10^{11}	100	HBR3	13	0
			HBR2	19	
			HBR	37	
			RBR	62	
100	10^{11}	100	HBR3	13	0
			HBR2	19	
			HBR	37	
			RBR	62	

a. To evaluate, the number of bits shall be multiplied by the unit interval (UI) in picoseconds (e.g., for HBR, 10^{11} bits at HBR = $370\text{ps/UI} \times 10^{11}\text{UI} = 37\text{ seconds}$).

DisplayPort Active Cable Testing

- Active Cable NE is TP2_EQ in CTS
- Active Cable FE is TP3 in CTS
- Use TP3_EQ Tx Compliance Test point on Scope



USB Type-C Power Delivery Debugging



Mercury™ T2C/T2P USB2.0 Type-C Power Delivery Protocol Analyzers

The screenshot displays the Mercury T2C/T2P software interface, featuring several windows for protocol analysis:

- Detail View provides packet details:** A callout points to a window showing detailed information about a selected packet, including its structure and specific fields.
- Tooltips explain protocol events:** A callout points to a tooltip explaining a specific event or term within the software's interface.
- Capture and display packets on the CC (Configuration Channel) wire:** A callout points to a window titled "Trace View" showing a sequence of packets on the Configuration Channel (CC) wire.
- Capture and display Vendor Defined Messages (VDM):** A callout points to a window titled "Trace View" showing a sequence of Vendor Defined Messages (VDM).
- Zero Time Search™ only shows events that occur in the trace:** A callout points to a search feature labeled "Zero Time Search™" which filters results to show events within the current trace.
- vBus power draw is shown graphically and synchronized with protocol events (Mercury T2P only):** A callout points to a "Power Tracker" window showing a graph of vBus power draw over time, synchronized with protocol events.

**Cost Effective Solution for
CC & SBU Line Debug**



DisplayPort 2.0 Preview



DisplayPort 2.0 PHY Testing Preview

- New UHBR Bit Rates
 - UHBR10, UHBR13, UHBR20
 - Higher Efficiency through 128/132b encoding
- Continues to Support USB Type-C Connector & Cables
- Test Methods will evolve from Thunderbolt 3
 - Genesis of USB4 and DisplayPort 2 PHY Specifications.

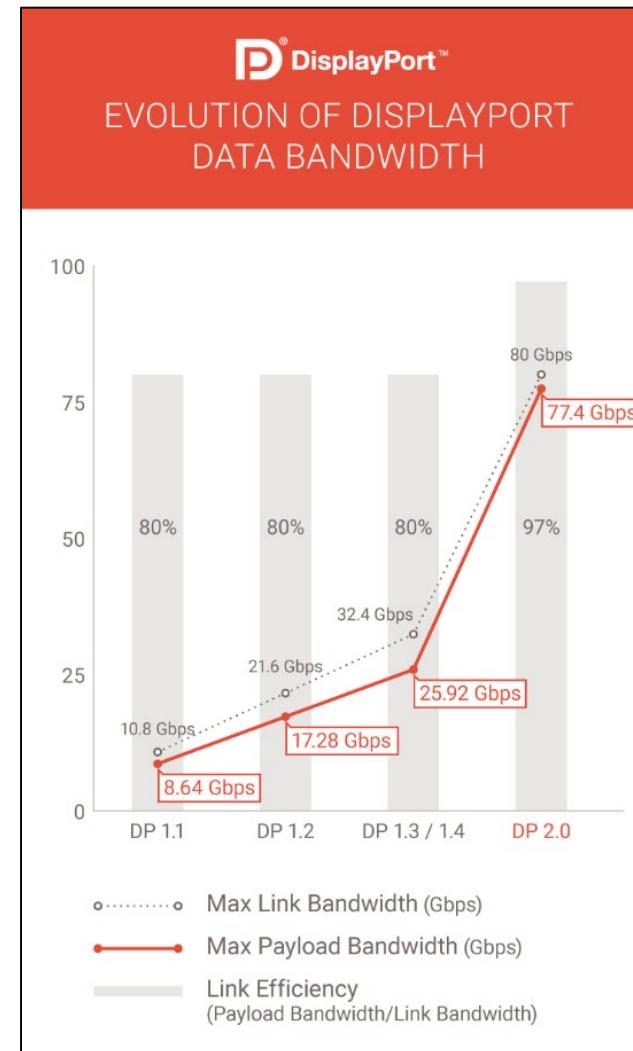


Image Source: <https://www.anandtech.com/show/14590/vesa-announces-displayport-20-standard-bandwidth-for-8k-monitors-beyond>

Test Equipment for DisplayPort 2.0 (USB4/Thunderbolt3)

■ High Performance Real Time Oscilloscope

- USB-C Connector Supports 20Gb/s Signaling
- TBT3 CTS (20Gb/s) requires 21GHz Scope, 80GS/s
 - BW selected based on Rx bandwidth/noise tradeoff
- WaveMaster 8 Zi-B Series – 25GHz (minimum); 80GS/s on 2Ch – “**Lane-by-Lane Testing**”
- LabMaster 10Zi-A Series – 25GHz (minimum); 80GS/s on up to 80Ch – “**Multi-Lane Simultaneous Testing**”
- QualiPHY Software for Compliance Test Automation



Teledyne Lecroy WaveMaster 8 Zi-B
Oscilloscope Models 4GHz to 30GHz
for data rates up to 20Gb/s (single lane)



Teledyne LeCroy LabMaster 10Zi-A
Oscilloscope models from 25 GHz to 100 GHz,
to support 16 Gb/s, 32 Gb/s and beyond

■ High Performance BERT (Bit Error Rate Tester)

- Teledyne Lecroy partners with Anritsu for data rates 10Gb/s and above
- MP1900 is specified BERT for TBT3 Rx Testing
 - Exceptionally Low Jitter Noise Floor – critical for Rx Calibration & Test

■ SW, Fixtures, Cables, Connectors, Adapters

- Standard Specific dictated by vendor specific MOIs (Methods of Implementation)
- Wilder-Tech is leading supplier of high speed test fixtures



Anritsu MP1900A SQA-R
High speed BERT from 2.4 to 32.1 Gb/s

Part 1: DisplayPort PHY (Physical) Layer Compliance Summary

- DP 1.4 is deployed version of PHY specification
- Teledyne LeCroy provides automated DP 1.4 Source Compliance testing using oscilloscope and QPHY-DisplayPort software
- Teledyne LeCroy oscilloscopes provides calibration and eye/jitter measurements for Sink and Active Cable PHY testing
- DP2.0 is in early stages of development
- Teledyne LeCroy is the only TE vendor to provide PHY & Link Layer Testing for DisplayPort

Part 2: Protocol Compliance Testing for DP1.4

- General protocols
- Link Layer compliance
- FEC and FEC compliance
- Display Stream Compression (DSC) and DSC compliance
- HDCP and HDCP compliance

Date: Wed, September 25, 2019

Time: 11AM Pacific | 2PM Eastern

neal.Kendall@teledyne.com

Questions?

