

# Essentials of DisplayPort Protocols at HBR3 Link Rates - 8.1Gbps

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Webinar – April– 2018



# Agenda

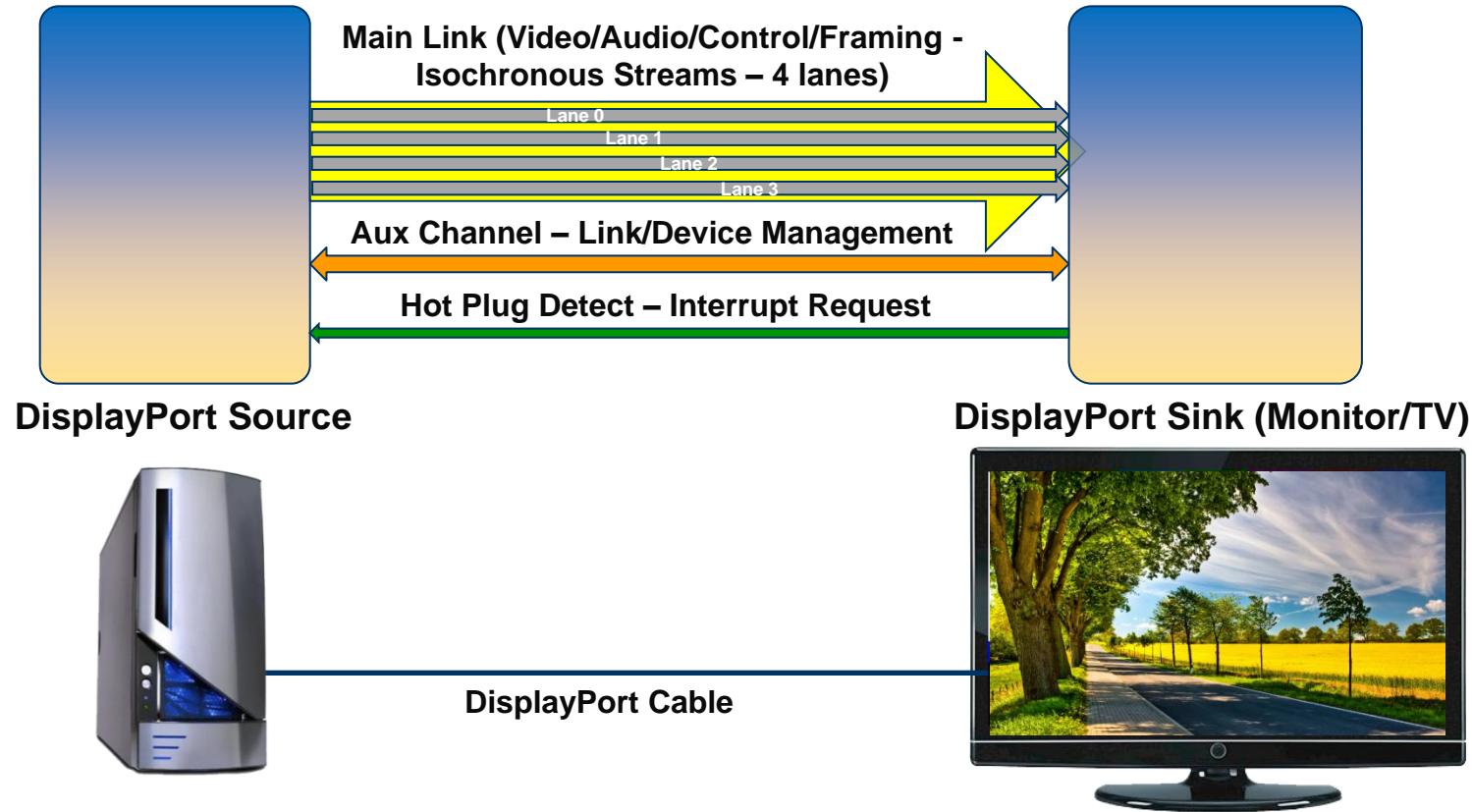
- Aux Channel
    - Link Training at 8.1Gbps Link Rates
    - HDCP 2.2 (not covered in detail)
  - Main Link – Video/Audio Stream Transmission
    - Video packets
    - Metadata (Main Stream Attributes)
    - Secondary data packets (Audio)
    - Control symbols
  - Q & A
- ◆ Please Check out our other “Essentials of” Webinars:
- ◆ [Essentials of DisplayPort Protocols](#)
  - ◆ [Essentials of HDCP 2.2 Protocols](#)
  - ◆ [Essentials of DisplayPort Display Stream \(DSC\) Protocols](#)

Please feel free to contact me, Neal Kendall at:

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If you have any questions.

# DisplayPort Anatomy



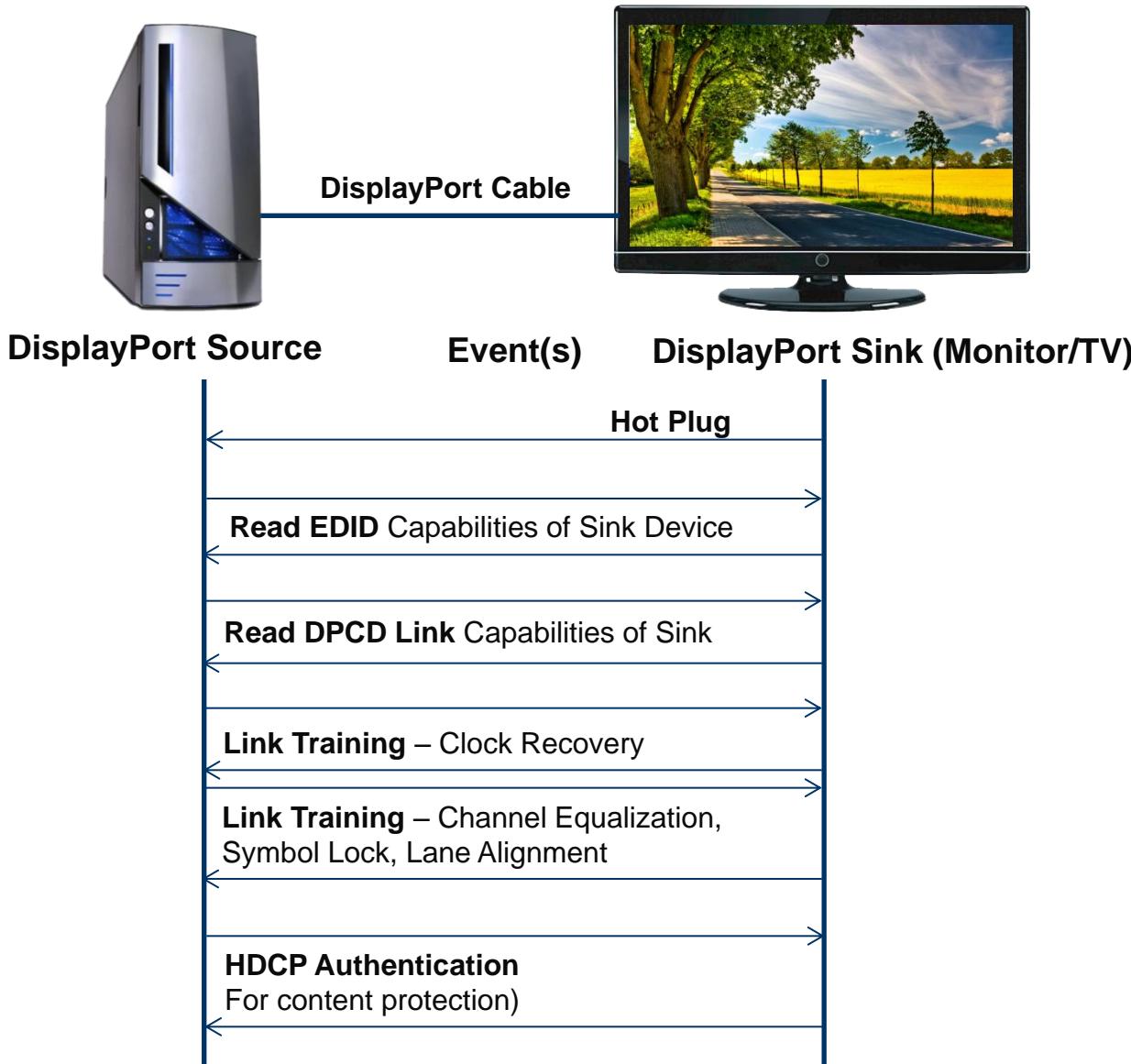
- Main Link: Unidirectional, high-bandwidth channel used to transport video, audio and metadata and protocol control elements.
- Main Link 1, 2 or 4 Lane Configurations.
- Main Link 4 link rates:
  - 1.62Gbps (Reduced Bit Rate)
  - 2.7Gbps (High Bit Rate)
  - 5.4Gbps (High Bit Rate 2)
  - 8.1Gbps (High Bit Rate 3)  
introduced in DisplayPort 1.3/4.
- No clock channel. Sink recovers clock using link transitions.
- Aux Channel: Bidirectional, half duplex channel with a data rate of 1Mbps. Link Training, DPCD Register status, HDCP authentication & EDID.
- Hot plug lead:
  - Connection Detection.
  - Interrupt mechanism in cases where there is a failure.

# DisplayPort Connection Sequence

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# DisplayPort Connection Sequence



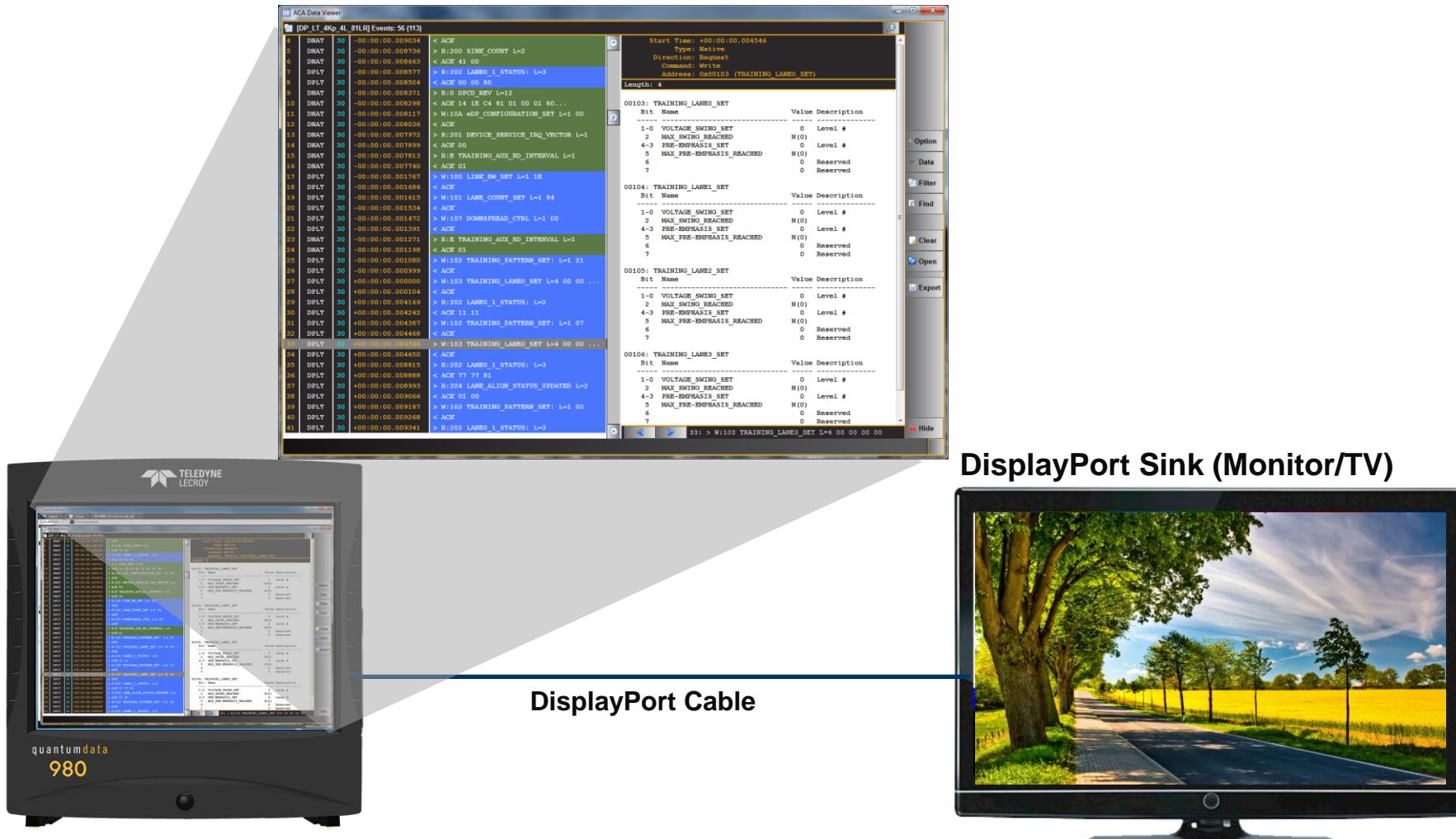
- Hot Plug. Indication to the Source that there is a Display device connect to it.
- EDID read. EDID is a data structure provided by a DisplayPort display that describe its capabilities to a DisplayPort video source.
- Link Training. Link training establishes the physical link parameters (number of lanes, link rate, voltage swing, pre-emphasis, equalization) used for transmission of video and audio over the main link.
- Link Training has two phases:
  - Clock Recovery and
  - Channel Equalization which includes Symbol Lock and Inter-Lane alignment.
- If the video/audio content is flagged for content protection, the High-bandwidth Digital Content Protection (HDCP) authentication protocol is used.

# DisplayPort Aux Channel Monitoring

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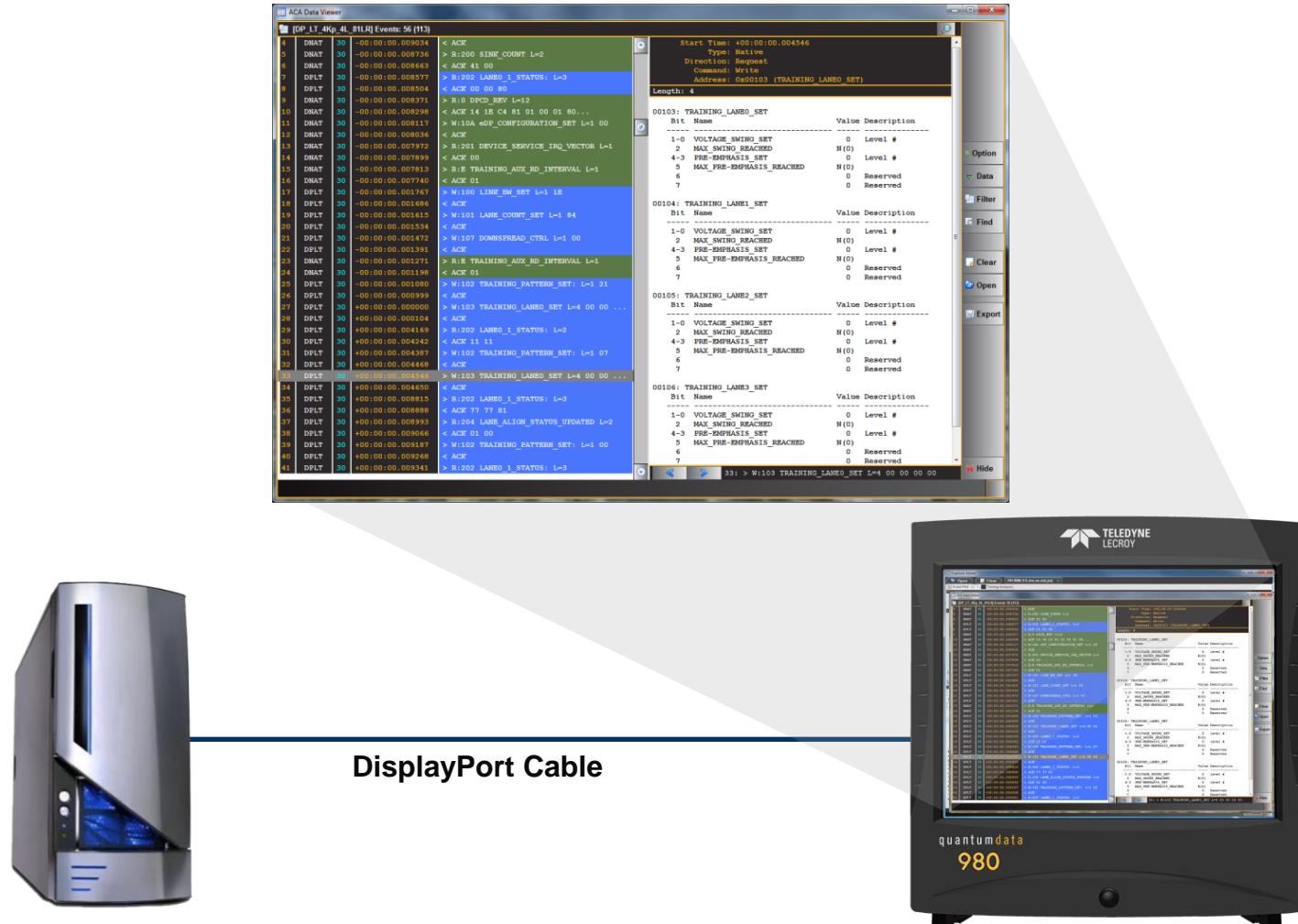


# Monitoring the DP Aux Channel – Emulating a DP Source to Test a DP Display



**Teledyne LeCroy quantumdata 980 Test Platform  
with DP 1.4 Video Generator / Protocol Analyzer  
module emulating DisplayPort Source**

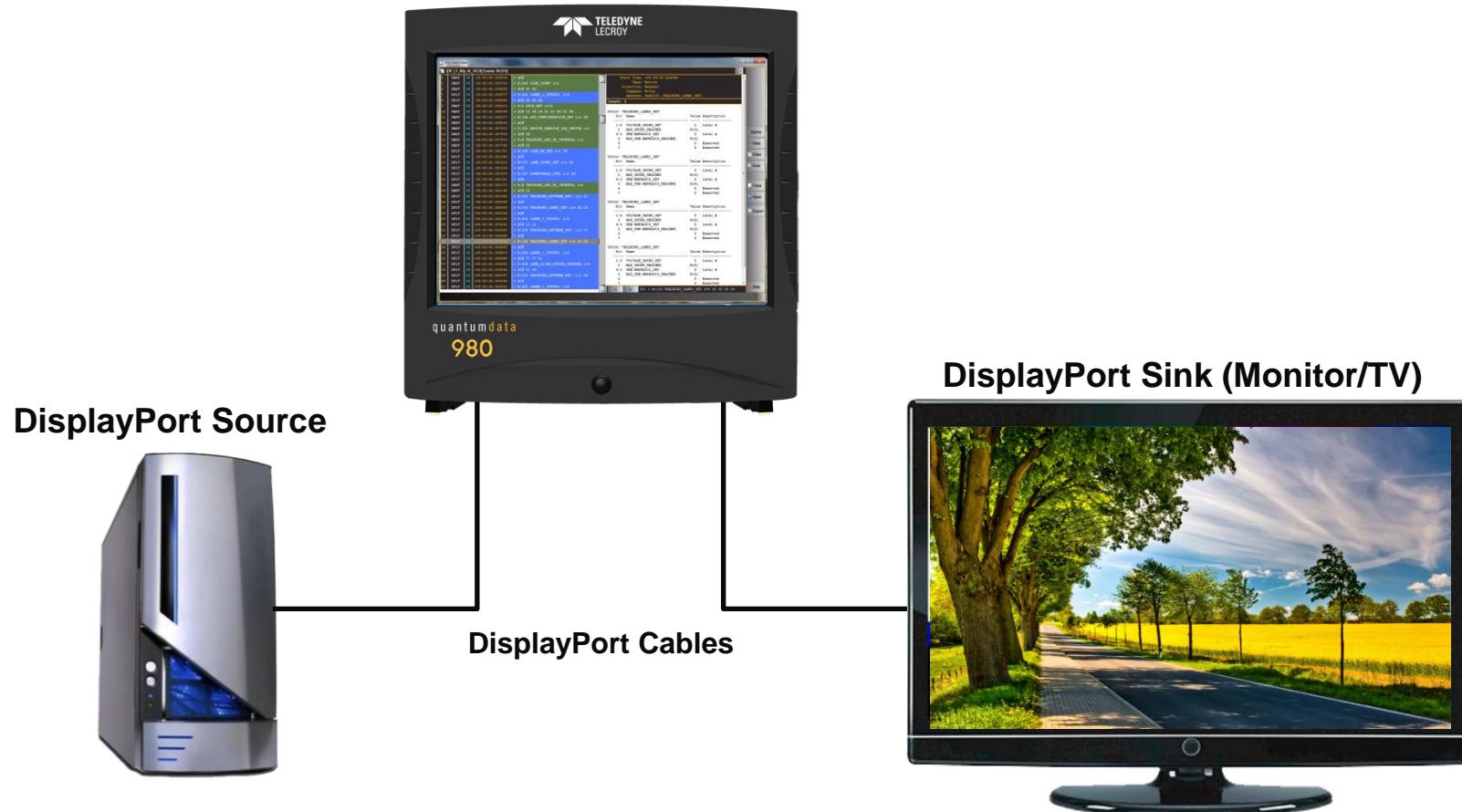
# Monitoring the DP Aux Channel – Emulating a DP Sink to Test a DP Display



with DP 1.4 Video Generator / Protocol Analyzer  
module emulating DisplayPort Sink

# Passive Monitoring of Aux Channel Between a DP Sink and Display

Teledyne LeCroy quantumdata 980 Test Platform  
with DP 1.4 Video Generator / Protocol Analyzer  
Passively Monitoring DP Aux Channel



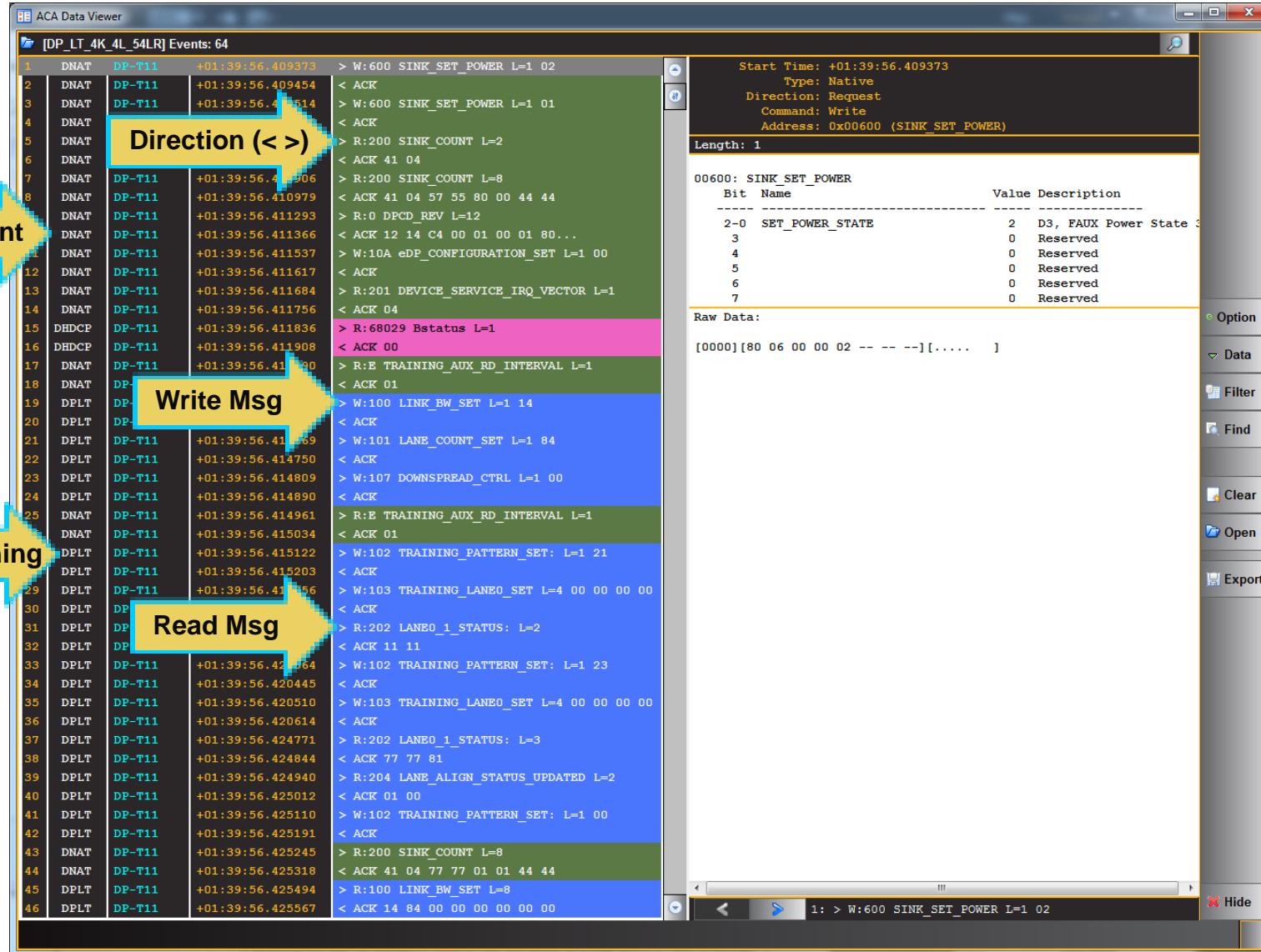
# 980 Auxiliary Channel Analyzer Panels

The screenshot shows the ACA Data Viewer interface with two main panels:

- Transaction Log Panel (Left):** Displays a list of events in a table format. The columns include: Index, Transaction Type, Lane ID, Time, and Transaction Details. A yellow arrow points to the "Time" column header, and another yellow arrow points to the "Detail Panel".
- Detail Panel (Right):** Provides detailed information for the selected transaction. It includes:
  - Header: Start Time: +01:39:56.420249, Type: Native, Direction: Reply, Command: ACK.
  - Text: Reply to Read Request.
  - Table: 00202: LANE0\_1\_STATUS. It lists bits 0-7 with their names and descriptions. For example, bit 0 is LANE0\_CR\_DONE with value Y(1).
  - Table: 00203: LANE2\_3\_STATUS. Similar to the first, it lists bits 0-7 for LANE2 and LANE3.
  - Text: Raw Data: [0000] [00 11 11 -- -- -- --] [...]

- Two panels:
  - 1) Transaction Log Panel
  - 2) Details panel.
- Details of the highlighted transaction in the Log panel appears in the Details panel.
- Time goes from top to bottom on the Transaction Log panel.

# 980 Auxiliary Channel Analyzer Transactions



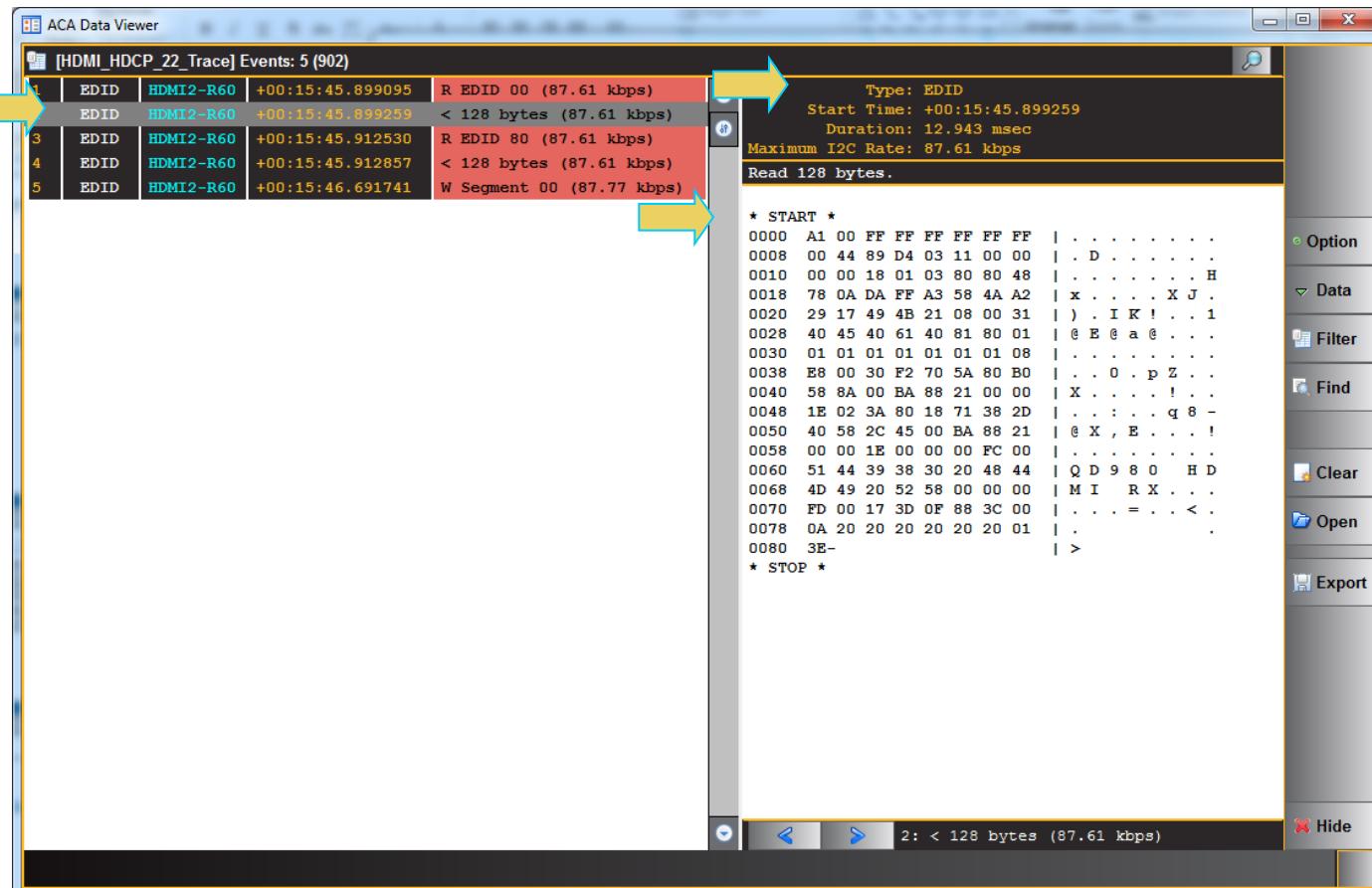
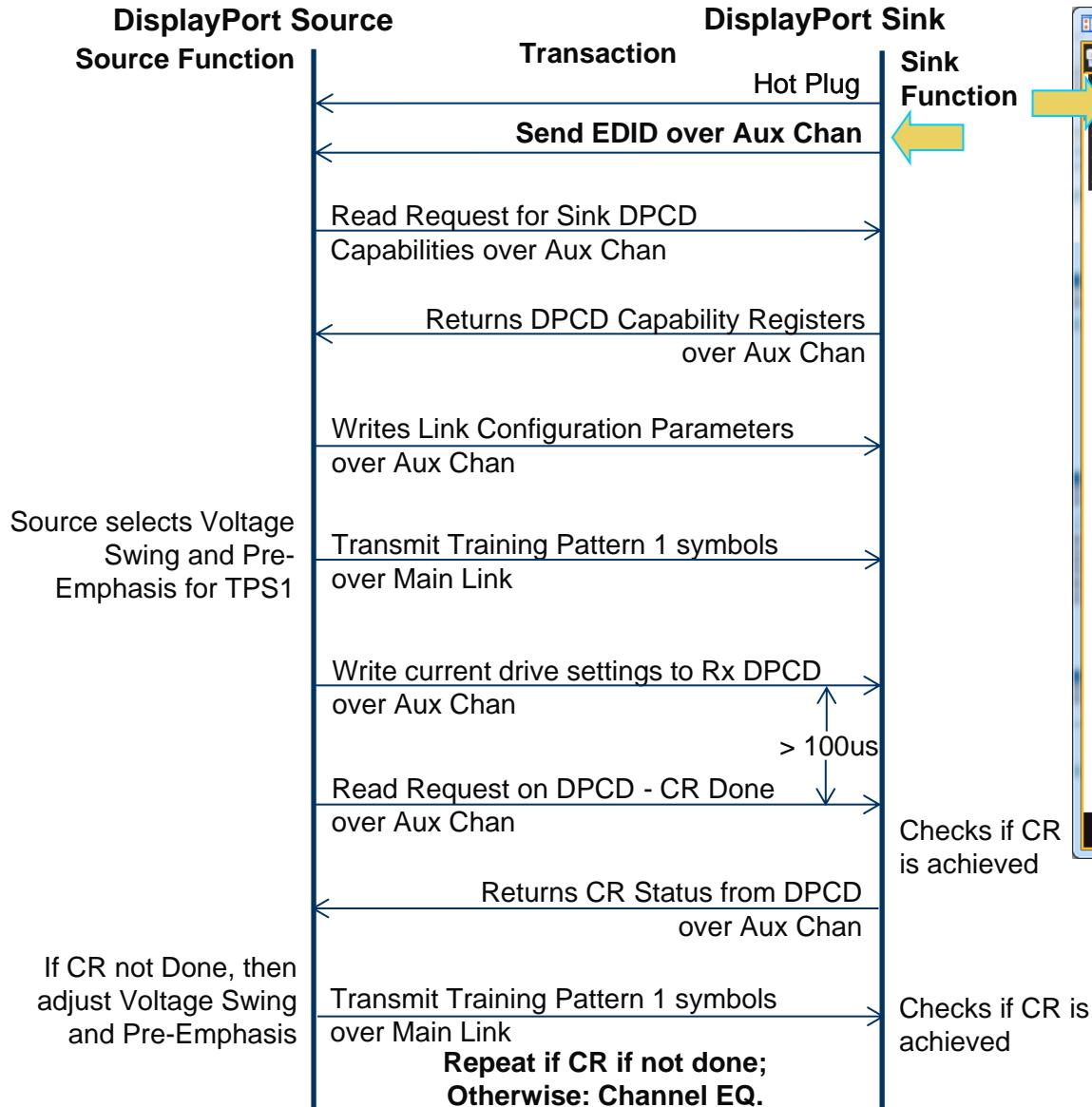
- Direction of transaction is provided (< >).
- Read and Write is indicated (R W).
- Message type indicated (e.g. DPLT for DisplayPort Link Training). Color coding also used to distinguish between transaction types.

# DisplayPort Connection Sequence Link Training

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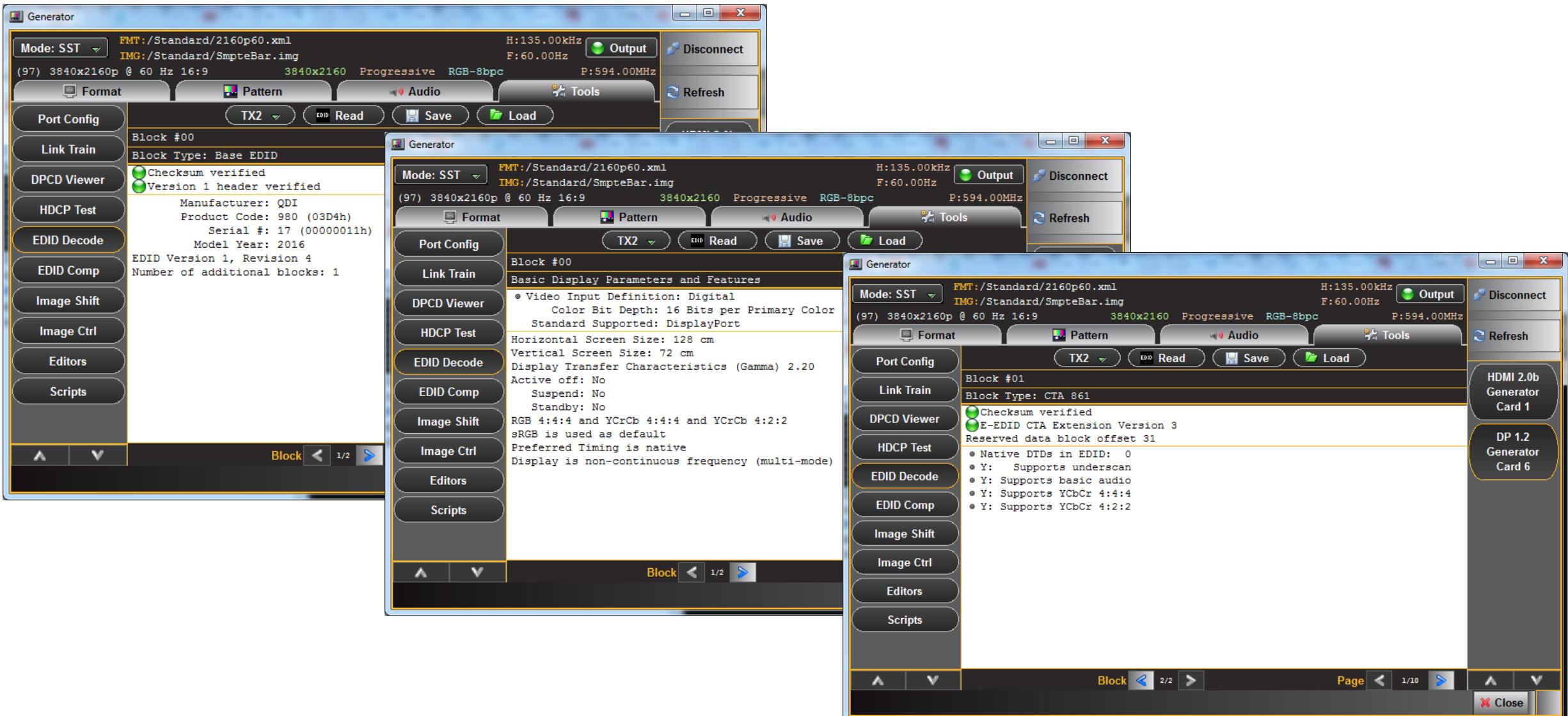


# Connection Sequence – EDID Read



Source Reads EDID from Sink

# Connection Sequence – Sample EDID Contents



# Connect

## DisplayPort Source Function

Source selects Voltage Swing and Pre Emphasis for TPS

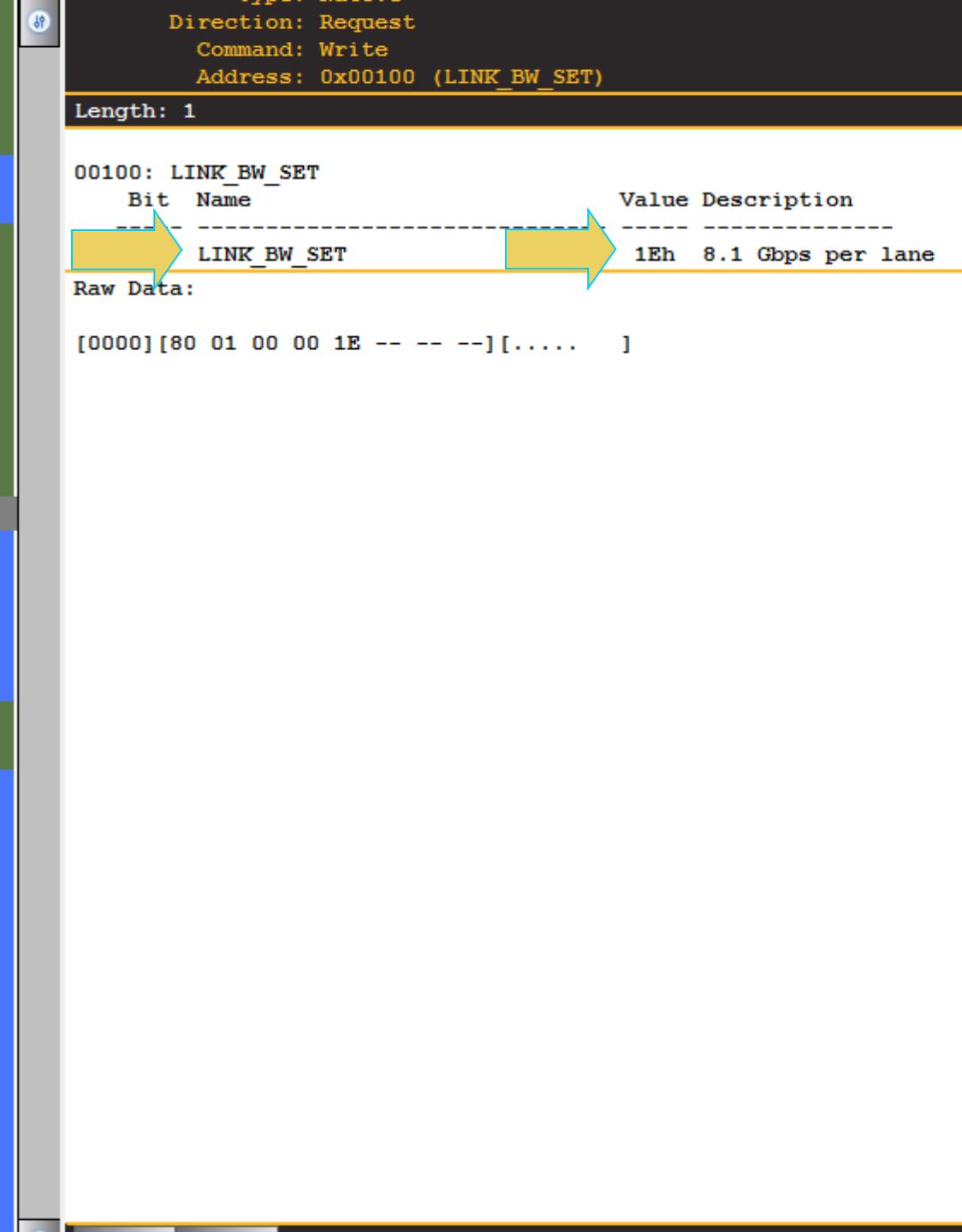
If CR not Done, then  
adjust Voltage Swing  
and Pre-Emphasis

2	DNAT	DP-T30	< ACK
3	DNAT	DP-T30	> W:600 SINK_SET_POWER L=1 01
4	DNAT	DP-T30	< ACK
5	DNAT	DP-T30	> R:200 SINK_COUNT L=2
6	DNAT	DP-T30	< ACK 41 00
7	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=3
8	DPLT	DP-T30	< ACK 02 00 80
9	DNAT	DP-T30	> R:0 DPCD_REV L=12
10	DNAT	DP-T30	< ACK 14 1E C4 81 01 00 01 80...
11	DNAT	DP-T30	> W:10A eDP_CONFIGURATION_SET L=1 00
12	DNAT	DP-T30	< ACK
13	DNAT	DP-T30	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
14	DNAT	DP-T30	< ACK 00
15	DNAT	DP-T30	> R:E TRAINING_AUX_RD_INTERVAL L=1
16	DNAT	DP-T30	< ACK 01
17	DPLT	DP-T30	> W:100 LINK_BW_SET L=1 1E
18	DPLT	DP-T30	< ACK
19	DPLT	DP-T30	> W:101 LANE_COUNT_SET L=1 84
20	DPLT	DP-T30	< ACK
21	DPLT	DP-T30	> W:107 DOWNSPREAD_CTRL L=1 00
22	DPLT	DP-T30	< ACK
23	DNAT	DP-T30	> R:E TRAINING_AUX_RD_INTERVAL L=1
24	DNAT	DP-T30	< ACK 01
25	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 21
26	DPLT	DP-T30	< ACK
27	DPLT	DP-T30	> W:103 TRAINING_LANE0_SET L=4 09 09 09 09
28	DPLT	DP-T30	< ACK
29	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=2
30	DPLT	DP-T30	< ACK 11 11
31	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 07
32	DPLT	DP-T30	< ACK
33	DPLT	DP-T30	> W:103 TRAINING_LANE0_SET L=4 09 09 09 09
34	DPLT	DP-T30	< ACK
35	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=3
36	DPLT	DP-T30	< ACK 77 77 81
37	DPLT	DP-T30	> R:204 LANE_ALIGN_STATUS_UPDATED L=2

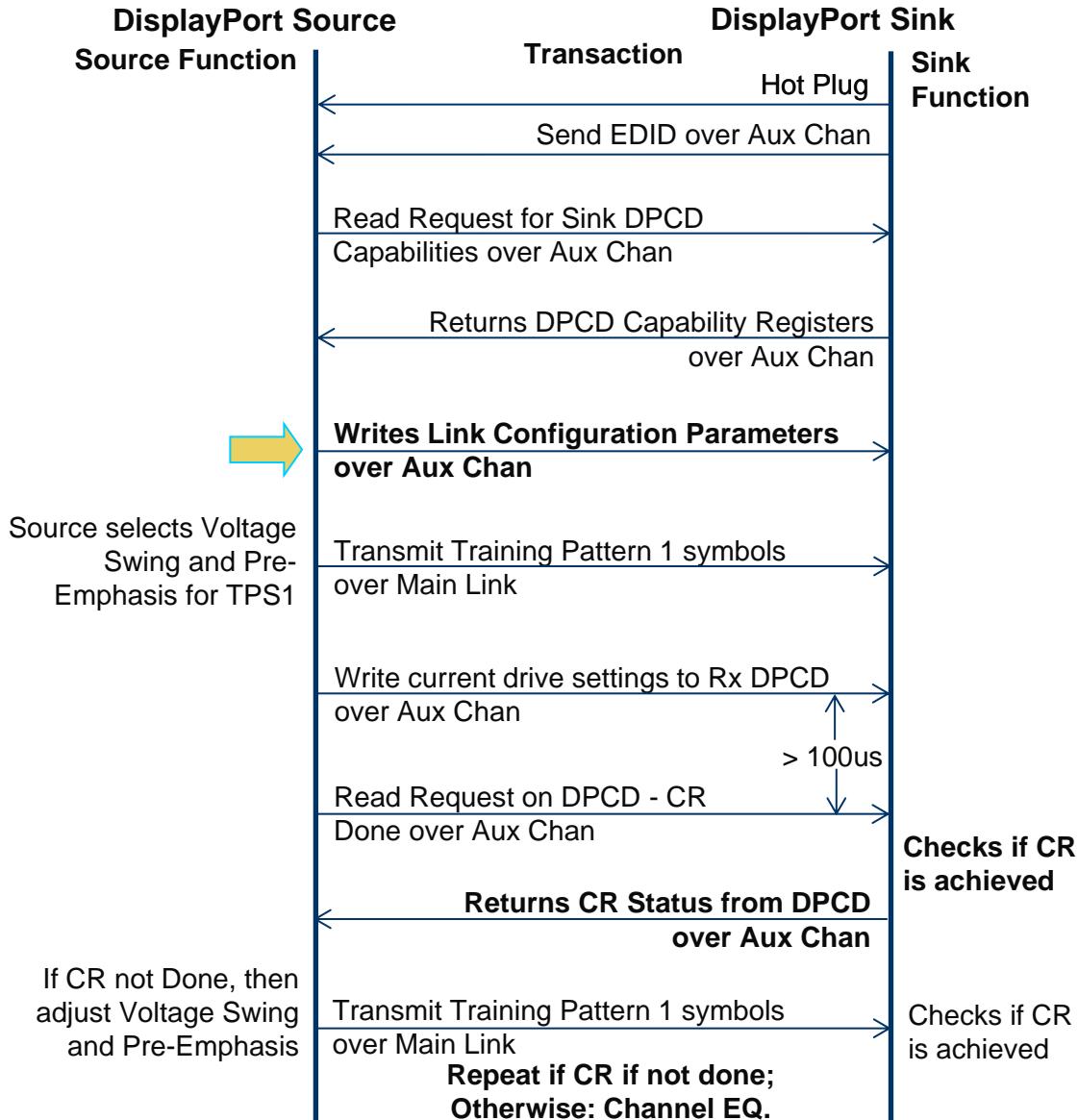
Type: Native	
Direction: Reply	
Command: ACK	
Reply to Read Request.	
00000: DPCD_REV	
Bit Name	Value Description
7-4 MAJOR_REV	1
3-0 MINOR_REV	4
00001: MAX_LINK_RATE	
Bit Name	Value Description
7-0 MAX_LINK_RATE	1Eh 8.1 Gbps per lane
00002: MAX_LANE_COUNT	
Bit Name	Value Description
4-0 MAX_LANE_COUNT	4 4 lanes
5 POST_LT_ADJ_REQ_SUP	N(0)
6 TPS3_SUPPORTED	Y(1)
7 ENHANCED_FRAME_CAP	Y(1)
00003: MAX_DOWNSPREAD	
Bit Name	Value Description
0 MAX_DOWNSPREAD	1 Up to 0.5%
1	0 Reserved
2	0 Reserved
3	0 Reserved
4	0 Reserved
5	0 Reserved
6 NO_AUX_HANDSHAKE_LINK_TRAINING	N(0)
7 TPS4_SUPPORTED	Y(1)
00004: NORP	
Bit Name	Value Description
0 Number of receive ports	1 2 ports
1	0 Reserved
2	0 Reserved
3	0 Reserved
4	0 Reserved
5 5V DP PWR CAP	N(0)

# Connections

DisplayPort Source Function	DP-T30	DP-T30
	DNAT	< ACK
	DNAT	> W:600 SINK_SET_POWER L=1 01
	DNAT	< ACK
	DNAT	> R:200 SINK_COUNT L=2
	DNAT	< ACK 41 00
	DPLT	> R:202 LANE0_1_STATUS: L=3
	DPLT	< ACK 02 00 80
	DNAT	> R:0 DPCD_REV L=12
	DNAT	< ACK 14 1E C4 81 01 00 01 80...
	DNAT	> W:10A eDP_CONFIGURATION_SET L=1 00
	DNAT	< ACK
	DNAT	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
	DNAT	< ACK 00
	DNAT	> R:E TRAINING_AUX_RD_INTERVAL L=1
	DNAT	< ACK 01
	DPLT	> W:100 LINK_BW_SET L=1 1E
Source selects Voltage Swing and Pre-Emphasis for TPS1	DPLT	< ACK
	DPLT	> W:101 LANE_COUNT_SET L=1 84
	DPLT	< ACK
	DPLT	> W:107 DOWNSPREAD_CTRL L=1 00
	DPLT	< ACK
	DNAT	> R:E TRAINING_AUX_RD_INTERVAL L=1
	DNAT	< ACK 01
	DPLT	> W:102 TRAINING_PATTERN_SET: L=1 21
	DPLT	< ACK
	DPLT	> W:103 TRAINING_LANE0_SET L=4 09 09 09 09
	DPLT	< ACK
	DPLT	> R:202 LANE0_1_STATUS: L=2
	DPLT	< ACK 11 11
	DPLT	> W:102 TRAINING_PATTERN_SET: L=1 07
	DPLT	< ACK
	DPLT	> W:103 TRAINING_LANE0_SET L=4 09 09 09 09
	DPLT	< ACK
	DPLT	> R:202 LANE0_1_STATUS: L=3
	DPLT	< ACK 77 77 81
	DPLT	> R:204 LANE_ALIGN_STATUS_UPDATED L=2
	DPLT	< ACK 01 00

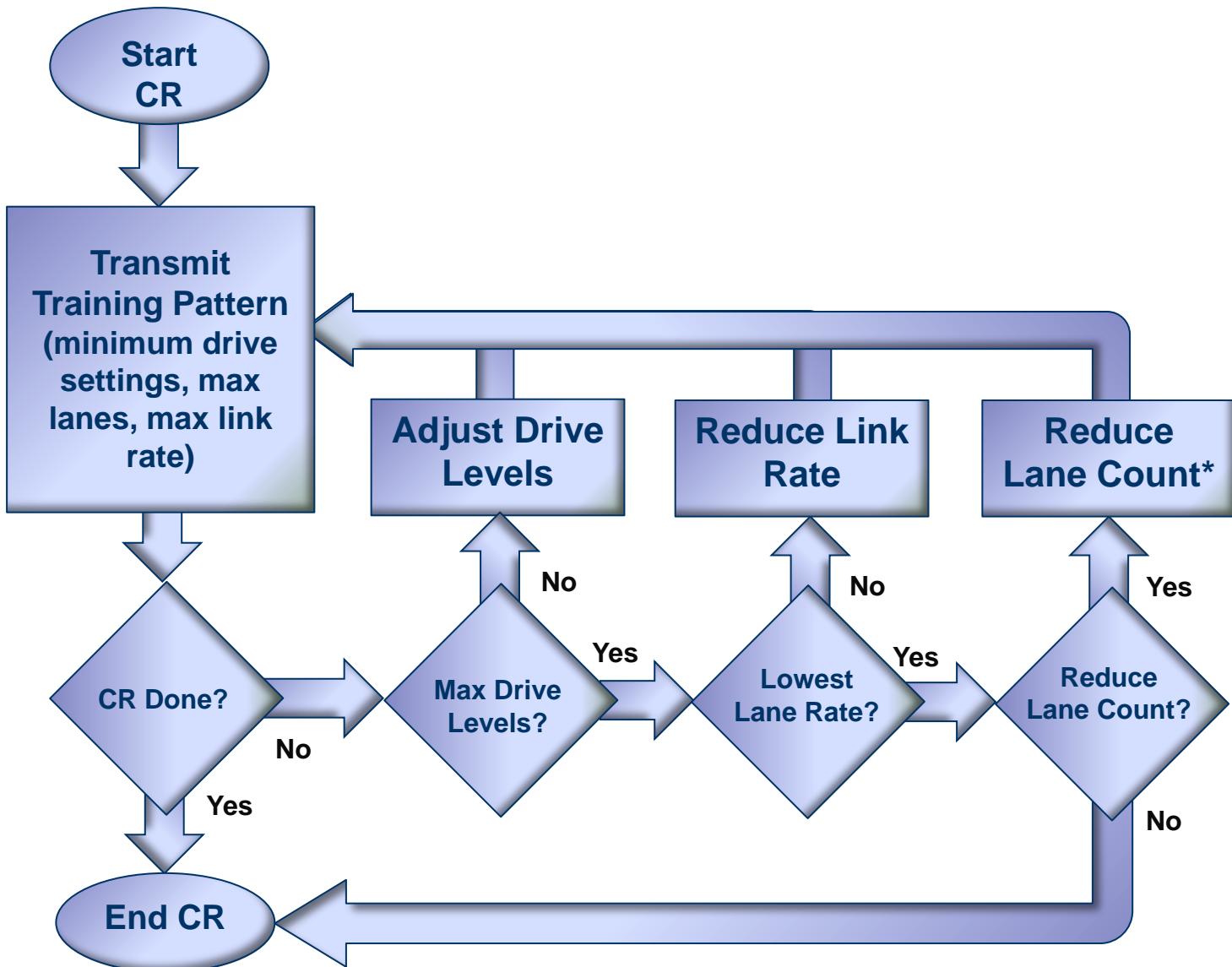


# Connection Sequence – Link Training Clock Recovery Sequence



- Clock Recover needed because DisplayPort, like most high speed serial interfaces, **does not have a separate clock channel**—the clock is derived from the bit stream.
- Receiver needs a reference clock of its own at approximately the same frequency.
- Very difficult to have two clocks—one on the transmitter and one on the receiver—that have the same clock frequency.
- **Receiver has to align its clock to the edge transitions** of the incoming data stream using a PLL.
- An unscrambled **special sequence of bits** has to be used (“training sequence” to optimize edge sampling for clock alignment.
- Clock recover begins with the following settings:
  - Lowest drive levels, i.e. voltage swing and pre-emphasis (unless embedded applications).
  - Maximum Link Rate supported, typically HBR2 5.4Gb/s/lane or HBR3 at 8.1Gb/s/lane.
  - Maximum number of lanes supported, typically 2 or 4.

# Connection Sequence – Link Training Clock Recovery



- Link Training Clock Recovery.
- There are 3 things that can be changed while still meeting the requirements of the video format being transmitted; listed in priority order:
  - Drive levels, i.e. voltage swing and pre-emphasis.
  - Link Rate, i.e. RBR at 1.62 Gb/s/lane through HBR3 at 8.1Gb/s/lane.
  - Number of lanes. **Lanes can be reduced if the CR shows that the lower lanes were successfully locked.**

# Connection

DisplayPort Source Function

Source selects Voltage Swing and Pre-Emphasis for TPS1

If CR not Done, then adjust Voltage Swing and Pre-Emphasis

1	DNAT	DP-T30	> W:600 SINK_SET_POWER L=1 02
2	DNAT	DP-T30	< ACK
3	DNAT	DP-T30	> W:600 SINK_SET_POWER L=1 01
4	DNAT	DP-T30	< ACK
5	DNAT	DP-T30	> R:200 SINK_COUNT L=2
6	DNAT	DP-T30	< ACK 41 00
7	DPLT	DP-T30	> R:202 LANEO_1_STATUS: L=3
8	DPLT	DP-T30	< ACK 02 00 80
9	DNAT	DP-T30	> R:0 DPCD_REV L=12
10	DNAT	DP-T30	< ACK 14 1E C4 81 01 00 01 80...
11	DNAT	DP-T30	> W:10A eDP_CONFIGURATION_SET L=1 00
12	DNAT	DP-T30	< ACK
13	DNAT	DP-T30	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
14	DNAT	DP-T30	< ACK 00
15	DNAT	DP-T30	> R:E TRAINING_AUX_RD_INTERVAL L=1
16	DNAT	DP-T30	< ACK 01
17	DPLT	DP-T30	> W:100 LINK_BW_SET L=1 1E
18	DPLT	DP-T30	< ACK
19	DPLT	DP-T30	> W:101 LANEO_SET L=1 84
20	DPLT	DP-T30	< ACK
21	DPLT	DP-T30	> W:107 DOWNSPREAD_CTRL L=1 00
22	DPLT	DP-T30	< ACK
23	DNAT	DP-T30	> R:E TRAINING_AUX_RD_INTERVAL L=1
24	DNAT	DP-T30	< ACK 01
25	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 21
26	DPLT	DP-T30	< ACK
27	DPLT	DP-T30	> W:103 TRAINING_LANE0_SET L=4 09 09 09 09
28	DPLT	DP-T30	< ACK
29	DPLT	DP-T30	> R:202 LANEO_1_STATUS: L=2
30	DPLT	DP-T30	< ACK 11 11
31	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 07
32	DPLT	DP-T30	< ACK
33	DPLT	DP-T30	> W:103 TRAINING_LANE0_SET L=4 09 09 09 09
34	DPLT	DP-T30	< ACK
35	DPLT	DP-T30	> R:202 LANEO_1_STATUS: L=3
36	DPLT	DP-T30	< ACK 77 77 81

Start Time: +00:58:37.052516  
 Type: Native  
 Direction: Request  
 Command: Write  
 Address: 0x00101 (LANE\_COUNT\_SET)

Length: 1

00101: LANE\_COUNT\_SET

Bit	Name	Value Description
4-0	LANE_COUNT_SET	4 4 lanes
5	POST_LT_ADJ_REQ_GRANTED	N(0)
6		0 Reserved
7	ENHANCED_FRAME_CAP	Y(1)

Raw Data:

[0000] [80 01 01 00 84 -- --] [.....]

# Connections

DisplayPort Source Function

Source selects Voltage Swing and Pre-Emphasis for TP

If CR not Done, then adjust Voltage Swing and Pre-Emphasis

1	DNAT	DP-T30	> W:600 SINK_SET_POWER L=1 02
2	DNAT	DP-T30	< ACK
3	DNAT	DP-T30	> W:600 SINK_SET_POWER L=1 01
4	DNAT	DP-T30	< ACK
5	DNAT	DP-T30	> R:200 SINK_COUNT L=2
6	DNAT	DP-T30	< ACK 41 00
7	DPLT	DP-T30	> R:202 LANEO_1_STATUS: L=3
8	DPLT	DP-T30	< ACK 02 00 80
9	DNAT	DP-T30	> R:0 DPCD_REV L=12
10	DNAT	DP-T30	< ACK 14 1E C4 81 01 00 01 80...
11	DNAT	DP-T30	> W:10A eDP_CONFIGURATION_SET L=1 00
12	DNAT	DP-T30	< ACK
13	DNAT	DP-T30	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
14	DNAT	DP-T30	< ACK 00
15	DNAT	DP-T30	> R:E TRAINING_AUX_RD_INTERVAL L=1
16	DNAT	DP-T30	< ACK 01
17	DPLT	DP-T30	> W:100 LINK_BW_SET L=1 1E
18	DPLT	DP-T30	< ACK
19	DPLT	DP-T30	> W:101 LANE_COUNT_SET L=1 84
20	DPLT	DP-T30	< ACK
	DPLT	DP-T30	> W:107 DOWNSPREAD_CTRL L=1 00
22	DPLT	DP-T30	< ACK
23	DNAT	DP-T30	> R:E TRAINING_AUX_RD_INTERVAL L=1
24	DNAT	DP-T30	< ACK 01
25	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 21
26	DPLT	DP-T30	< ACK
27	DPLT	DP-T30	> W:103 TRAINING_LANEO_SET L=4 09 09 09 09
28	DPLT	DP-T30	< ACK
29	DPLT	DP-T30	> R:202 LANEO_1_STATUS: L=2
30	DPLT	DP-T30	< ACK 11 11
31	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 07
32	DPLT	DP-T30	< ACK
33	DPLT	DP-T30	> W:103 TRAINING_LANEO_SET L=4 09 09 09 09
34	DPLT	DP-T30	< ACK
35	DPLT	DP-T30	> R:202 LANEO_1_STATUS: L=3
36	DPLT	DP-T30	< ACK 77 77 81
37	DPLT	DP-T30	> R:204 LANE_ALIGN_STATUS_UPDATED L=0

Start Time: +00:58:37.052657  
 Type: Native  
 Direction: Request  
 Command: Write  
 Address: 0x00107 (DOWNSPREAD\_CTRL)

Length: 1

00107: DOWNSPREAD\_CTRL

Bit	Name	Value	Description
0		0	Reserved
1		0	Reserved
2		0	Reserved
3		0	Reserved
4	SPREAD_AMP	N(0)	
5		0	Reserved
6		0	Reserved
7	MSA_TIMING_PAR_IGNORE_EN	N(0)	

Raw Data:

[0000] [80 01 07 00 00 -- -- --] [.....]

# Connections

## DisplayPort Source Function

Source selects Voltage Swing and Pre-Emphasis for TPS1

If CR not Done, then adjust Voltage Swing and Pre-Emphasis

1	DNAT	DP-T30	> W:600 SINK_SET_POWER L=1 02
2	DNAT	DP-T30	< ACK
3	DNAT	DP-T30	> W:600 SINK_SET_POWER L=1 01
4	DNAT	DP-T30	< ACK
5	DNAT	DP-T30	> R:200 SINK_COUNT L=2
6	DNAT	DP-T30	< ACK 41 00
7	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=3
8	DPLT	DP-T30	< ACK 02 00 80
9	DNAT	DP-T30	> R:0 DPCD_REV L=12
10	DNAT	DP-T30	< ACK 14 1E C4 81 01 00 01 80...
11	DNAT	DP-T30	> W:10A eDP_CONFIGURATION_SET L=1 00
12	DNAT	DP-T30	< ACK
13	DNAT	DP-T30	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
14	DNAT	DP-T30	< ACK 00
15	DNAT	DP-T30	> R:E TRAINING_AUX_RD_INTERVAL L=1
16	DNAT	DP-T30	< ACK 01
17	DPLT	DP-T30	> W:100 LINK_BW_SET L=1 1E
18	DPLT	DP-T30	< ACK
19	DPLT	DP-T30	> W:101 LANE_COUNT_SET L=1 84
20	DPLT	DP-T30	< ACK
21	DPLT	DP-T30	> W:107 DOWNSPREAD_CTRL L=1 00
22	DPLT	DP-T30	< ACK
23	DNAT	DP-T30	> R:E TRAINING_AUX_RD_INTERVAL L=1
24	DNAT	DP-T30	< ACK 01
25	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 21
26	DPLT	DP-T30	< ACK
27	DPLT	DP-T30	> W:103 TRAINING_LANE0_SET L=4 09 09 09 09
28	DPLT	DP-T30	< ACK
29	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=2
30	DPLT	DP-T30	< ACK 11 11
31	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 07
32	DPLT	DP-T30	< ACK
33	DPLT	DP-T30	> W:103 TRAINING_LANE0_SET L=4 09 09 09 09
34	DPLT	DP-T30	< ACK
35	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=3
36	DPLT	DP-T30	< ACK 77 77 81
37	DPLT	DP-T30	> R:204 LANE_ALIGN_STATUS_UPDATED L=2

Start Time:	+00:56:37.052978		
Type:	Native		
Direction:	Request		
Command:	Write		
Address:	0x00102 (TRAINING_PATTERN_SET:)		
Length:	1		
<b>00102: TRAINING_PATTERN_SET:</b>			
Bit	Name	Value	Description
3-0	TRAINING_PATTERN_SELECT	1	Pattern 1
4	RECOVERED_CLOCK_OUT_EN	N(0)	
5	SCRAMBLING_DISABLE	Y(1)	
7-6	SYMBOL_ERROR_COUNT_SEL	0	Disparity and Symbol
<b>Raw Data:</b>			
[0000] [80 01 02 00 21 -- -- --] [....!]			

# Connections

## DisplayPort Source Function

Source selects Voltage Swing and Pre-Emphasis for TPS1

If CR not Done, then adjust Voltage Swing and Pre-Emphasis

```

2  DNAT 30 < ACK
3  DNAT 30 > W:600 SINK_SET_POWER L=1 01
4  DNAT 30 < ACK
5  DNAT 30 > R:200 SINK_COUNT L=2
6  DNAT 30 < ACK 41 00
7  DPLT 30 > R:202 LANE0_1_STATUS: L=3
8  DPLT 30 < ACK 00 00 80
9  DNAT 30 > R:0 DPCD_REV L=12
10 DNAT 30 < ACK 14 1E C4 81 01 00 01 80...
11 DNAT 30 > W:10A eDP_CONFIGURATION_SET L=1 00
12 DNAT 30 < ACK
13 DNAT 30 > R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
14 DNAT 30 < ACK 00
15 DNAT 30 > R:E TRAINING_AUX_RD_INTERVAL L=1
16 DNAT 30 < ACK 01
17 DPLT 30 > W:100 LINK_BW_SET L=1 1E
18 DPLT 30 < ACK
19 DPLT 30 > W:101 LANE_COUNT_SET L=1 84
20 DPLT 30 < ACK
21 DPLT 30 > W:107 DOWNSPREAD_CTRL L=1 00
22 DPLT 30 < ACK
23 DNAT 30 > R:E TRAINING_AUX_RD_INTERVAL L=1
24 DNAT 30 < ACK 01
25 DPLT 30 > W:102 TRAINING_PATTERN_SET: L=1 21
26 DPLT 30 < ACK
27 DPLT 30 > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
28 DPLT 30 < ACK
29 DPLT 30 > R:202 LANE0_1_STATUS: L=2
30 DPLT 30 < ACK 11 11
31 DPLT 30 > W:102 TRAINING_PATTERN_SET: L=1 07
32 DPLT 30 < ACK
33 DPLT 30 > W:103 TRAINING_LANE0_SET L=4 00 00 00 00
34 DPLT 30 < ACK
35 DPLT 30 > R:202 LANE0_1_STATUS: L=3

```

Type: Native  
 Direction: Request  
 Command: Write  
 Address: 0x00103 (TRAINING\_LANE0\_SET)

Length: 4

### 00103: TRAINING\_LANE0\_SET

Bit	Name	Value	Description
1-0	VOLTAGE_SWING_SET	0	Level #
2	MAX_SWING_REACHED	N(0)	
4-3	PRE-EMPHASIS_SET	0	Level #
5	MAX_PRE-EMPHASIS_REACHED	N(0)	
6		0	Reserved
7		0	Reserved

### 00104: TRAINING\_LANE1\_SET

Bit	Name	Value	Description
1-0	VOLTAGE_SWING_SET	0	Level #
2	MAX_SWING_REACHED	N(0)	
4-3	PRE-EMPHASIS_SET	0	Level #
5	MAX_PRE-EMPHASIS_REACHED	N(0)	
6		0	Reserved
7		0	Reserved

### 00105: TRAINING\_LANE2\_SET

Bit	Name	Value	Description
1-0	VOLTAGE_SWING_SET	0	Level #
2	MAX_SWING_REACHED	N(0)	
4-3	PRE-EMPHASIS_SET	0	Level #
5	MAX_PRE-EMPHASIS_REACHED	N(0)	
6		0	Reserved
7		0	Reserved

### 00106: TRAINING\_LANE3\_SET

Bit	Name	Value	Description
1-0	VOLTAGE_SWING_SET	0	Level #
2	MAX_SWING_REACHED	N(0)	
4-3	PRE-EMPHASIS_SET	0	Level #

# Connections

DisplayPort Source Function

Source selects Voltage Swing and Pre-Emphasis for TPS1

If CR not Done, then adjust Voltage Swing and Pre-Emphasis

2	DNAT	30	-00:00:00.008091	< ACK
3	DNAT	30	-00:00:00.008034	> W:600 SINK_SET_POWER L=1 01
4	DNAT	30	-00:00:00.007954	< ACK
5	DNAT	30	-00:00:00.007682	> R:200 SINK_COUNT L=2
6	DNAT	30	-00:00:00.007609	< ACK 41 00
7	DPLT	30	-00:00:00.007532	> R:202 LANE0_1_STATUS: L=3
8	DPLT	30	-00:00:00.007459	< ACK 02 00 80
9	DNAT	30	-00:00:00.007349	> R:0 DPCD_REV L=12
10	DNAT	30	-00:00:00.007277	< ACK 14 1E C4 81 01 00 01 80...
11	DNAT	30	-00:00:00.007108	> W:10A eDP_CONFIGURATION_SET L=1 00
12	DNAT	30	-00:00:00.007027	< ACK
13	DNAT	30	-00:00:00.006968	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
14	DNAT	30	-00:00:00.006895	< ACK 00
15	DNAT	30	-00:00:00.006816	> R:E TRAINING_AUX_RD_INTERVAL L=1
16	DNAT	30	-00:00:00.006743	< ACK 01
17	DPLT	30	-00:00:00.001190	> W:100 LINK_BW_SET L=1 1E
18	DPLT	30	-00:00:00.001109	< ACK
19	DPLT	30	-00:00:00.001045	> W:101 LANE_COUNT_SET L=1 84
20	DPLT	30	-00:00:00.000964	< ACK
21	DPLT	30	-00:00:00.000904	> W:107 DOWNSPREAD_CTRL L=1 00
22	DPLT	30	-00:00:00.000824	< ACK
23	DNAT	30	-00:00:00.000754	> R:E TRAINING_AUX_RD_INTERVAL L=1
24	DNAT	30	-00:00:00.000681	< ACK 01
25	DPLT	30	-00:00:00.000583	> W:102 TRAINING_PATTERN_SET: L=1 21
26	DPLT	30	-00:00:00.000502	< ACK
27	DPLT	30	+00:00:00.000000	> W:103 TRAINING_LANE0_SET L=4 09 09 09 09
28	DPLT	30	+00:00:00.000104	< ACK
29	DPLT	30	+00:00:00.004095	> R:202 LANE0_1_STATUS: L=2
30	DPLT	30	+00:00:00.004168	< ACK 11 11
31	DPLT	30	+00:00:00.004300	> W:102 TRAINING_PATTERN_SET: L=1 07
32	DPLT	30	+00:00:00.004380	< ACK
33	DPLT	30	+00:00:00.004450	> W:103 TRAINING_LANE0_SET L=4 09 09 09 09
34	DPLT	30	+00:00:00.004554	< ACK
35	DPLT	30	+00:00:00.008625	> R:202 LANE0_1_STATUS: L=3
36	DPLT	30	+00:00:00.008698	< ACK 77 77 81
37	DPLT	30	+00:00:00.008798	> R:204 LANE_ALIGN_STATUS_UPDATED L=2

Type: Native  
 Direction: Request  
 Command: Read  
 Address: 0x00202 (LANE0\_1\_STATUS:)  
 Length: 2  
 Raw Data:  
 [0000] [90 02 02 01 -- -- -- --] [....]

# Connect

## DisplayPort Source Function

Source selects Voltage Swing and Pre-Emphasis for TP

If CR not Done, then adjust Voltage Swing and Pre-Emphasis

8	DPLT	DP-T30	< ACK 02 00 80
9	DNAT	DP-T30	> R:0 DPCD_REV L=12
10	DNAT	DP-T30	< ACK 14 1E C4 81 01 00 01 80...
11	DNAT	DP-T30	> W:10A eDP_CONFIGURATION_SET L=1 00
12	DNAT	DP-T30	< ACK
13	DNAT	DP-T30	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
14	DNAT	DP-T30	< ACK 00
15	DNAT	DP-T30	> R:E TRAINING_AUX_RD_INTERVAL L=1
16	DNAT	DP-T30	< ACK 01
17	DPLT	DP-T30	> W:100 LINK_BW_SET L=1 1E
18	DPLT	DP-T30	< ACK
19	DPLT	DP-T30	> W:101 LANE_COUNT_SET L=1 84
20	DPLT	DP-T30	< ACK
21	DPLT	DP-T30	> W:107 DOWNSPREAD_CTRL L=1 00
22	DPLT	DP-T30	< ACK
23	DNAT	DP-T30	> R:E TRAINING_AUX_RD_INTERVAL L=1
24	DNAT	DP-T30	< ACK 01
25	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 21
26	DPLT	DP-T30	< ACK
27	DPLT	DP-T30	> W:103 TRAINING_LANE0_SET L=4 09 09 09 09
28	DPLT	DP-T30	< ACK
29	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=2
	DPLT	DP-T30	< ACK 11 11
31	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 07
32	DPLT	DP-T30	< ACK
33	DPLT	DP-T30	> W:103 TRAINING_LANE0_SET L=4 09 09 09 09
34	DPLT	DP-T30	< ACK
35	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=3
36	DPLT	DP-T30	< ACK 77 77 81
37	DPLT	DP-T30	> R:204 LANE_ALIGN_STATUS_UPDATED L=2
38	DPLT	DP-T30	< ACK 01 00
39	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 00
40	DPLT	DP-T30	< ACK
41	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=3
42	DPLT	DP-T30	< ACK 77 77 01
43	DPLT	DP-T30	> R:100 LINK_BW_SET L=8
44	DPLT	DP-T30	< ACK 1F 84 00 09 09 09 09 09

Type: Native  
Direction: Reply  
Command: ACK

Reply to Read Request.

00202: LANE0\_1\_STATUS:

Bit	Name	Value	Description
0	LANE0_CR_DONE	Y(1)	
1	LANE0_CHANNEL_EQ_DONE	N(0)	
2	LANE0_SYMBOL_LOCKED	N(0)	
3		0	Reserved
4	LANE1_CR_DONE	Y(1)	
5	LANE1_CHANNEL_EQ_DONE	N(0)	
6	LANE1_SYMBOL_LOCKED	N(0)	
7		0	Reserved

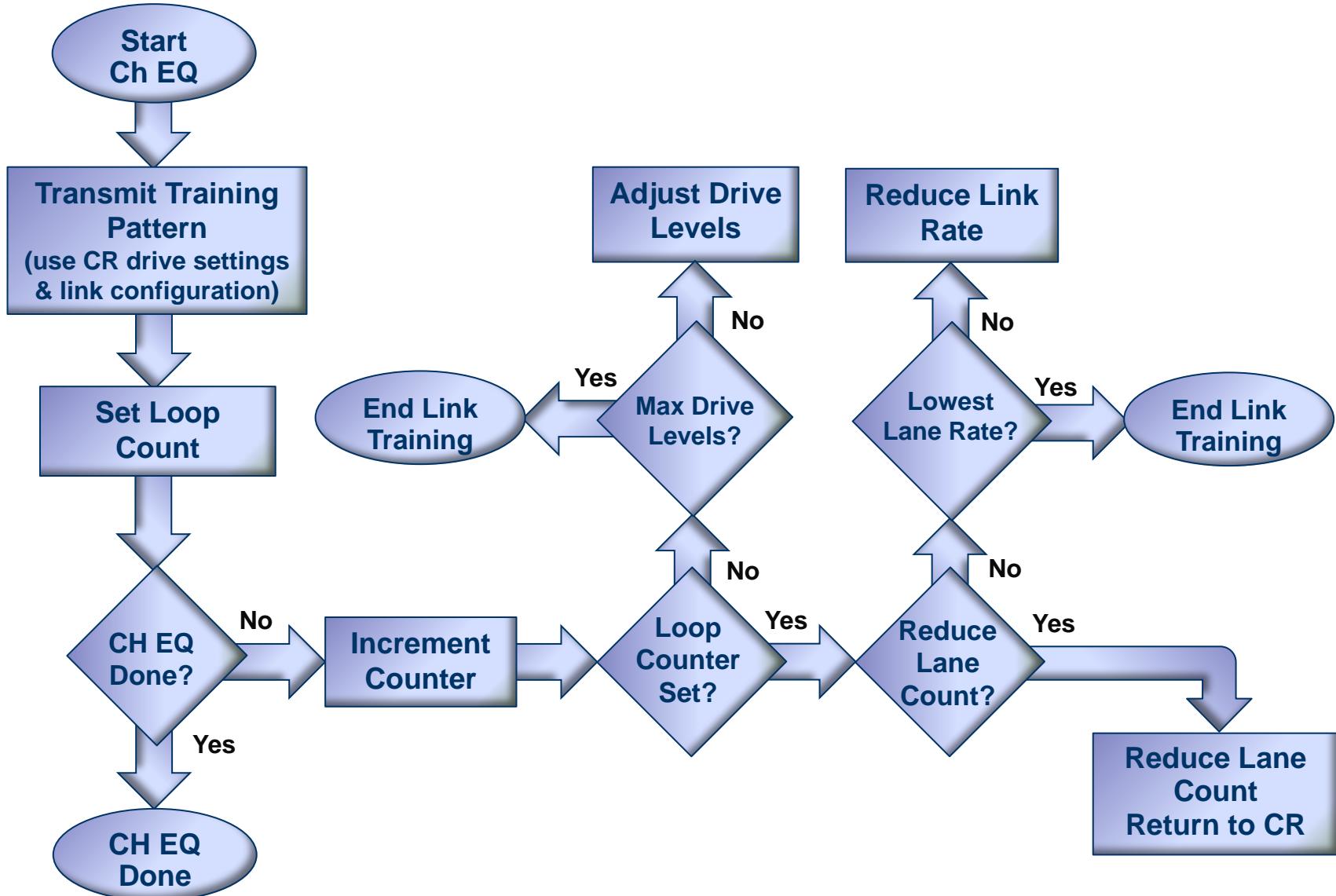
00203: LANE2\_3\_STATUS

Bit	Name	Value	Description
0	LANE2_CR_DONE	Y(1)	
1	LANE2_CHANNEL_EQ_DONE	N(0)	
2	LANE2_SYMBOL_LOCKED	N(0)	
3		0	Reserved
4	LANE3_CR_DONE	Y(1)	
5	LANE3_CHANNEL_EQ_DONE	N(0)	
6	LANE3_SYMBOL_LOCKED	N(0)	
7		0	Reserved

Raw Data:

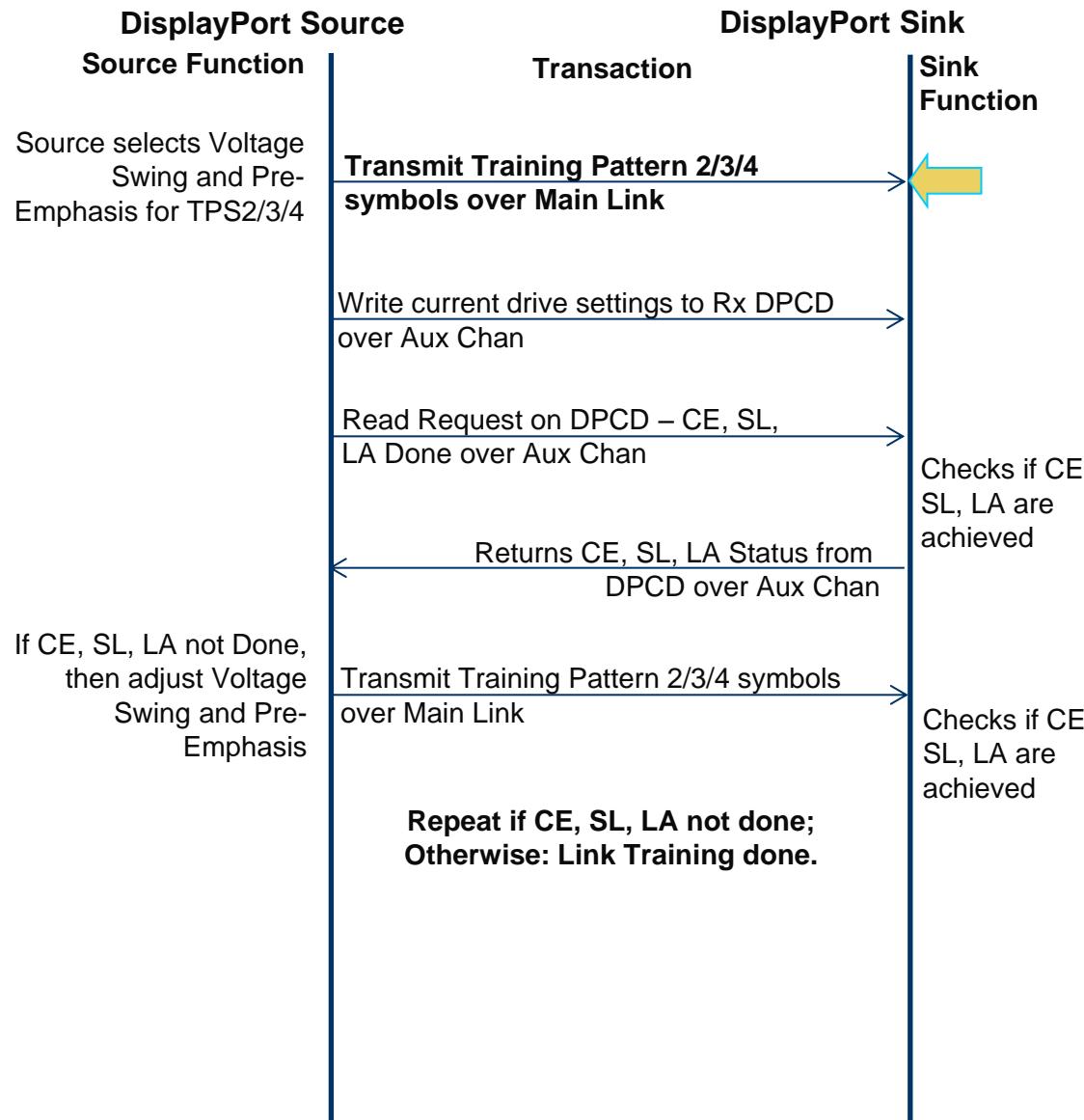
[0000] [00 11 11 -- -- -- --] [...]

# Connection Sequence – Channel EQ, Symbol Lock and Interlane Alignment

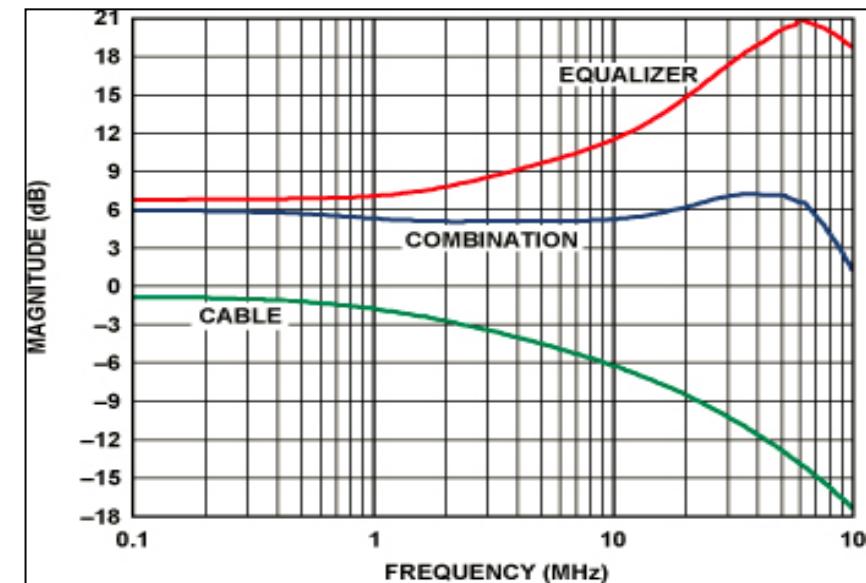


- There are 3 things that can be changed while still meeting the requirements of the video format being transmitted; listed in priority order:
  - Drive levels, i.e. voltage swing and pre-emphasis.
  - Link Rate, i.e. RBR at 1.62 Gb/s/lane through HBR3 at 8.1Gb/s/lane.
  - Number of lanes. Lanes can be reduced if the CR shows that the lower lanes were successfully locked.

# Connection Sequence – Link Training Channel EQ, Symbol Lock, Interlane Alignment



- **Symbol Lock and Equalization.**
  - Starts with **same link configuration and drive settings** used for Clock Recovery.
  - Symbol Lock is achieved when the receiver has **identified and aligned on the 8b/10b symbol boundaries**.
  - Cable acts like a low pass filter attenuating the harmonics of the fundamental frequency and smearing out the bits resulting in inter-symbol interference.
  - Cable equalization is the process of **altering the frequency response of a video amplifier to compensate for high frequency losses in a cable**.



# Connections

## DisplayPort Source Function

Source selects Voltage  
Swing and Pre-  
Emphasis for TPS2/3

If CE, SL, LA not Done  
then adjust Voltage  
Swing and Pre-  
Emph

7	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=3
8	DPLT	DP-T30	< ACK 02 00 80
9	DNAT	DP-T30	> R:0 DPCD_REV L=12
10	DNAT	DP-T30	< ACK 14 1E C4 81 01 00 01 80...
11	DNAT	DP-T30	> W:10A eDP_CONFIGURATION_SET L=1 00
12	DNAT	DP-T30	< ACK
13	DNAT	DP-T30	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
14	DNAT	DP-T30	< ACK 00
15	DNAT	DP-T30	> R:E TRAINING_AUX_RD_INTERVAL L=1
16	DNAT	DP-T30	< ACK 01
17	DPLT	DP-T30	> W:100 LINK_BW_SET L=1 1E
18	DPLT	DP-T30	< ACK
19	DPLT	DP-T30	> W:101 LANE_COUNT_SET L=1 84
20	DPLT	DP-T30	< ACK
21	DPLT	DP-T30	> W:107 DOWNSPREAD_CTRL L=1 00
22	DPLT	DP-T30	< ACK
23	DNAT	DP-T30	> R:E TRAINING_AUX_RD_INTERVAL L=1
24	DNAT	DP-T30	< ACK 01
25	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 21
26	DPLT	DP-T30	< ACK
27	DPLT	DP-T30	> W:103 TRAINING_LANE0_SET L=4 09 09 09 09
28	DPLT	DP-T30	< ACK
29	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=2
30	DPLT	DP-T30	< ACK 11 11
31	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 07
32	DPLT	DP-T30	< ACK
33	DPLT	DP-T30	> W:103 TRAINING_LANE0_SET L=4 09 09 09 09
34	DPLT	DP-T30	< ACK
35	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=3
36	DPLT	DP-T30	< ACK 77 77 81
37	DPLT	DP-T30	> R:204 LANE_ALIGN_STATUS_UPDATED L=2
38	DPLT	DP-T30	< ACK 01 00
39	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 00
40	DPLT	DP-T30	< ACK
41	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=3
42	DPLT	DP-T30	< ACK 77 77 01
43	DPLT	DP-T30	> R:100 LINK_BW_SET L=8

Start Time:	+00:58:37.057861		
Type:	Native		
Direction:	Request		
Command:	Write		
Address:	0x00102 (TRAINING_PATTERN_SET:)		
Length:	1		
00102: TRAINING_PATTERN_SET:			
Bit	Name	Value	Description
3-0	TRAINING_PATTERN_SELECT	7	Pattern 4
4	RECOVERED_CLOCK_OUT_EN	N(0)	
5	SCRAMBLING_DISABLE	N(0)	
7-6	SYMBOL_ERROR_COUNT_SEL	0	Disparity and Symbol error
Raw Data:		[0000] [80 01 02 00 07 -- -- --] [.....]	

# Connections

## DisplayPort Source Function

Source selects Voltage Swing and Pre-Emphasis for TPS2/3/4

If CE, SL, LA not Done then adjust Voltage Swing and Pre-Emphasis

7	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=3
8	DPLT	DP-T30	< ACK 02 00 80
9	DNAT	DP-T30	> R:0 DPCD_REV L=12
10	DNAT	DP-T30	< ACK 14 1E C4 81 01 00 01 80...
11	DNAT	DP-T30	> W:10A eDP_CONFIGURATION_SET L=1 00
12	DNAT	DP-T30	< ACK
13	DNAT	DP-T30	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
14	DNAT	DP-T30	< ACK 00
15	DNAT	DP-T30	> R:E TRAINING_AUX_RD_INTERVAL L=1
16	DNAT	DP-T30	< ACK 01
17	DPLT	DP-T30	> W:100 LINK_BW_SET L=1 1E
18	DPLT	DP-T30	< ACK
19	DPLT	DP-T30	> W:101 LANE_COUNT_SET L=1 84
20	DPLT	DP-T30	< ACK
21	DPLT	DP-T30	> W:107 DOWNSPREAD_CTRL L=1 00
22	DPLT	DP-T30	< ACK
23	DNAT	DP-T30	> R:E TRAINING_AUX_RD_INTERVAL L=1
24	DNAT	DP-T30	< ACK 01
25	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 21
26	DPLT	DP-T30	< ACK
27	DPLT	DP-T30	> W:103 TRAINING_LANE0_SET L=4 09 09 09 09
28	DPLT	DP-T30	< ACK
29	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=2
30	DPLT	DP-T30	< ACK 11 11
31	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 07
32	DPLT	DP-T30	< ACK
33	DPLT	DP-T30	> W:103 TRAINING_LANE0_SET L=4 09 09 09 09
34	DPLT	DP-T30	< ACK
35	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=3
36	DPLT	DP-T30	< ACK 77 77 81
37	DPLT	DP-T30	> R:204 LANE_ALIGN_STATUS_UPDATED L=2
38	DPLT	DP-T30	< ACK 01 00
39	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 00
40	DPLT	DP-T30	< ACK
41	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=3
42	DPLT	DP-T30	< ACK 77 77 01

Start Time:	+00:58:37.058011
Type:	Native
Direction:	Request
Command:	Write
Address:	0x00103 (TRAINING_LANE0_SET)
Length:	4
00103: TRAINING_LANE0_SET	
Bit	Name
-----	-----
1-0	VOLTAGE_SWING_SET
2	MAX_SWING_REACHED
4-3	PRE-EMPHASIS_SET
5	MAX_PRE-EMPHASIS_REACHED
6	
7	
Value Description	
1	Level #
N(0)	
1	Level #
N(0)	
0	Reserved
0	Reserved
00104: TRAINING_LANE1_SET	
Bit	Name
-----	-----
1-0	VOLTAGE_SWING_SET
2	MAX_SWING_REACHED
4-3	PRE-EMPHASIS_SET
5	MAX_PRE-EMPHASIS_REACHED
6	
7	
Value Description	
1	Level #
N(0)	
1	Level #
N(0)	
0	Reserved
0	Reserved
00105: TRAINING_LANE2_SET	
Bit	Name
-----	-----
1-0	VOLTAGE_SWING_SET
2	MAX_SWING_REACHED
4-3	PRE-EMPHASIS_SET
5	MAX_PRE-EMPHASIS_REACHED
6	
7	
Value Description	
1	Level #
N(0)	
1	Level #
N(0)	
0	Reserved
0	Reserved
00106: TRAINING_LANE3_SET	
Bit	Name
-----	-----
1-0	VOLTAGE_SWING_SET
2	MAX_SWING_REACHED
4-3	PRE-EMPHASIS_SET
5	MAX_PRE-EMPHASIS_REACHED
6	
7	
Value Description	
1	Level #
N(0)	
1	Level #
N(0)	

# Connections

## DisplayPort Source Function

Source selects Voltage  
Swing and Pre-  
Emphasis for TPS2/3/4

If CE, SL, LA not Done  
then adjust Voltage  
Swing and Pre-  
Emphasis

9	DNAT	DP-T30	> R:0 DPCD_REV L=12
10	DNAT	DP-T30	< ACK 14 1E C4 81 01 00 01 80...
11	DNAT	DP-T30	> W:10A eDP_CONFIGURATION_SET L=1 00
12	DNAT	DP-T30	< ACK
13	DNAT	DP-T30	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
14	DNAT	DP-T30	< ACK 00
15	DNAT	DP-T30	> R:E TRAINING_AUX_RD_INTERVAL L=1
16	DNAT	DP-T30	< ACK 01
17	DPLT	DP-T30	> W:100 LINK_BW_SET L=1 1E
18	DPLT	DP-T30	< ACK
19	DPLT	DP-T30	> W:101 LANE_COUNT_SET L=1 84
20	DPLT	DP-T30	< ACK
21	DPLT	DP-T30	> W:107 DOWNSPREAD_CTRL L=1 00
22	DPLT	DP-T30	< ACK
23	DNAT	DP-T30	> R:E TRAINING_AUX_RD_INTERVAL L=1
24	DNAT	DP-T30	< ACK 01
25	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 21
26	DPLT	DP-T30	< ACK
27	DPLT	DP-T30	> W:103 TRAINING_LANE0_SET L=4 09 09 09 09
28	DPLT	DP-T30	< ACK
29	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=2
30	DPLT	DP-T30	< ACK 11 11
31	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 07
32	DPLT	DP-T30	< ACK
33	DPLT	DP-T30	> W:103 TRAINING_LANE0_SET L=4 09 09 09 09
34	DPLT	DP-T30	< ACK
35	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=3
36	DPLT	DP-T30	ACK 77 77 81
37	DPLT	DP-T30	> R:204 LANE_ALIGN_STATUS_UPDATED L=2
38	DPLT	DP-T30	< ACK 01 00
39	DPLT	DP-T30	> W:102 TRAINING_PATTERN_SET: L=1 00
40	DPLT	DP-T30	< ACK
41	DPLT	DP-T30	> R:202 LANE0_1_STATUS: L=3
42	DPLT	DP-T30	< ACK 77 77 01

Direction: Reply Command: ACK		
Reply to Read Request.		
00202: LANE0_1_STATUS:		
Bit	Name	Value Description
0	LANE0_CR_DONE	Y(1)
1	LANE0_CHANNEL_EQ_DONE	Y(1)
2	LANE0_SYMBOL_LOCKED	Y(1)
3		0 Reserved
4	LANE1_CR_DONE	Y(1)
5	LANE1_CHANNEL_EQ_DONE	Y(1)
6	LANE1_SYMBOL_LOCKED	Y(1)
7		0 Reserved
00203: LANE2_3_STATUS		
Bit	Name	Value Description
0	LANE2_CR_DONE	Y(1)
1	LANE2_CHANNEL_EQ_DONE	Y(1)
2	LANE2_SYMBOL_LOCKED	Y(1)
3		0 Reserved
4	LANE3_CR_DONE	Y(1)
5	LANE3_CHANNEL_EQ_DONE	Y(1)
6	LANE3_SYMBOL_LOCKED	Y(1)
7		0 Reserved
00204: LANE_ALIGN_STATUS_UPDATED		
Bit	Name	Value Description
0	INTERLANE_ALIGN_DONE	Y(1)
1	POST_LT_ADJ_REQ_IN_PROGRESS	N(0)
2		0 Reserved
3		0 Reserved
4		0 Reserved
5		0 Reserved
6	DOWNTSTREAM_PORT_STATUS_CHANGED	N(0)
7	LINK_STATUS_UPDATED	Y(1)
Raw Data:		
[0000] [00 77 77 81 -- -- --] [.ww. ]		

# Connecticut

## DisplayPort Source Function

Source selects Voltage Swing and Pre-Emphasis for TPS2/3/4

If CE, SL, LA not Done,  
then adjust Voltage  
Swing and Pre-  
Emphasis

```
28 DNAT 61 < ACK 01
29 DPLT 61 > W:100 LINK_BW_SET L=1 0A
30 DPLT 61 < ACK
31 DPLT 61 > R:100 LINK_BW_SET L=2
32 DPLT 61 < ACK 0A 84
33 DPLT 61 > W:102 TRAINING_PATTERN_SET: L=1 21
34 DPLT 61 < ACK
35 DPLT 61 > W:103 TRAINING_LANE0_SET L=4 11 11 1...
36 DPLT 61 < ACK
37 DPLT 61 > R:202 LANE0_1_STATUS: L=2
38 DPLT 61 < ACK 11 11
39 DPLT 61 > W:102 TRAINING_PATTERN_SET: L=1 22
40 DPLT 61 < ACK
41 DPLT 61 > W:103 TRAINING_LANE0_SET L=4 11 11 1...
42 DPLT 61 < ACK
43 DPLT 61 > R:202 LANE0_1_STATUS: L=3
44 DPLT 61 < ACK 73 77 81
45 DPLT 61 > R:204 LANE_ALIGN_STATUS_UPDATED L=2
46 DPLT 61 < ACK 01 00
47 DPLT 61 > W:102 TRAINING_PATTERN_SET: L=1 00
48 DPLT 61 < ACK
49 DPLT 61 > R:202 LANE0_1_STATUS: L=3
50 DPLT 61 < ACK 73 77 01
51 DNAT 61 > R:E TRAINING_AUX_RD_INTERVAL L=1
52 DNAT 61 < ACK 01
53 DPLT 61 > W:102 TRAINING_PATTERN_SET: L=1 21
54 DPLT 61 < ACK
55 DPLT 61 > W:103 TRAINING_LANE0_SET L=4 11 11 1...
56 DPLT 61 < ACK
57 DPLT 61 > R:202 LANE0_1_STATUS: L=2
58 DPLT 61 < ACK 11 11
59 DPLT 61 > W:102 TRAINING_PATTERN_SET: L=1 22
60 DPLT 61 < ACK
61 DPLT 61 > W:103 TRAINING_LANE0_SET L=4 11 11 1...
```

Type: Native  
Direction: Reply  
Command: ACK

Reply to Read Request.

**00202: LANE0\_1\_STATUS:**

Bit	Name	Value	Description
0	LANE0_CR_DONE	Y(1)	
1	LANE0_CHANNEL_EQ_DONE	Y(1)	
2	LANE0_SYMBOL_LOCKED	N(0)	
3		0	Reserved
4	LANE1_CR_DONE	Y(1)	
5	LANE1_CHANNEL_EQ_DONE	Y(1)	
6	LANE1_SYMBOL_LOCKED	N(0)	
7		0	Reserved

**00203: LANE2\_3\_STATUS**

Bit	Name	Value	Description
0	LANE2_CR_DONE	Y(1)	
1	LANE2_CHANNEL_EQ_DONE	Y(1)	
2	LANE2_SYMBOL_LOCKED	N(0)	
3		0	Reserved
4	LANE3_CR_DONE	Y(1)	
5	LANE3_CHANNEL_EQ_DONE	Y(1)	
6	LANE3_SYMBOL_LOCKED	N(0)	
7		0	Reserved

**00204: LANE\_ALIGN\_STATUS\_UPDATED**

Bit	Name	Value	Description
0	INTERLANE_ALIGN_DONE	Y(1)	
1		0	Reserved
2		0	Reserved
3		0	Reserved
4		0	Reserved
5		0	Reserved
6	DOWNTREAM_PORT_STATUS_CHANGED	N(0)	
7	LINK_STATUS_UPDATED	Y(1)	

# Connections

## DisplayPort Source Function

Source selects Voltage Swing and Pre-Emphasis for TPS2/3/4

If CE, SL, LA not Done, then adjust Voltage Swing and Pre-Emphasis

7	DNAT	61	> W:600 SINK_SET_POWER L=1 01
8	DNAT	61	< ACK
9	DNAT	61	> R:200 SINK_COUNT L=2
10	DNAT	61	< ACK 41 00
11	DPLT	61	> R:202 LANE0_1_STATUS: L=3
12	DPLT	61	< ACK 57 55 00
13	DNAT	61	> R:0 DPCD_REV L=12
14	DNAT	61	< ACK 12 0A 04 01 01 00 01 80...
15	DNAT	61	> W:10A eDP_CONFIGURATION_SET L=1 00
16	DNAT	61	< ACK
17	DNAT	61	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
18	DNAT	61	< ACK 00
19	DNAT	61	> R:E TRAINING_AUX_RD_INTERVAL L=1
20	DNAT	61	< ACK 01
21	DPLT	61	> W:100 LINK_BW_SET L=1 0A
22	DPLT	61	< ACK
23	DPLT	61	> W:101 LANE_COUNT_SET L=1 84
24	DPLT	61	< ACK
25	DPLT	61	> W:107 DOWNSPREAD_CTRL L=1 00
26	DPLT	61	< ACK
27	DNAT	61	> R:E TRAINING_AUX_RD_INTERVAL L=1
28	DNAT	61	< ACK 01
29	DPLT	61	> W:100 LINK_BW_SET L=1 0A
30	DPLT	61	< ACK
31	DPLT	61	> R:100 LINK_BW_SET L=2
32	DPLT	61	< ACK 0A 84
33	DPLT	61	> W:102 TRAINING_PATTERN_SET: L=1 21
34	DPLT	61	< ACK
35	DPLT	61	> W:103 TRAINING_LANE0_SET L=4 11 11 1...
36	DPLT	61	< ACK
37	DPLT	61	> R:202 LANE0_1_STATUS: L=2
38	DPLT	61	< ACK 11 11
39	DPLT	61	> W:102 TRAINING_PATTERN_SET: L=1 22
40	DPLT	61	< ACK
41	DPLT	61	> W:103 TRAINING_LANE0_SET L=4 11 11 1...
42	DPLT	61	< ACK

Start Time: +00:07:51.363578			
Type:	Native		
Direction:	Reply		
Command:	ACK		
Reply to Read Request.			
00202: LANE0_1_STATUS:			
Bit	Name	Value Description	
0	LANE0_CR_DONE	Y(1)	
1	LANE0_CHANNEL_EQ_DONE	Y(1)	
2	LANE0_SYMBOL_LOCKED	N(0)	
3		0 Reserved	
4	LANE1_CR_DONE	Y(1)	
5	LANE1_CHANNEL_EQ_DONE	Y(1)	
6	LANE1_SYMBOL_LOCKED	Y(1)	
7		0 Reserved	
00203: LANE2_3_STATUS			
Bit	Name	Value Description	
0	LANE2_CR_DONE	Y(1)	
1	LANE2_CHANNEL_EQ_DONE	Y(1)	
2	LANE2_SYMBOL_LOCKED	Y(1)	
3		0 Reserved	
4	LANE3_CR_DONE	Y(1)	
5	LANE3_CHANNEL_EQ_DONE	Y(1)	
6	LANE3_SYMBOL_LOCKED	Y(1)	
7		0 Reserved	
00204: LANE_ALIGN_STATUS_UPDATED			
Bit	Name	Value Description	
0	INTERLANE_ALIGN_DONE	Y(1)	
1		0 Reserved	
2		0 Reserved	
3		0 Reserved	
4		0 Reserved	
5		0 Reserved	
6	DOWNSTREAM_PORT_STATUS_CHANGED	N(0)	
7	LINK_STATUS_UPDATED	Y(1)	
Raw Data:			
[00001]00 73 77 81		15.5V	1

# Connect

## DisplayPort Source Function

Source selects Voltage Swing and Pre-Emphasis for TPS

If CR not Done, then adjust Voltage Swing and Pre-Emphas

12	DPLT	61	+02:04:52.429277	< ACK 57 55 80
13	DNAT	61	+02:04:52.429376	> R:0 DPCD_REV L=12
14	DNAT	61	+02:04:52.429448	< ACK 12 14 04 01 01 00 01 80...
15	DNAT	61	+02:04:52.429604	> W:10A eDP_CONFIGURATION_SET L=1 00
16	DNAT	61	+02:04:52.429684	< ACK
17	DNAT	61	+02:04:52.429736	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
18	DNAT	61	+02:04:52.429808	< ACK 00
19	DNAT	61	+02:04:52.429880	> R:E TRAINING_AUX_RD_INTERVAL L=1
20	DNAT	61	+02:04:52.429952	< ACK 01
21	DNAT	61	+02:04:52.430015	> R:0 DPCD_REV L=12
22	DNAT	61	+02:04:52.430088	< ACK 12 14 04 01 01 00 01 80...
23	DPLT	61	+02:04:52.432752	> W:100 LINK_BW_SET L=1 14
24	DPLT	61	+02:04:52.432832	< ACK
25	DPLT	61	+02:04:52.432888	> W:101 LANE_COUNT_SET L=1 84
26	DPLT	61	+02:04:52.432968	< ACK
27	DPLT	61	+02:04:52.433022	> W:107 DOWNSPREAD_CTRL L=1 00
28	DPLT	61	+02:04:52.433102	< ACK
29	DNAT	61	+02:04:52.433163	> R:E TRAINING_AUX_RD_INTERVAL L=1
30	DNAT	61	+02:04:52.433235	< ACK 01
31	DPLT	61	+02:04:52.433316	> W:102 TRAINING_PATTERN_SET: L=1 21
32	DPLT	61	+02:04:52.433396	< ACK
33	DPLT	61	+02:04:52.433592	> W:103 TRAINING_LANE0_SET L=4 00 00 00 00
34	DPLT	61	+02:04:52.433695	< ACK
35	DPLT	61	+02:04:52.437670	> R:202 LANE0_1_STATUS: L=2
36	DPLT	61	+02:04:52.437742	< ACK 00 00
37	DPLT	61	+02:04:52.437829	> R:206 ADJUST_REQUEST_LANE0_1 L=2
				ACK 66 66
39	DPLT	61	+02:04:52.438097	> W:103 TRAINING_LANE0_SET L=4 0A 0A 0A 0A
40	DPLT	61	+02:04:52.438200	< ACK
41	DPLT	61	+02:04:52.442175	> R:202 LANE0_1_STATUS: L=2
42	DPLT	61	+02:04:52.442247	< ACK 11 11
43	DPLT	61	+02:04:52.442349	> W:102 TRAINING_PATTERN_SET: L=1 22
44	DPLT	61	+02:04:52.442429	< ACK
45	DPLT	61	+02:04:52.442491	> W:103 TRAINING_LANE0_SET L=4 0A 0A 0A 0A
46	DPLT	61	+02:04:52.442594	< ACK
47	DPLT	61	+02:04:52.446576	> R:202 LANE0_1_STATUS: L=3

Type: Native
Direction: Reply
Command: ACK
Reply to Read Request.
00206: ADJUST_REQUEST_LANE0_1
Bit Name Value Description
1-0 VOLTAGE_SWING_LANE0 2 Level #
3-2 PRE-EMPHASIS_LANE0 1 Level #
5-4 VOLTAGE_SWING_LANE1 2 Level #
7-6 PRE-EMPHASIS_LANE1 1 Level #
00207: ADJUST_REQUEST_LANE2_3
Bit Name Value Description
1-0 VOLTAGE_SWING_LANE2 2 Level #
3-2 PRE-EMPHASIS_LANE2 1 Level #
5-4 VOLTAGE_SWING_LANE3 2 Level #
7-6 PRE-EMPHASIS_LANE3 1 Level #
Raw Data:
[0000] [00 66 66 -- -- -- --] [.ff ]

# Connect

DisplayPort

Source Function

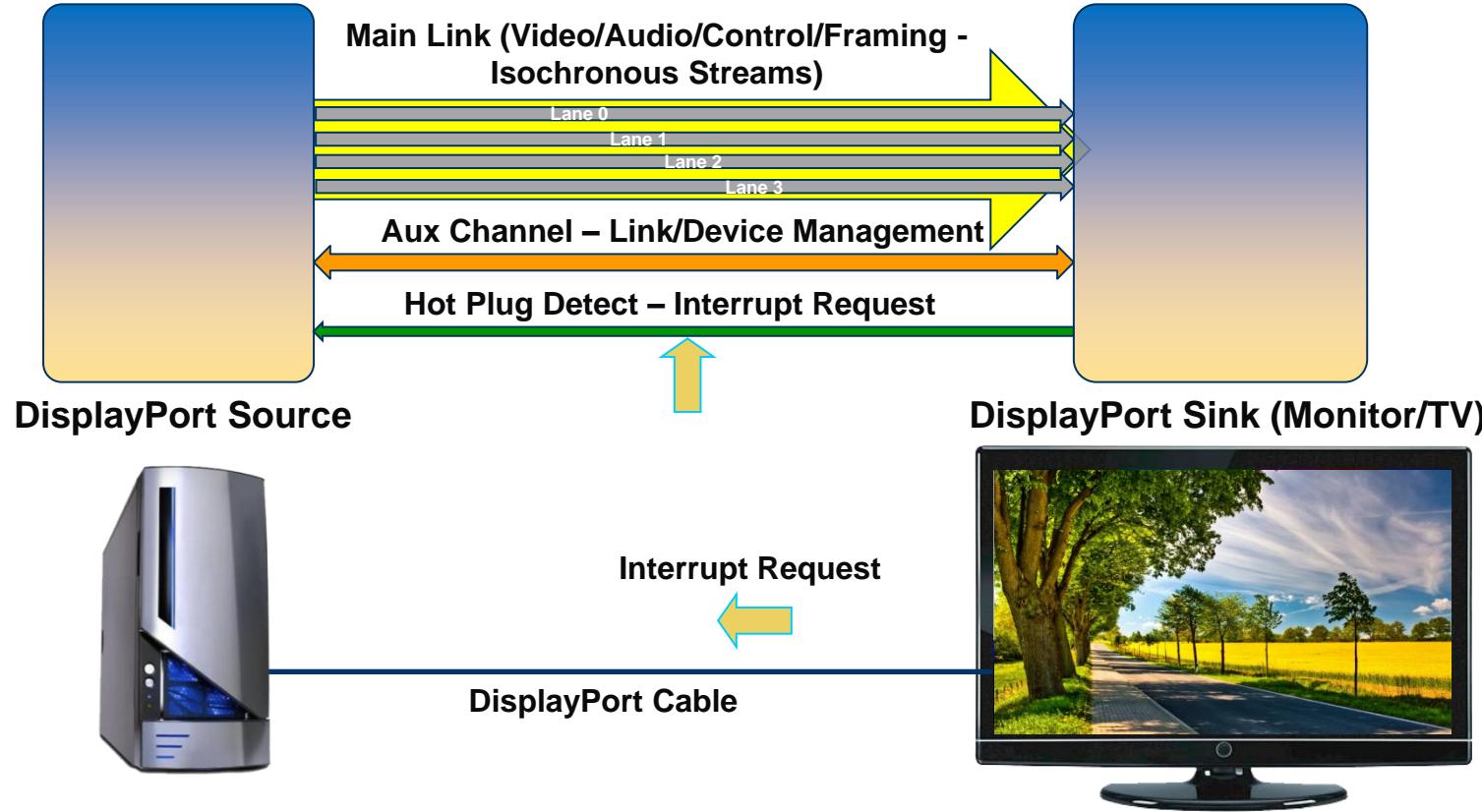
Source selects Voltage Swing and Pre-Emphasis for TPS

If CR not Done, then adjust Voltage Swing and Pre-Emphasis

11	DPLT	61	+02:04:52.429205	> R:202 LANE0_1_STATUS: L=3
12	DPLT	61	+02:04:52.429277	< ACK 57 55 80
13	DNAT	61	+02:04:52.429376	> R:0 DPCD_REV L=12
14	DNAT	61	+02:04:52.429448	< ACK 12 14 04 01 01 00 01 80...
15	DNAT	61	+02:04:52.429604	> W:10A eDP_CONFIGURATION_SET L=1 00
16	DNAT	61	+02:04:52.429684	< ACK
17	DNAT	61	+02:04:52.429736	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
18	DNAT	61	+02:04:52.429808	< ACK 00
19	DNAT	61	+02:04:52.429880	> R:E TRAINING_AUX_RD_INTERVAL L=1
20	DNAT	61	+02:04:52.429952	< ACK 01
21	DNAT	61	+02:04:52.430015	> R:0 DPCD_REV L=12
22	DNAT	61	+02:04:52.430088	< ACK 12 14 04 01 01 00 01 80...
23	DPLT	61	+02:04:52.432752	> W:100 LINK_BW_SET L=1 14
24	DPLT	61	+02:04:52.432832	< ACK
25	DPLT	61	+02:04:52.432888	> W:101 LANE_COUNT_SET L=1 84
26	DPLT	61	+02:04:52.432968	< ACK
27	DPLT	61	+02:04:52.433022	> W:107 DOWNSPREAD_CTRL L=1 00
28	DPLT	61	+02:04:52.433102	< ACK
29	DNAT	61	+02:04:52.433163	> R:E TRAINING_AUX_RD_INTERVAL L=1
30	DNAT	61	+02:04:52.433235	< ACK 01
31	DPLT	61	+02:04:52.433316	> W:102 TRAINING_PATTERN_SET: L=1 21
32	DPLT	61	+02:04:52.433396	< ACK
33	DPLT	61	+02:04:52.433592	> W:103 TRAINING_LANE0_SET L=4 00 00 00 00
34	DPLT	61	+02:04:52.433695	< ACK
35	DPLT	61	+02:04:52.437670	> R:202 LANE0_1_STATUS: L=2
36	DPLT	61	+02:04:52.437742	< ACK 00 00
37	DPLT	61	+02:04:52.437829	> R:206 ADJUST_REQUEST_LANE0_1 L=2
38	DPLT	61	+02:04:52.437901	< ACK 66 66
39	DPLT	61	+02:04:52.438074	> W:103 TRAINING_LANE0_SET L=4 0A 0A 0A 0A
40	DPLT	61	+02:04:52.438200	< ACK
41	DPLT	61	+02:04:52.442175	> R:202 LANE0_1_STATUS: L=2
42	DPLT	61	+02:04:52.442247	< ACK 11 11
43	DPLT	61	+02:04:52.442349	> W:102 TRAINING_PATTERN_SET: L=1 22
44	DPLT	61	+02:04:52.442429	< ACK
45	DPLT	61	+02:04:52.442491	> W:103 TRAINING_LANE0_SET L=4 0A 0A 0A 0A
46	DPLT	61	+02:04:52.442594	< ACK
47	DPLT	61	+02:04:52.446576	> R:202 LANE0_1_STATUS: L=3

Start Time:	+02:04:52.438097		
Type:	Native		
Direction:	Request		
Command:	Write		
Address:	0x00103	(TRAINING_LANE0_SET)	
Length:	4		
<b>00103: TRAINING_LANE0_SET</b>			
Bit	Name	Value Description	
1-0	VOLTAGE_SWING_SET	2	Level #
2	MAX_SWING_REACHED	N(0)	
4-3	PRE-EMPHASIS_SET	1	Level #
5	MAX_PRE-EMPHASIS_REACHED	N(0)	
6		0	Reserved
7		0	Reserved
<b>00104: TRAINING_LANE1_SET</b>			
Bit	Name	Value Description	
1-0	VOLTAGE_SWING_SET	2	Level #
2	MAX_SWING_REACHED	N(0)	
4-3	PRE-EMPHASIS_SET	1	Level #
5	MAX_PRE-EMPHASIS_REACHED	N(0)	
6		0	Reserved
7		0	Reserved
<b>00105: TRAINING_LANE2_SET</b>			
Bit	Name	Value Description	
1-0	VOLTAGE_SWING_SET	2	Level #
2	MAX_SWING_REACHED	N(0)	
4-3	PRE-EMPHASIS_SET	1	Level #
5	MAX_PRE-EMPHASIS_REACHED	N(0)	
6		0	Reserved
7		0	Reserved
<b>00106: TRAINING_LANE3_SET</b>			
Bit	Name	Value Description	
1-0	VOLTAGE_SWING_SET	2	Level #
2	MAX_SWING_REACHED	N(0)	
4-3	PRE-EMPHASIS_SET	1	Level #
5	MAX_PRE-EMPHASIS_REACHED	N(0)	
6		0	Reserved
7		0	Reserved

# Auxiliary Channel Analyzer (ACA) – Link Maintenance



- If Link Training is successful, then Link Maintenance mode.
- Link Training does not guarantee that the link will behave without errors.
- In Link Maintenance mode, the Link Policy function may force a retrain if there is a failure on the link.
- Link retraining is necessary when there is a loss of Clock Lock, Symbol Lock or Inter-Lane Alignment.
- Failure results in an IRQ interrupt using the Hot Plug Detect lead. The interrupt is a low-going pulse.
- Source re-initiates Link Training.

# Auxiliary Channel

## DisplayPort Source Source Function

Source selects Voltage  
Swing and Pre-  
Emphasis for TPS2/3/4

Transmit  
symbol

Write count  
over Aux

Read R  
LA Done

←

If CE, SL, LA not Done,  
then adjust Voltage  
Swing and Pre-  
Emphasis

Transmit  
over Main

Re-  
Org

←

64	DPLT	61	< ACK
65	DPLT	61	> R:202 LANE0_1_STATUS: L=2
66		61	
67	DPLT	61	> W:102 TRAINING_PATTERN_SET: L=1 23
68	DPLT	61	< ACK
69	DPLT	61	> W:103 TRAINING_LANE0_SET L=4 00 00 00 00 00
70	DPLT	61	< ACK
71	DPLT	61	> R:202 LANE0_1_STATUS: L=3
	DPLT	61	< ACK 77 77 81
73	DPLT	61	> R:204 LANE_ALIGN_STATUS_UPDATED L=2
74	DPLT	61	< ACK 01 00
75	DPLT	61	> W:102 TRAINING_PATTERN_SET: L=1 00
76	DPLT	61	< ACK
77	DPLT	61	> R:202 LANE0_1_STATUS: L=3
78	DPLT	61	< ACK 77 77 81
79	DPLT	61	> R:100 LINK_BW_SET L=8
80	DPLT	61	< ACK 0A 84 00 00 00 00 00 00
81	DPLT	61	> R:202 LANE0_1_STATUS: L=3
82	DPLT	61	< ACK 00 00 80
83	DPLT	61	HPD Falling Edge
84	DPHP	61	HPD Rising Edge
85	DPLT	61	> W:100 LINK_BW_SET L=1 0A
86	DPLT	61	< ACK
87	DPLT	61	> W:101 LANE_COUNT_SET L=1 84
88	DPLT	61	< ACK
89	DPLT	61	> W:107 DOWNSPREAD_CTRL L=1 00
90	DPLT	61	< ACK
91	DPLT	61	> W:102 TRAINING_PATTERN_SET: L=1 21
92	DPLT	61	< ACK
93	DPLT	61	> W:103 TRAINING_LANE0_SET L=4 00 00 00 00
94	DPLT	61	< ACK
95	DPLT	61	> R:202 LANE0_1_STATUS: L=2
96	DPLT	61	< ACK 11 11
97	DPLT	61	> W:102 TRAINING_PATTERN_SET: L=1 23
98	DPLT	61	< ACK
99	DPLT	61	> W:102 TRAINING_LINES_SET L=4 00 00 00 00

Start Time: +02:19:23.547559

Type: Native

Direction: Reply

Command: ACK

Reply to Read Request.

00202: LANE0\_1\_STATUS:

Bit	Name	Line Description
0	LANE0_CR_DONE	Y(1)
1	LANE0_CHANNEL_EQ_DONE	Y(1)
2	LANE0_SYMBOL_LOCKED	Y(1)
3		0 Reserved
4	LANE1_CR_DONE	Y(1)
5	LANE1_CHANNEL_EQ_DONE	Y(1)
6	LANE1_SYMBOL_LOCKED	Y(1)
7		0 Reserved

00203: LANE2\_3\_STATUS

Bit	Name	Value Description
0	LANE2_CR_DONE	Y(1)
1	LANE2_CHANNEL_EQ_DONE	Y(1)
2	LANE2_SYMBOL_LOCKED	Y(1)
3		0 Reserved
4	LANE3_CR_DONE	Y(1)
5	LANE3_CHANNEL_EQ_DONE	Y(1)
6	LANE3_SYMBOL_LOCKED	Y(1)
7		0 Reserved

00204: LANE\_ALIGN\_STATUS\_UPDATED

Bit	Name	Value Description
0	INTERLANE_ALIGN_DONE	Y(1)
1		0 Reserved
2		0 Reserved
3		0 Reserved
4		0 Reserved
5		0 Reserved
6	DOWNTSTREAM_PORT_STATUS_CHANGED	N(0)
7	LINK_STATUS_UPDATED	Y(1)

Raw Data:

[00202][00 77 77 81]

[00203][00 84 00 00 00 00 00 00]

[00204][00 11 11]

[00202][00 77 77 81]

[00203][00 84 00 00 00 00 00 00]

[00204][00 11 11]

[00202][00 77 77 81]

[00203][00 84 00 00 00 00 00 00]

[00204][00 11 11]

[00202][00 77 77 81]

[00203][00 84 00 00 00 00 00 00]

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[00204][00 11 11]

[00202][00 77 77 81]

[00203][00 84 00 00 00 00 00 00]

[00204][00 11 11]

[00202][00 77 77 81]

[00203][00 84 00 00 00 00 00 00]

[00204][00 11 11]

[00202][00 77 77 81]

[00203][00 84 00 00 00 00 00 00]

[00204][00 11 11]

[00202][00 77 77 81]

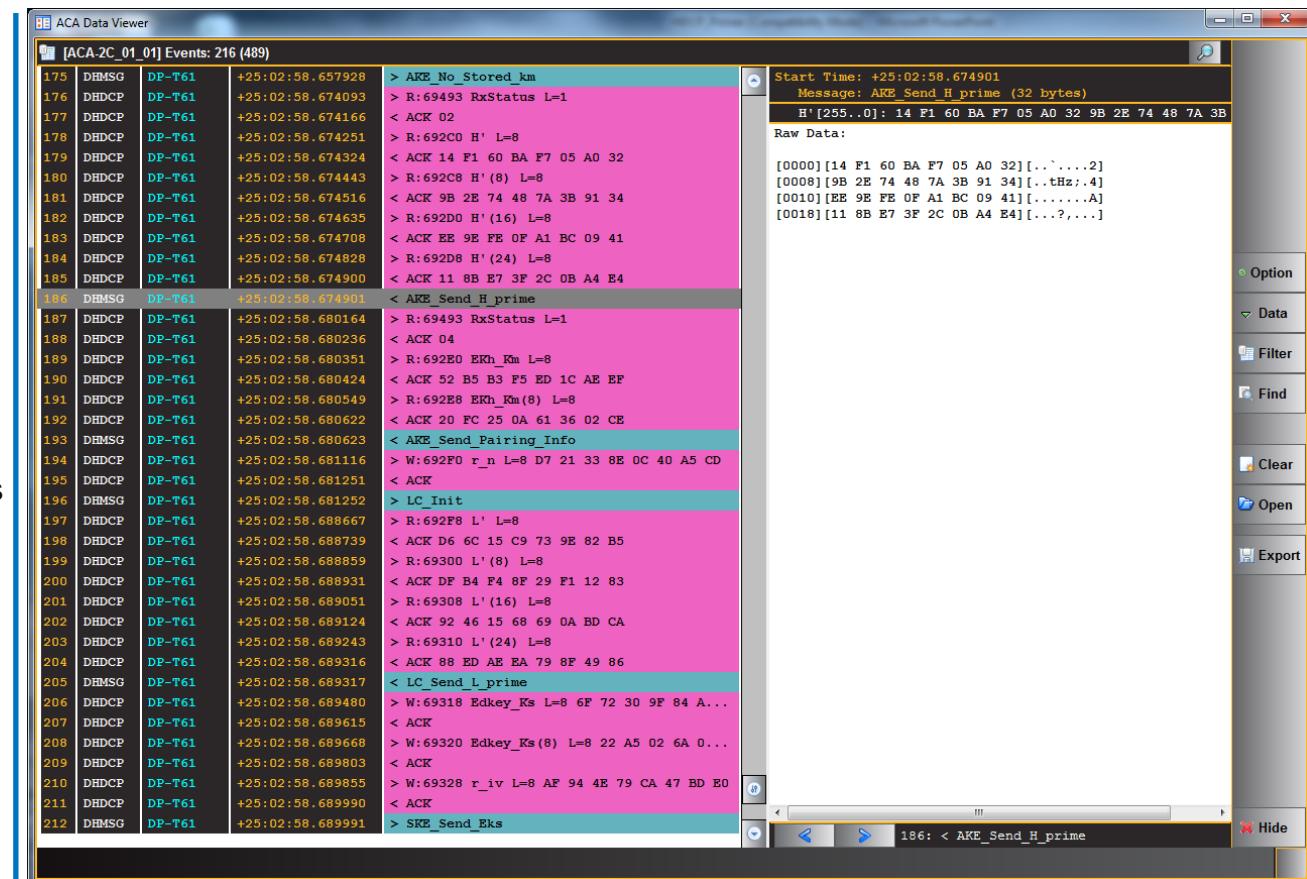
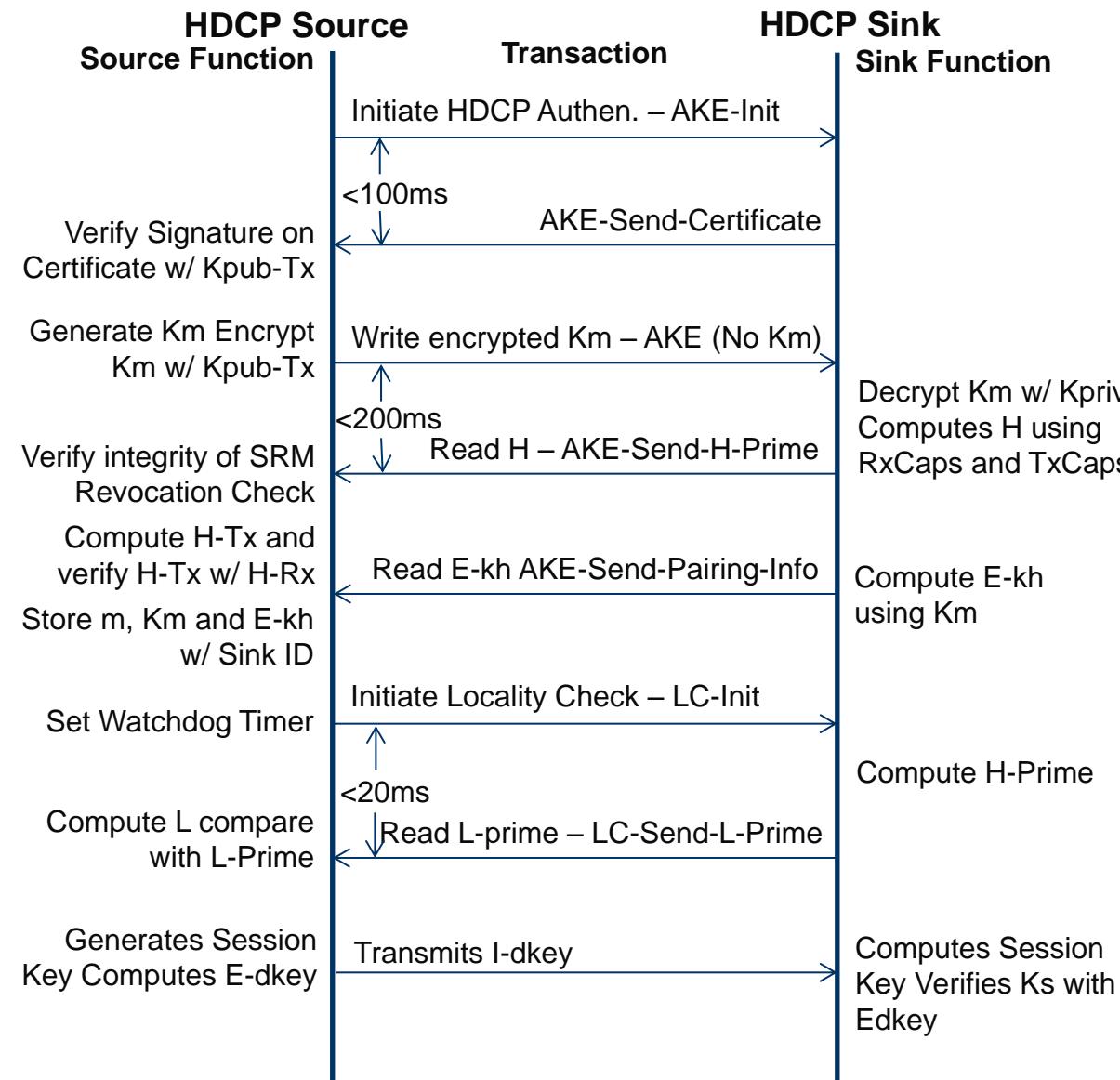
[00203][00 84 00 00 00 00 00 00]

# DisplayPort Connection Sequence HDCP 2.2 Authentication

Webinar – April– 2018



# HDCP 2.2 Authentication Transactions



- Shows transactions associated with Source sending Master Key, Sink sending H-prime and Pairing information, Source initiating Locality Check, Sink sending L-prime to verify locality check and Source sending Session Key.

# HDCP 2.2 Compliance Test – Test Results Viewer

Compliance Test Results Viewer

DP HDCP 2.2 TX (1.0) Compliance Test Results

Results Name: DP\_HDCP\_22\_Source\_Comp\_1      Manufacturer: ACME  
Date Tested: April 5, 2017 6:25 PM      Model Name: XYZ  
Overall Status: CTS 1.0 - Pass      Port Tested: 1

[HTML Report](#)

Test Results

Test Name / Details	Status
1A-01: Regular Procedure: With previously connected Receiver (With stored Km)	Pass
1A-02: Regular Procedure: With newly connected Receiver (Without stored Km)	Pass
1A-03: Regular Procedure: Receiver disconnect after AKE Init	Pass
1A-04: Regular Procedure: Receiver disconnect after Km	Pass
1A-05: Regular Procedure: Receiver disconnect after locality check	Pass
1A-06: Regular Procedure: Receiver disconnect after Ks	Pass
1A-07: Regular Procedure: Receiver sends REAUTH REQ after Ks	Pass
1A-08: Irregular Procedure: Verify Receiver Certificate	Pass
1A-10: Irregular Procedure: Invalid H'	Pass
1A-11: Irregular Procedure: Pairing Failure	Pass
1A-12: Irregular Procedure: Locality Failure	Pass

1A-01: Regular Procedure: With previously connected Receiver (With stored Km)

Instrument: SP\_980 [10.30.196.14]      Continue Test Execution      Close

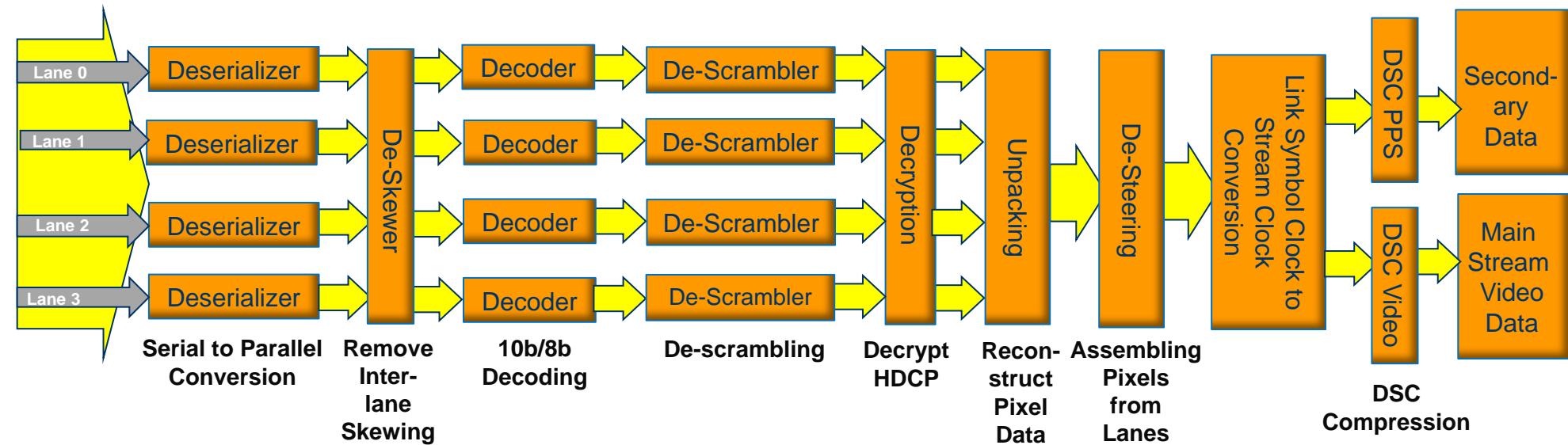


# DisplayPort Main Link Protocol

Webinar – April– 2018



# DisplayPort Main Link Stream Generation in Sink (980 Receiver w/o DSC/FEC)

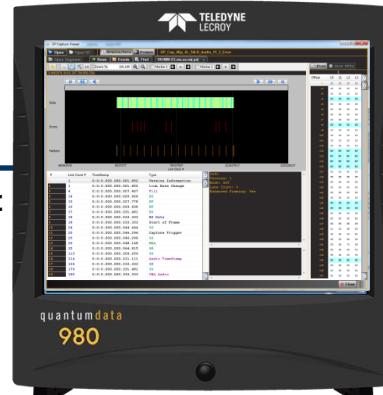


- Two types of link symbols:
  - Data symbols (e.g. pixel, metadata)
  - Control symbols (K-Chars) to frame the data symbols.
- Pixel Steering – The process of mapping the pixel data to each of the 2 or 4 lanes.
- Framing, Packing, Stuffing – Adding control symbols and creating Transfer Units.
- Encryption – HDCP.
- Inter-Lane Skewing – Offset the link symbols (by 2 link clocks) for each lane. **Reduces susceptibility to external noise pulses** that could corrupt critical data across all lanes.

DisplayPort Source



DisplayPort Cable



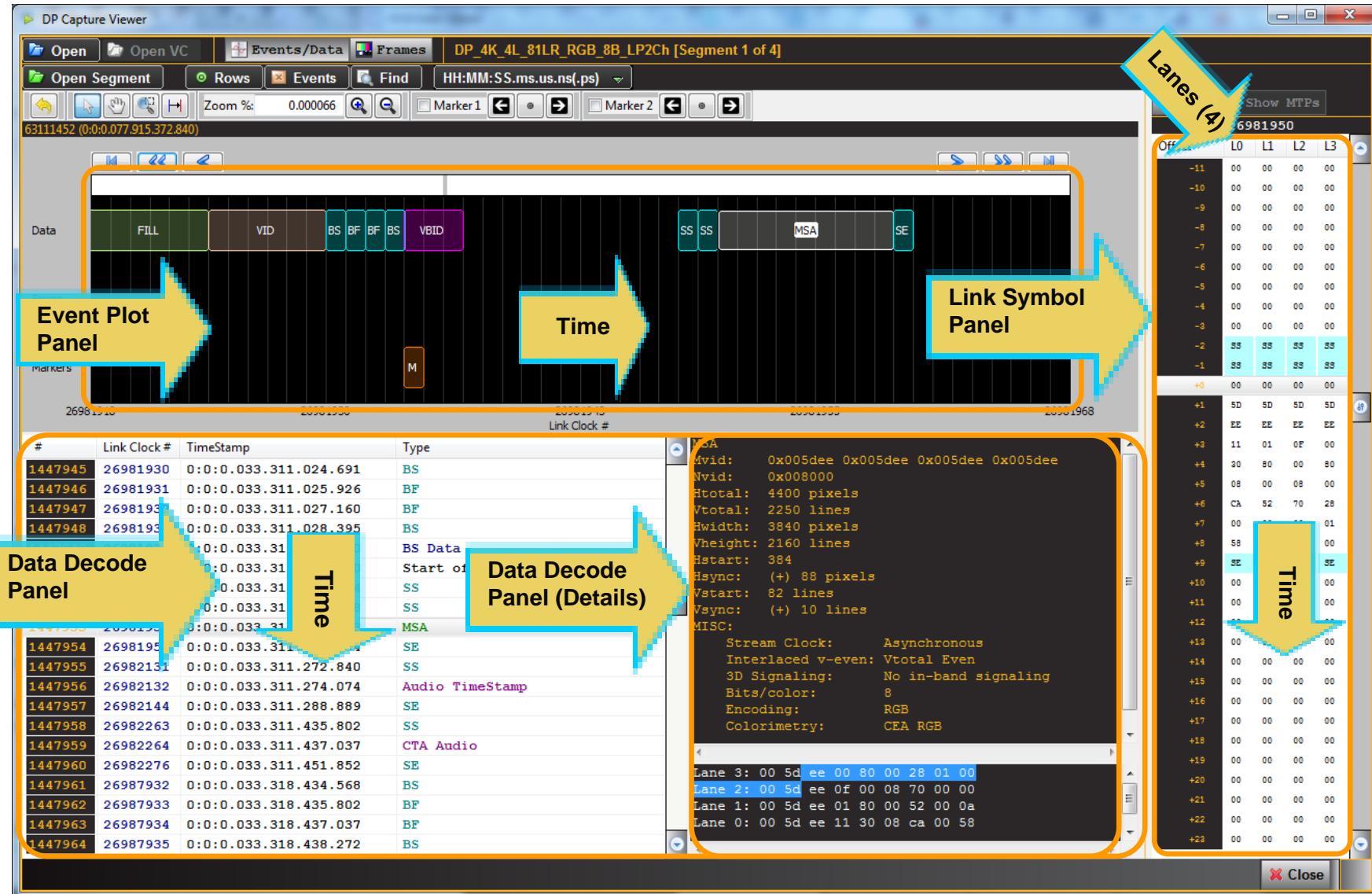
DisplayPort Receiver

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# **DisplayPort**

# **Main Link View - 980 Capture Viewer**

# DisplayPort Capture Viewer



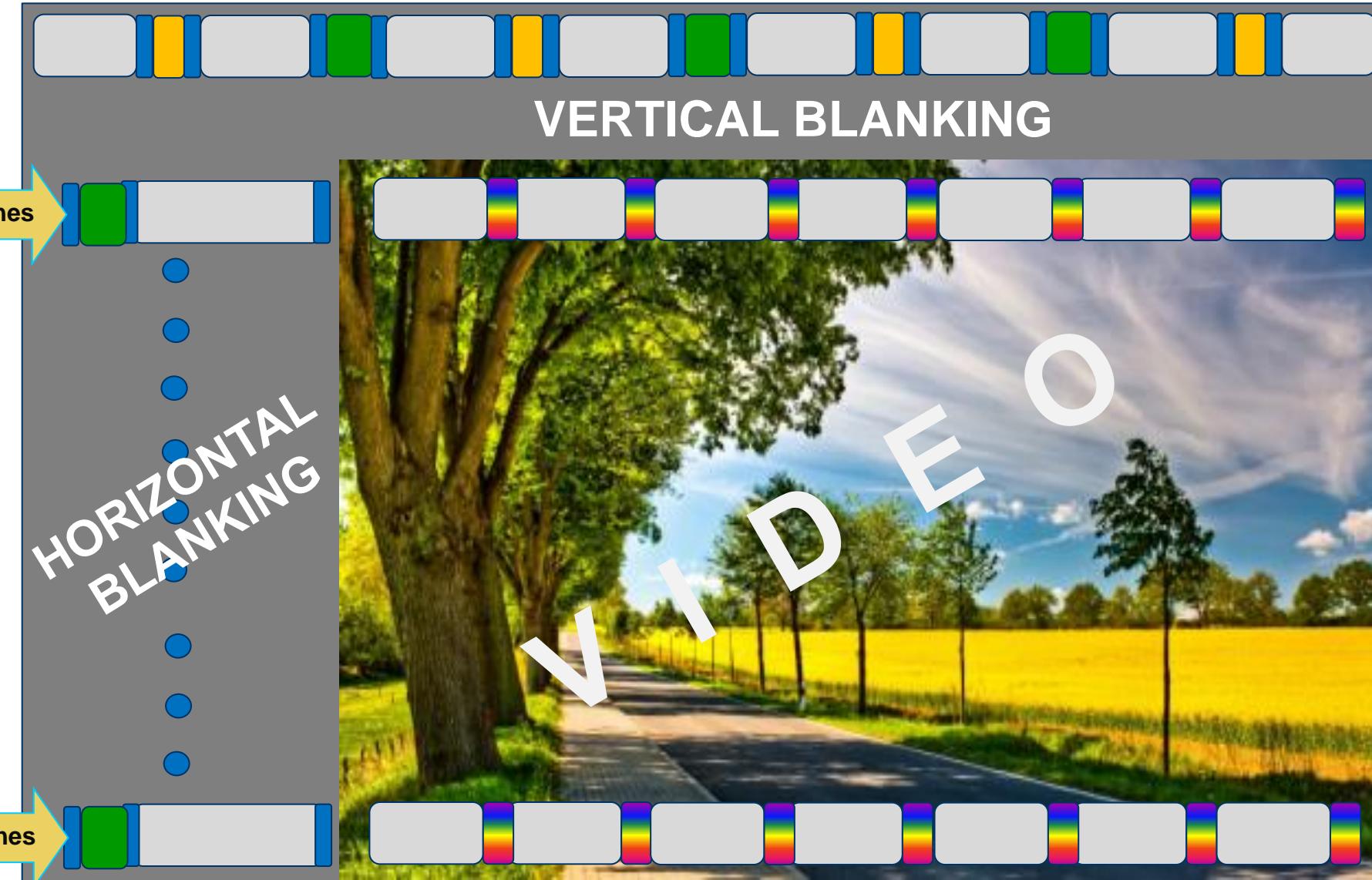
- There are 3 separate panels in the Capture Viewer: 1) Event Plot, 2) Data Decode, 3) Link Symbol panel (all lanes).
- The panels are all in sync with one another.
- Transaction details are shown in Data Decode Details panel.
- Event time is left to right (or top to bottom on the Link Symbol Panel).
- You can search for events and specific control characters.
- You can filter the list to gain a specific view of any one event type or set of event types.

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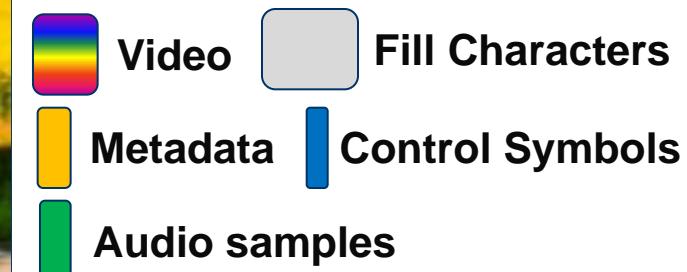
# **Main Link Framing Protocol Symbols**

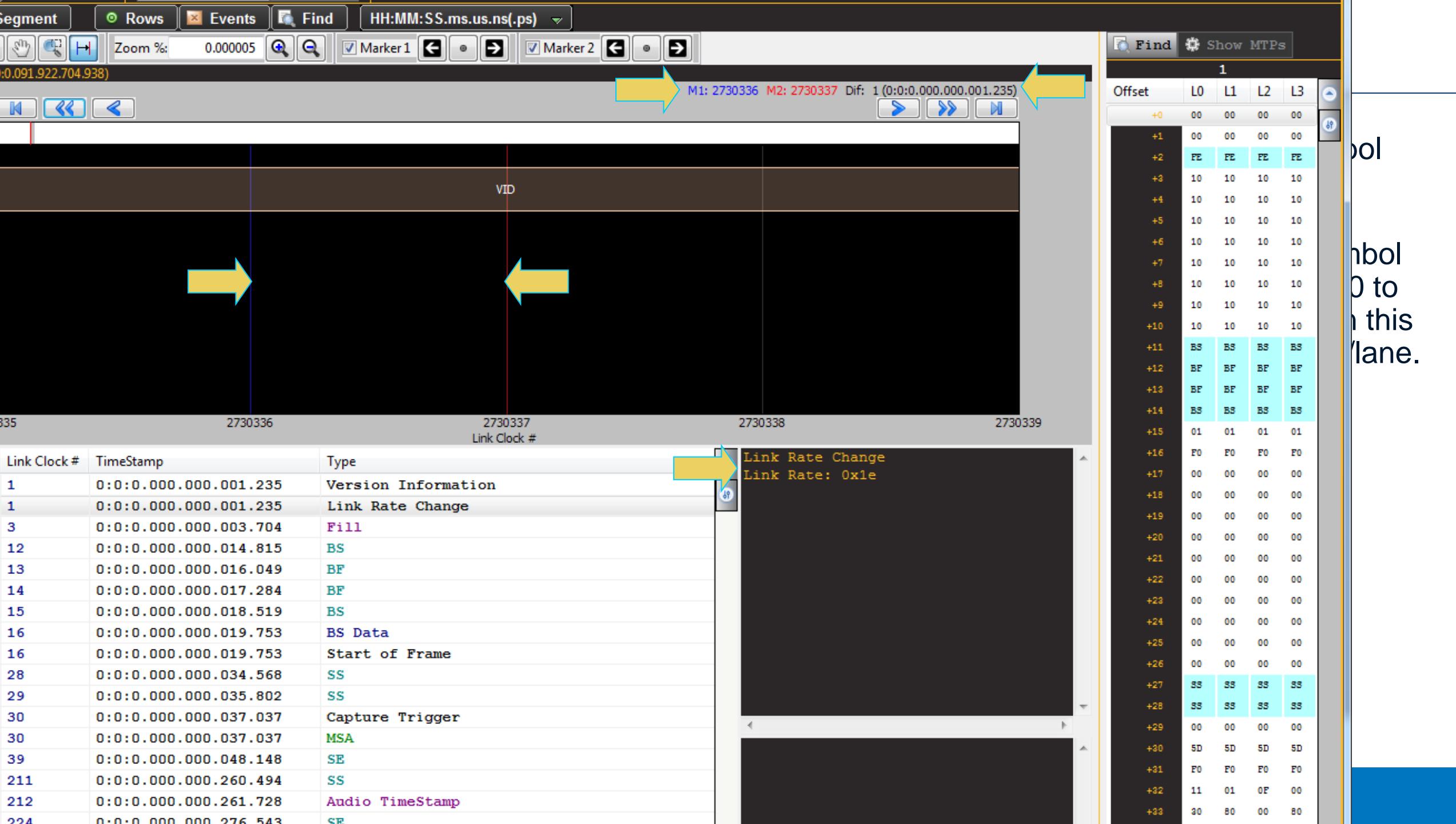
## **8.1Gbps Link Rate**

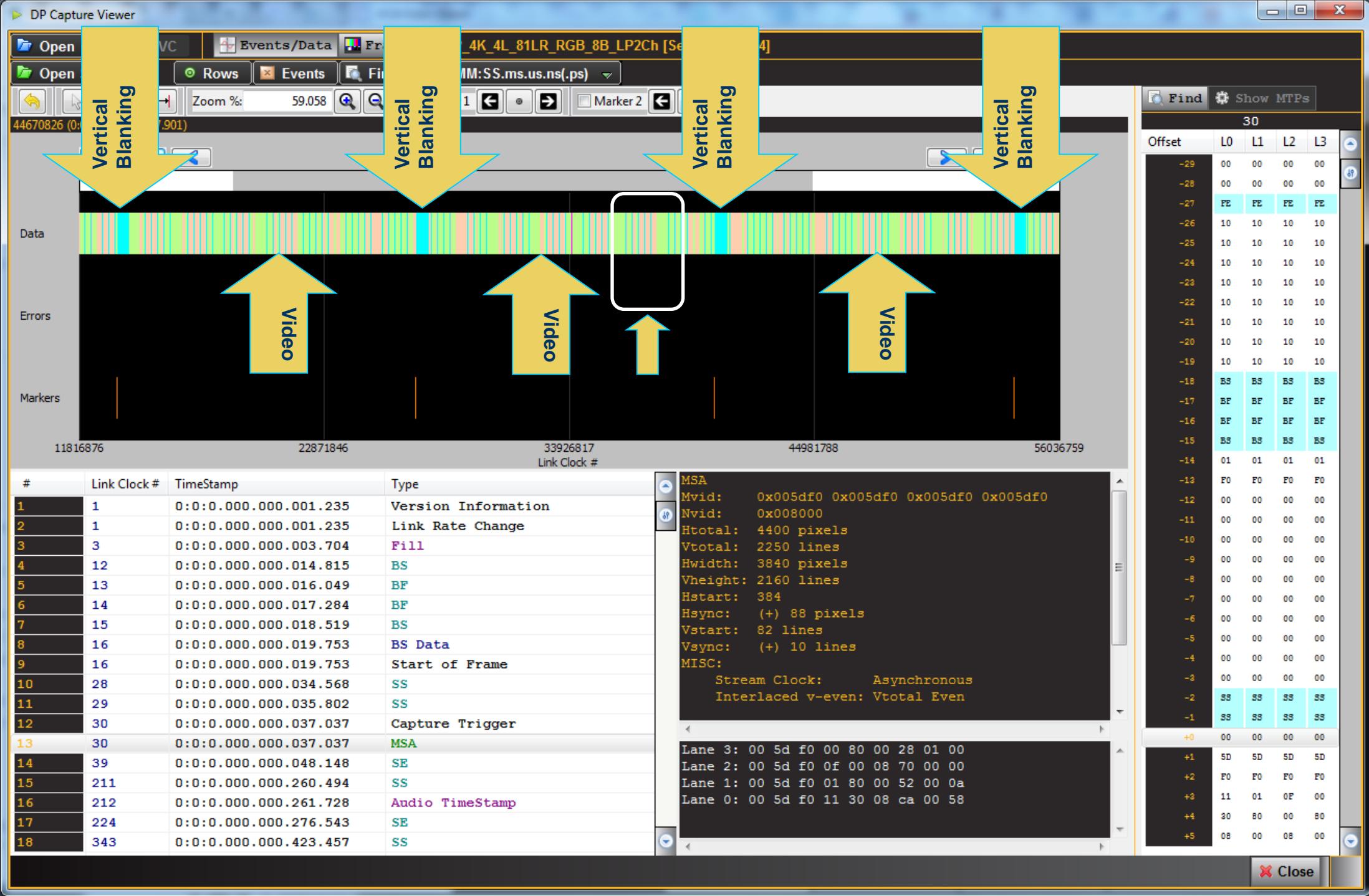
# DisplayPort Main Link Protocol – One Video Frame



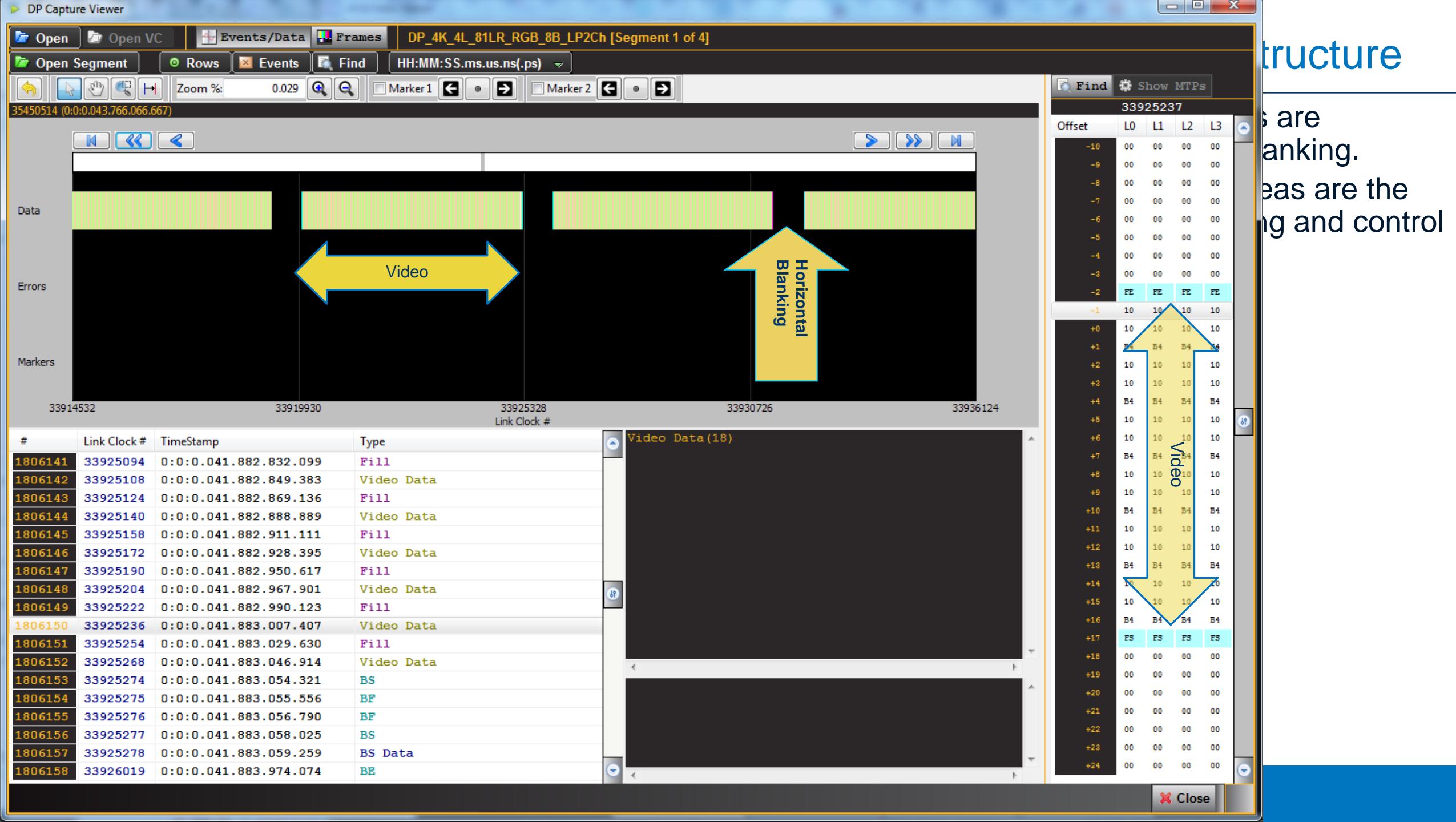
- Video packets occur during the active video period.
- Metadata: Main Stream Attributes (MSA) and Secondary Data Packets (SDP) occur during the vertical blanking period and are identified with Framing control characters.
- Fill characters are zeros for filling up (stuffing) the unused link symbols.

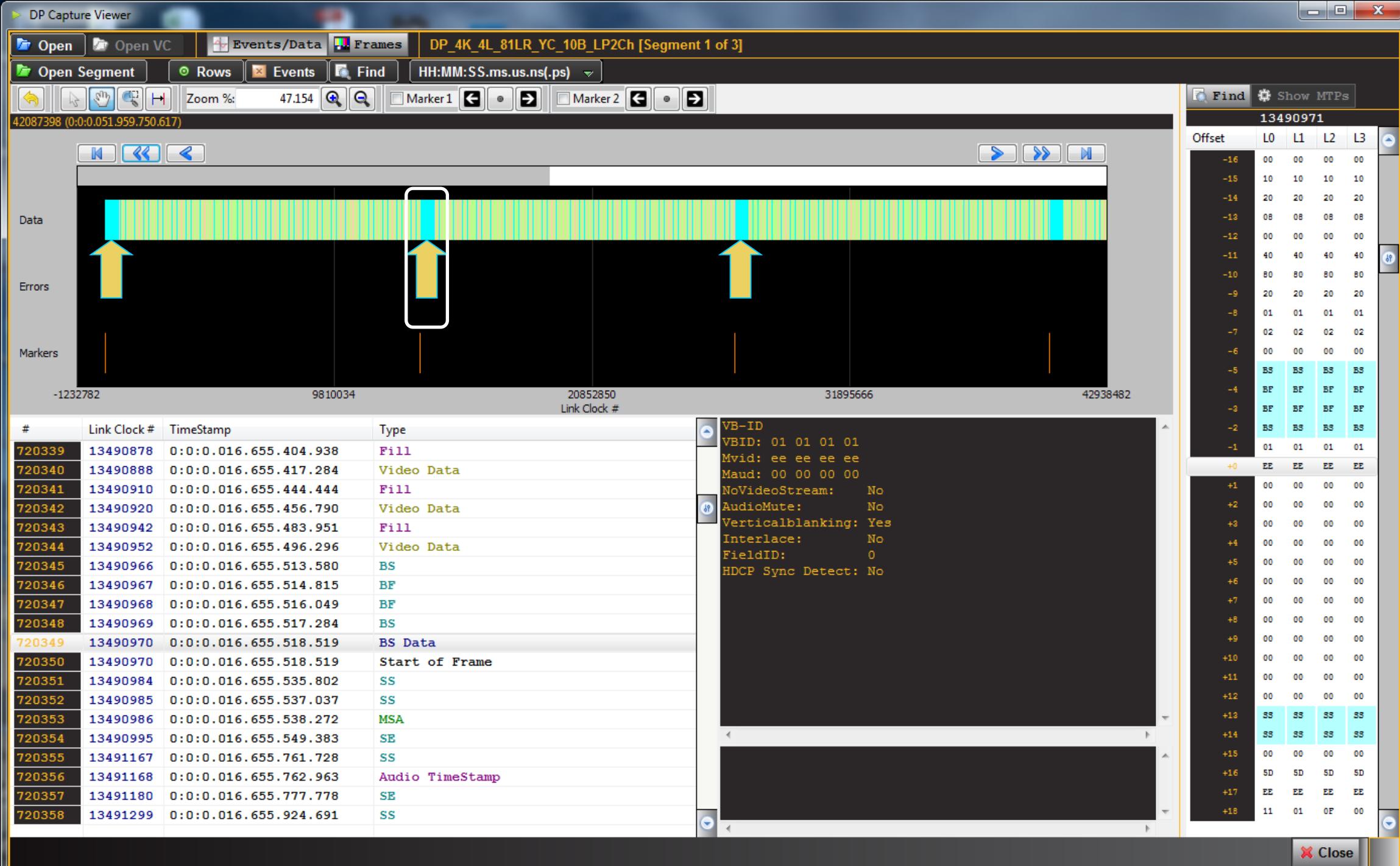




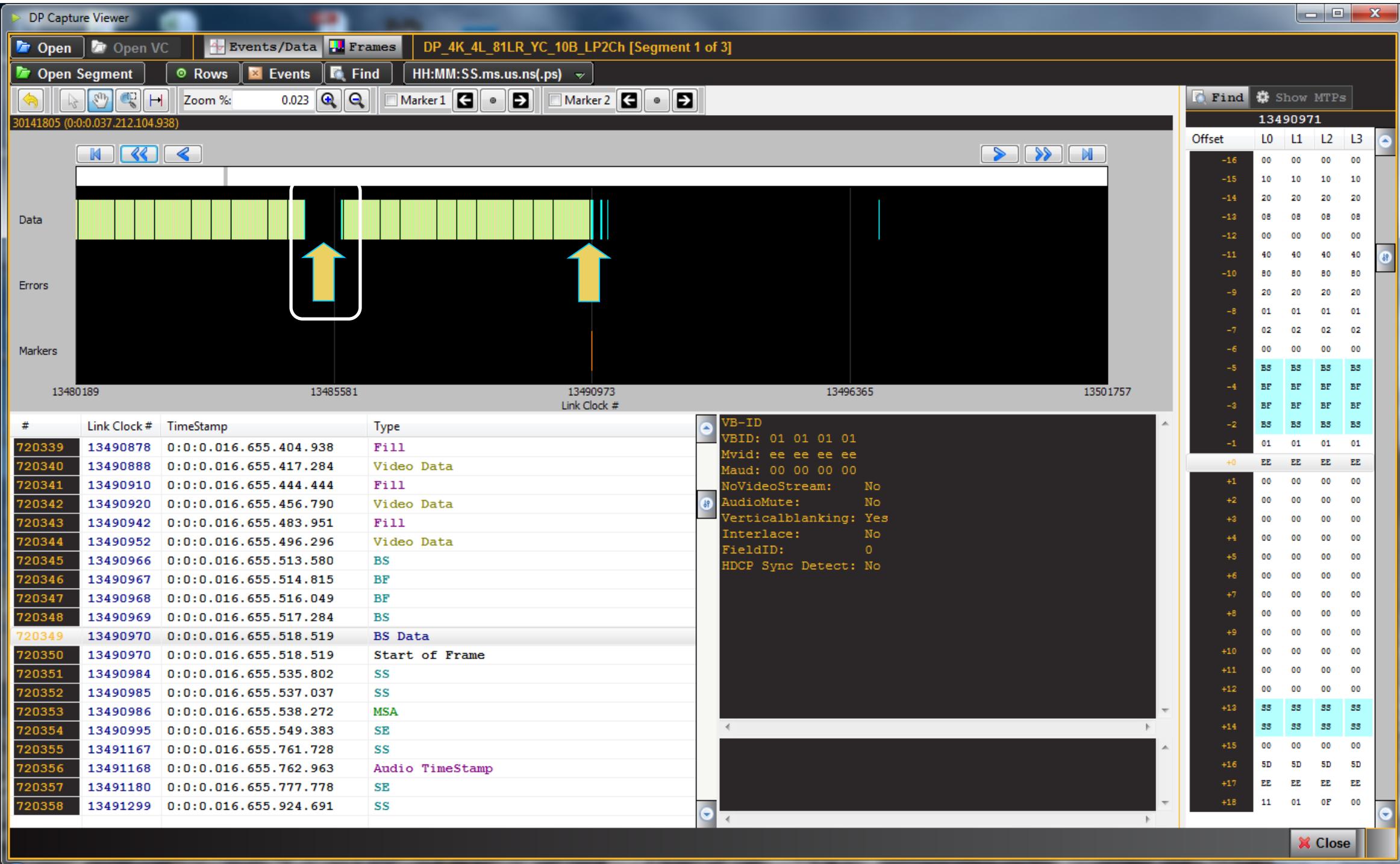


Picture  
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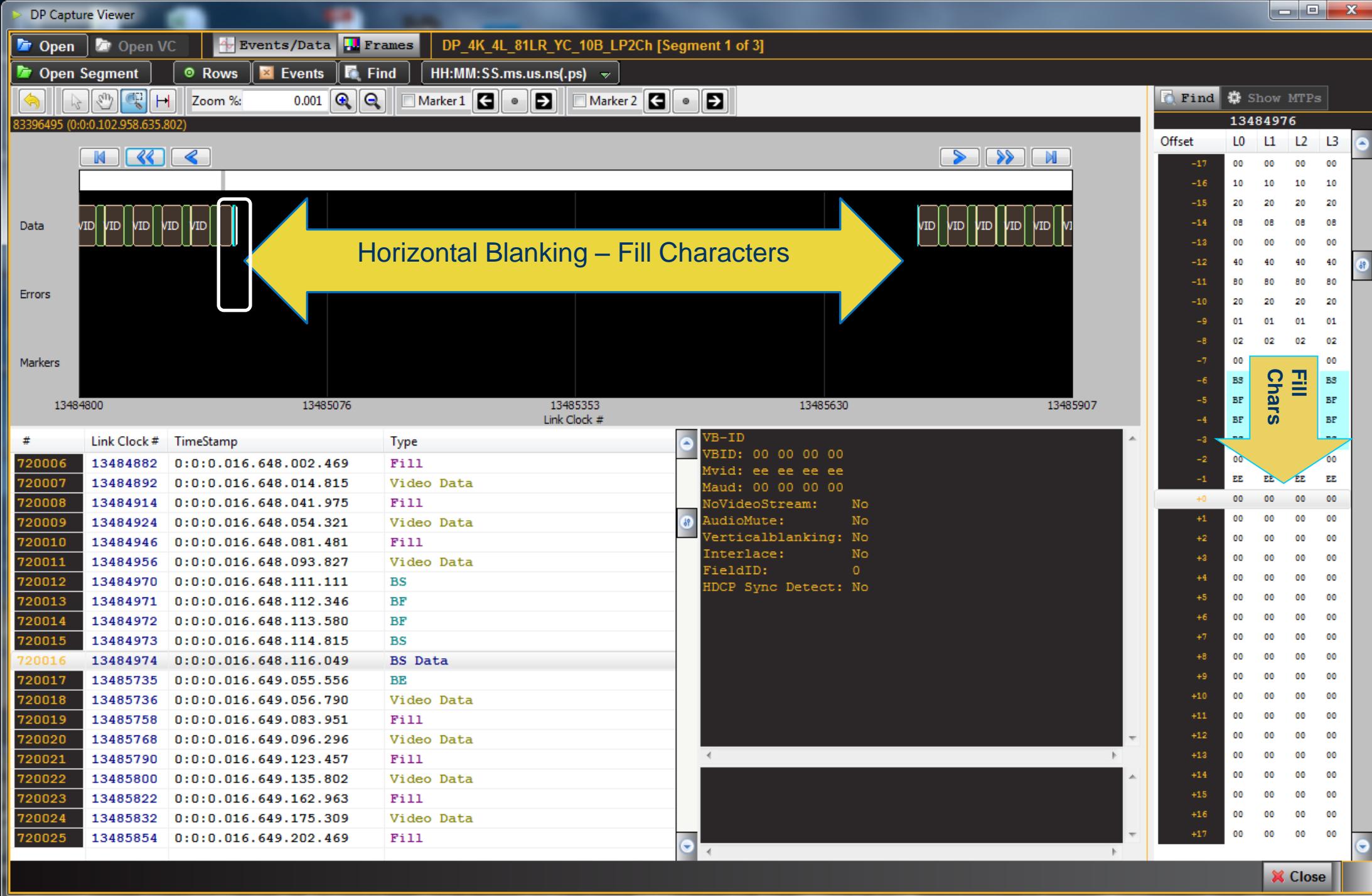




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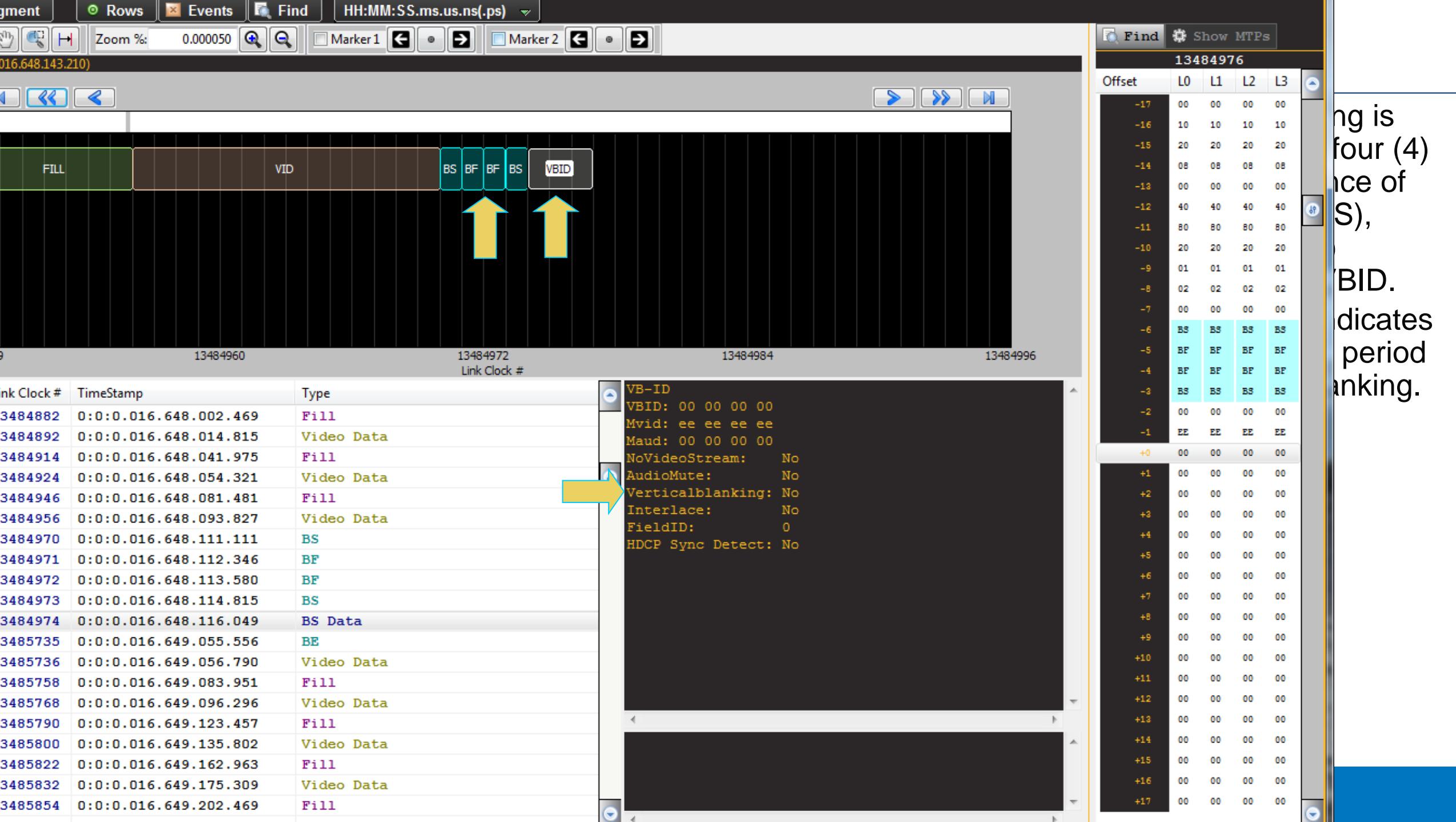


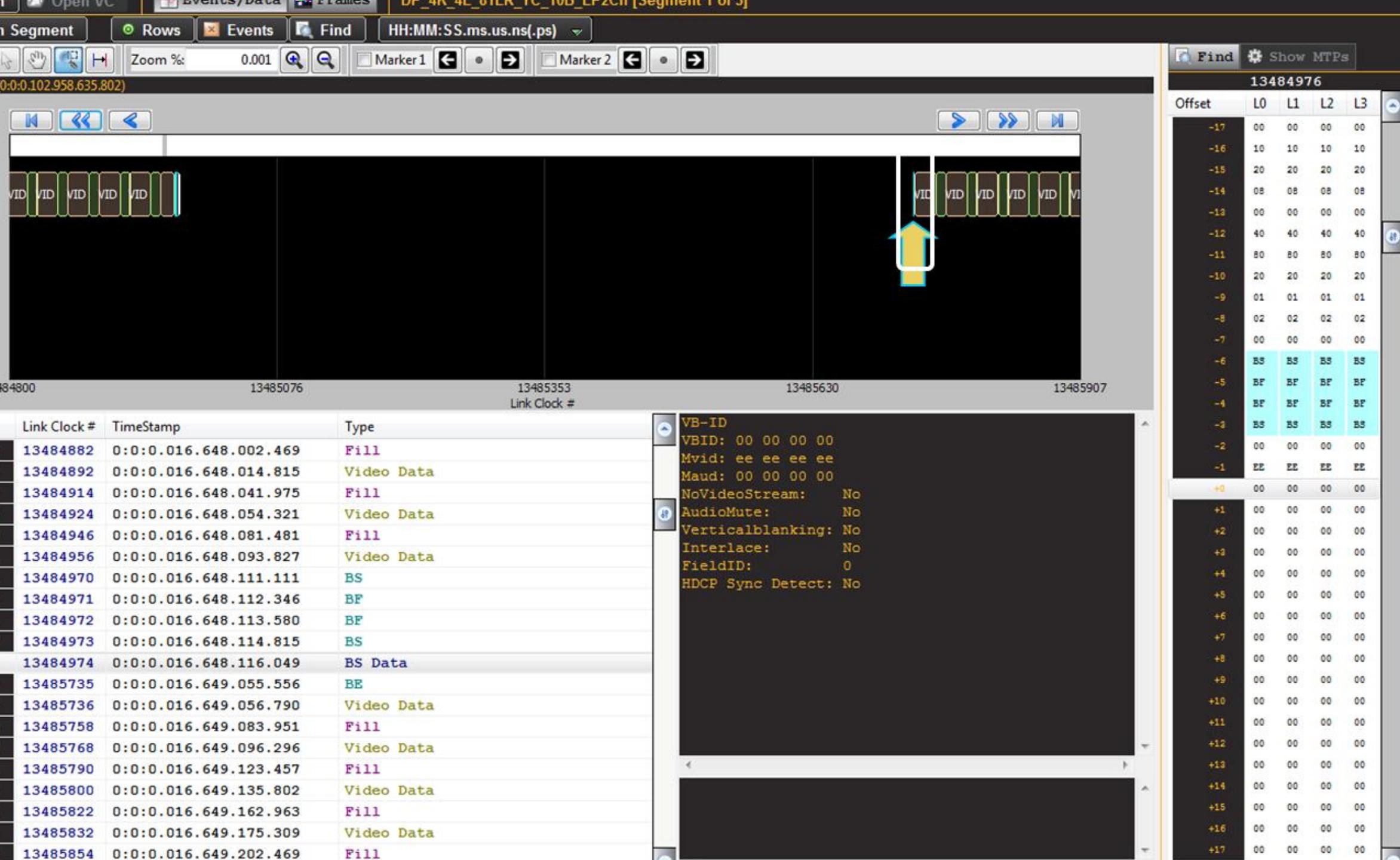
video  
beginning  
g.  
g

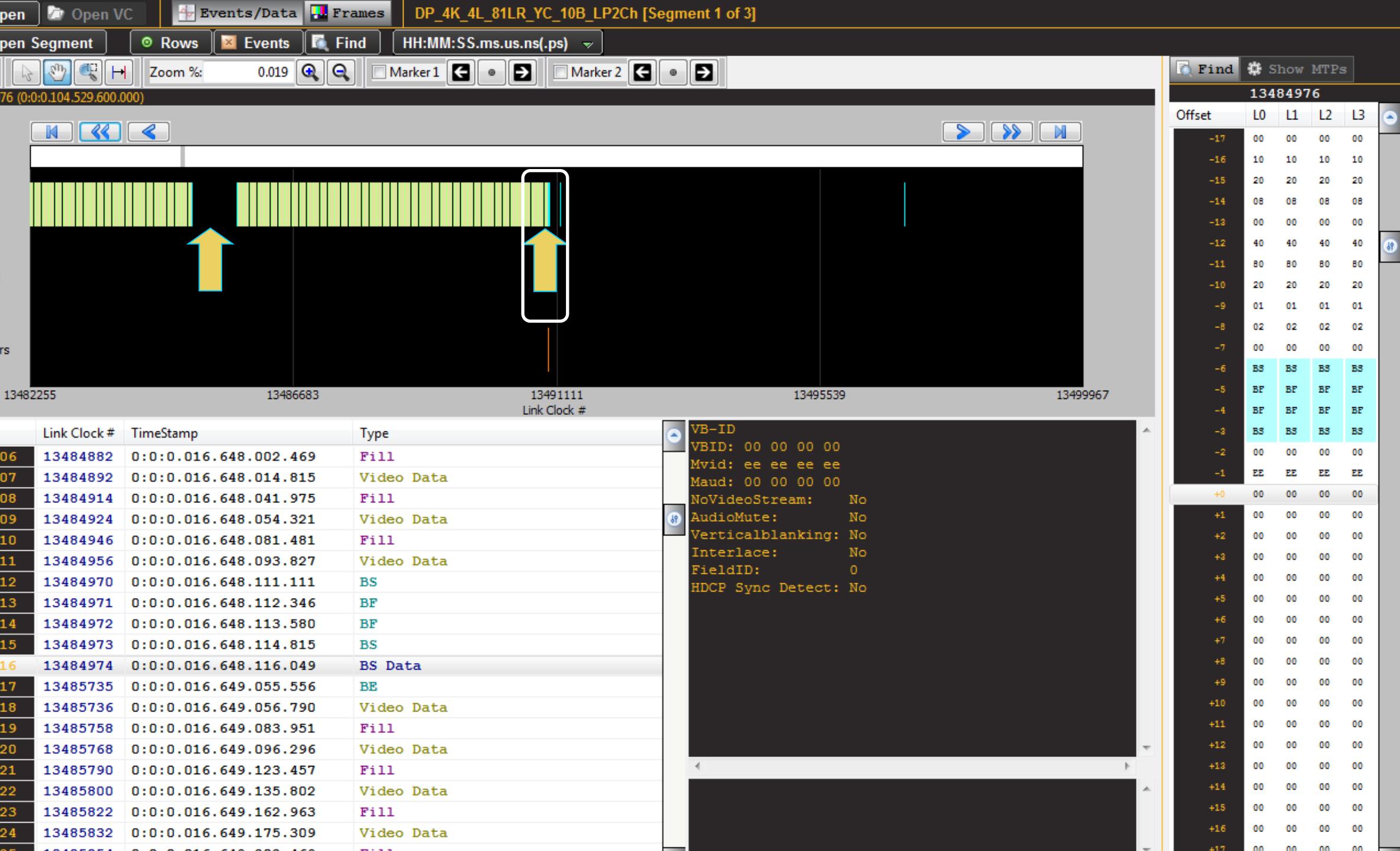


planking is fill

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d on the Link  
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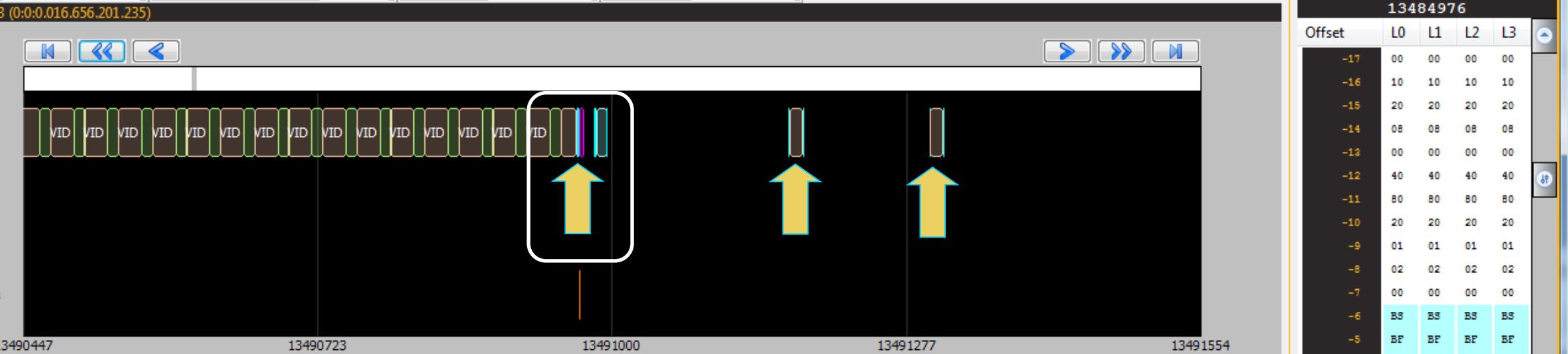






en Segment Rows Events Find HH:MM:SS.ms.us.ns(ps)

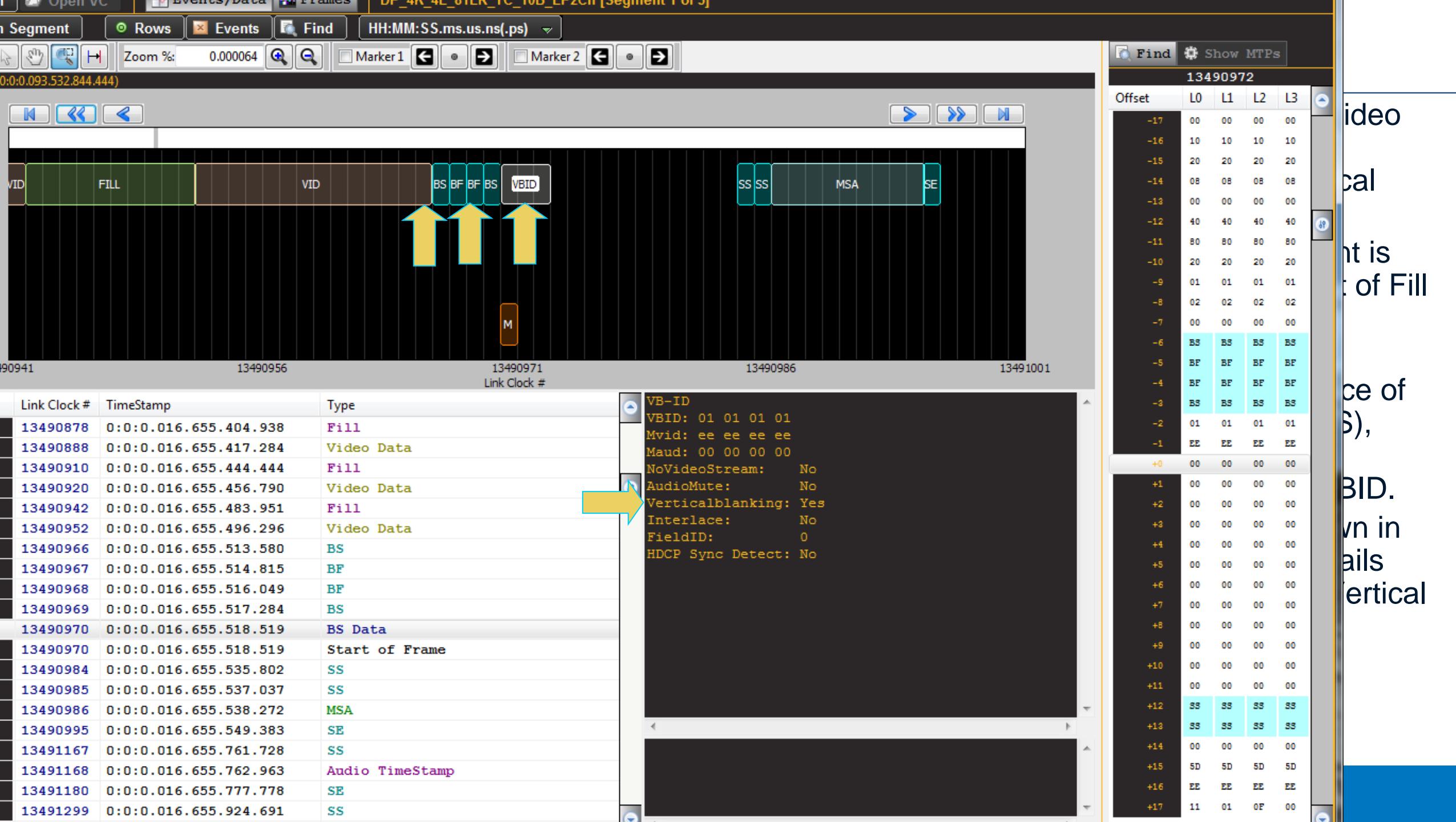
Zoom % 0.001 Find Marker 1 Marker 2



VB-ID  
VBID: 00 00 00 00  
Mvid: ee ee ee ee  
Maud: 00 00 00 00  
NoVideoStream: No  
AudioMute: No  
Verticalblanking: No  
Interlace: No  
FieldID: 0  
HDCP Sync Detect: No

Offset	L0	L1	L2	L3
-17	00	00	00	00
-16	10	10	10	10
-15	20	20	20	20
-14	08	08	08	08
-13	00	00	00	00
-12	40	40	40	40
-11	80	80	80	80
-10	20	20	20	20
-9	01	01	01	01
-8	02	02	02	02
-7	00	00	00	00
-6	BS	BS	BS	BS
-5	BF	BF	BF	BF
-4	BF	BF	BF	BF
-3	BS	BS	BS	BS
-2	00	00	00	00
-1	EE	EE	EE	EE
+0	00	00	00	00
+1	00	00	00	00
+2	00	00	00	00
+3	00	00	00	00
+4	00	00	00	00
+5	00	00	00	00
+6	00	00	00	00
+7	00	00	00	00
+8	00	00	00	00
+9	00	00	00	00
+10	00	00	00	00
+11	00	00	00	00
+12	00	00	00	00
+13	00	00	00	00
+14	00	00	00	00
+15	00	00	00	00
+16	00	00	00	00
+17	00	00	00	00

video  
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sible as  
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vertical



Open VC Events/Data Frames DP\_4K\_4L\_81LR\_YC\_10B\_LP2Ch [Segment 1 of 3]

en Segment Rows Events Find HH:MM:SS.ms.us.ns(ps)

Zoom %: 0.000076 Marker 1 Marker 2

2 (0:0:073.003.743.210)

**VID** BSBFBFBS VBID SSSS MSA SE

3490947 13490964 13490982 Link Clock # 13491000 13491018

Link Clock #	TimeStamp	Type
3	13490942	Fill
4	13490952	Video Data
5	13490966	BS
6	13490967	BF
7	13490968	BF
8	13490969	BS
9	13490970	BS Data
0	13490970	Start of Frame
1	13490984	SS
2	13490985	SS
3	13490986	MSA
4	13490995	SE
5	13491167	SS
6	13491168	Audio TimeStamp
7	13491180	SE
8	13491299	SS
9	13491300	CTA Audio
0	13491312	SE
1	13496968	BS
2	13496969	BF

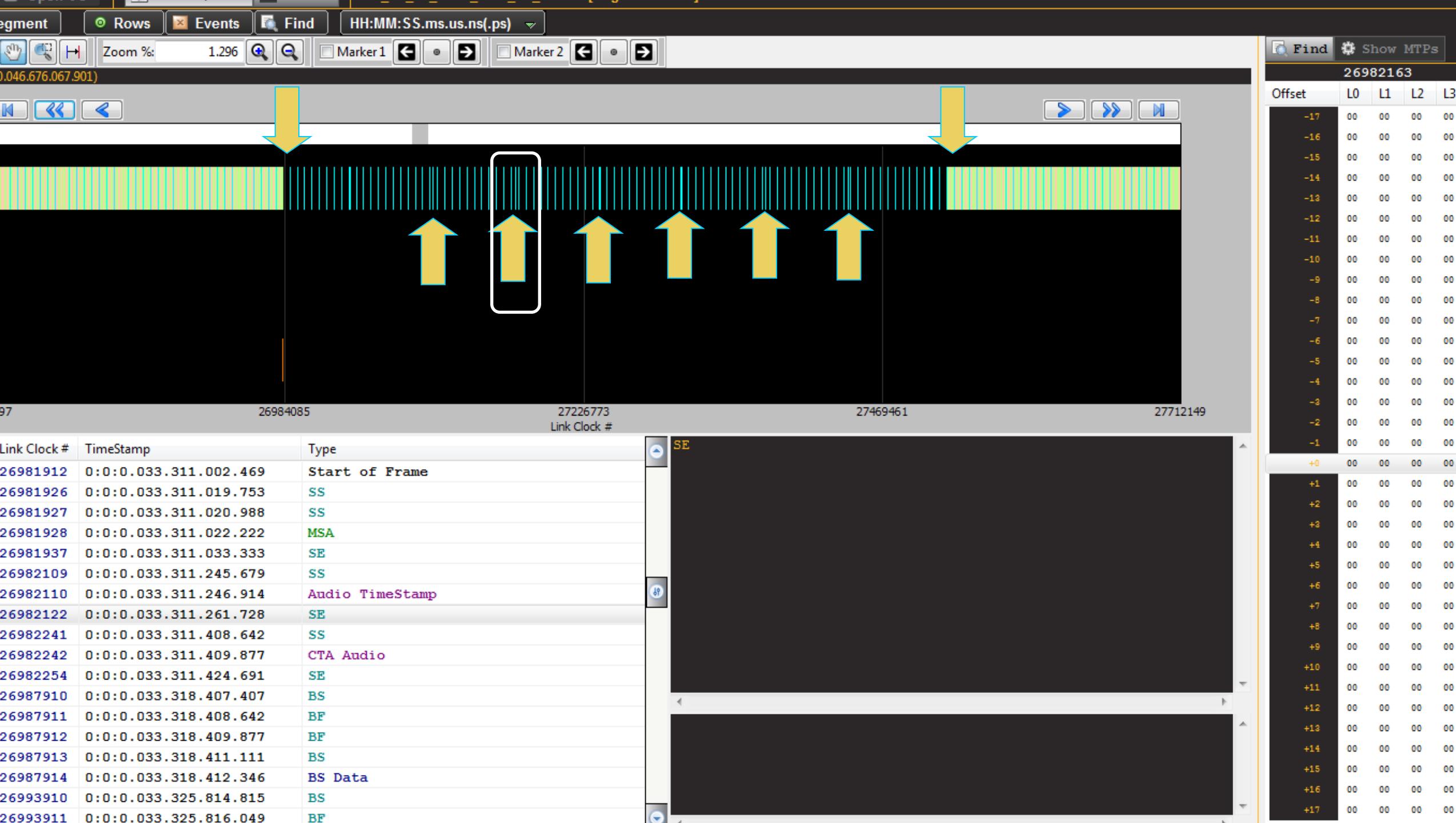
**MSA**

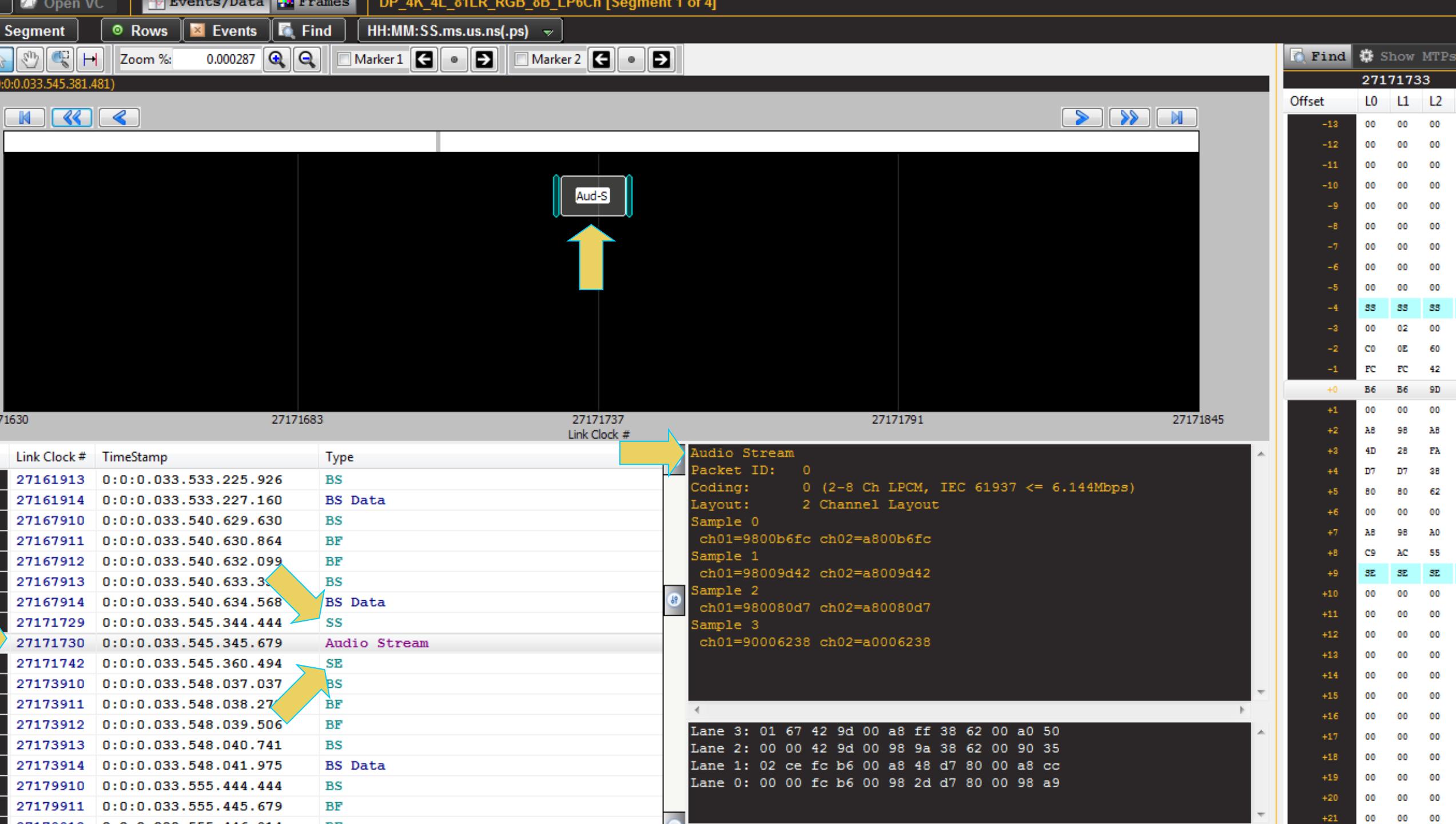
Mvid: 0x005dee 0x005dee 0x005dee 0x005dee  
 Nvid: 0x008000  
 Htotal: 4400 pixels  
 Vtotal: 2250 lines  
 Hwidth: 3840 pixels  
 Vheight: 2160 lines  
 Hstart: 384  
 Hsync: (+) 88 pixels  
 Vstart: 82 lines  
 Vsync: (+) 10 lines  
 MISC:  
 Stream Clock: Asynchronous  
 Interlaced v-even: Vtotal Even  
 3D Signaling: No in-band signaling  
 Bits/color: 10  
 Encoding: Y444  
 Colorimetry: YCbCr BT709

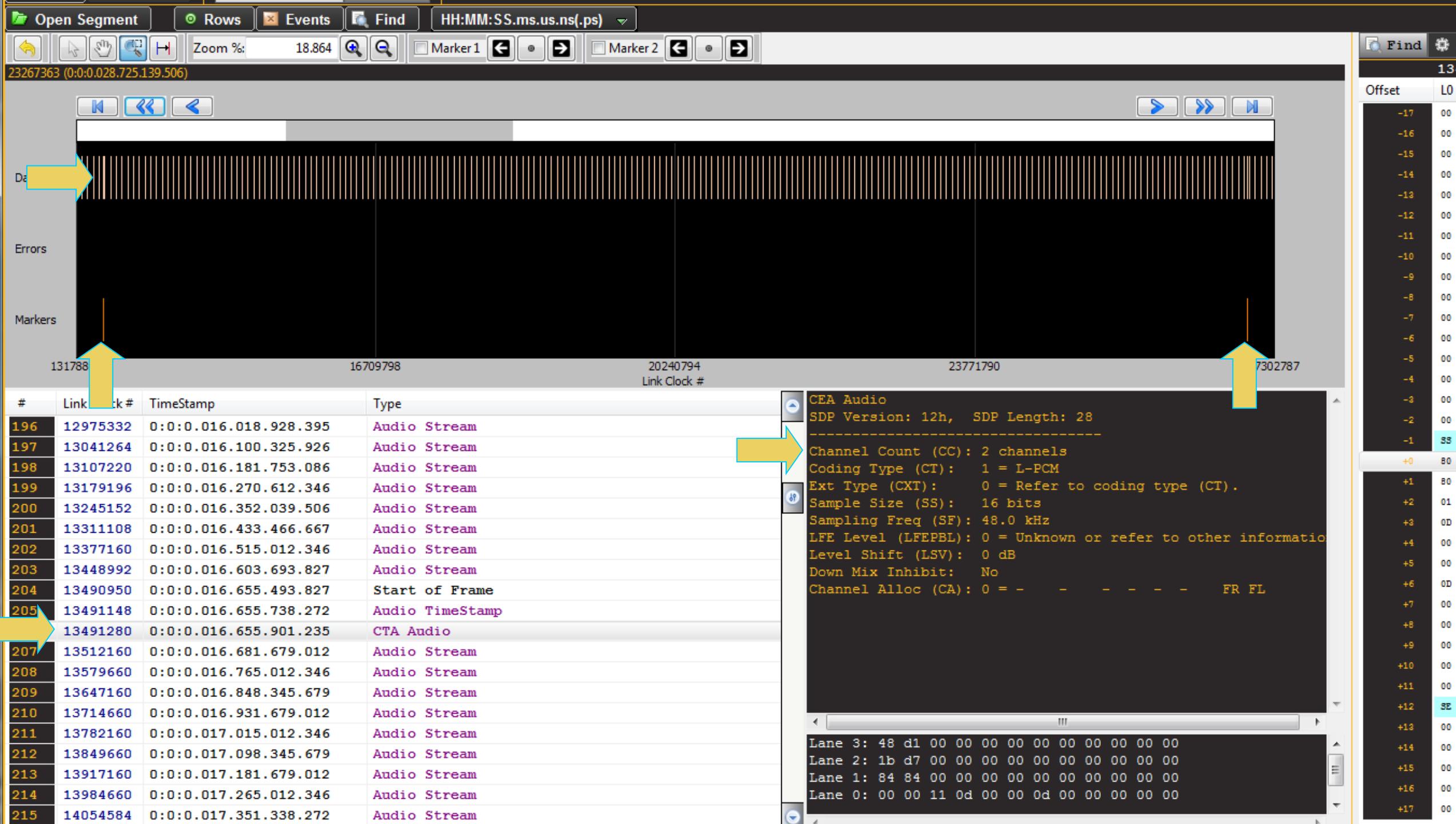
Lane 3: 00 5d ee 00 80 00 5c 01 00  
 Lane 2: 00 5d ee 0f 00 08 70 00 00  
 Lane 1: 00 5d ee 01 80 00 52 00 0a  
 Lane 0: 00 5d ee 11 30 08 ca 00 58

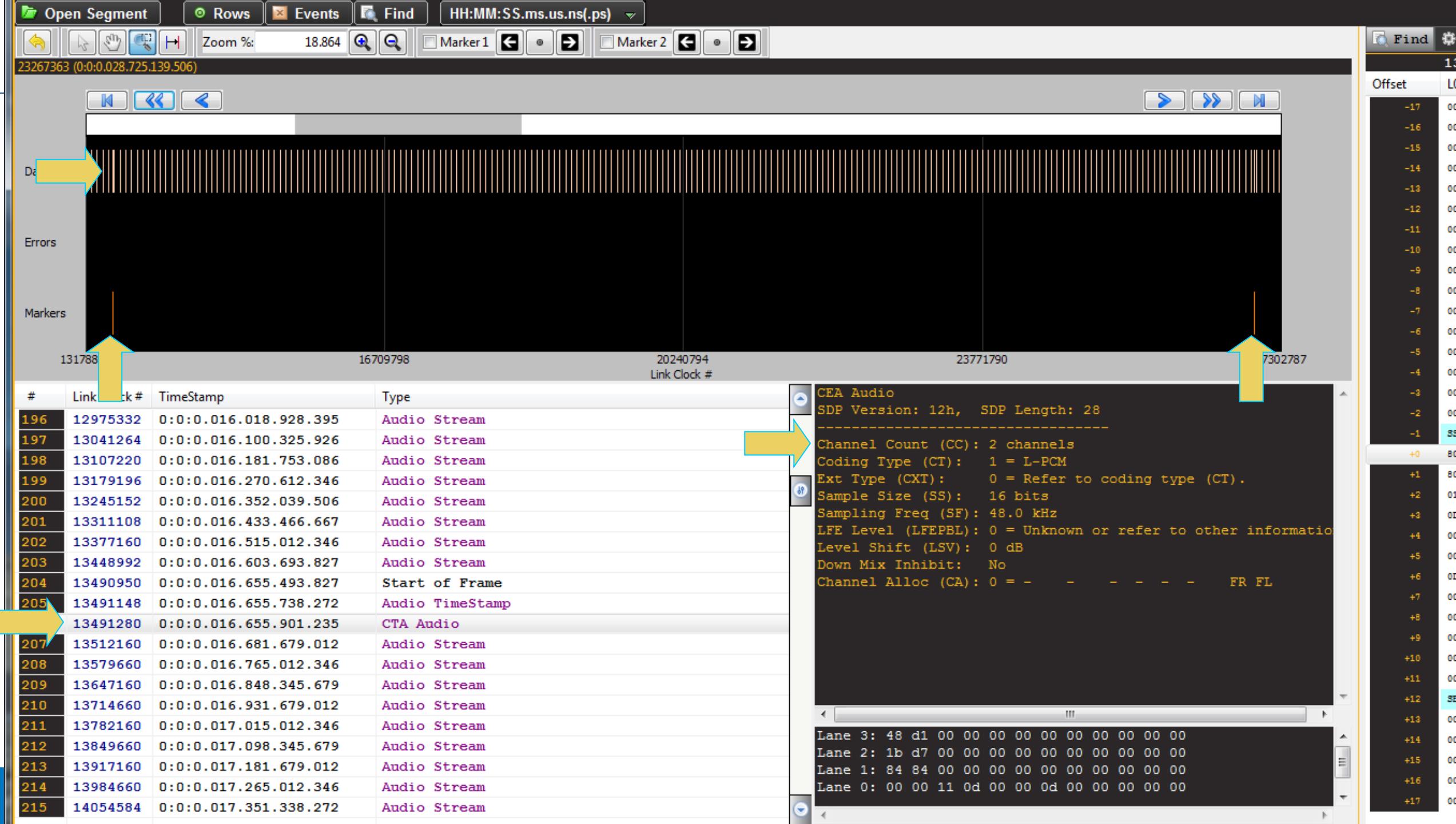
Find Show MTPs 13490986

Offset	L0	L1	L2	L3
-17	BS	BS	BS	BS
-16	01	01	01	01
-15	EE	EE	EE	EE
-14	00	00	00	00
-13	00	00	00	00
-12	00	00	00	00
-11	00	00	00	00
-10	00	00	00	00
-9	00	00	00	00
-8	00	00	00	00
-7	00	00	00	00
-6	00	00	00	00
-5	00	00	00	00
-4	00	00	00	00
-3	00	00	00	00
-2	SS	SS	SS	SS
-1	SS	SS	SS	SS
+0	00	00	00	00
+1	5D	5D	5D	5D
+2	EE	EE	EE	EE
+3	11	01	0F	00
+4	30	80	00	80
+5	08	00	08	00
+6	CA	52	70	5C
+7	00	00	00	01
+8	58	0A	00	00
+9	SE	SE	SE	SE
+10	00	00	00	00
+11	00	00	00	00
+12	00	00	00	00
+13	00	00	00	00
+14	00	00	00	00
+15	00	00	00	00
+16	00	00	00	00
+17	00	00	00	00

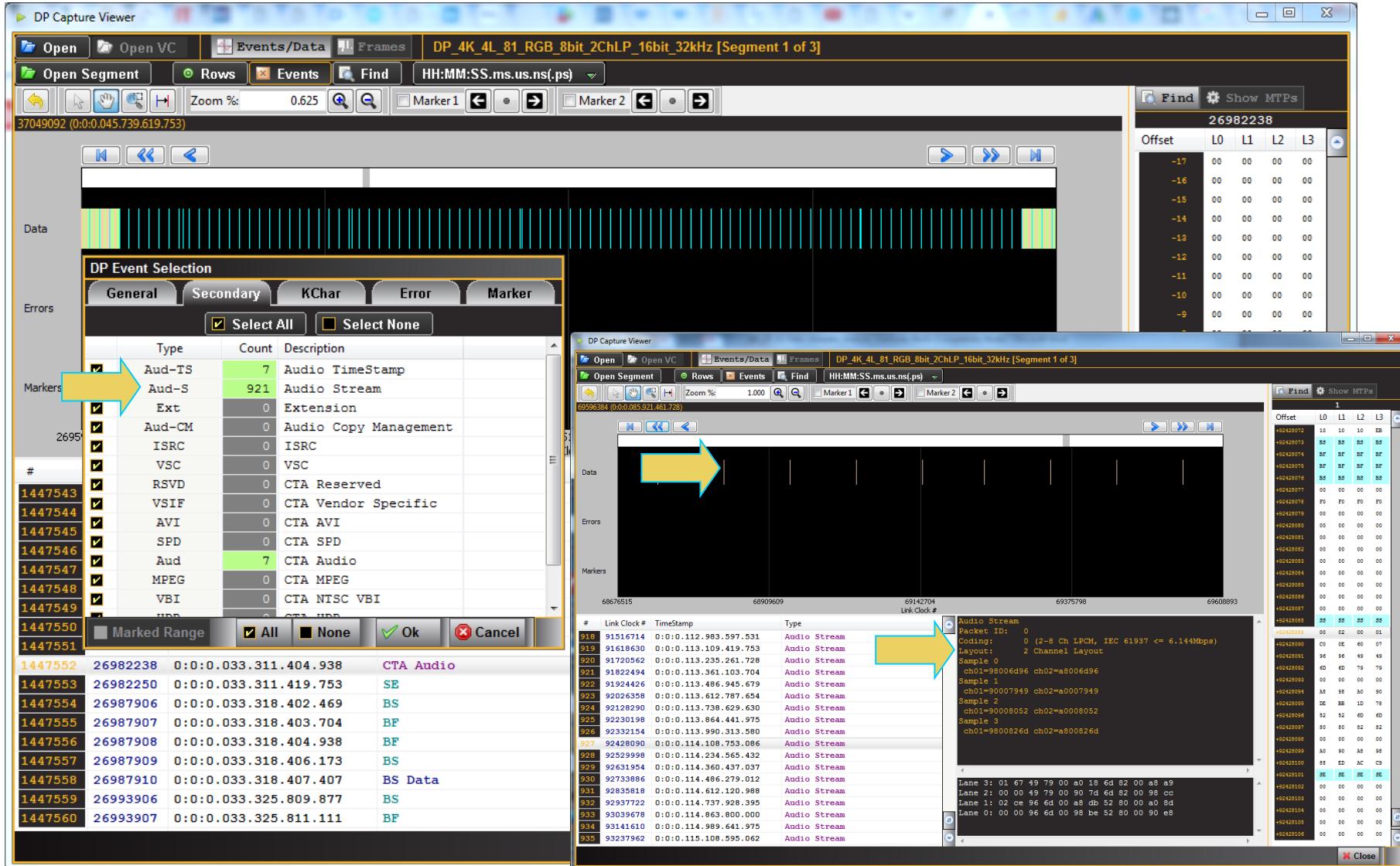






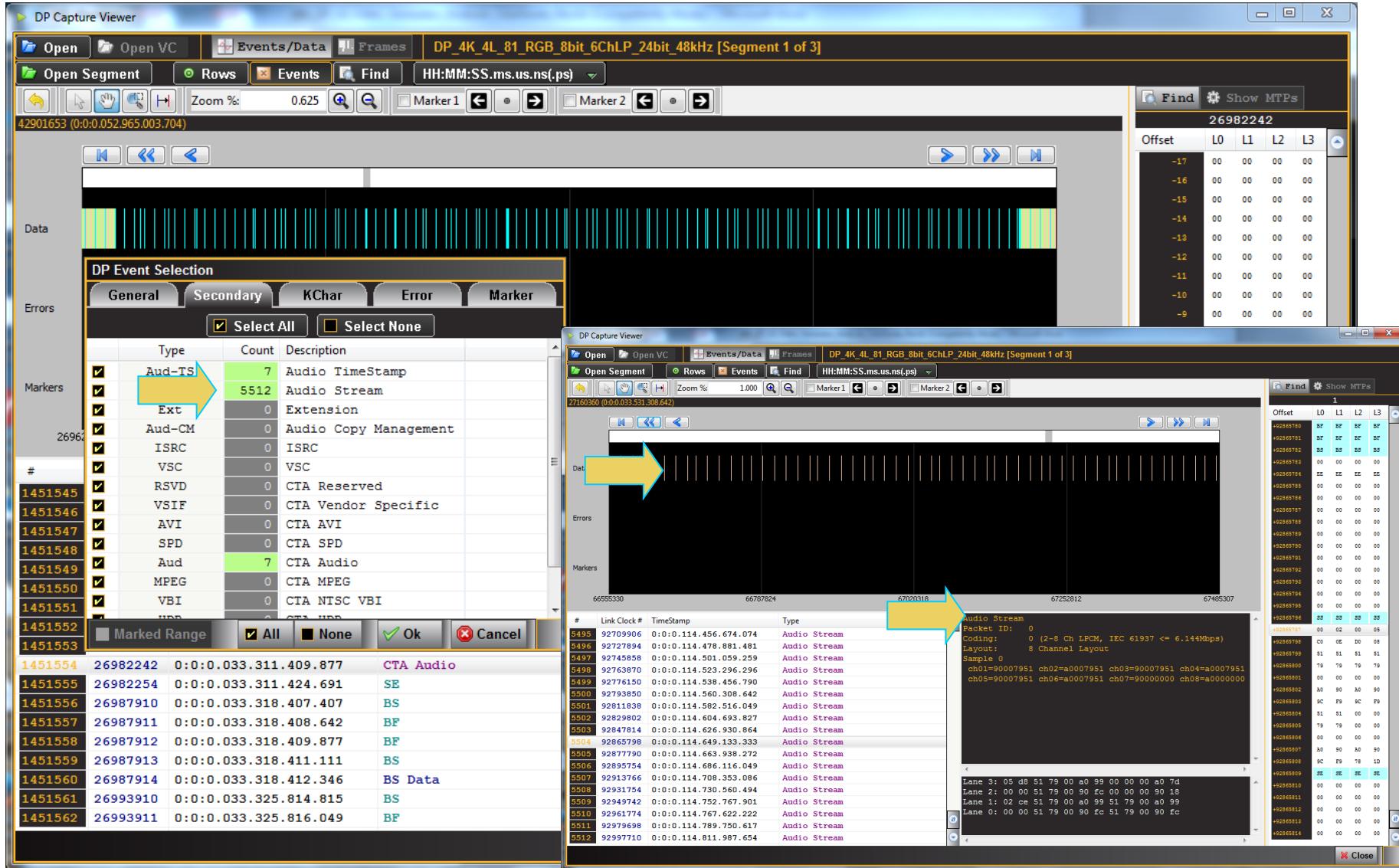


# DisplayPort Main Link Protocol – Audio Sample Packets (2 channel)

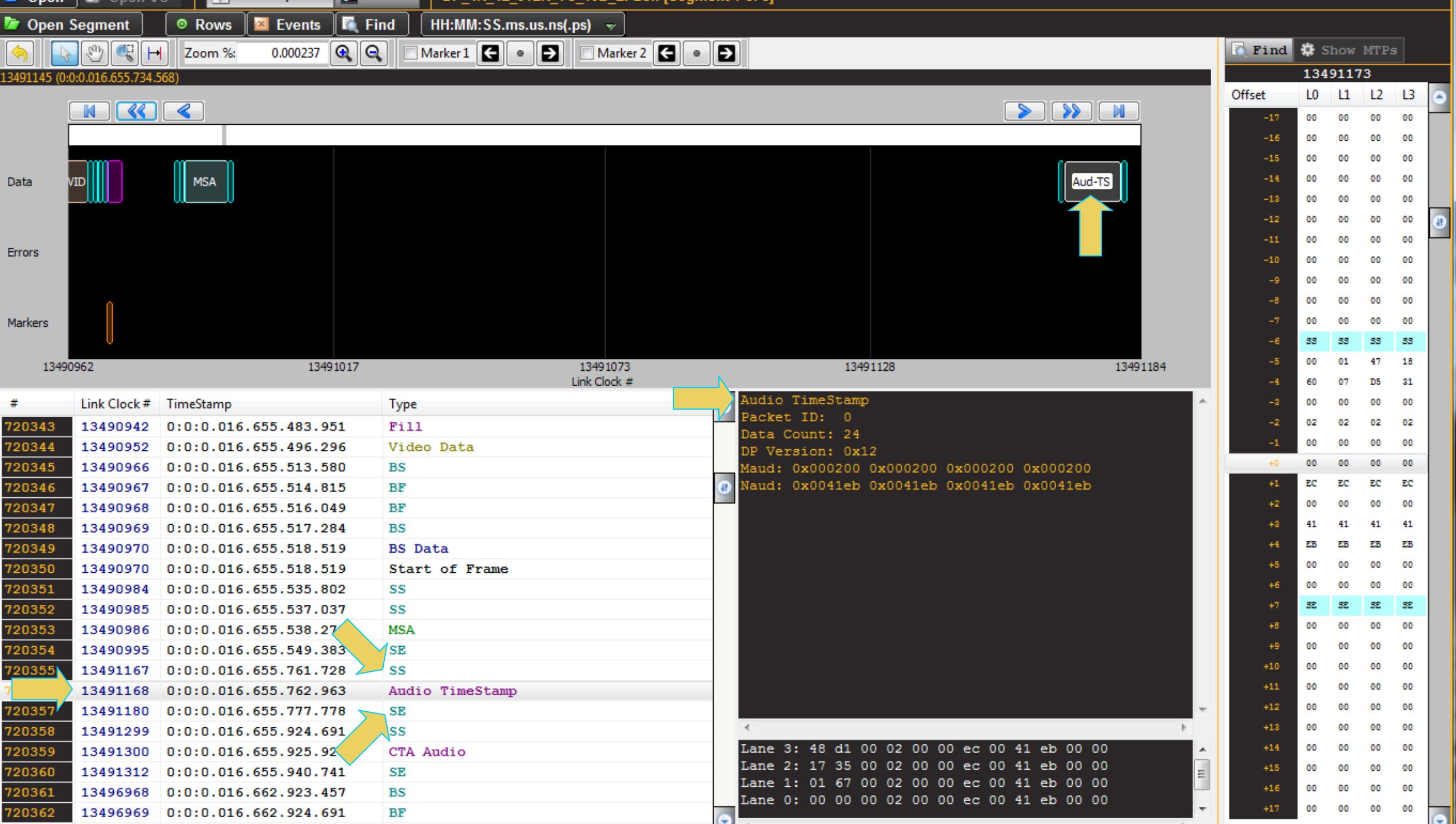


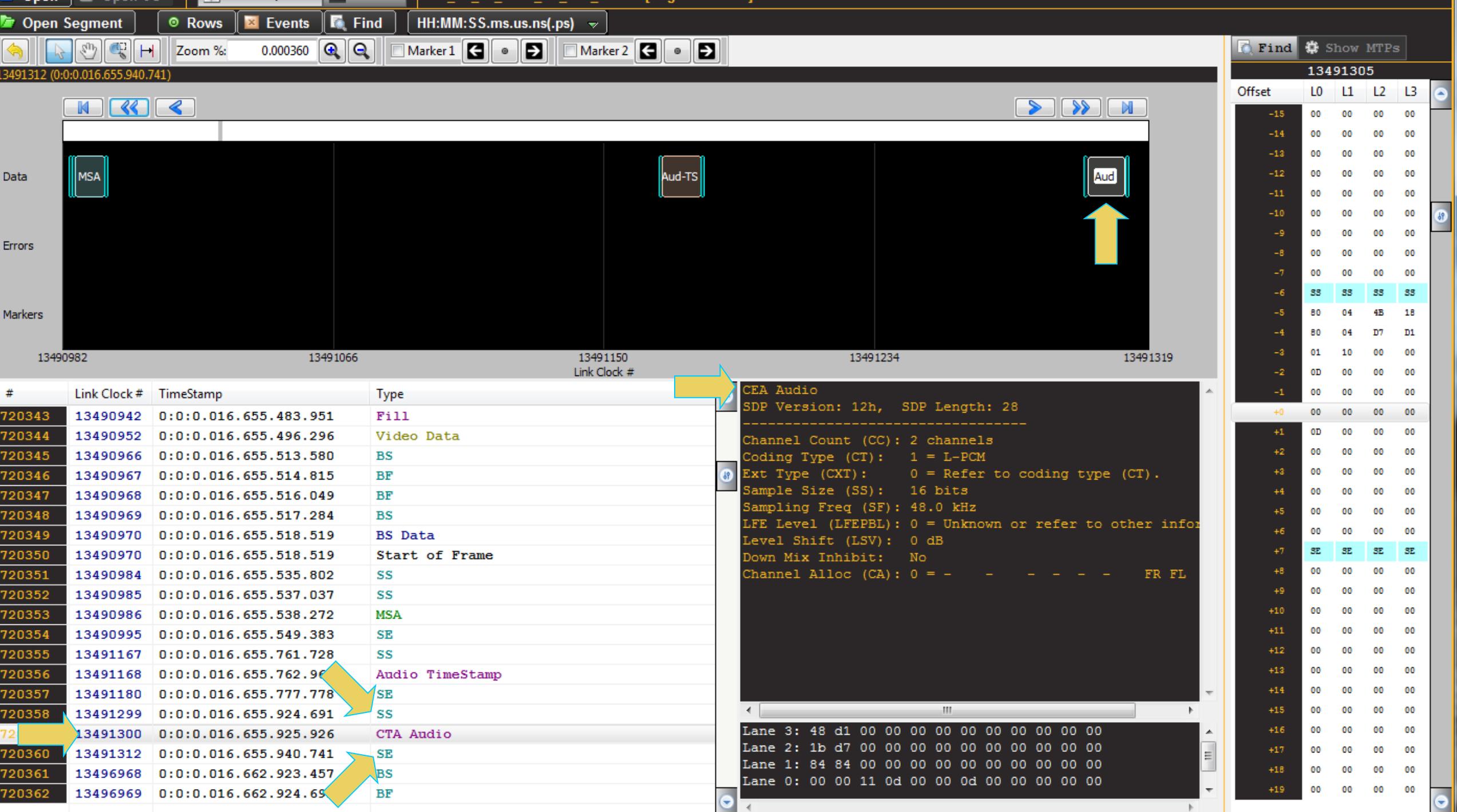
- Density of audio sample packets depends on the number of channels, sampling rate, bits per sample and audio format.
- Two (2) Channel LPCM data at 32kHz with 16 bits per sample (example left) will have fewer audio sample packets than 5.1 Channel LPCM audio at 48kHz sampling rate and 24 bits per sample.

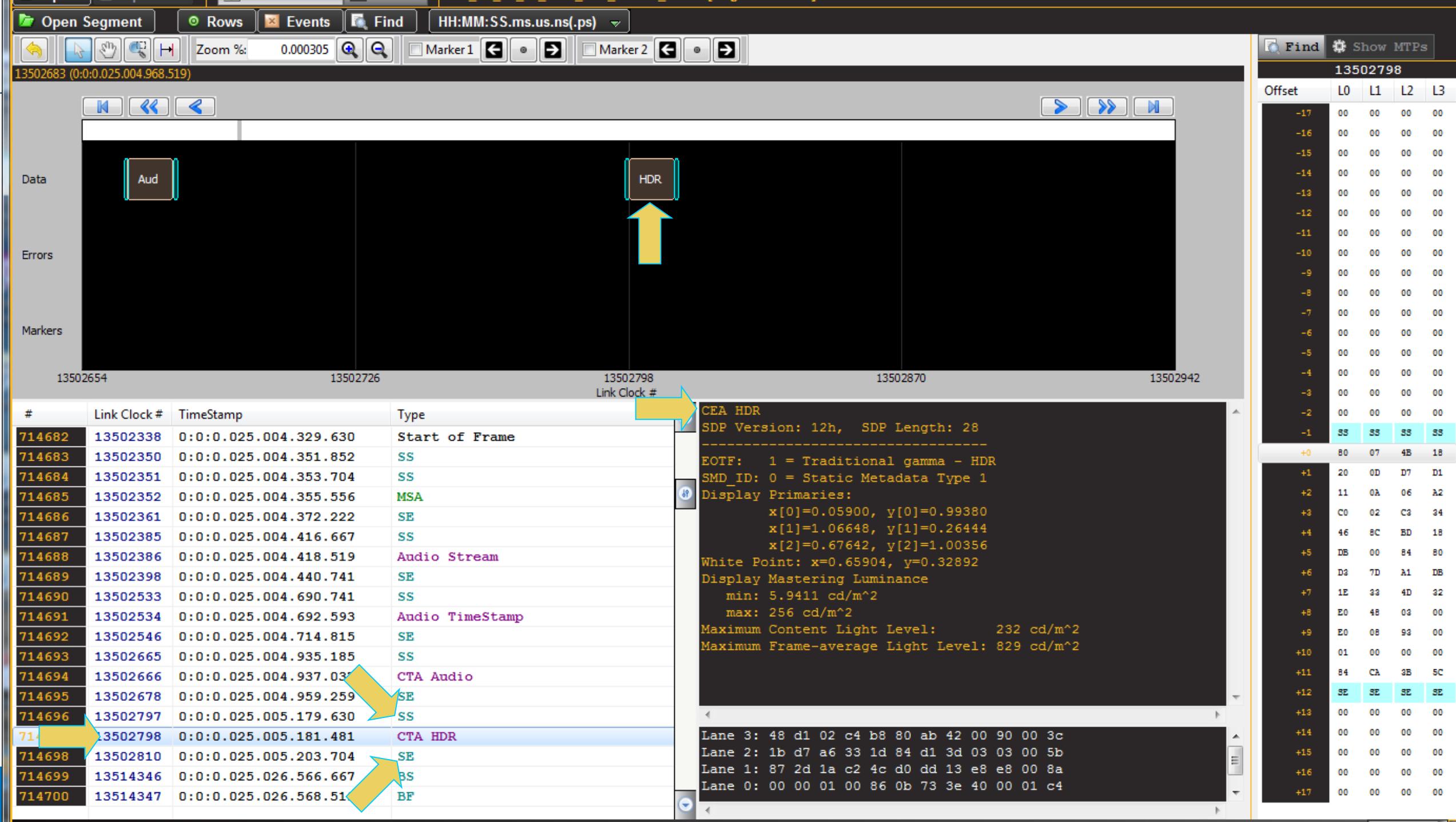
# DisplayPort Main Link Protocol – Audio Sample Packets (5.1 channel)

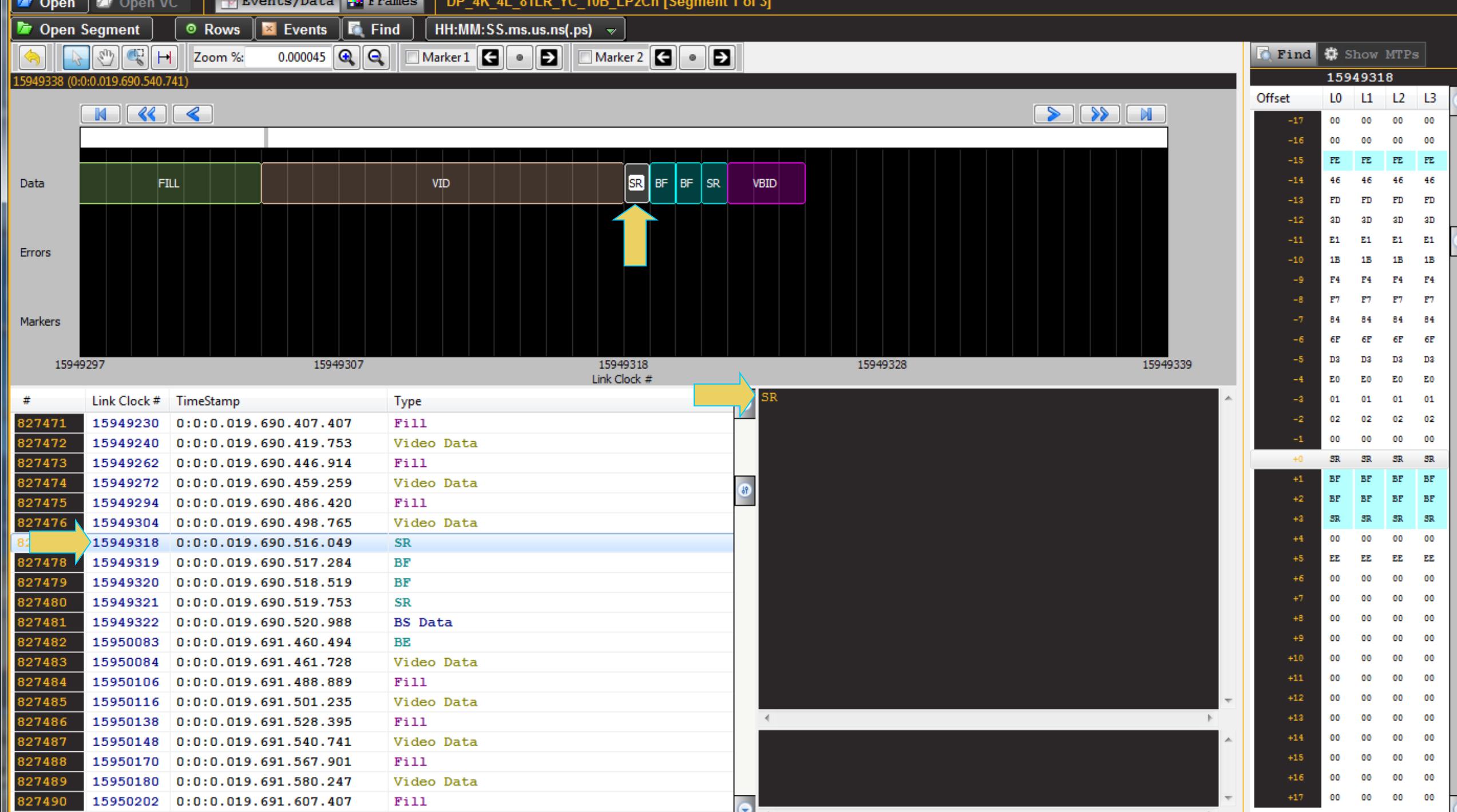


- Density of audio sample packets depends on the number of channels, sampling rate, bits per sample and audio format.
- Two (2) Channel LPCM data at 32kHz with 16 bits per sample (example left) will have fewer audio sample packets than 5.1 Channel LPCM audio at 48kHz sampling rate and 24 bits per sample.





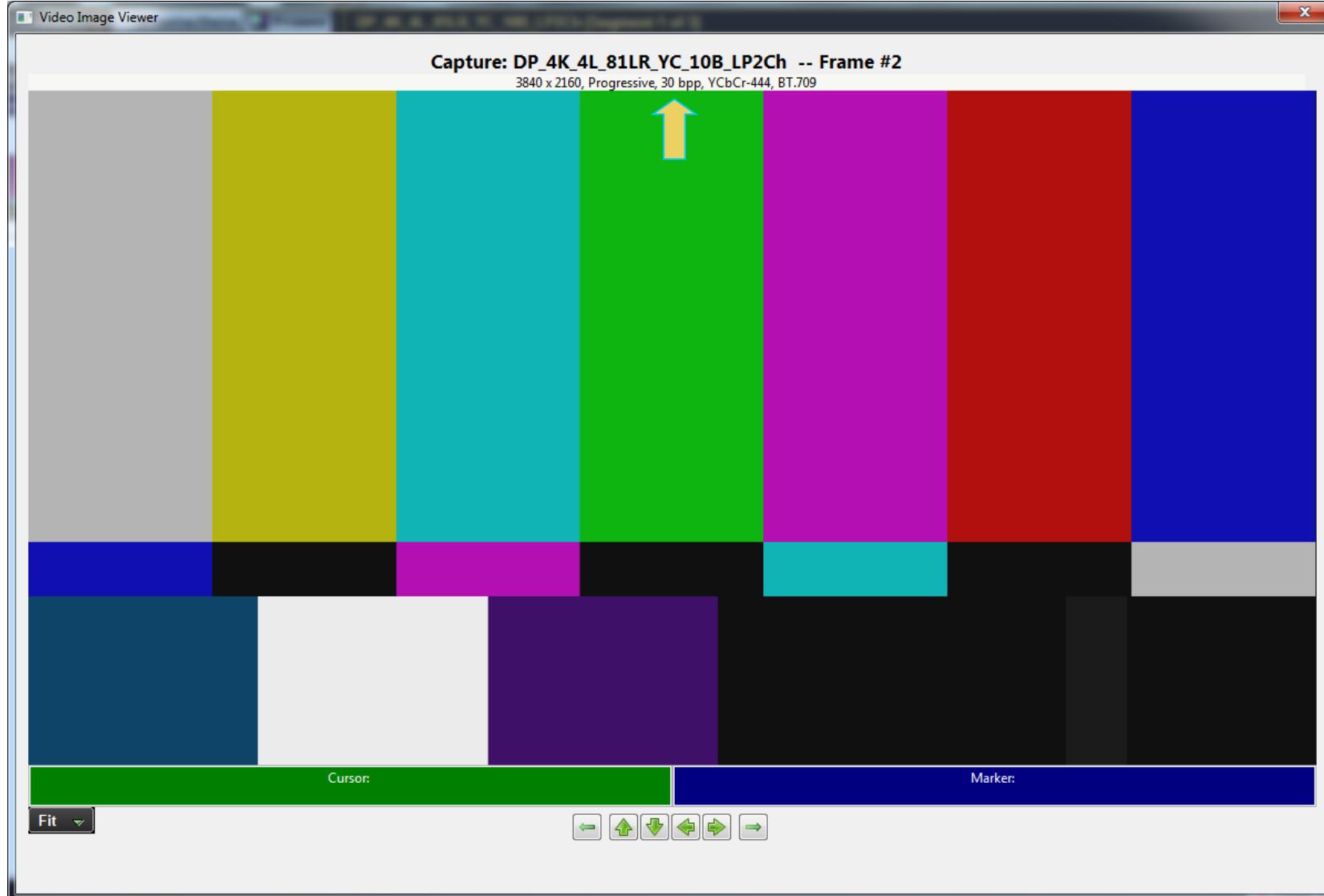




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# Main Link Video Pixel Mapping (Steering) at 8.1Gbps Link Rate on 4 Lanes

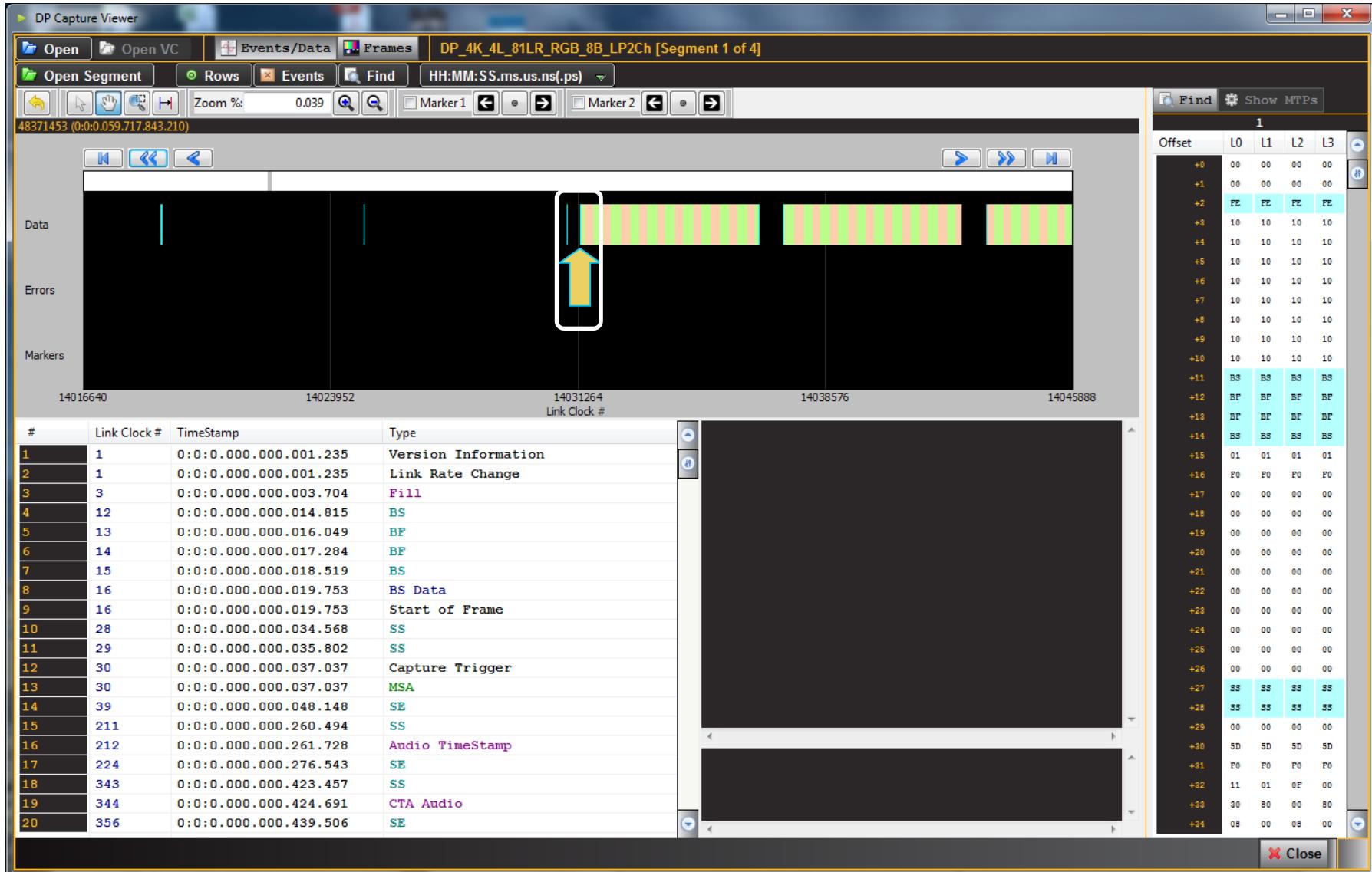
# DisplayPort Main Link Protocol – Pixel Mapping



- Pixels data values are spread out mapped “steered” on the lanes that are used.
- The video frame is a test pattern SMPTEbar.

# DisplayPort Main Link Protocol – Pixel Mapping (8 bit)

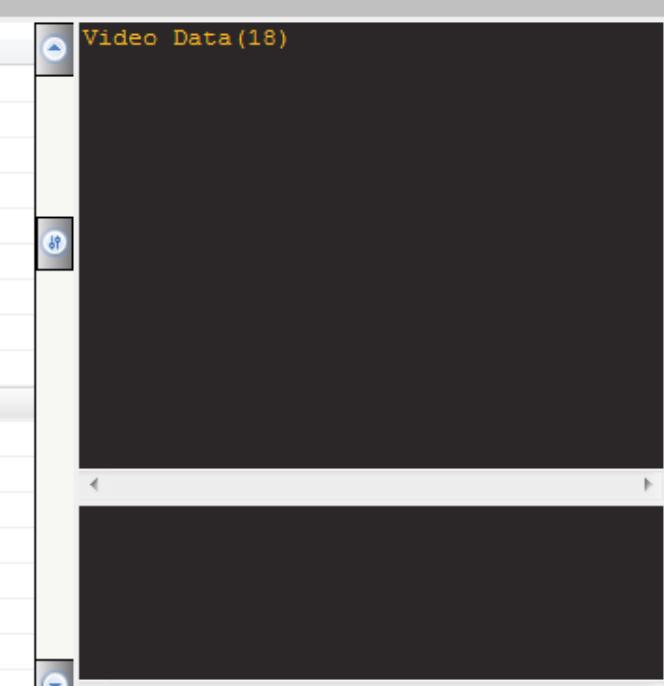
- Looking at the first pixel of a frame on a 4K video resolution with a link rate of 8.1 Gbps using four lanes using a color depth of 8 bits per component.



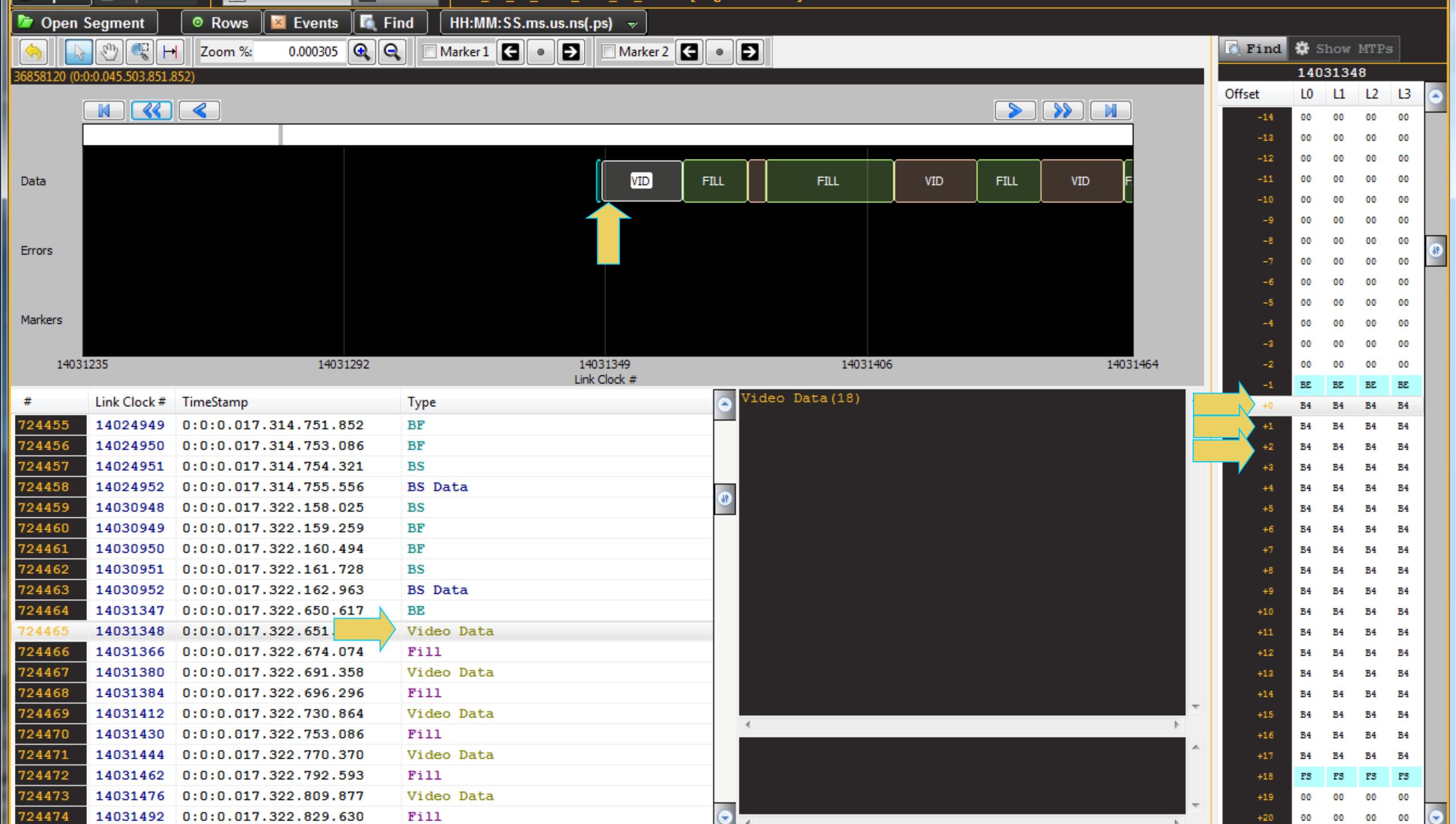
The screenshot shows a waveform viewer interface with a timeline from 20279579 to 20279808. The timeline is divided into several segments, each labeled with either 'VID' or 'FILL'. Two specific segments are highlighted with yellow arrows pointing upwards: one between approximately 20279636 and 20279693, and another between 20279693 and 20279750.

Offset	L0	L1	L2	L3
-7	FE	FE	FE	FE
-6	B4	B4	B4	B4
-5	B4	B4	B4	B4
-4	B4	B4	B4	B4
-3	B4	B4	B4	B4
-2	B4	B4	B4	B4
-1	B4	B4	B4	B4
+0	B4	B4	B4	B4
+1	B4	B4	B4	B4
+2	B4	B4	B4	B4
+3	B4	B4	B4	B4
+4	B4	B4	B4	B4
+5	B4	B4	B4	B4
+6	B4	B4	B4	B4

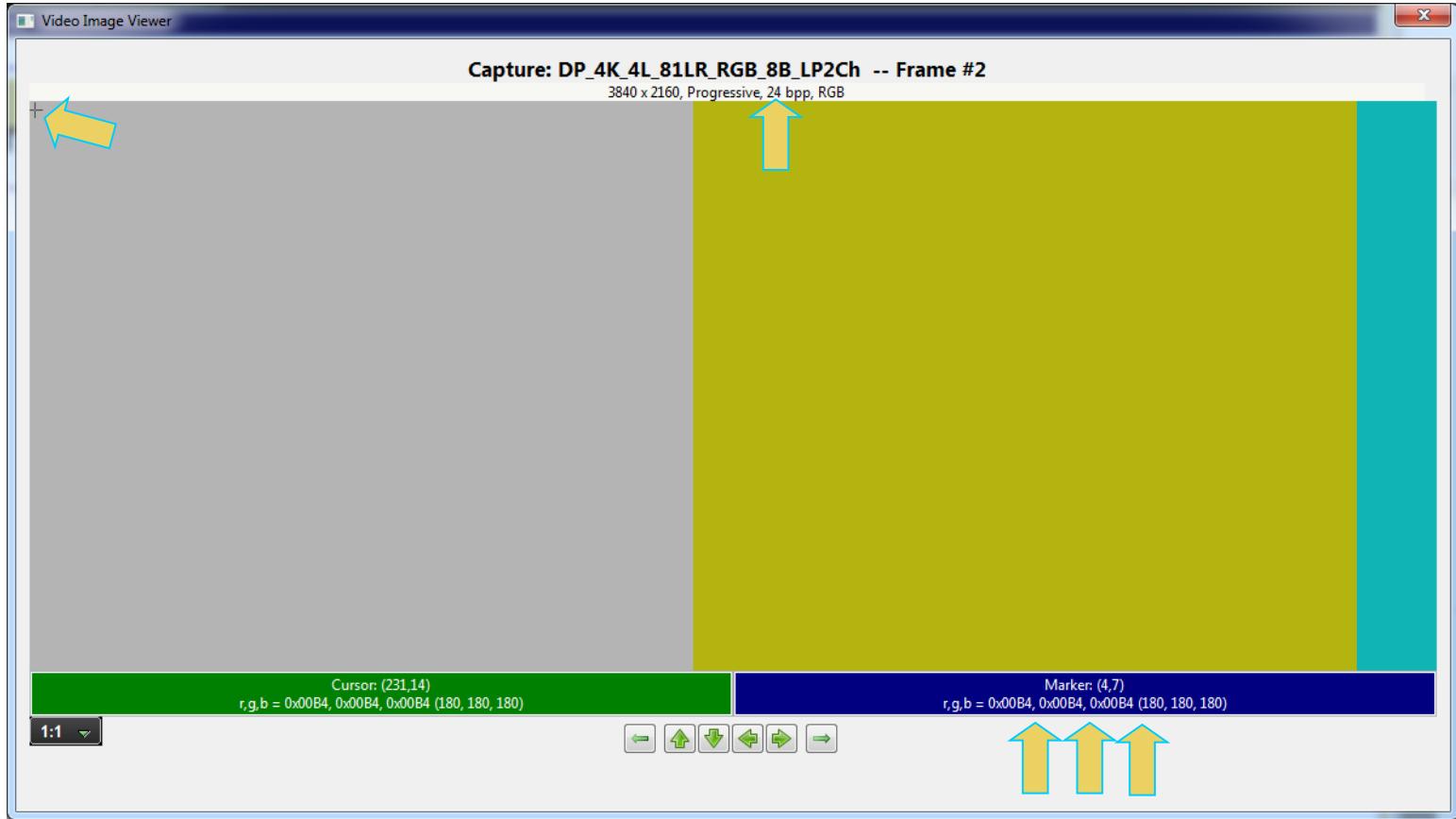
#	Link Clock #	TimeStamp	Type
1073505	20279534	0:0:0.025.036.461.728	Fill
1073506	20279548	0:0:0.025.036.479.012	Video Data
1073507	20279566	0:0:0.025.036.501.235	Fill
1073508	20279580	0:0:0.025.036.518.519	Video Data
1073509	20279598	0:0:0.025.036.540.741	Fill
1073510	20279612	0:0:0.025.036.558.025	Video Data
1073511	20279628	0:0:0.025.036.577.778	Fill
1073512	20279644	0:0:0.025.036.597.531	Video Data
1073513	20279662	0:0:0.025.036.619.753	Fill
1073514	20279676	0:0:0.025.036.637.037	Video Data
1073515	20279694	0:0:0.025.036.659.259	Fill
1073516	20279708	0:0:0.025.036.676.543	Video Data
1073517	20279726	0:0:0.025.036.698.765	Fill
1073518	20279740	0:0:0.025.036.716.049	Video Data
1073519	20279758	0:0:0.025.036.738.272	Fill
1073520	20279772	0:0:0.025.036.755.556	Video Data
1073521	20279788	0:0:0.025.036.775.309	Fill
1073522	20279804	0:0:0.025.036.795.062	Video Data



Offset	L0	L1	L2	L3
-1	00	00	00	00
-2	FE	FE	FE	FE
-1	B4	B4	B4	B4
-6	B4	B4	B4	B4
-5	B4	B4	B4	B4
-4	B4	B4	B4	B4
-3	B4	B4	B4	B4
-2	B4	B4	B4	B4
-1	B4	B4	B4	B4
+0	B4	B4	B4	B4
+1	B4	B4	B4	B4
+2	B4	B4	B4	B4
+3	B4	B4	B4	B4
+4	B4	B4	B4	B4
+5	B4	B4	B4	B4
+6	B4	B4	B4	B4
+7	B4	B4	B4	B4
+8	B4	B4	B4	B4
+9	B4	B4	B4	B4
+10	B4	B4	B4	B4
+11	FS	FS	FS	FS
+12	00	00	00	00
+13	00	00	00	00
+14	00	00	00	00
+15	00	00	00	00
+16	00	00	00	00
+17	00	00	00	00
+18	00	00	00	00
+19	00	00	00	00
+20	00	00	00	00
+21	00	00	00	00
+22	00	00	00	00
+23	00	00	00	00
+24	FE	FE	FE	FE
+25	B4	B4	B4	B4



# DisplayPort Main Link Protocol – Pixel Mapping Steering (8 bit)

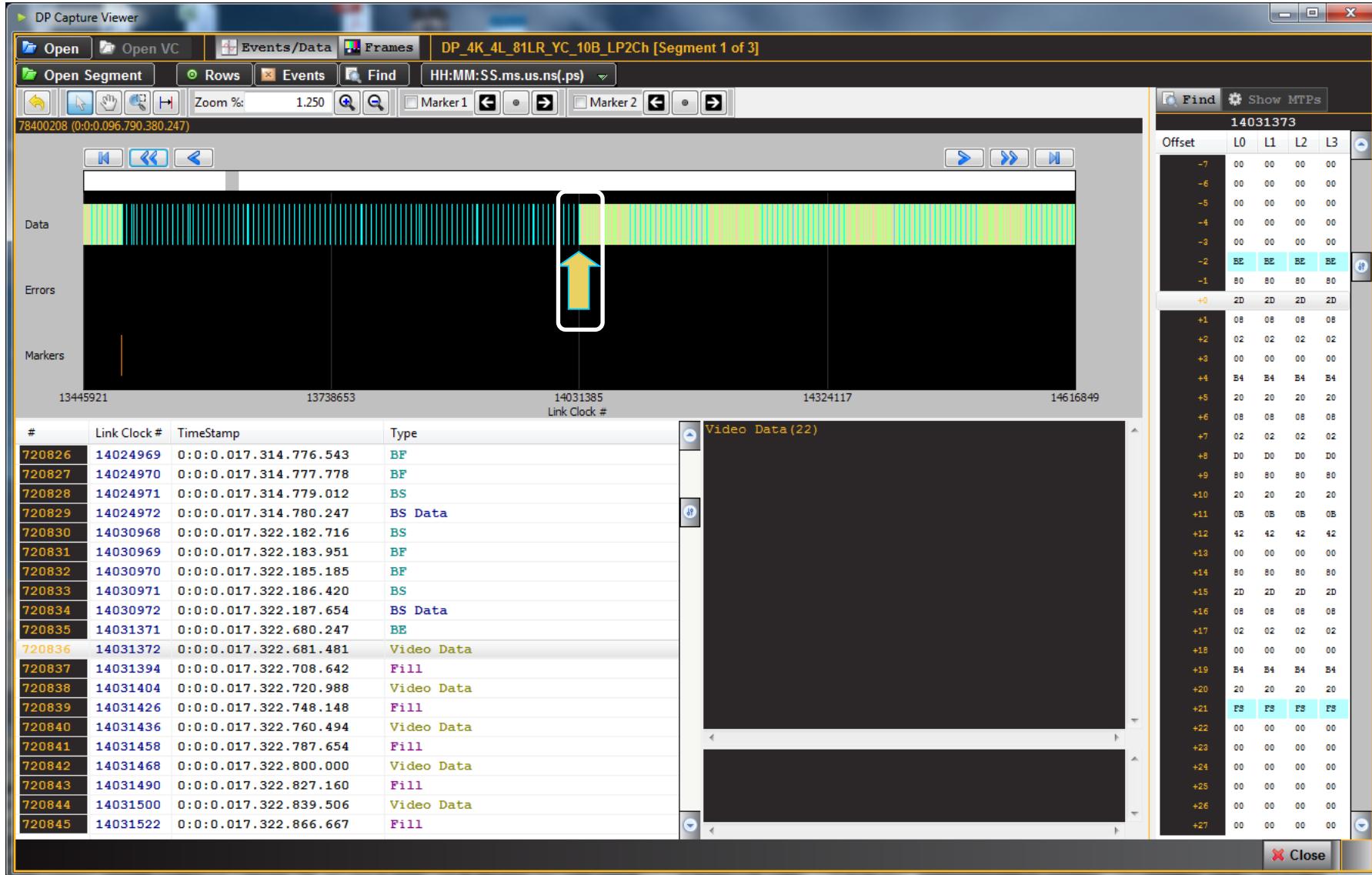


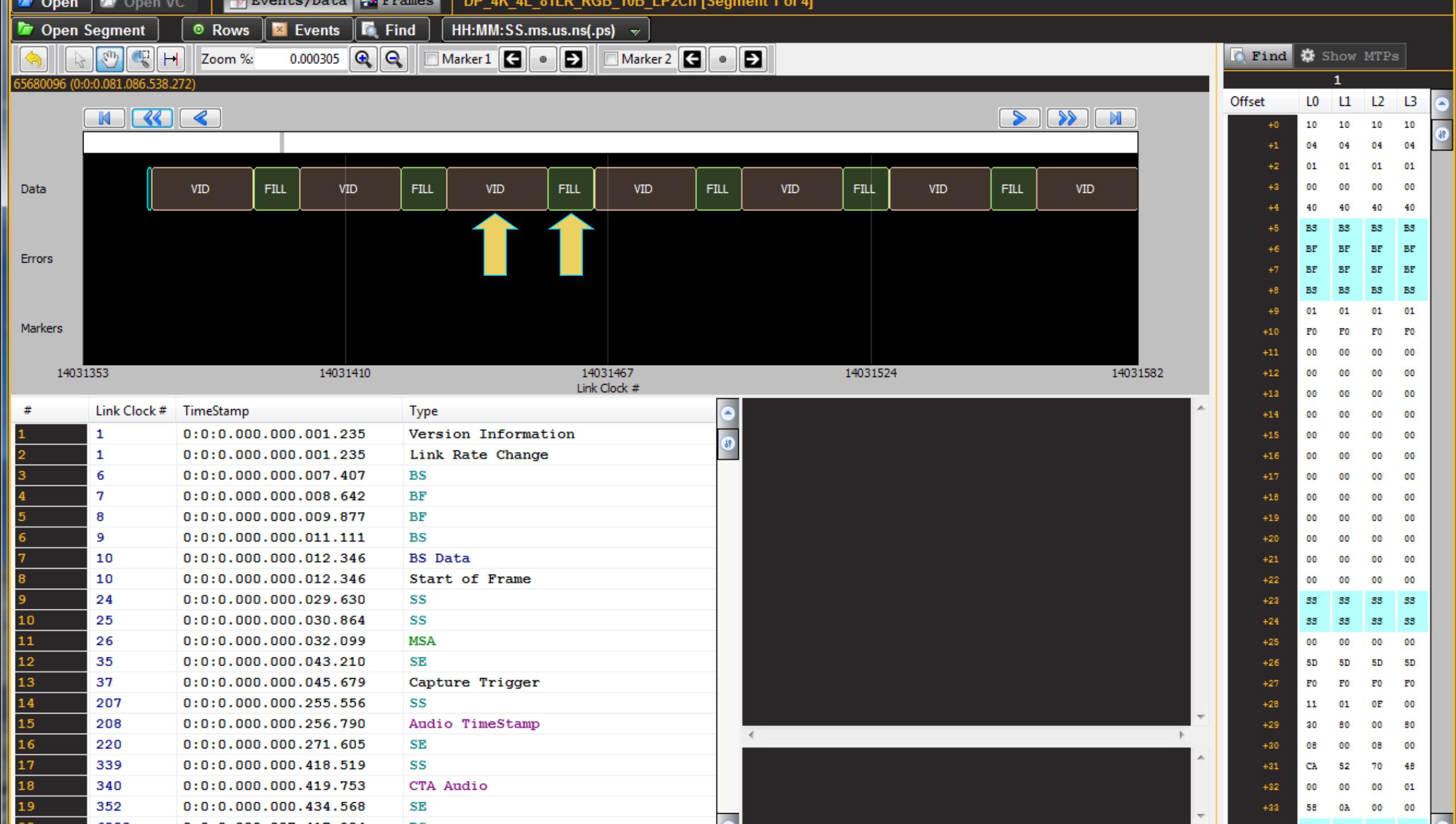
- Looking at the first video transfer unit in a frame.
  - Notice that the RGB values are uniform across the lanes with a pixel value of B4 representing the color of the first set of pixels in the frame:

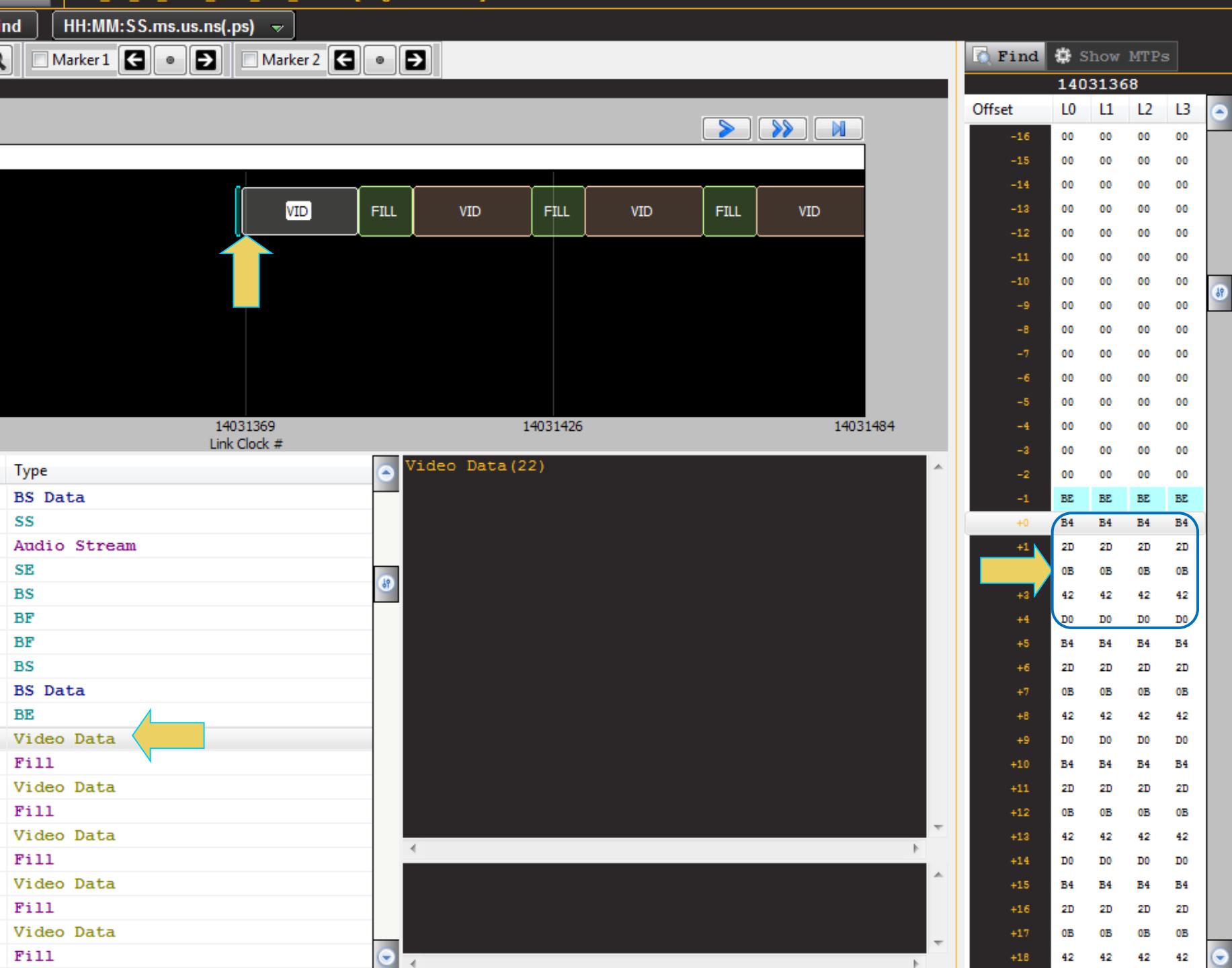
Lane0	Lane1	Lane2	Lane3
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R0-B4	R1-B4	R2-B4	R3-B4
G0-B4	G1-B4	G2-B4	G3-B4
B0-B4	B1-B4	B2-B4	B3-B4
B 4			
1011 0100	1011 0100	1011 0100	1011 0100
B 4			
1011 0100	1011 0100	1011 0100	1011 0100
B 4			
1011 0100	1011 0100	1011 0100	1011 0100

# DisplayPort Main Link Protocol – Pixel Mapping (10 bit)

- Looking at the first pixel of a frame on a 4K video resolution at 60Hz with a link rate of 8.1 Gbps using four lanes with 10 bit color depth.







ng) (10 bit–4 Lanes)

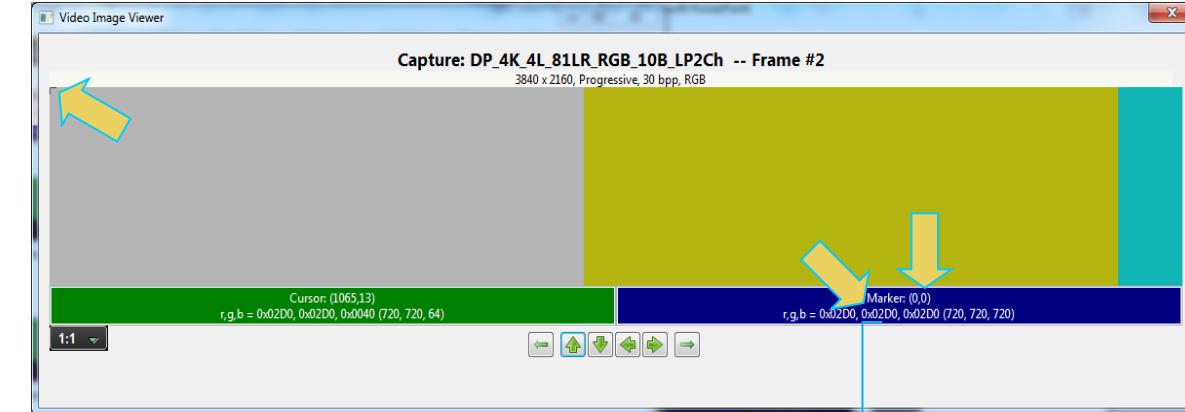
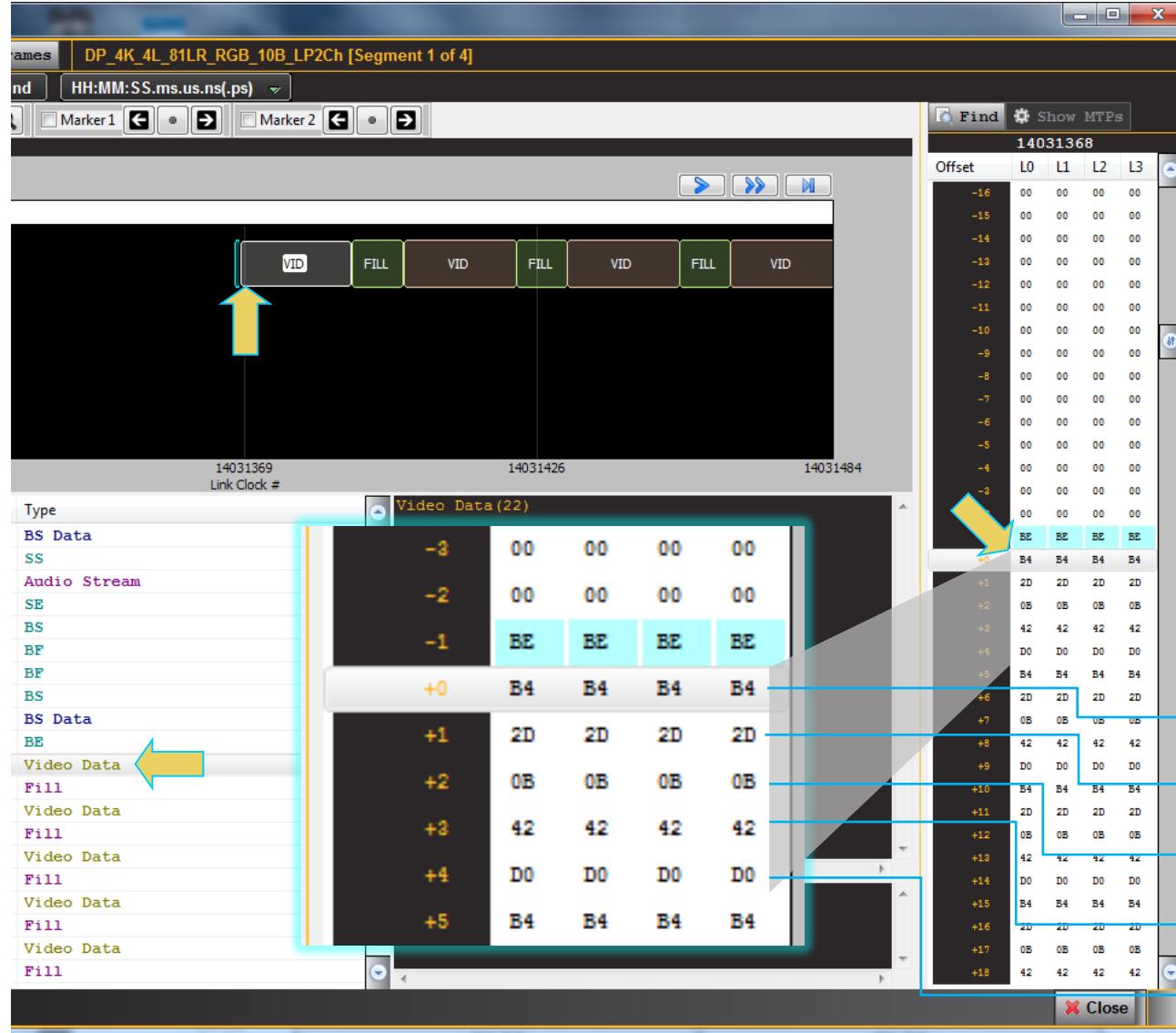
ng at the first video transfer  
a frame.

→ that the RGB values are  
ger uniform across the

is the pixel mapping  
ure:

Lane 2	Lane 3
R2-9:2	R3-9:2
9:4 R2-1:0   G2-9:4	R3-1:0   G3-9:4
9:6 G2-3:0   B2-9:6	G3-3:0   B3-9:6
9:8 B2-5:0   R6-9:8	B3-5:0   R7-9:8
R6-7:0	R7-7:0

# DisplayPort Main Link Protocol – Pixel Steering (10 bit–4 Lanes)

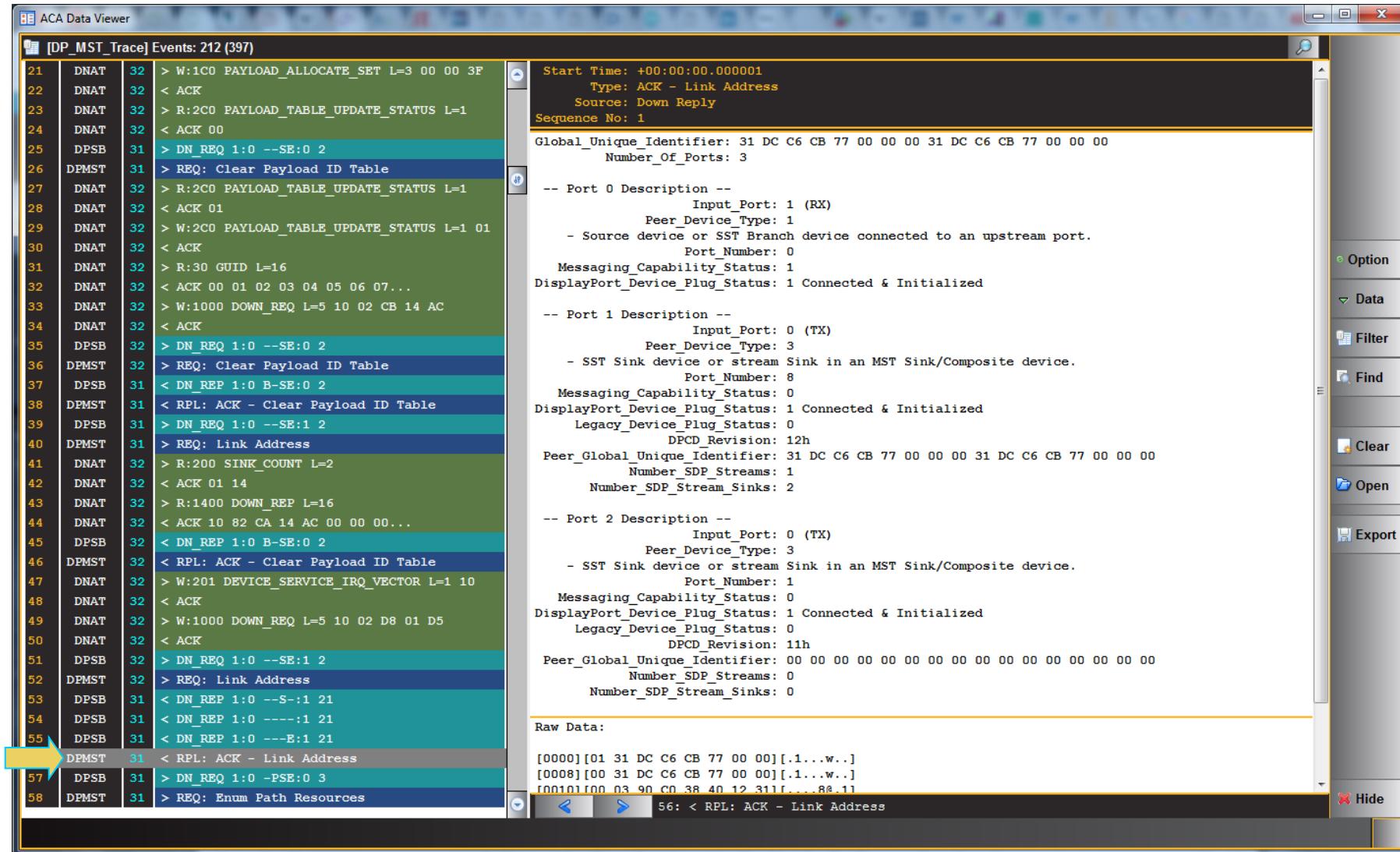


# DisplayPort Main Link Protocol Multi-Stream Transport (MST)

Webinar – April– 2018



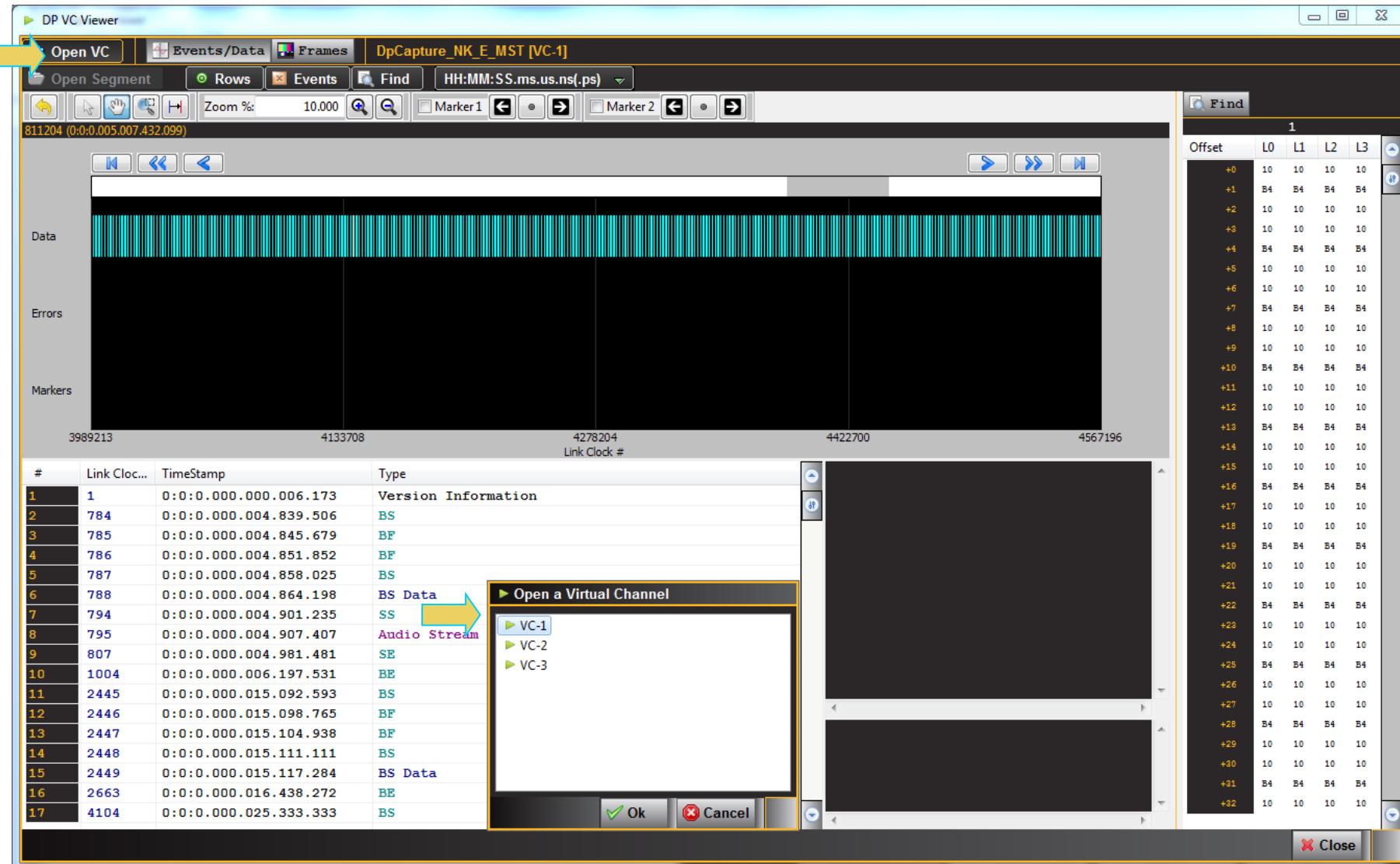
# 980 Auxiliary Channel Analyzer – Multi-Stream Transport Messages



- ACA showing MST messages during setup of Multi-Stream nodes.
- MST Side Band message also shown.

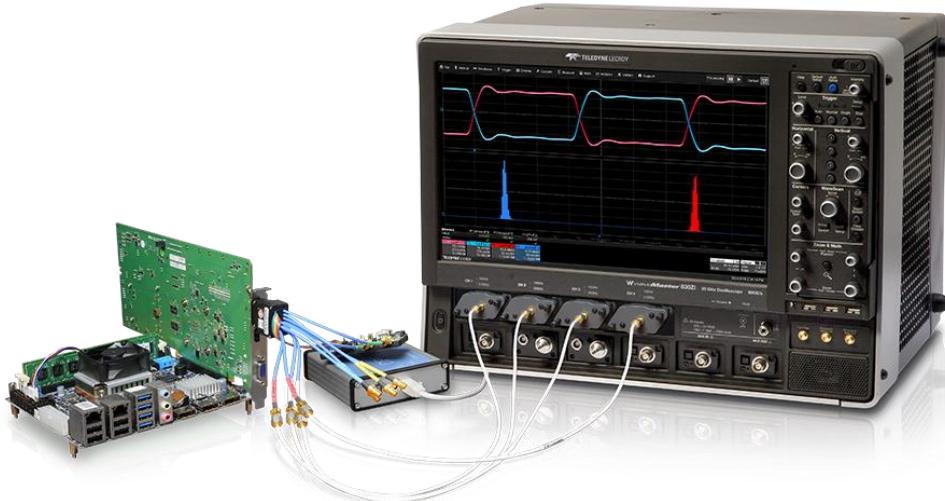
# 980 Capture Viewer – Viewing VCs of Multi-Stream Transport

- View capture of MST virtual channels.



# Teledyne LeCroy – DisplayPort Phy & Protocol Testing

DisplayPort Phy  
Compliance Testing  
at 8.1Gbps Link Rate



WaveMaster

DisplayPort Protocol  
Testing at  
8.1Gbps Link Rate



980B Test Platform

Thank you for attending  
Questions?

Please contact me, Neal Kendall at:  
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If you have any questions.