

Essentials of DisplayPort Forward Error Correction (FEC) Protocols

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Agenda

- DisplayPort Protocols Review
 - DisplayPort Link Training.
 - DisplayPort Main Stream Protocols.
- DisplayPort Display Stream Compression (DSC) Review
 - DSC Basic Operation
 - DSC Protocols
- DisplayPort Forward Error Correction (FEC) Operation
 - DisplayPort FEC Encoding
 - DisplayPort FEC Decoding
- Forward Error Correction (FEC) Overview
 - FEC Overview
 - Reed Solomon Theory of Operation
- DisplayPort Forward Error Correction (FEC) Compliance Testing
 - DisplayPort FEC Source Compliance Testing
 - DisplayPort FEC Sink Compliance Testing

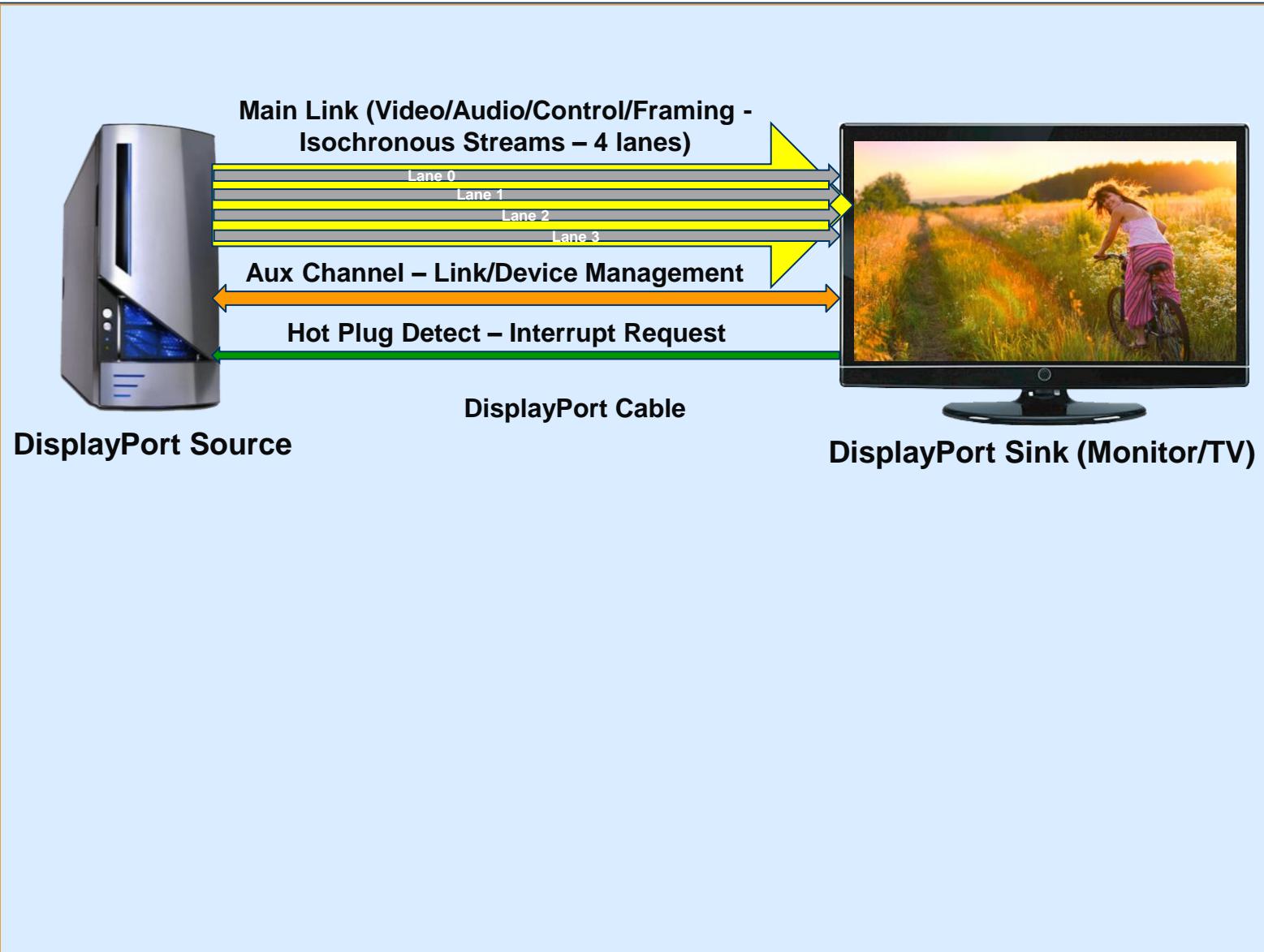
- ◆ Please Check out our DisplayPort “Essentials of” Webinars:
 - ◆ [Essentials of DisplayPort Protocols](#)
 - ◆ [Essentials of HDCP 2.2 Protocols](#)
 - ◆ [Essentials of DisplayPort Display Stream \(DSC\) Protocols](#)
 - ◆ [Essentials of DisplayPort Link Layer Compliance Testing](#)

Go To: https://www.quantumdata.com/980_dp_14.html

Check out our HDMI 2.1 “Essentials of” Webinars

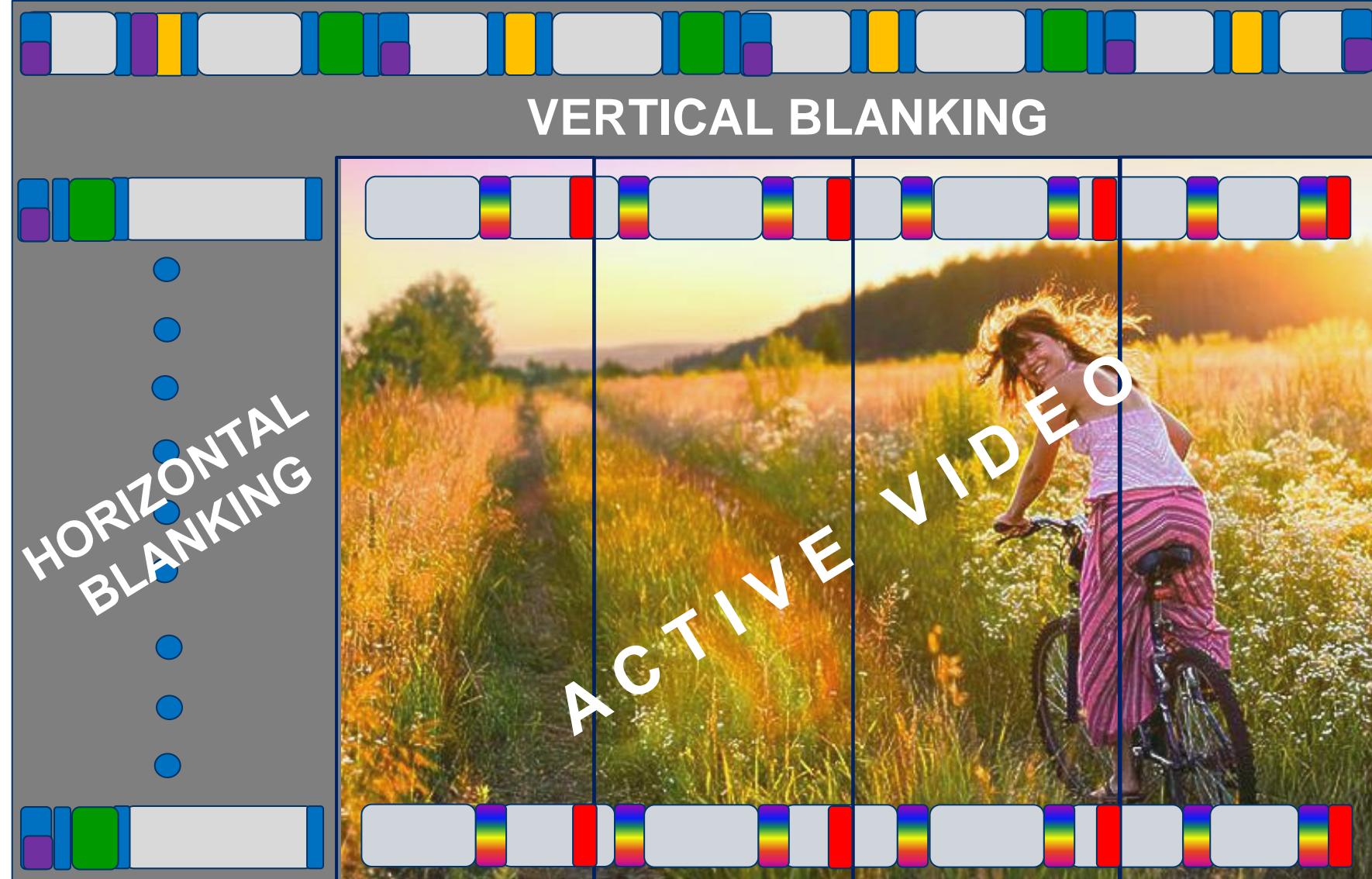
- ◆ [Essentials of HDCP 2.2 Protocols](#)
- ◆ [Essentials of HDMI Fixed Rate Link \(FRL\) Protocols](#)
- ◆ [Essentials of HDMI Enhanced Audio Return Channel \(eARC\) Protocols](#)

DisplayPort Anatomy



- **Main Link**: Unidirectional, high-bandwidth channel used to transport video, audio and metadata and protocol control elements.
- Main Link 1, 2 or 4 Lane Configurations.
- Main Link 4 link rates:
 - 1.62Gbps (Reduced Bit Rate)
 - 2.7Gbps (High Bit Rate)
 - 5.4Gbps (High Bit Rate 2)
 - 8.1Gbps (High Bit Rate 3)
- **No clock channel**. Sink recovers clock using link transitions.
- **Aux Channel**: Bidirectional, half duplex channel with a data rate of 1Mbps. Link Training, DPCD Register status, HDCP authentication & EDID.
- **No separate clock** for aux channel. Clock derived from the bitstream.
- Hot plug lead:
 - Connection Detection.
 - Interrupt mechanism in cases where there is a link failure.

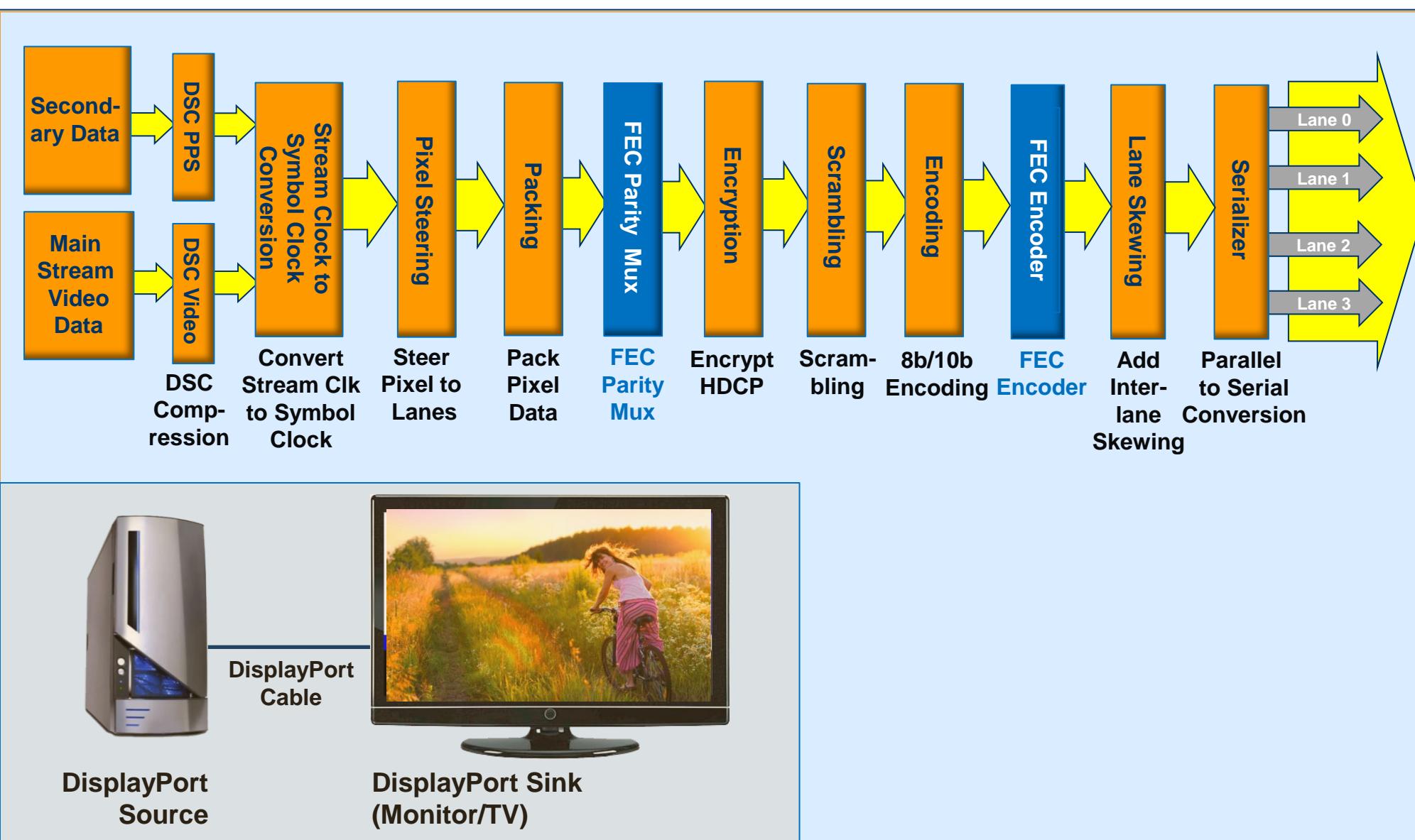
DisplayPort Main Link Protocol – One Video Frame



- Video packets occur during the active video period.
 - Metadata: Main Stream Attributes (MSA) and Secondary Data Packets (SDP) occur during the vertical blanking period.
 - There is a lot of **over capacity**. **Fill characters** are zeros for filling up (stuffing) the unused link symbols.

	Video		Fill Characters
	Metadata		Control Symbols
	Audio (SD)		Control VBID w/ Compression
	PPS		Flag Set
	EoC		

DisplayPort Main Link Transmitter Functional Blocks

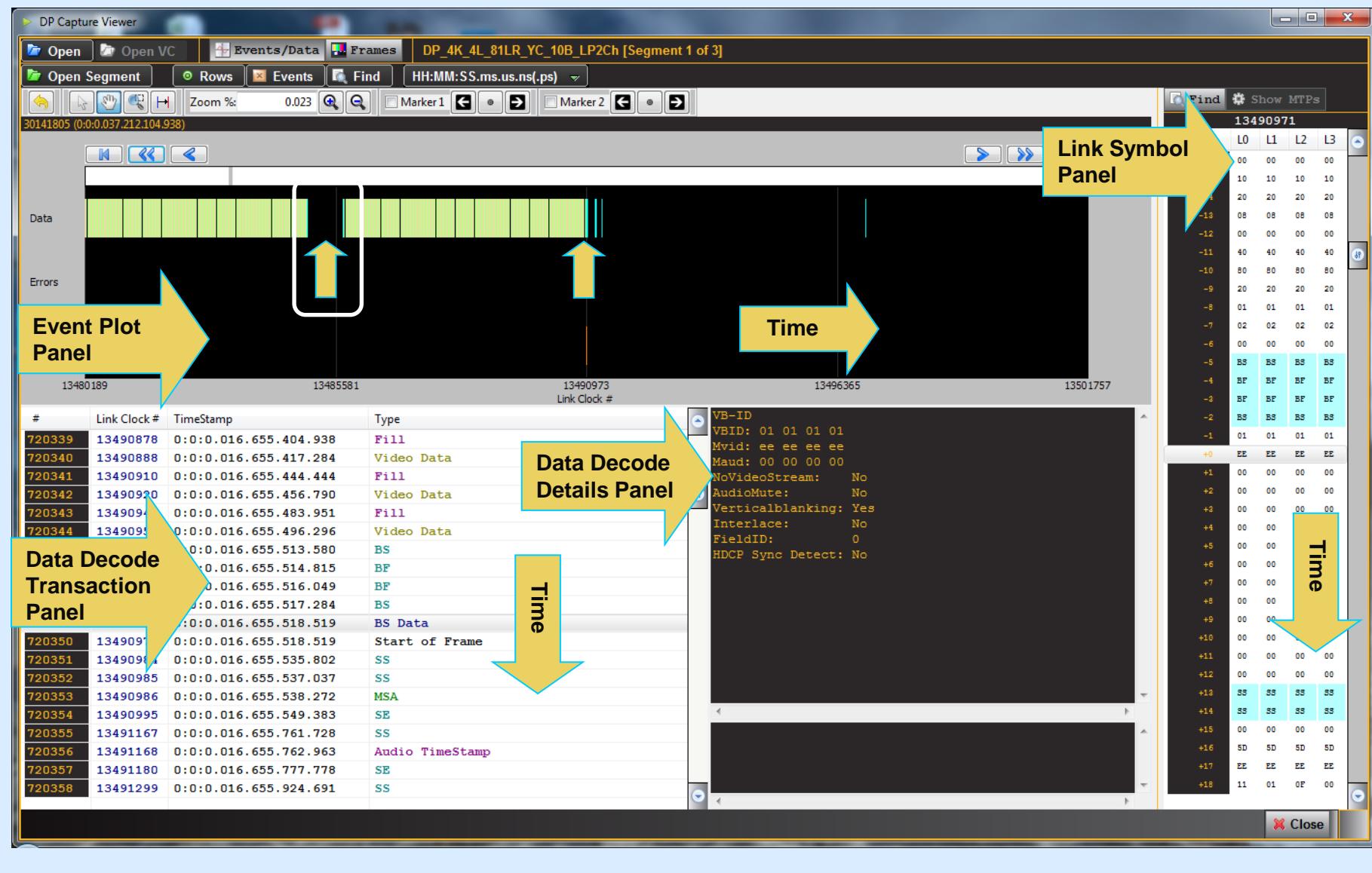


- **FEC Encoding Blocks:**
 - FEC Parity Muxer.
 - FEC Encoder.
- **FEC Parity Muxer:**
 - Inserts Parity Marker.
 - Initiates FEC enable sequence.
 - Inserts Parity placeholder.
- **FEC Encoder:**
 - Removes FEC Parity placeholders
 - Interleaves link symbols between lanes.
 - Calculates Parity Symbols
 - Interleaves Parity Symbols between lanes.
 - Creates Parity Codes from Parity Symbols
 - Muxes Parity Codes into Link Symbols.

DisplayPort Main Link Protocol Brief Overview

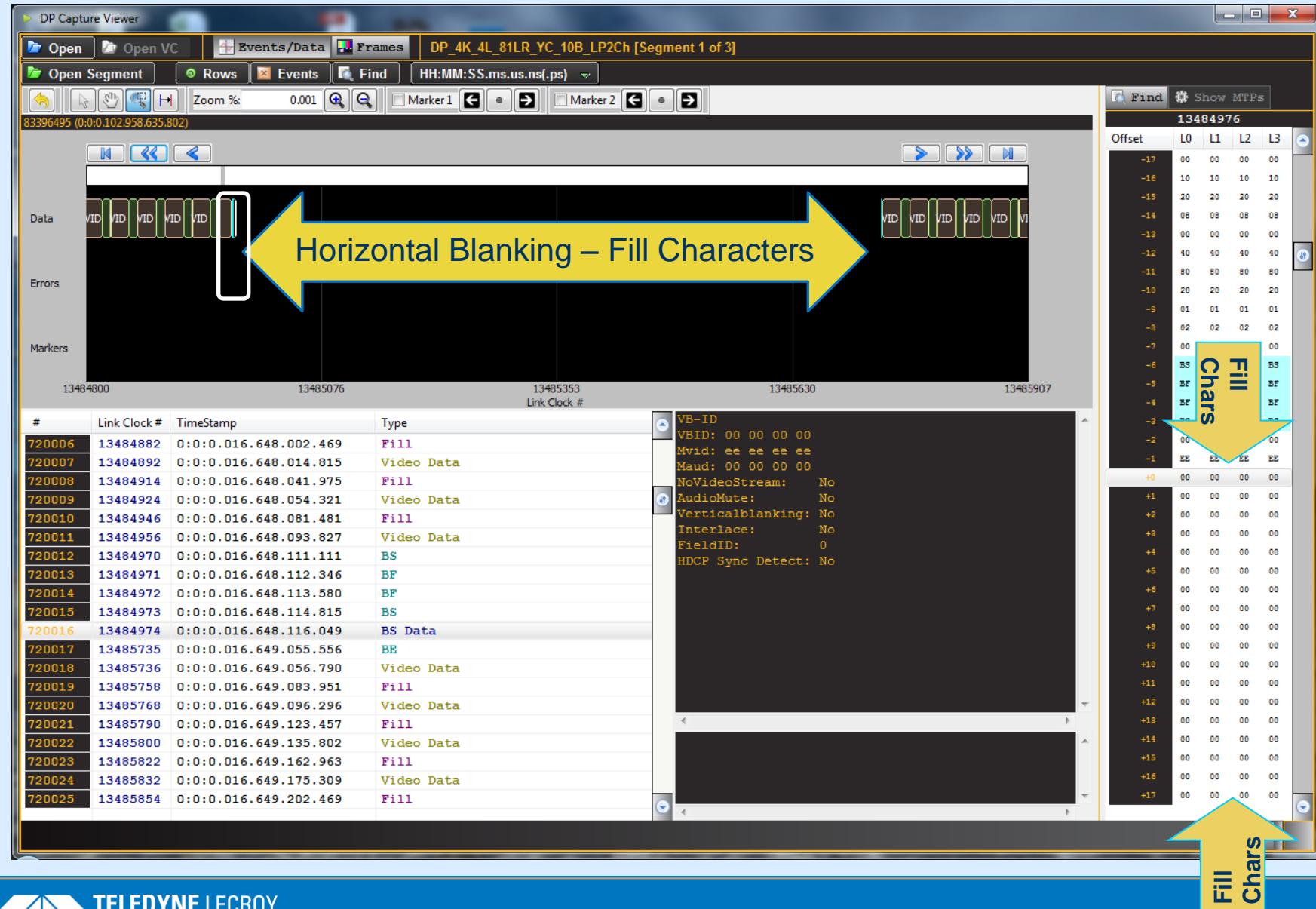


DisplayPort Main Link Protocol – Framing Control Symbols



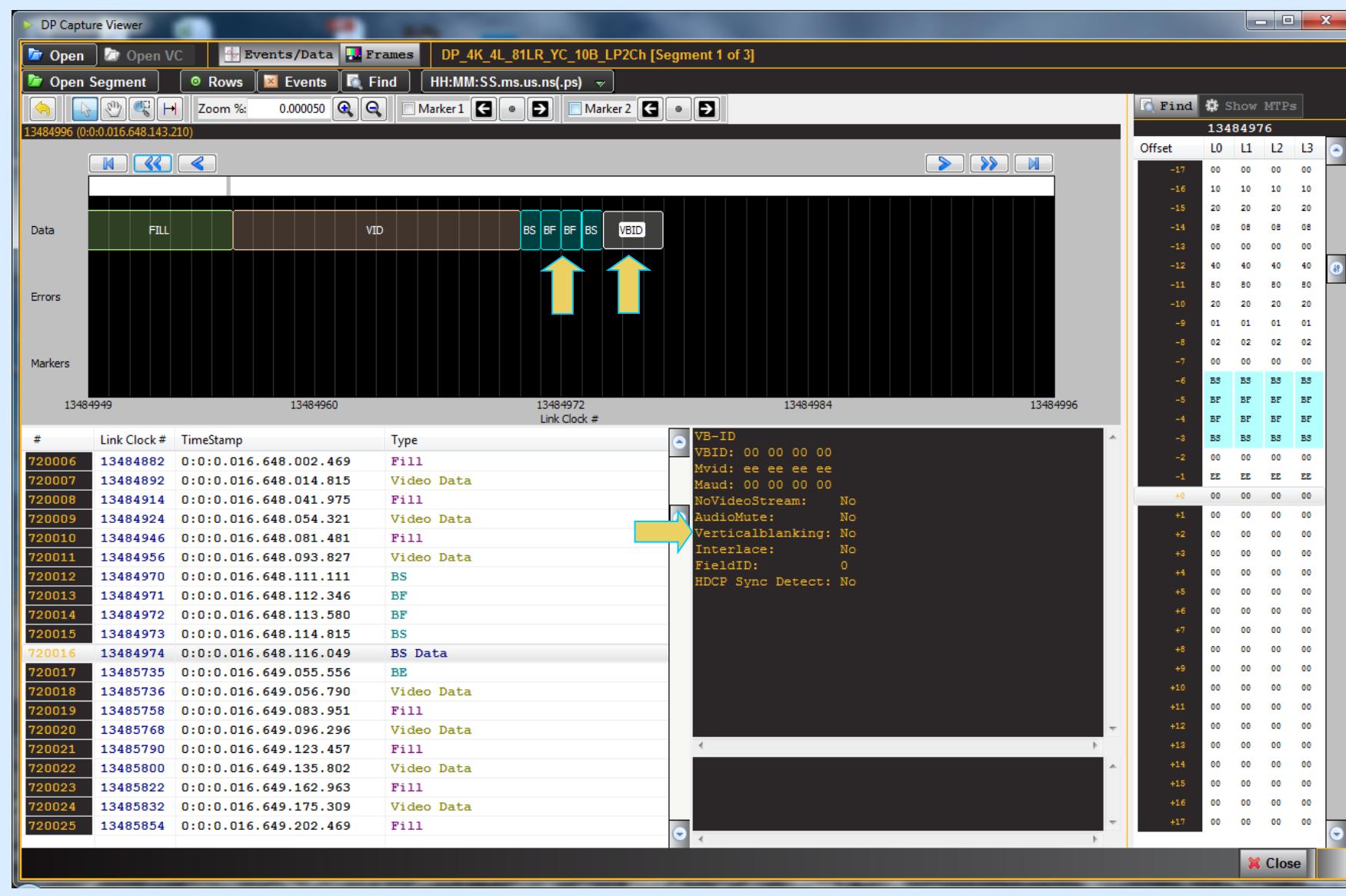
- Showing end of Video Display Frame, beginning of vertical blanking.
- Also showing the horizontal blanking region.

DisplayPort Main Link Protocol – Horizontal Blanking



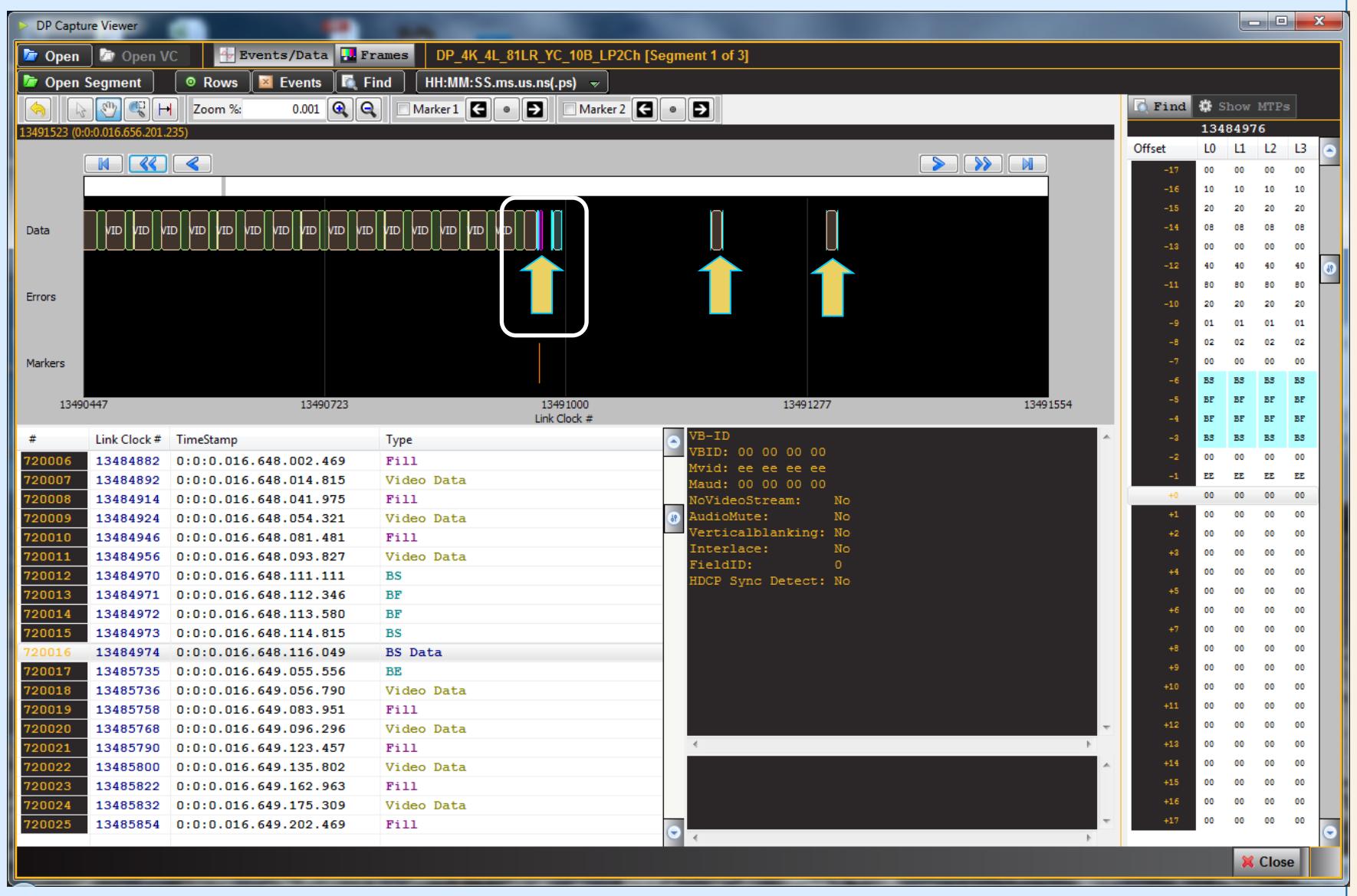
- Horizontal blanking is stuffed with fill characters.
- Fill characters are zeros as indicated on the Link Symbol panel.

DisplayPort Main Link Protocol – Horizontal Blanking



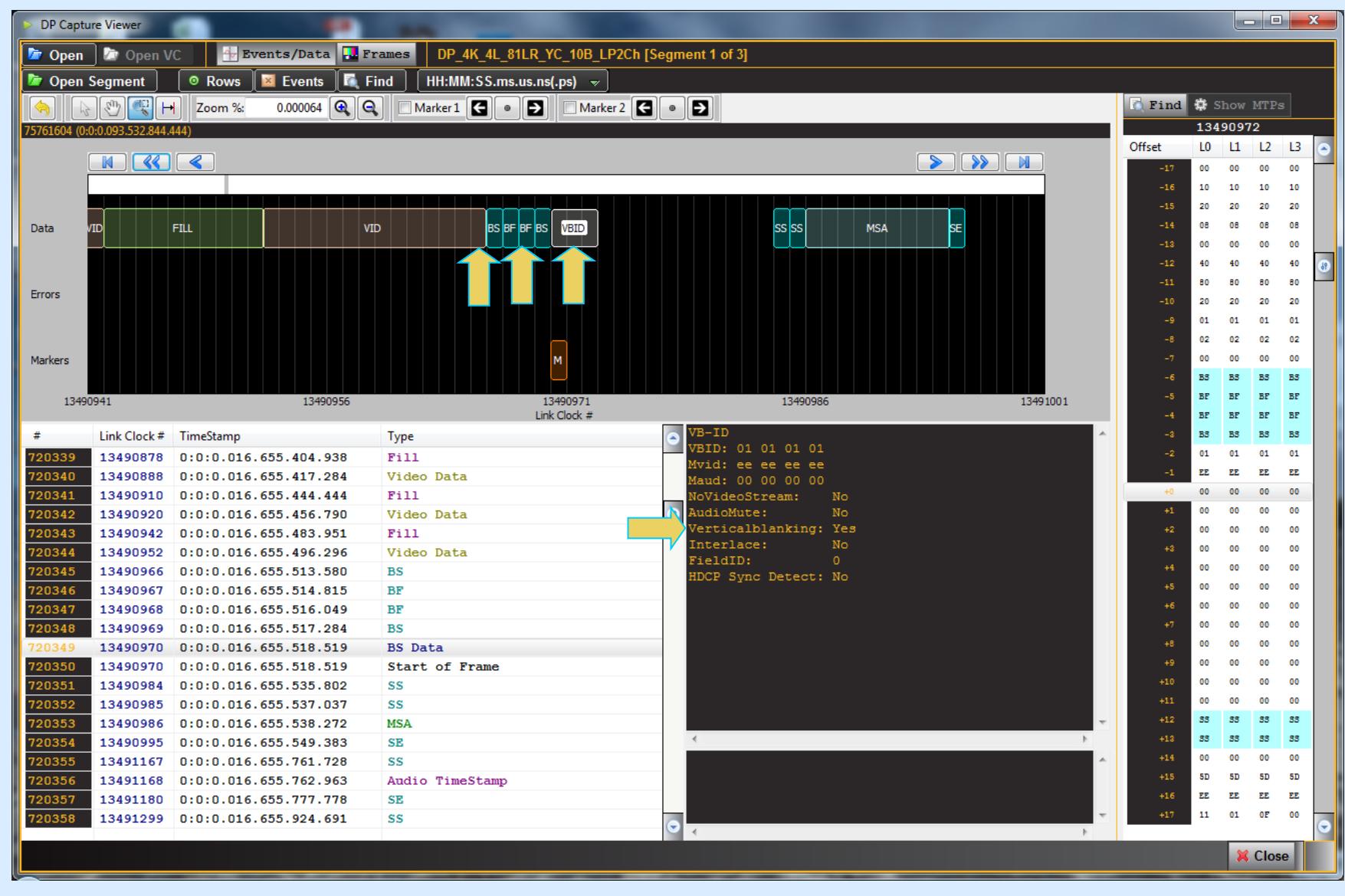
- Horizontal blanking is preceded by the four (4) character sequence of Blanking Start (BS), Blanking Fill (BF) followed by the VBID.
- The VBID data indicates that this blanking period is not Vertical Blanking.

DisplayPort Main Link Protocol – Framing Control Symbols



- Showing end of Video Display Frame, beginning of vertical blanking.
- Fill regions are visible as are some of the protocol elements in the vertical blanking region.

DisplayPort Main Link Protocol – Framing Control Symbols

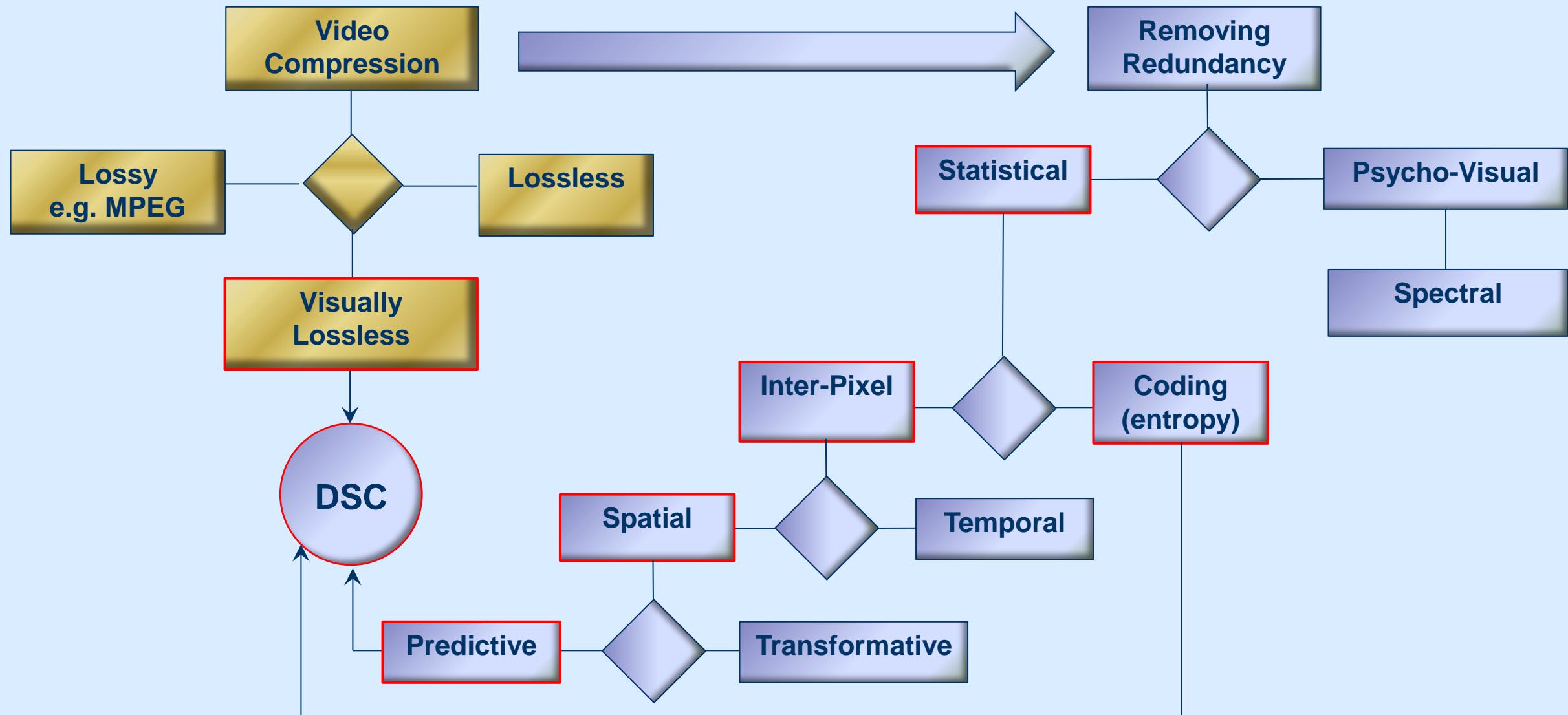


- Showing end of Video Display Frame, beginning of vertical blanking.
- Last video element is preceded by a set of Fill Characters.
- Then the four (4) character sequence of Blanking Start (BS), Blanking Fill (BF) followed by the VBID.
- VBID details shown in Data Decode Details panel indicating Vertical Blanking = Yes.

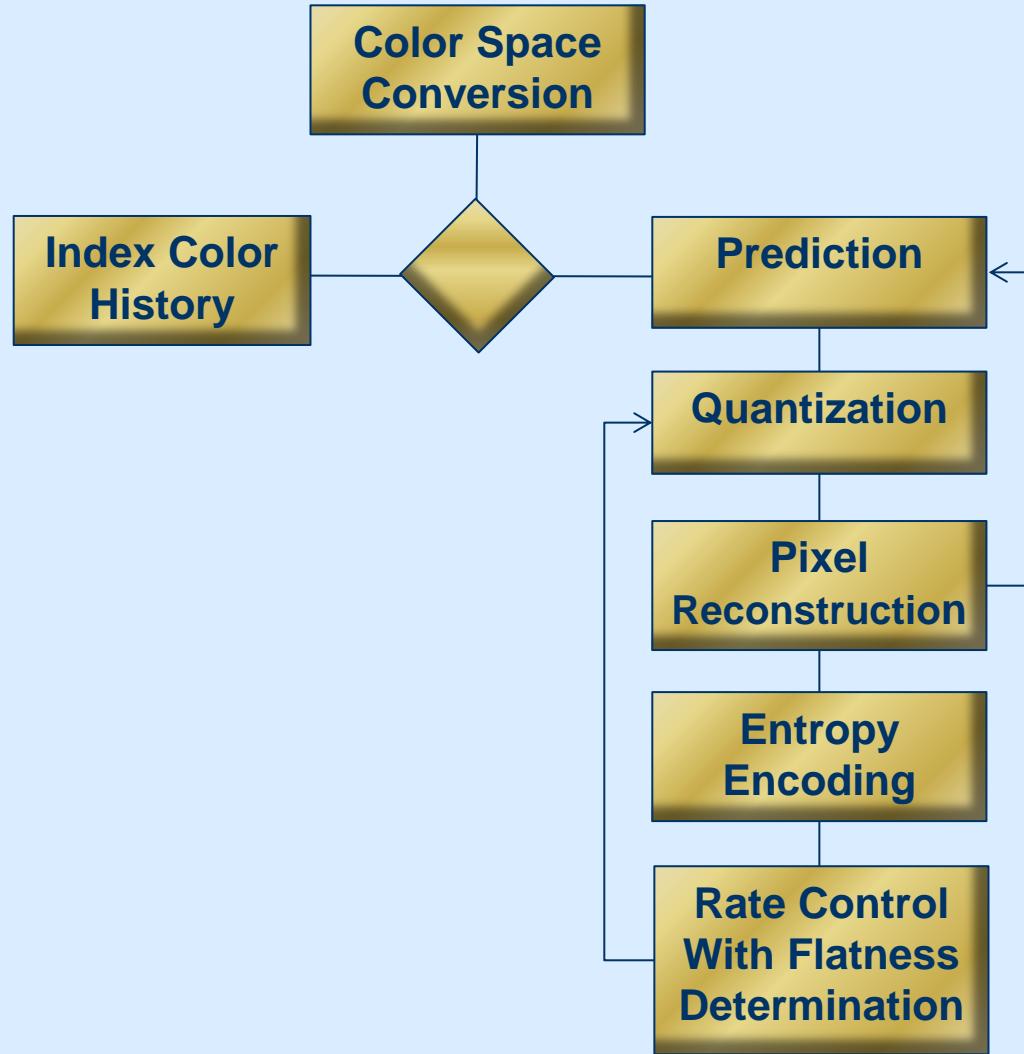
Display Stream Compression (DSC) Brief Overview



Video Compression Taxonomy



Display Stream Compression – How Does DSC Compression Work?



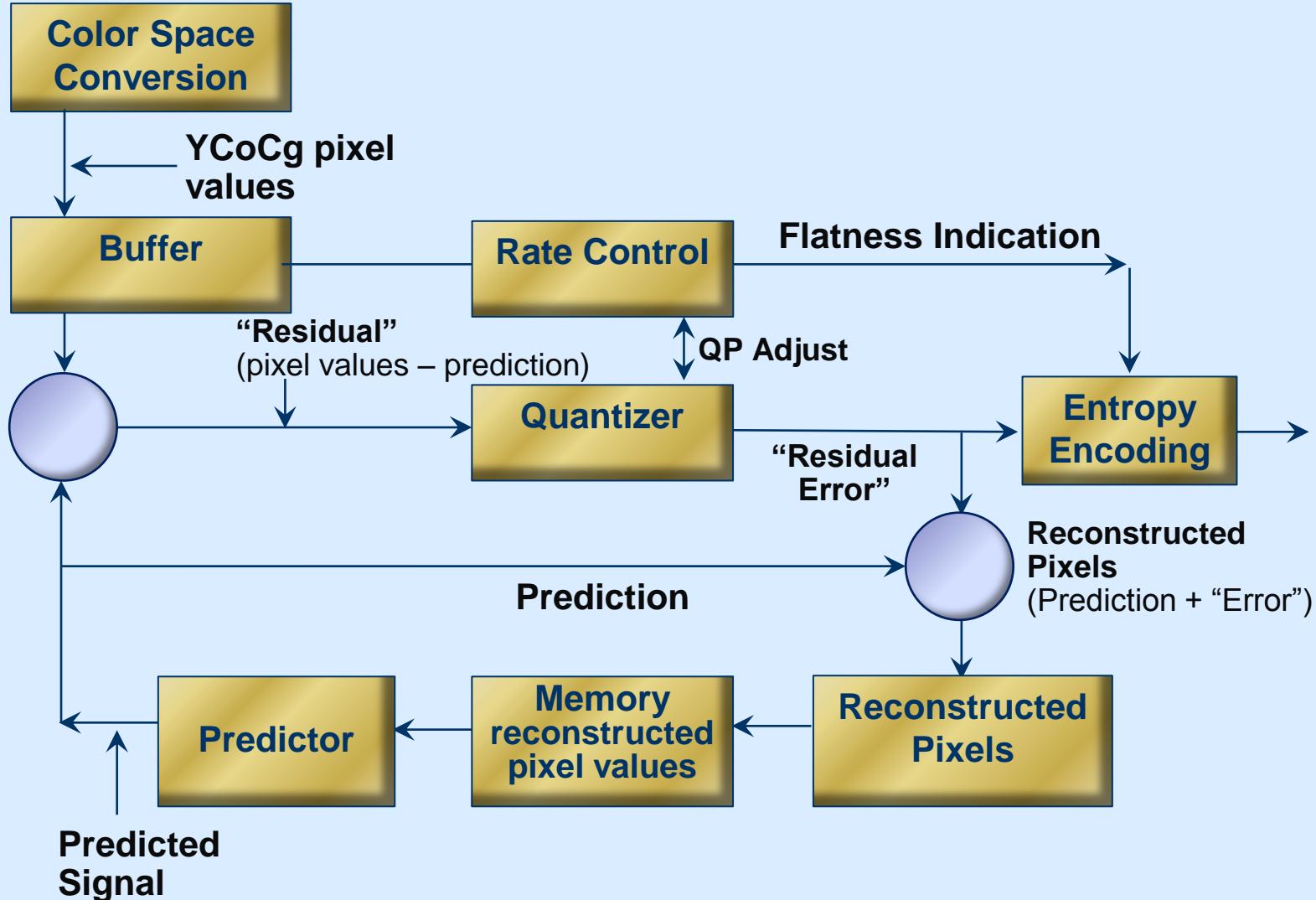
- Display Stream Compression – How it Works:
 1. Color Space Conversion – **RGB inputs are converted to YCoCg-R.**
 2. Prediction – One of three (3) models:
 - 1) Median-Adaptive, 2) Block, 3) Midpoint.**
 3. Indexed Color History – An **alternative to Prediction** where recently used pixel values are stored and available to be referenced.
 4. Quantization – Assigns bit values to a residual sample produces some level of error, i.e. **lossy component**.
 5. Pixel Reconstruction – Recreating the pixels in the encoder using the same method used in the decoder.
 6. Entropy Encoding – A way of encoding values such that the more frequently occurring values are encoded with fewer bits than less frequently occurring values.
 7. Rate Control – Process to ensure proper bitstream flow. Manages buffer fullness to ensure that it is not underflowed or overflowed. Controls quantization in association to flatness.
 8. Flatness determination – Flatness is the uniformity of pixel values or “smoothness” in an area of the video; contrasted with “business”.

Display Stream Compression – MMAP Prediction Method



- Prediction methods use a **simple assumption that adjacent pixels are highly correlated**. A current pixel value can be predicted reasonably well based on the neighboring pixel values.
- Temporal vs Spatial prediction.
 - Temporal prediction works **between frames**. Best when there is little motion between frames.
 - **Spatial prediction** works **within a frame**. Best with high motion areas.
 - Spatial redundancy is what is reduced in **DSC**.

Display Stream Compression – Prediction & Flatness Indication & QP Adjustment



- Prediction is **subtracted from actual pixel value to produce a “residual.”**
- Predictor uses “reconstructed pixels” in the prediction, not the actual pixel values.
- Quantizer converts the “Residual” into a quantized output (a “**Residual Error**”).
- The **prediction residual with the quantized error is transmitted over the display link.**
- **Prediction method** used is determined by the encoding and decoding algorithms; the selected prediction method is **not transmitted over the link**.
- “Flatness” is a **measure of smoothness or similarity** in pixel values in a region.
- Flatness is used by the Rate Controller to adjust the “**Quantization Parameter**” (QP) which controls the quantization error introduced depending on the flatness.
- The **flatter the region the less errors that can be tolerated** because they are far more noticeable than “busy” areas.
- **Indication of flatness is transmitted over the link** using a code sequence in the luma (Y) component values.

DSC / FEC Setup Sequence

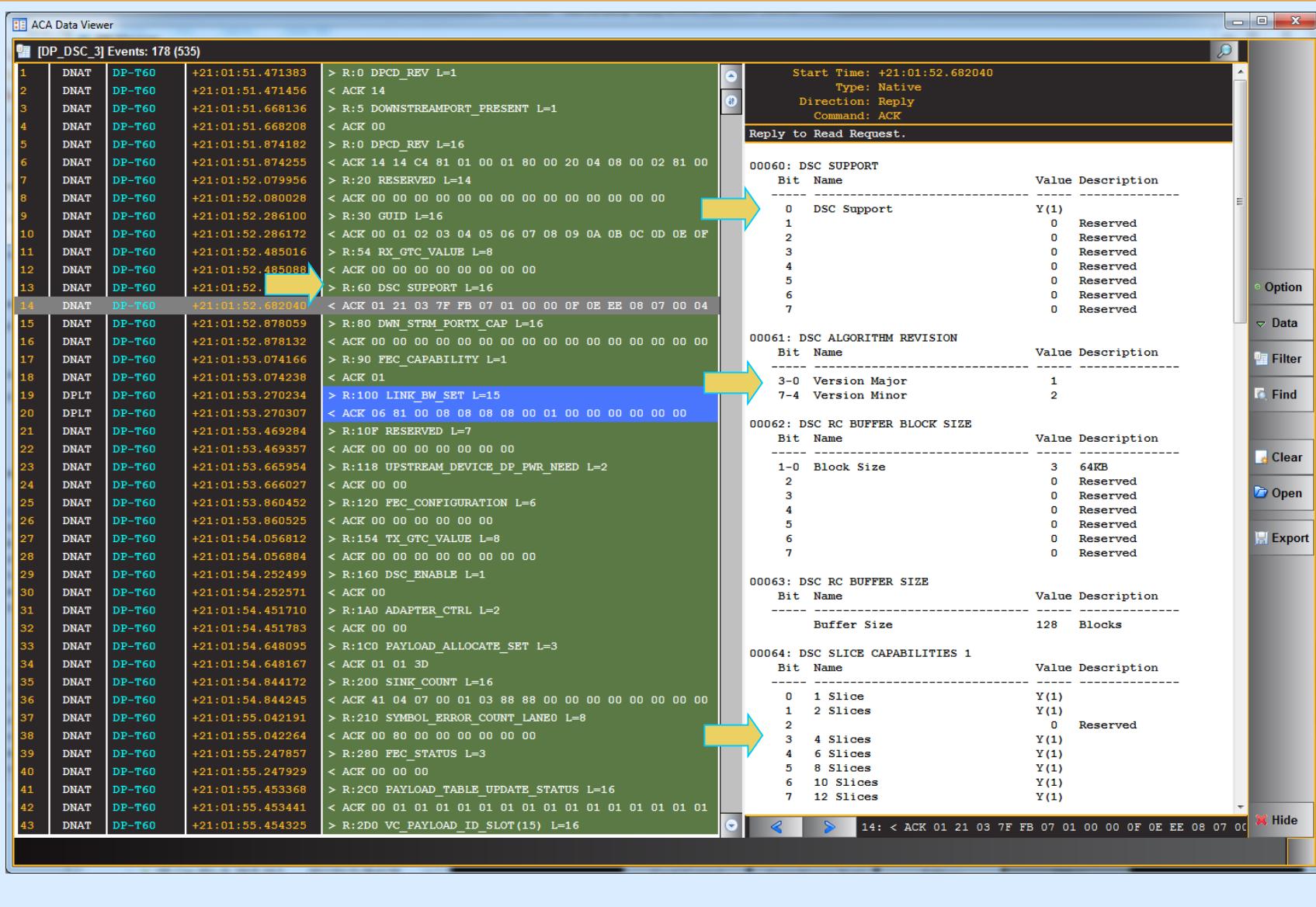


Display Port Connection Sequence with Forward Error Correction & DSC



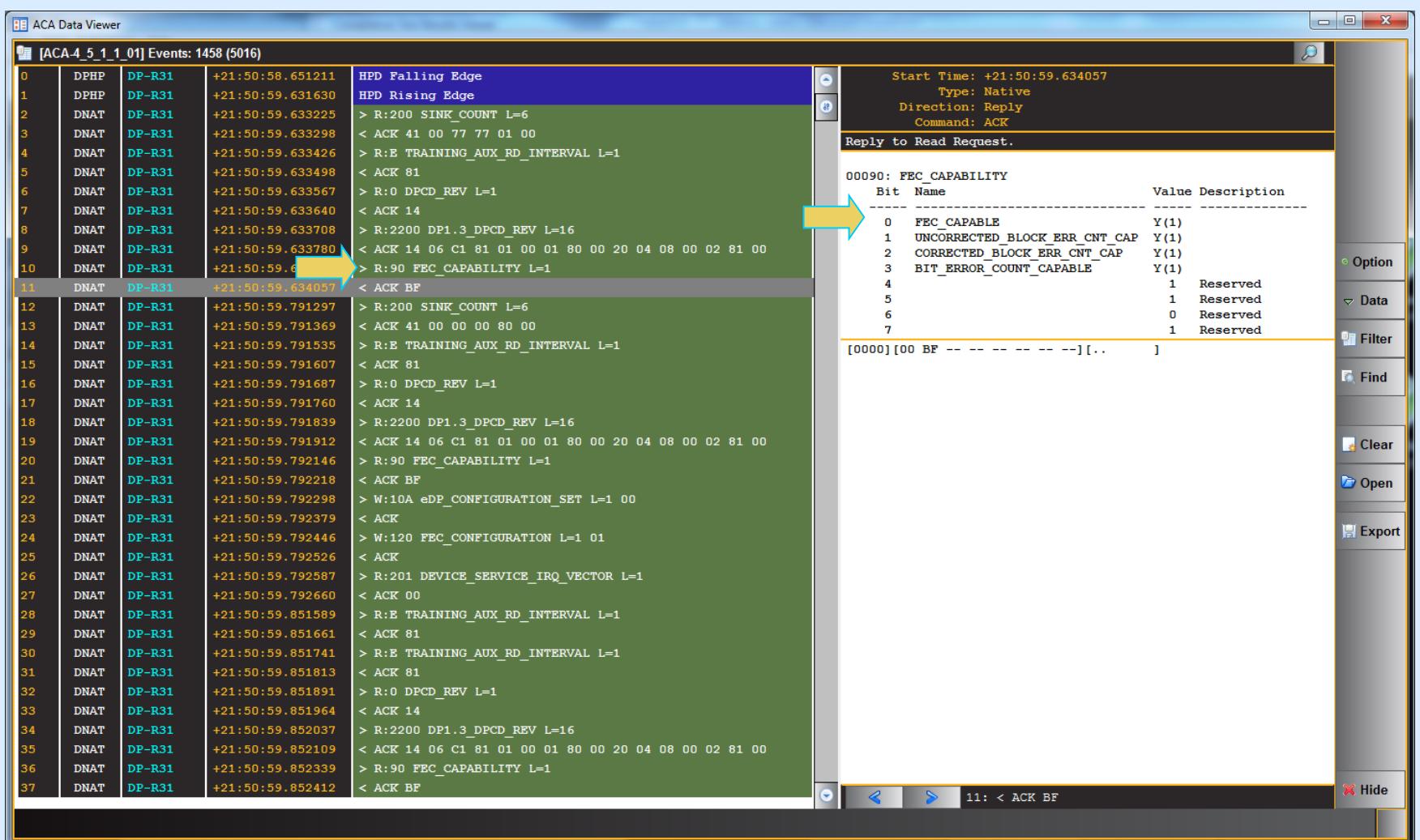
- **Hot Plug.** Indication to the Source that there is a Display device connect to it.
- **EDID read (Aux Chan).** EDID is a data structure provided by a DisplayPort display that describe its video and audio capabilities to a DisplayPort video source.
- **DPCD read (Aux Chan).** DPCD is a data structure provided by a DisplayPort device that describe its link capabilities and its **DSC and FEC capabilities** to a DisplayPort source.
- **Enable FEC.** Source writes to DPCD to enable FEC Ready bit.
- **Enable DSC.** Source writes to DPCD to enable DSC Decompression Enable bit.
- **Link Training (Aux Chan):** 1) Clock Recovery, 2) Channel Equalization, Symbol Lock and Inter-Lane alignment. **Note:** Link training establishes the physical link parameters (number of lanes, link rate, voltage swing, pre-emphasis, equalization) used for transmission of video and audio over the Main Link.
- **HDCP Authentication (Aux Chan).** For video/audio content flagged for content protection, High-bandwidth Digital Content Protection authentication is required.
- **FEC Enable (Main Link).** Transmit FEC Decode Enable sequence (K-Character sequence).
- **DSC/FEC AV Transmission.** Compressed, encrypted video transmission with FEC is initiated. Picture Parameter (PPS) metadata is transmitted, VB-ID compressed flag is set.

Connection Sequence – Read Sink DSC-Related DPCD Capabilities



- Source reads sink DPCD registers to determine DSC capabilities of sink.
- Example showing the following registers:
 - **DSC Support.** Indicates if DSC is supported in the DP sink.
 - **DSC Algorithm Revision.** Version of DSC supported.
 - **DSC Rate Control Buffer Block Size.** Block size of the memory blocks in the Rate Control Buffer.
 - **DSC Rate Control Buffer Size** – Number of RC memory blocks.
 - **DSC Slice Capabilities** – Indicates the number of slices supported.

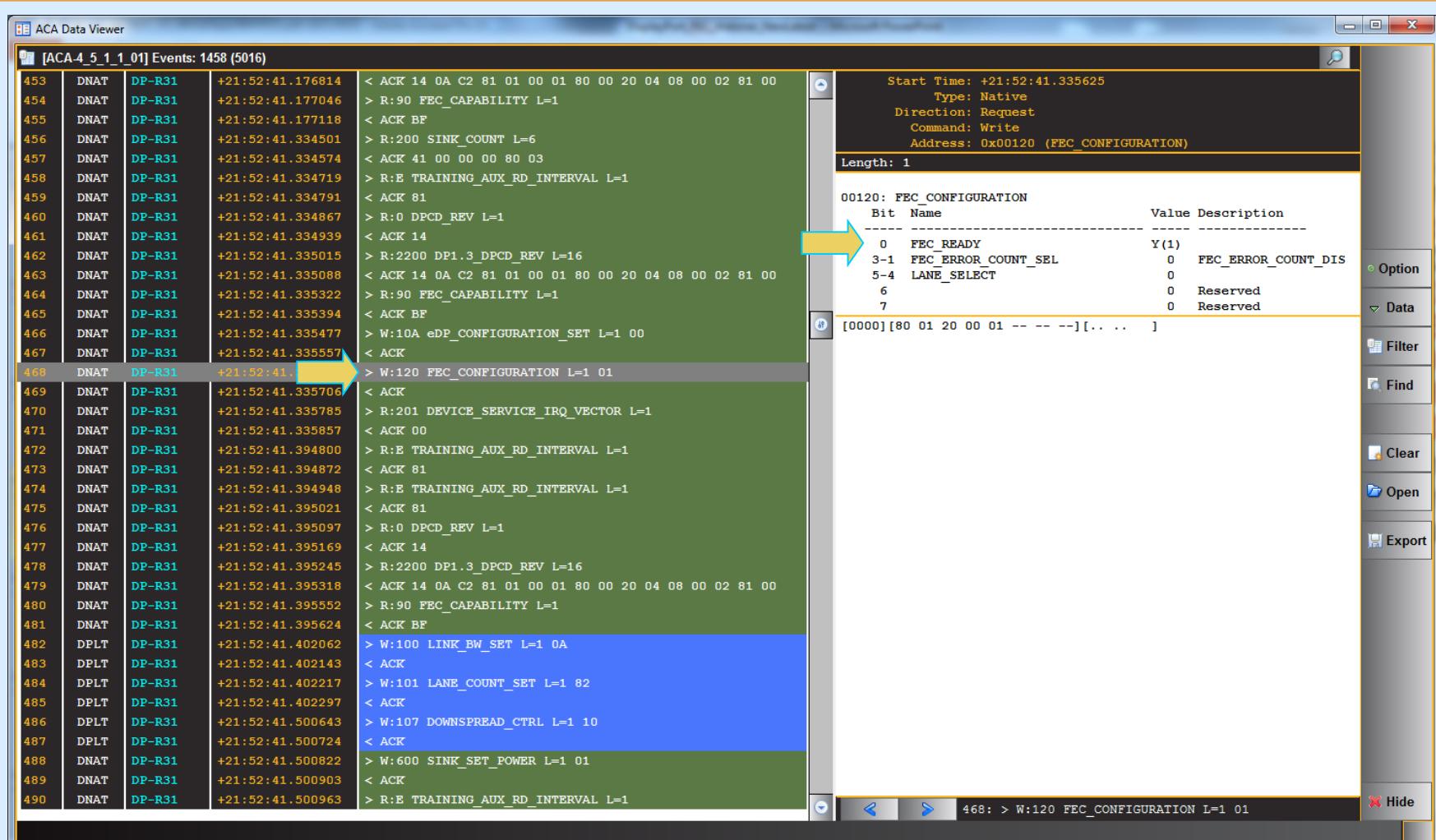
Connection Sequence – Read Sink FEC Capabilities in DPCD Registers



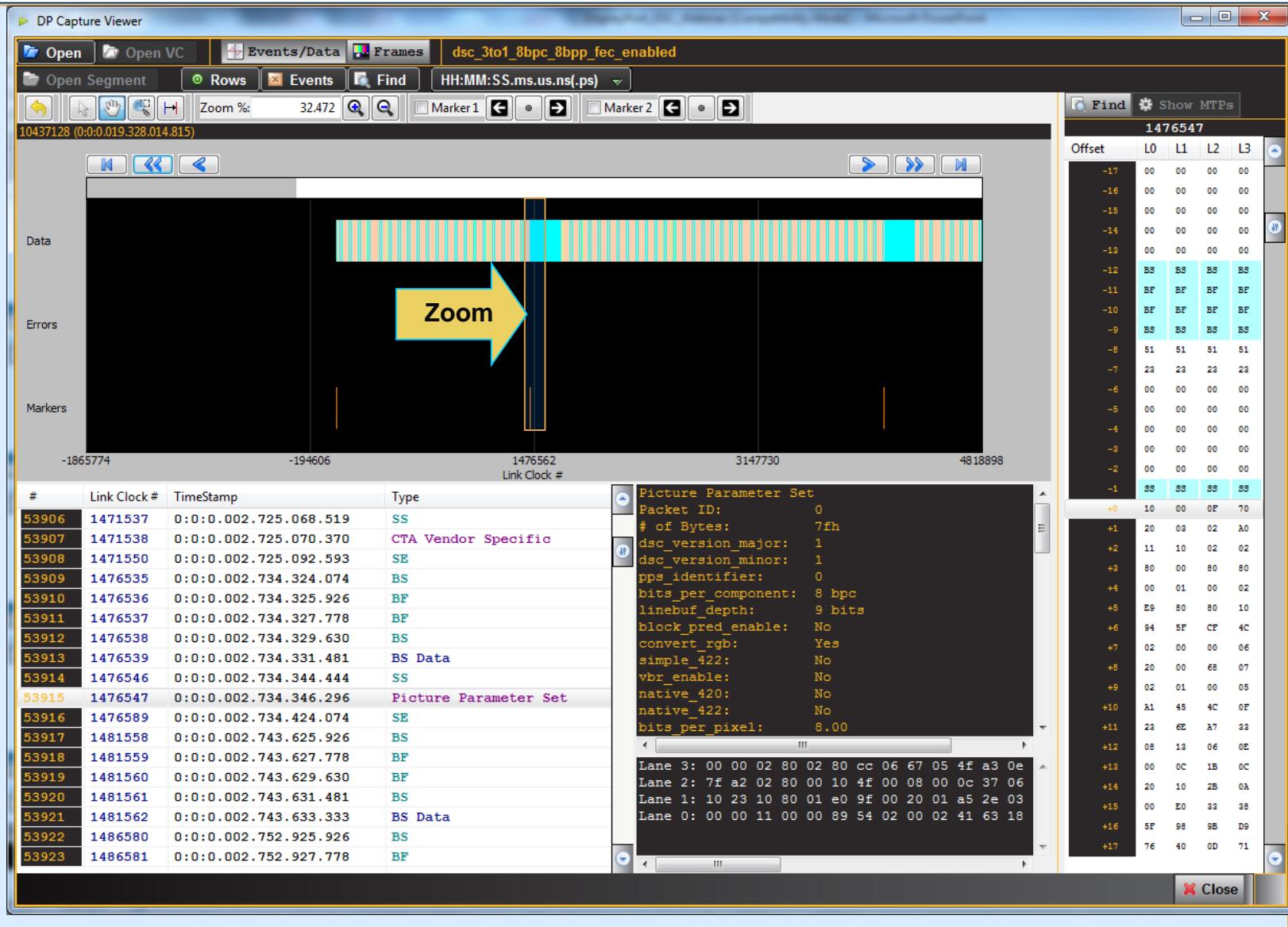
- Source reads sink DPCD FEC Capability registers to determine if sink is FEC capable.
- Source also verifies that sink has declared the FEC register counters.

Connection Sequence – Write Sink FEC Ready Flag in DPCD Registers

- Source writes sink DPCD FEC Configuration registers to set FEC Ready flag.

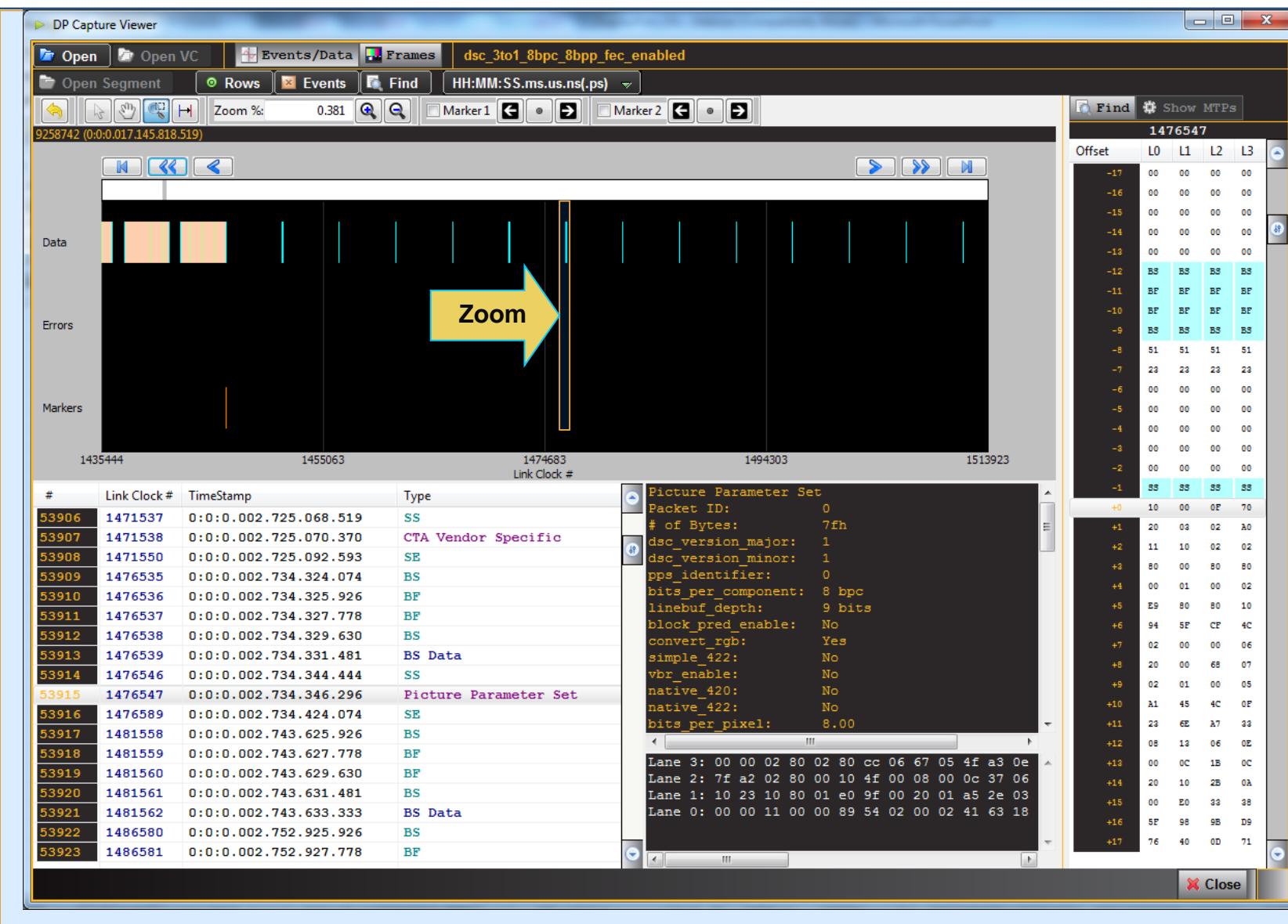


Display Stream Compression – Picture Parameter Set



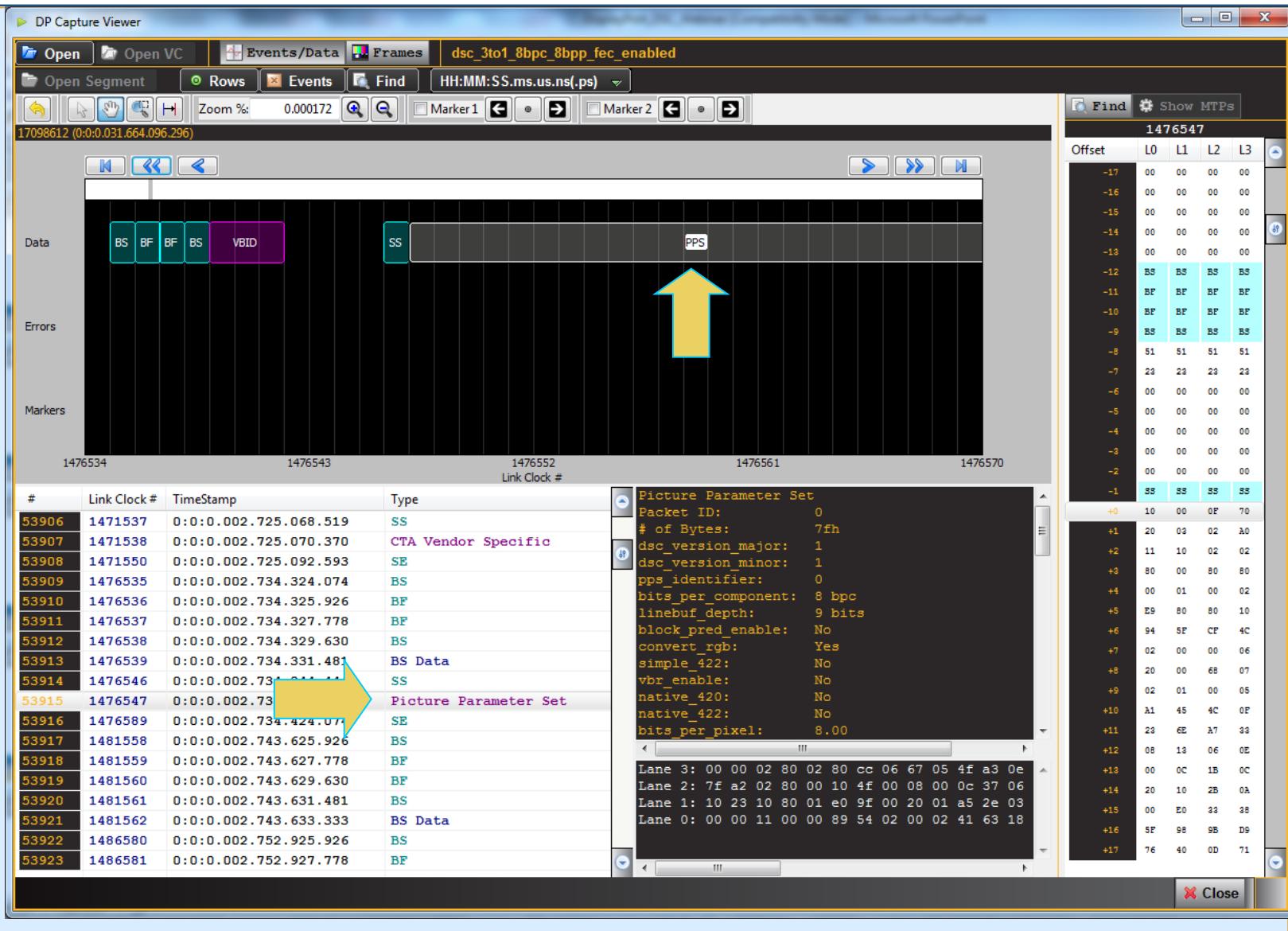
- Zoomed out view showing beginning of video and vertical blanking periods visible.

Display Stream Compression – Picture Parameter Set



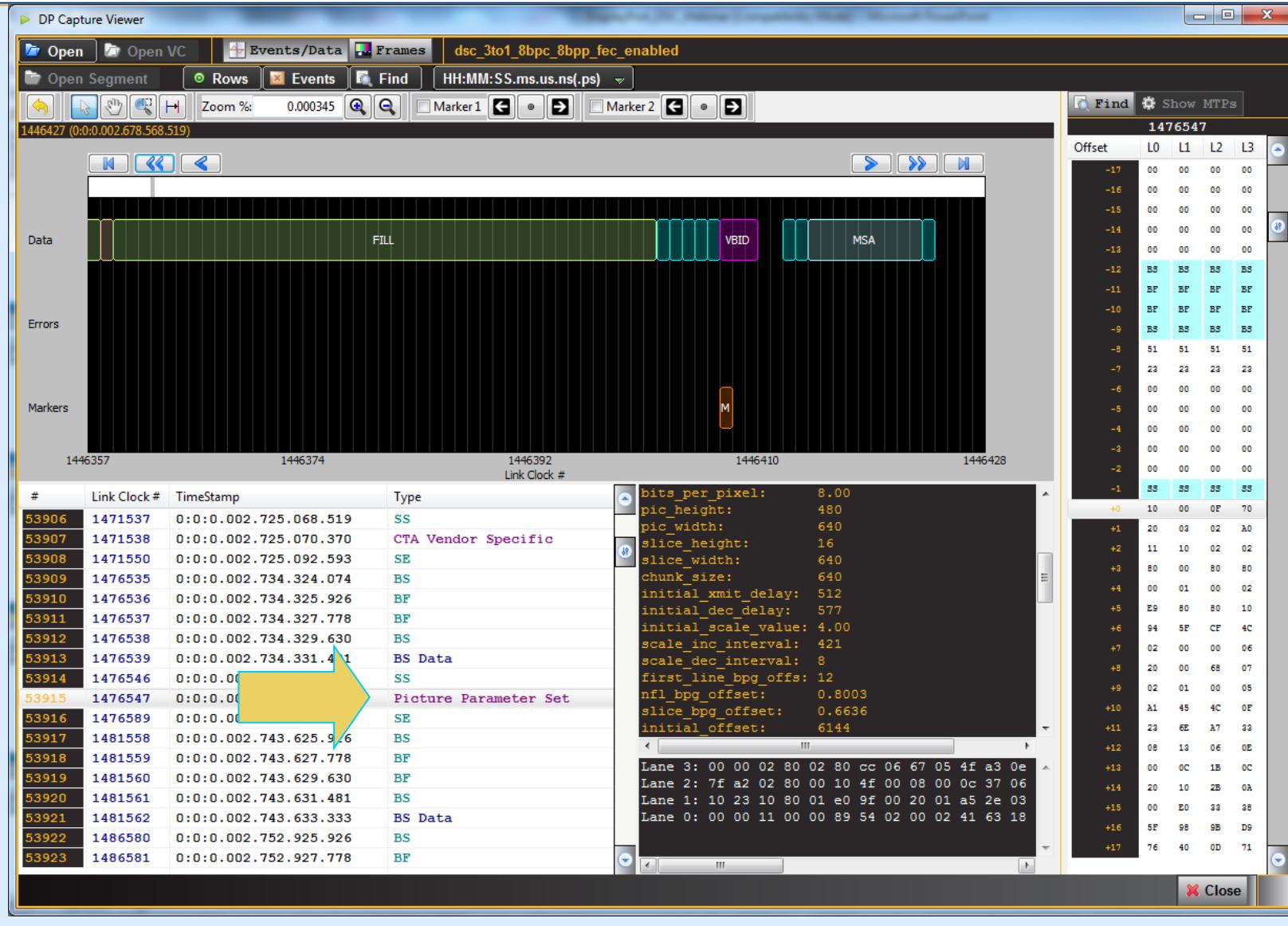
- Zoomed in to show end of a line of video with packets in the vertical blanking period shown.

Display Stream Compression – Picture Parameter Set



- Picture Parameter Set showing the following parameters:
 - Bits per Pixel – Specifies the target bits per pixel the encoder uses.
 - Picture Height – Number of lines in the video frame being encoded.
 - Picture Width – Number of pixels per line of the video frame being encoded.
 - Slice Height – Number of lines in each Slice.
 - Slice Width – Number of pixels per line of each Slice.
 - Chunk Size – Number of bytes (pixels) in a chunk. This is a function of the slice width.

Display Stream Compression – Picture Parameter Set (continued)



- Picture Parameter Set showing the following parameters:
 - Bits per Pixel – Specifies the target bits per pixel the encoder uses.
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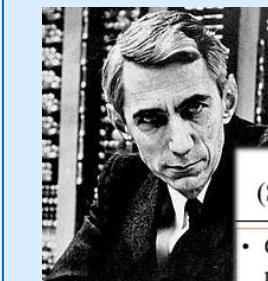
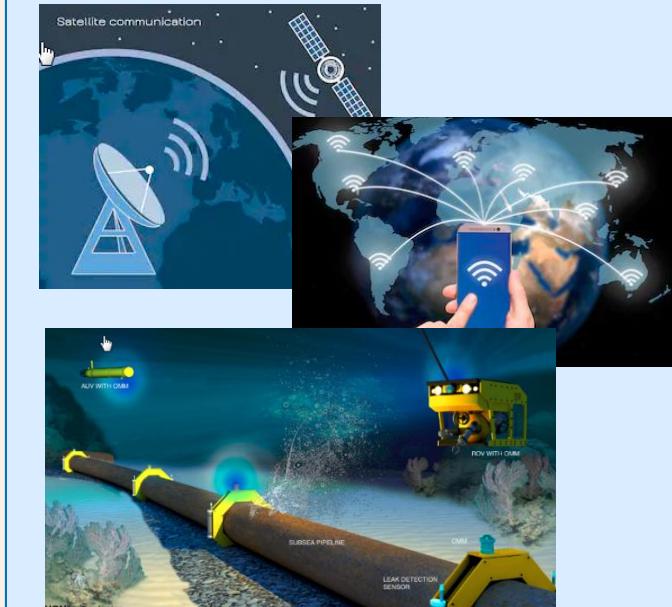
DisplayPort Forward Error Correction (FEC) Overview and Operation



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DisplayPort Forward Error Correction – Overview

- Forward Error Correction is a means for transmitting data reliably across a noisy channel.
- Error Handling Mechanisms:
 - Retransmission – Detecting errors and requesting a retransmission through a reverse channel.
 - Forward Error Correction – Used where the receiver does not have capabilities to request retransmission or doing so would result in intolerable latency.
- FEC applications include: Broadcast, Wireless communications, Satellite communication, underwater cable data transmission, now for video communication. Anywhere there is a noisy channel and where the latency of retransmission cannot be tolerated, FEC is the preferred solution for error handling.
- FEC technology allows today's systems to approach the Shannon limit. The Shannon Limit is the theoretical maximum bandwidth of a channel when taking in to account the noise of the channel.
- FEC provides a “Coding Gain” by enabling the system to transmit data reliably at a lower power level.



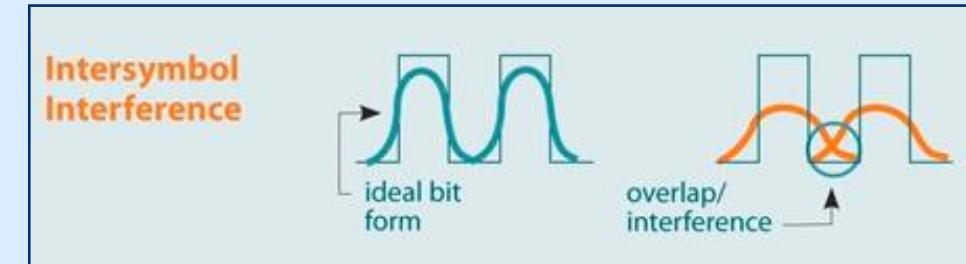
Shannon's Law

(Shannon's Limit for Information Capacity)

- Claude Shannon at Bell Labs figured out how much information a channel could theoretically carry
- $C = B \log_2 (1 + S/N)$ Note we are back to log base 2!
 - Where C is Information Capacity in bps
 - B is bandwidth in Hz
 - S/N is Signal-to-Noise ratio
 - (unitless...don't make into dB)

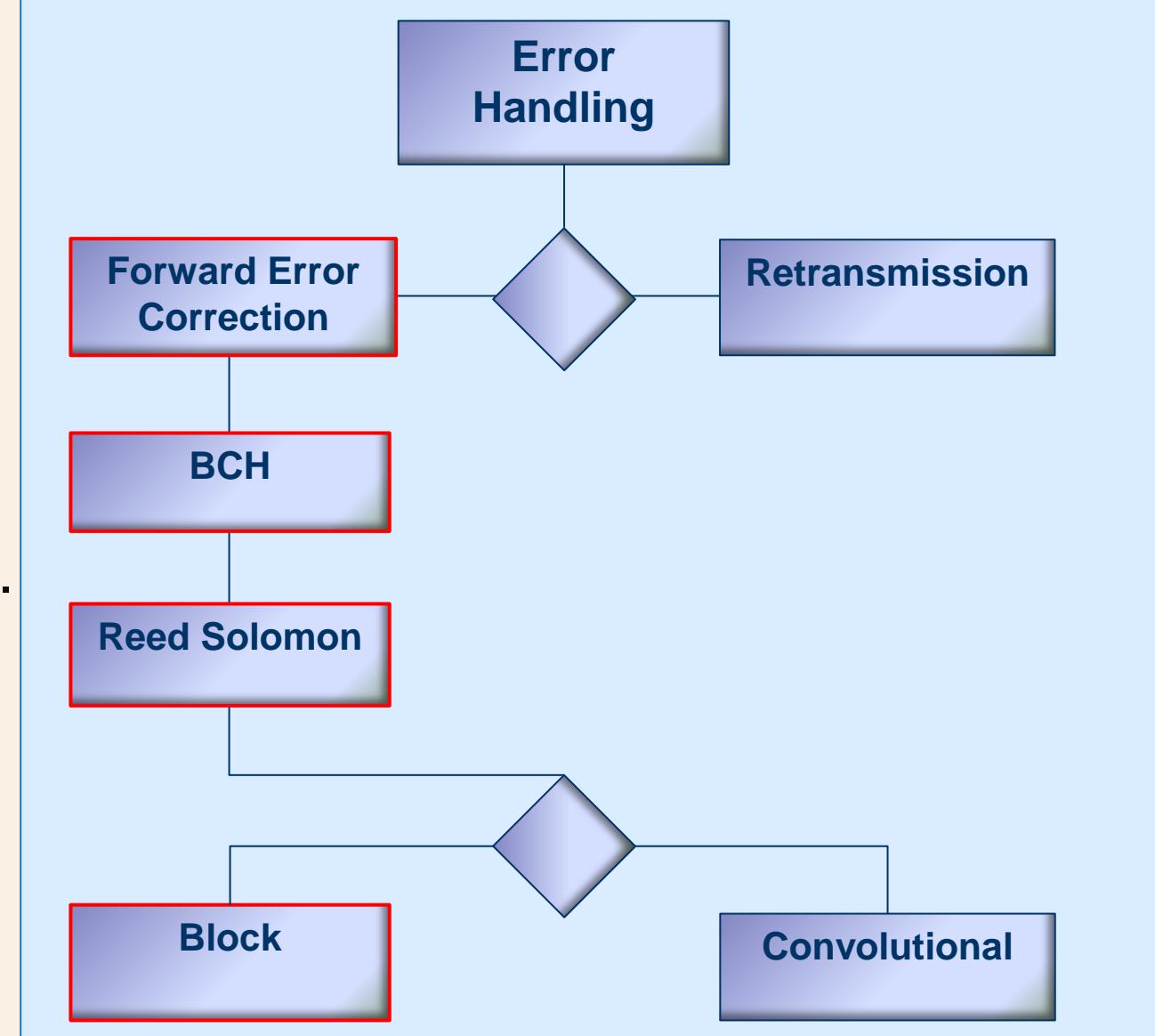
Why is Forward Error Correction (FEC) Needed for DisplayPort?

- FEC is needed for DisplayPort because:
 - Higher data rates are more prone to transmission errors. Errors caused by: impulse noise, cross talk, **signal distortion** which results in Inter-Symbol interference.
 - DSC compressed streams are more susceptible to visual artifacts. A single bit error in a compressed stream results in more pervasive artifacts whether in audio or video.
- In the case of Display Stream Compression (DSC), the partitioning of the DSC frame “Slices” limits the propagation of visual artifacts resulting from errors.
- DSC requires FEC but FEC doesn’t require DSC.
- FEC is well suited to the bursty nature of errors in high speed digital transmission.



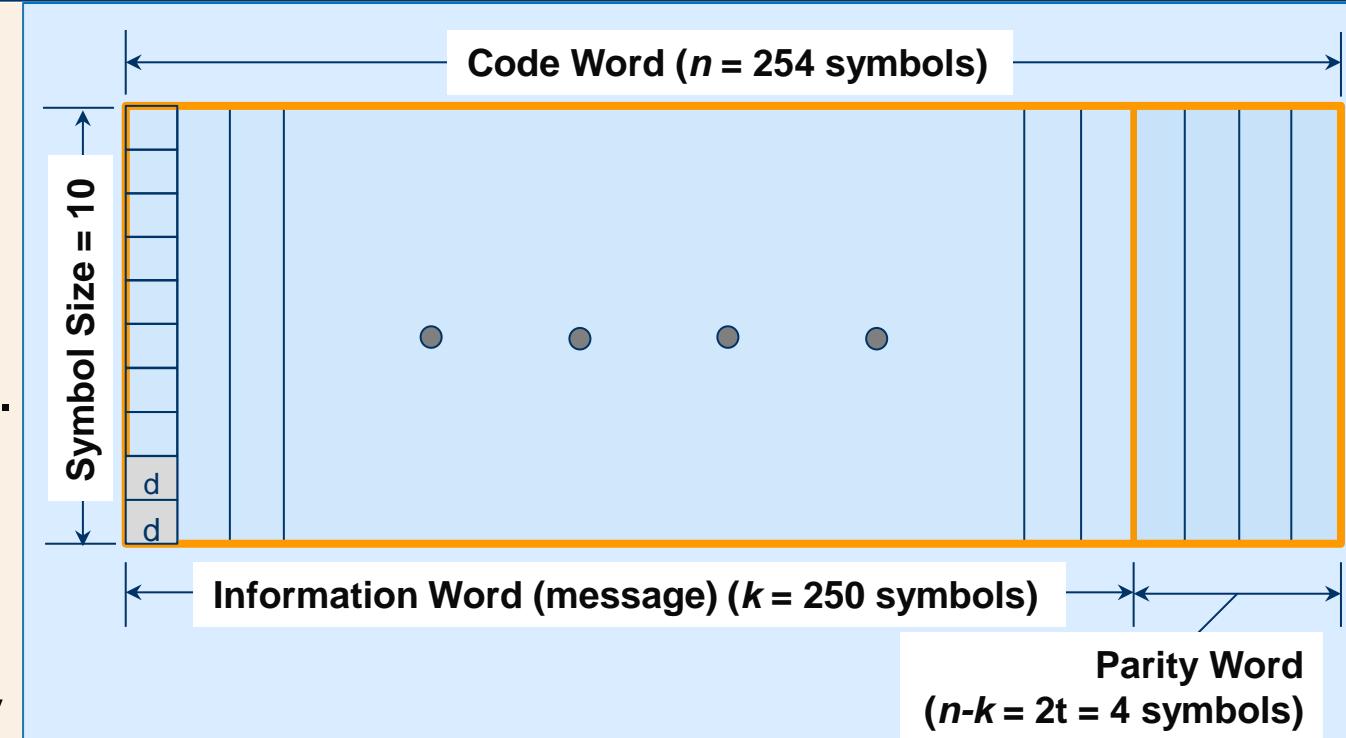
Reed Solomon Forward Error Correction – Overview

- Reed Solomon FEC has been applied to: mobile networks, broadcast, satellite communications, internet, data storage, barcodes, QR codes, etc.
- RS is excellent for handling burst errors because multiple bit errors in a symbol count as a single correctable error.
- Reed Solomon belongs to the BCH family of error correcting codes. But works on a block of symbols rather than bits at a time.
- RS is a Block Code – Reed Solomon operates on a block of data symbols at a time.
- RS is a Systemic Code – Code appends extra data bytes (parity bytes) to an information word without changing the information word.

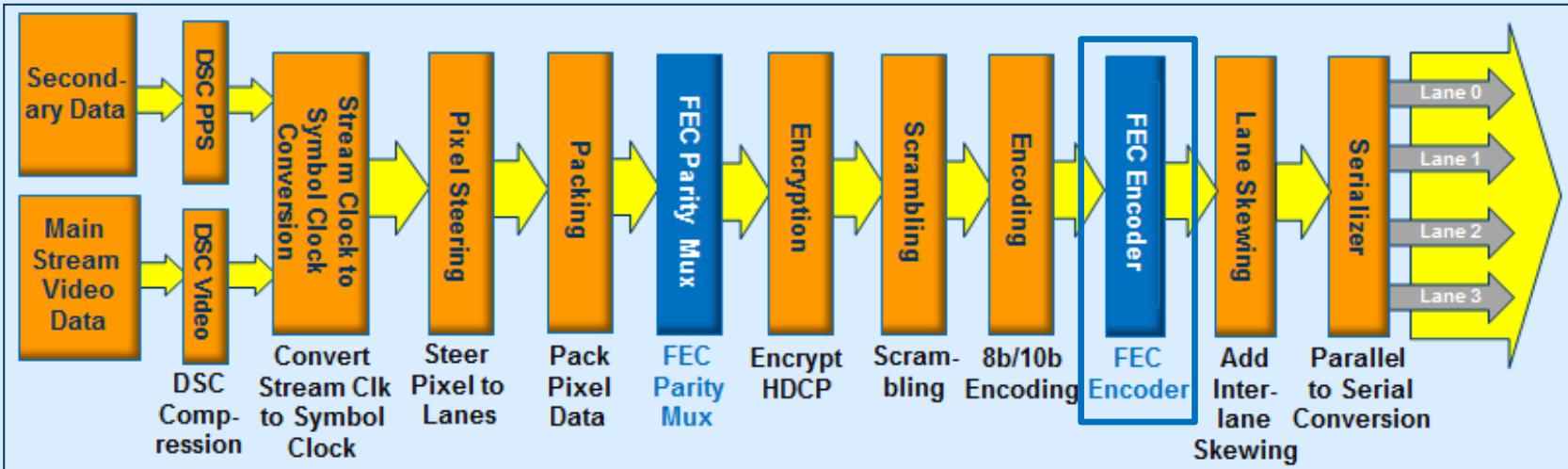


DisplayPort Forward Error Correction – Overview

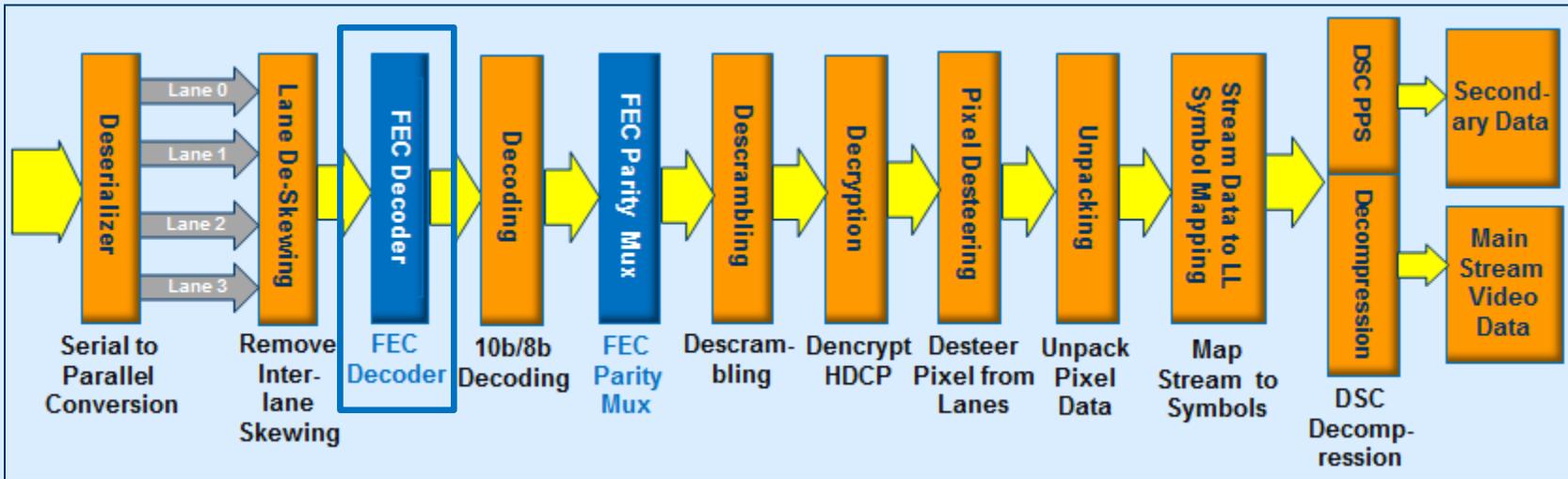
- DisplayPort uses Reed Solomon FEC which is a “Block” based forward error correction method.
- In the Block method, FEC works on a block of data at a time. Where:
 - k – is the “Information Word” (the block). The block contains a specific number of symbols. In DisplayPort FEC, k is 250 symbols.
 - n – is the “Code Word” which includes the information word and the FEC parity symbols. In DisplayPort FEC, n is 254 symbols.
 - t – is the “Error Correction Factor”. It is the number of symbol errors that can be corrected. It is half the number of parity symbols (4). In DisplayPort, t is 2 as two (2) symbol errors can be corrected per block.
 - m – is the symbol size; the smallest correctable entity. In DisplayPort, symbol size m is 10.
Note: If there are multiple errors per symbol, this counts as a single correctable symbol error.
 - The overhead for the DisplayPort implementation of FEC is 2.4%.



DisplayPort Main Link Functional Blocks – FEC Reed Solomon Encoding



- DisplayPort Transmitter Functional Block Diagram



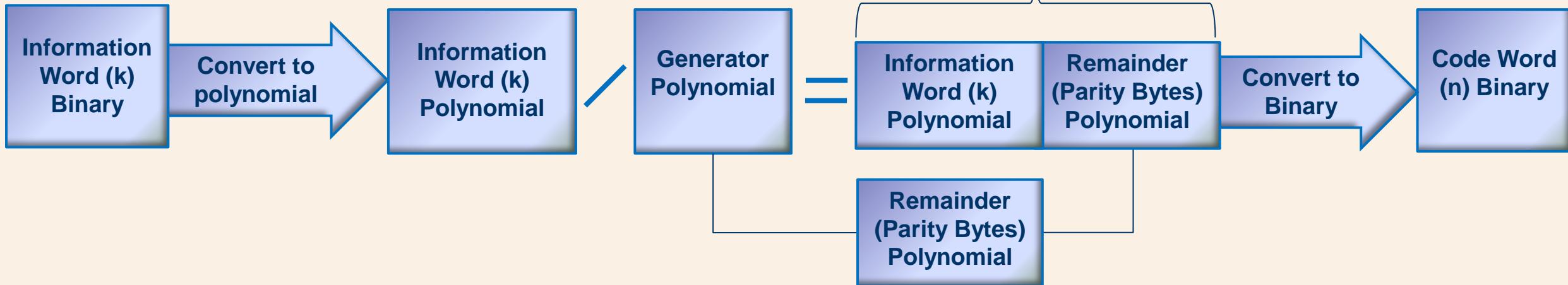
- DisplayPort Receiver Functional Block Diagram

Reed Solomon Forward Error Correction (FEC) – In a Nutshell (continued)

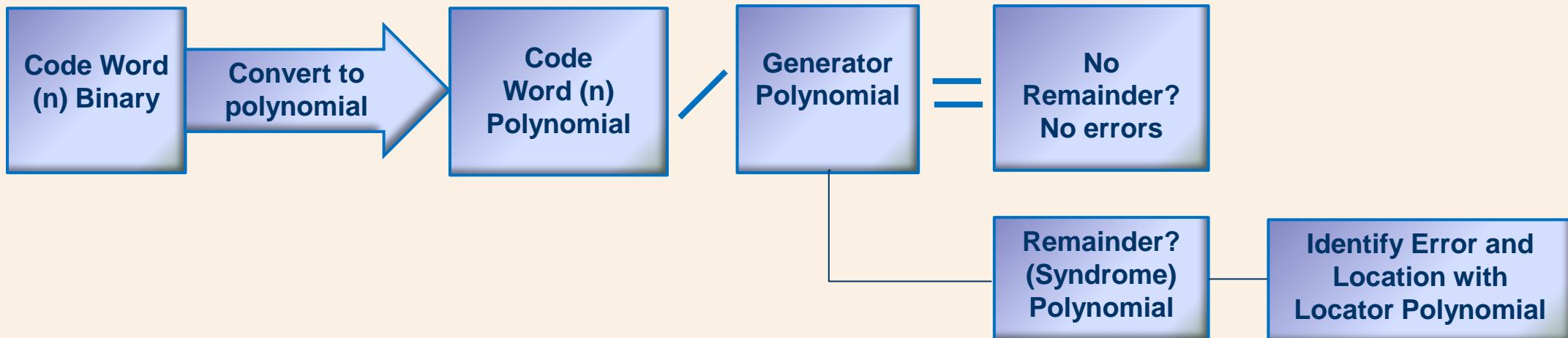
- **Basic Idea:**
 - The concept of Reed Solomon (RS) FEC is that the data is structured in a way that enables us to guess what the real data should be if there is a corruption just by correcting the structure.
 - With Reed Solomon FEC you add additional bytes “parity bytes” to the original message (“information word” [k]) resulting in a (“code word” [n]) to be transmitted in order to enable identification of a corrupted message with its most likely intended message.
 - The secret of RS encoding is that the valid code word values within a “finite field”, are maximally and relatively equally separated from one another in numerical space—Hamming distance.
- **Terminology:**
 - Finite Field (Galois Field) – A limited set of values whose relationship to one another is such that when you perform arithmetic on the members, another member of the field always results.
 - Polynomial – A mathematical expression consisting of variables and coefficients. The information words and code words are represented as polynomials in the FEC encoder and decoder. The binary numbers digits are the coefficients of a polynomial.
 - Generator Polynomial – A special primitive polynomial without factors used to generate RS-FEC Code Words. All Code Words are multiples of the generator polynomial.
 - Modulo (clock arithmetic) – A system of arithmetic of integers where the numbers wrap around when they reach a certain value. In RS-FEC the generator polynomial is the modulo operator.
 - Hamming Distance – The numerical distance between values of equal length.
 - Syndrome – A remainder following polynomial division. A syndrome is an error vector that is used to identify an error and locate where the error occurred and correct the error.

Reed Solomon Forward Error Correction (FEC) – In a Nutshell (continued)

RS-FEC Encoder



RS-FEC Decoder

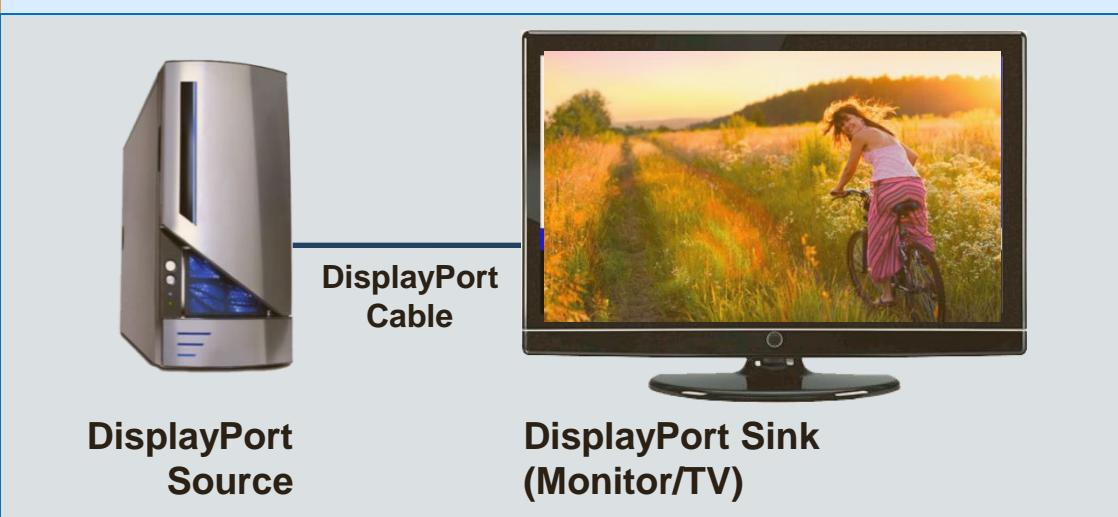
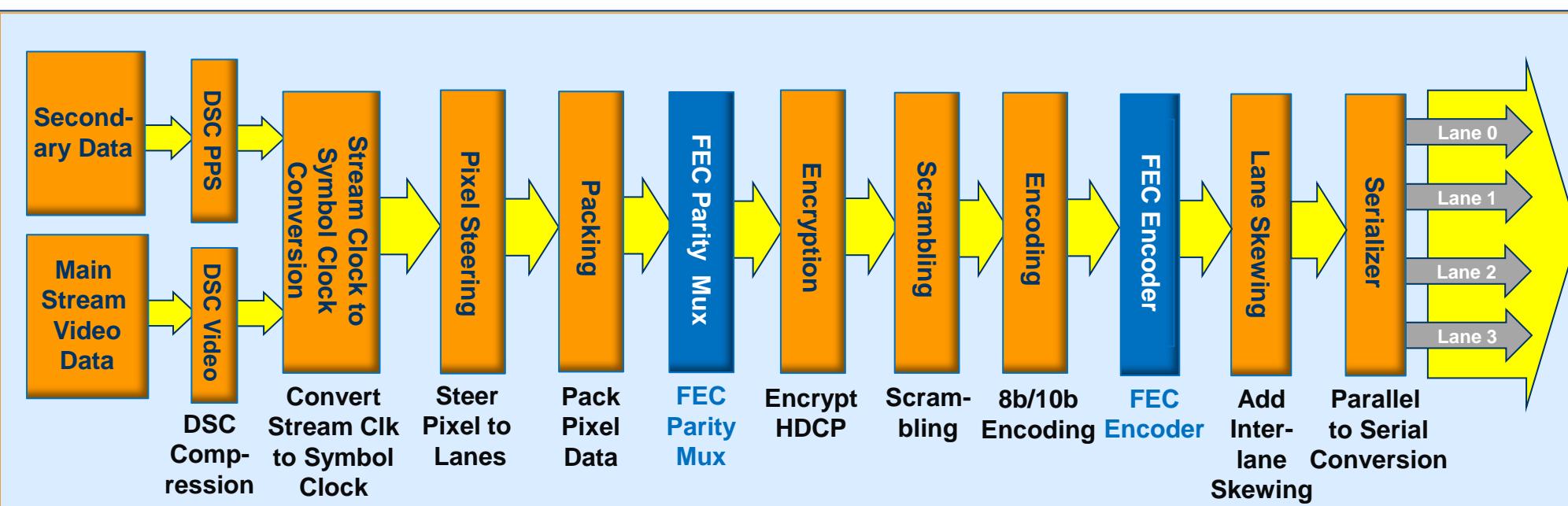


DisplayPort Forward Error Correction (FEC) Encoding Process



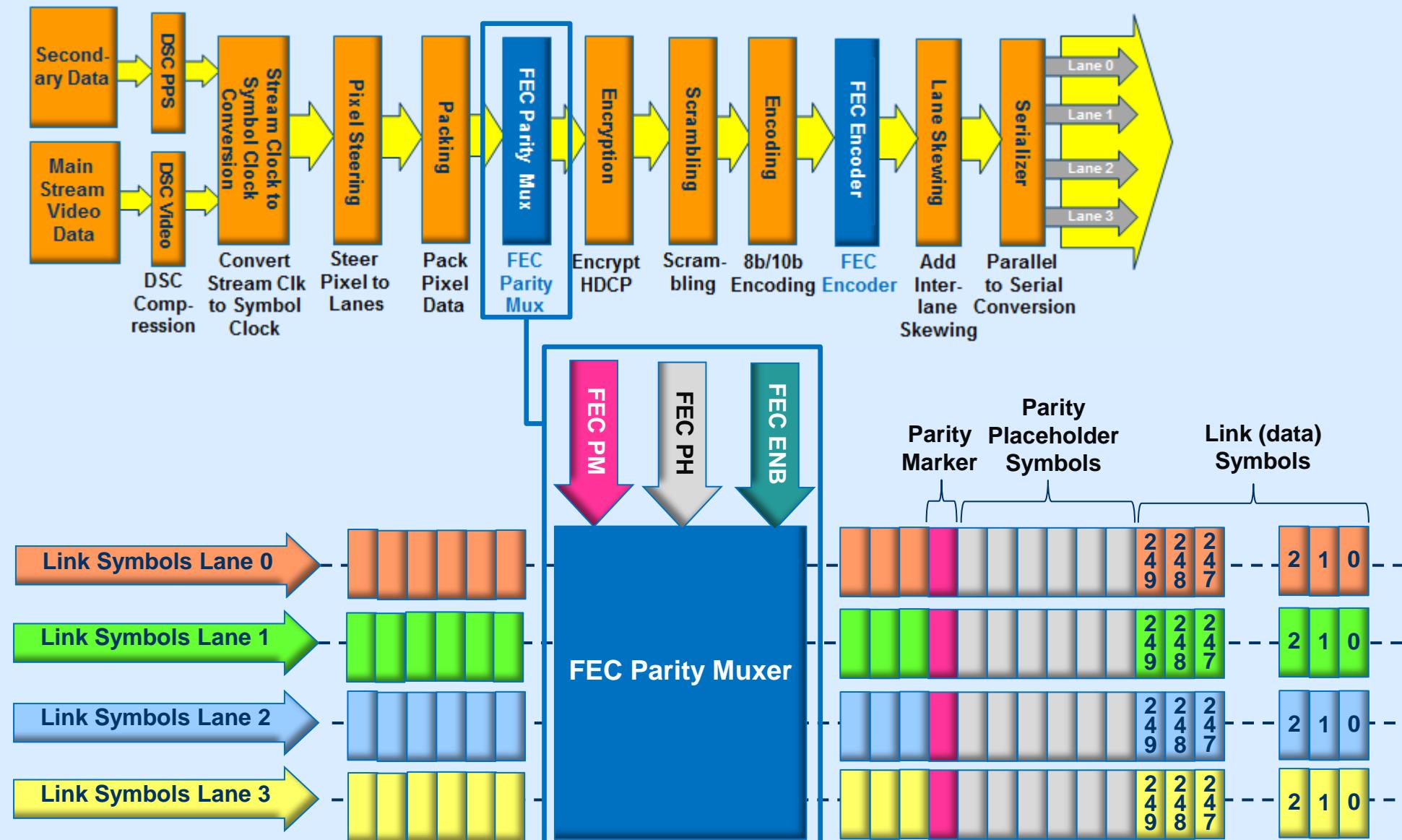
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DisplayPort Main Link Transmitter Functional Blocks



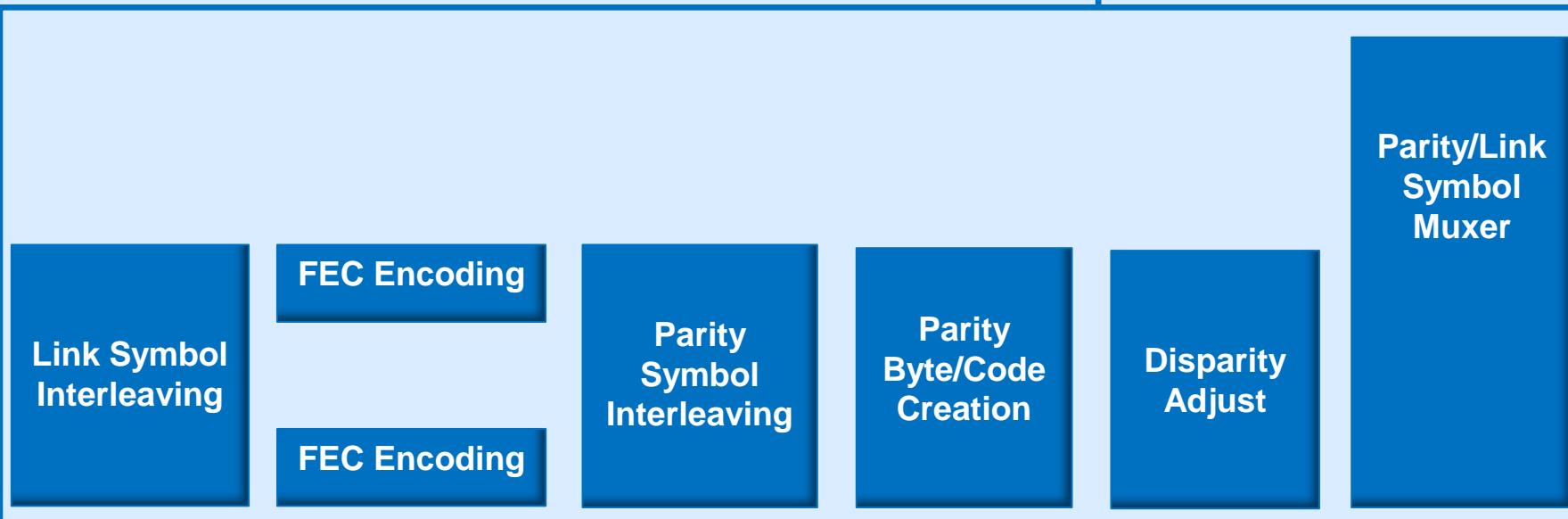
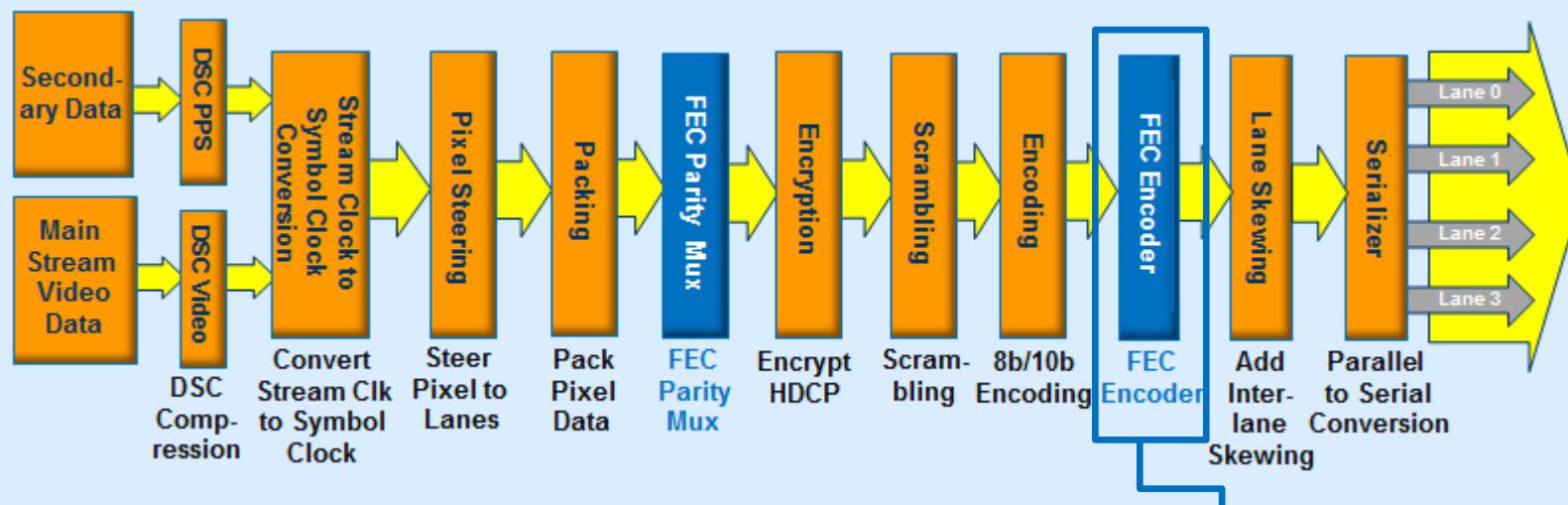
- **FEC Encoding Blocks:**
 - FEC Parity Muxer.
 - FEC Encoder.
- **FEC Parity Muxer:**
 - Inserts Parity Marker.
 - Initiates FEC enable sequence.
 - Inserts Parity placeholder.
- **FEC Encoder:**
 - Removes FEC Parity placeholders.
 - Interleaves symbols between lanes.
 - Calculates/Adds Parity Codes.
 - Interleaves Parity Codes between lanes
 - Accounts for disparity.
 - Muxes Parity Codes with link symbol.

DisplayPort Main Link Transmitter Functional Blocks (E.g. 4 lanes) – FEC Muxer



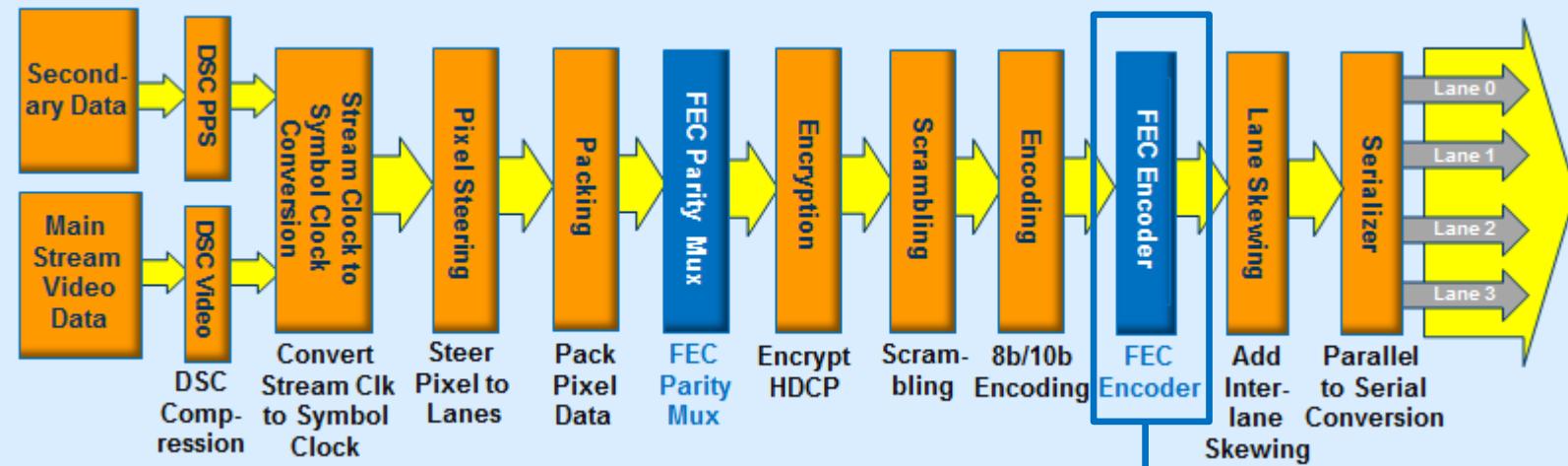
- FEC Muxer:**
- Insert Parity Marker:**
 - Add Parity Marker every 255 FEC blocks.
- Initiate FEC Enable Sequence:**
 - Send K-Character sequence to enable FEC.
- Insert Parity Placeholders:**
 - Placeholders are temporary.
 - They are removed and replace with Parity Codes by the FEC Encoder.

DisplayPort Main Link Transmitter Functional Blocks – FEC Encoder

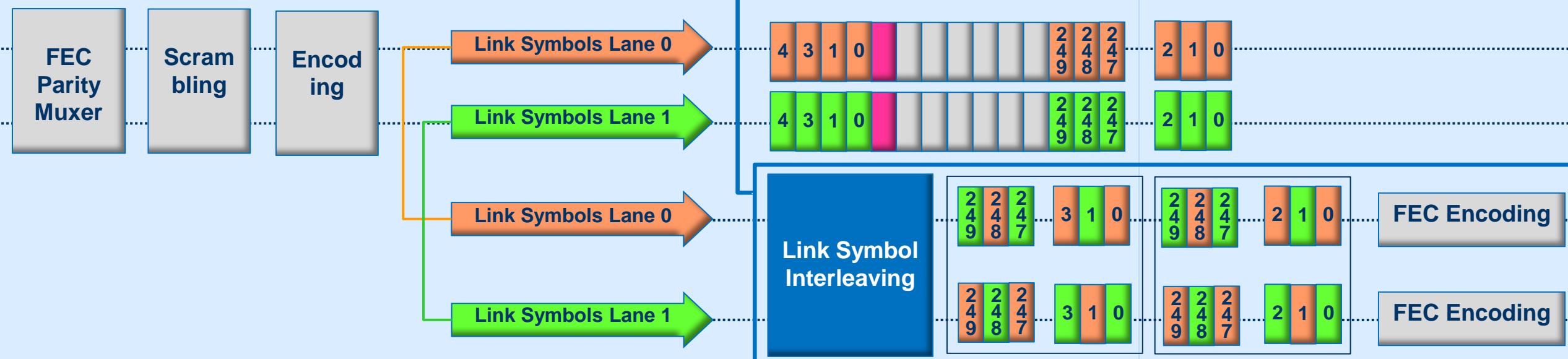


- **FEC Encoder:**
- **Link Symbol Interleaving:**
 - Interleaves symbols from lane pairs.
- **FEC Encoding:**
 - Calculates Reed Solomon Parity Symbols.
- **Parity Code Interleaving:**
 - Interleaves Parity Symbols from lane pairs.
- **Parity Byte Creation:**
 - Creates 5 Parity Bytes from 4 Parity Symbols.
- **Running Disparity Adjustment:**
 - Adds an adjusted disparity byte to Parity Codes.
- **Parity Code/Link Symbol Muxing:**
 - Multiplexes Parity Codes into Link Symbols.

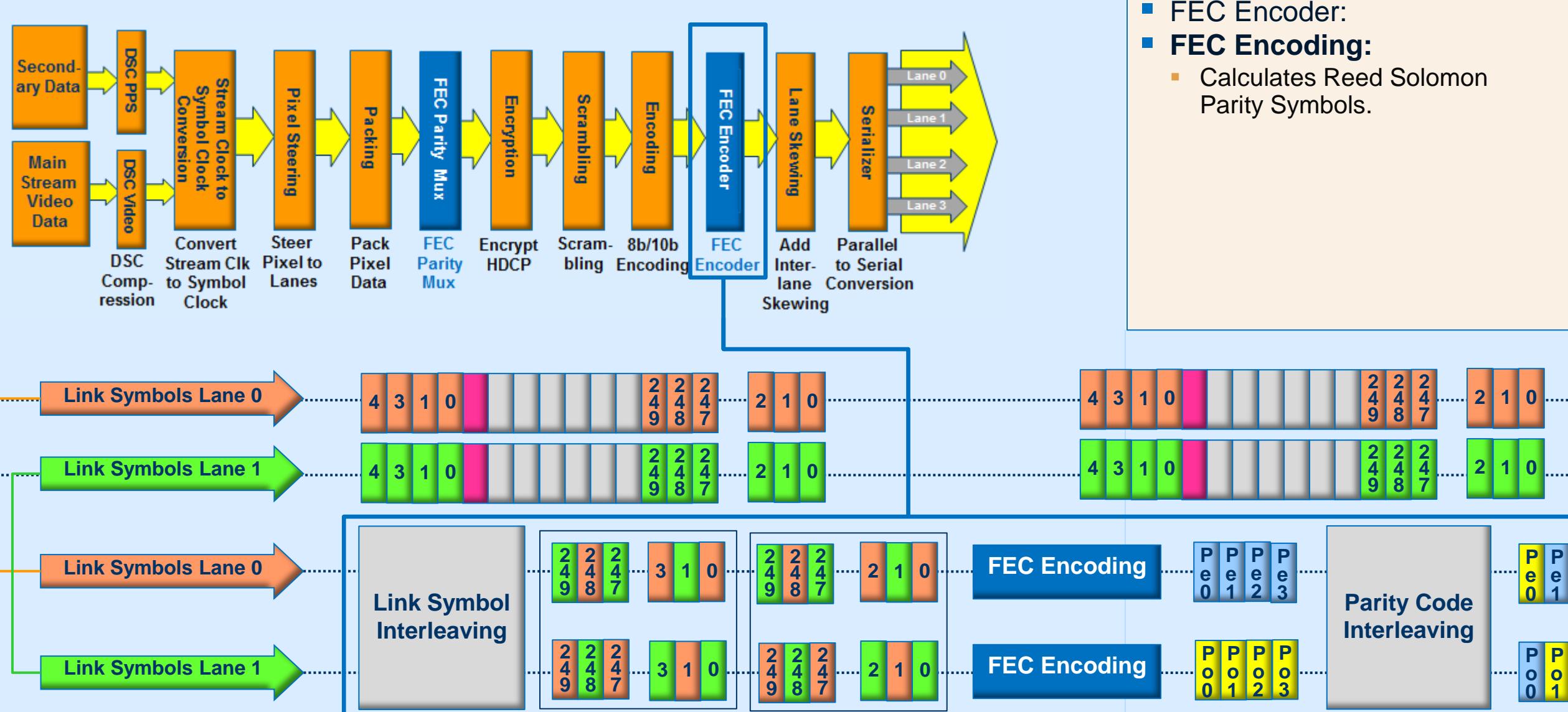
DP Main Link Transmitter Blocks (E.g. 2 Lanes) – FEC Encoder – Link Symbol Interleave



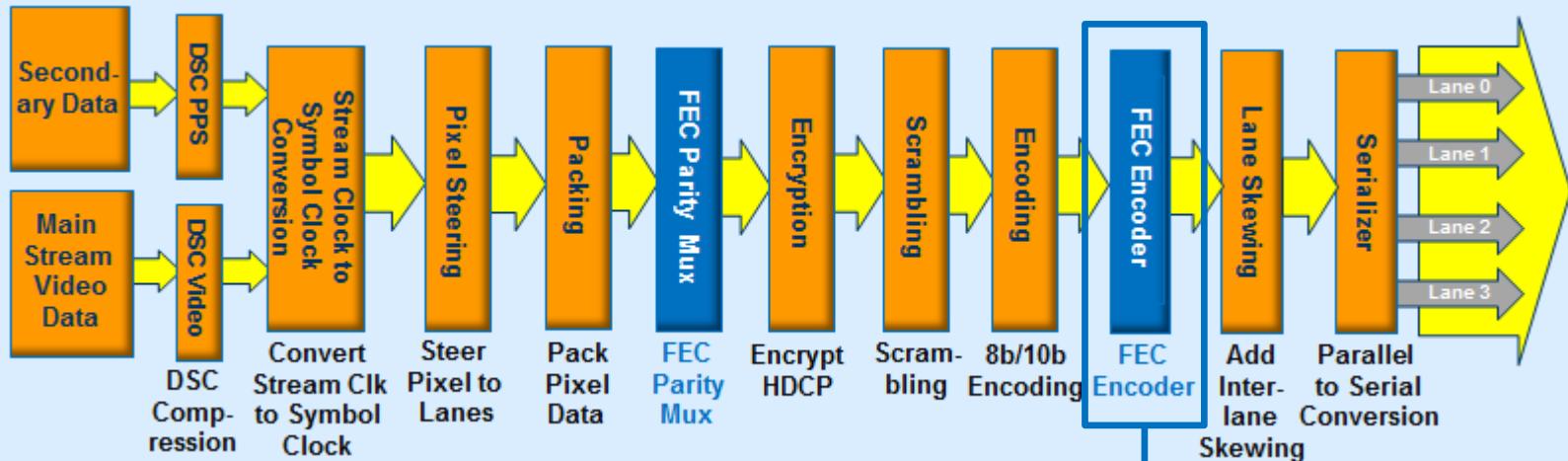
- FEC Encoder:
- **Link Symbol Interleaving:**
 - Interleaves link symbols from lane pairs.
 - Interleaving provides for better error correction where burst errors occur.



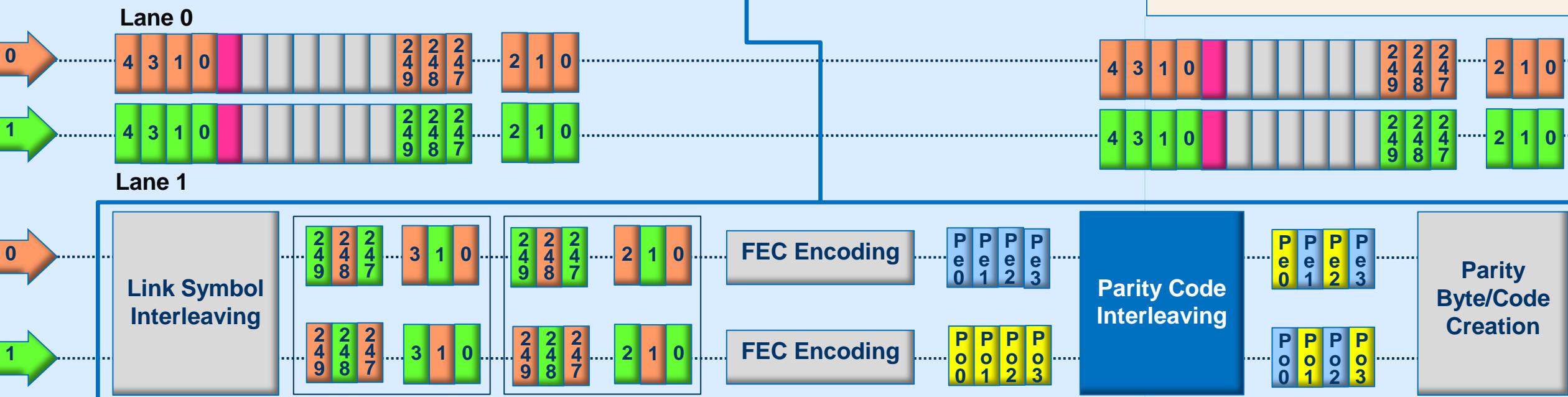
DP Main Link Transmitter Functional Blocks – FEC Encoder – FEC Encoding



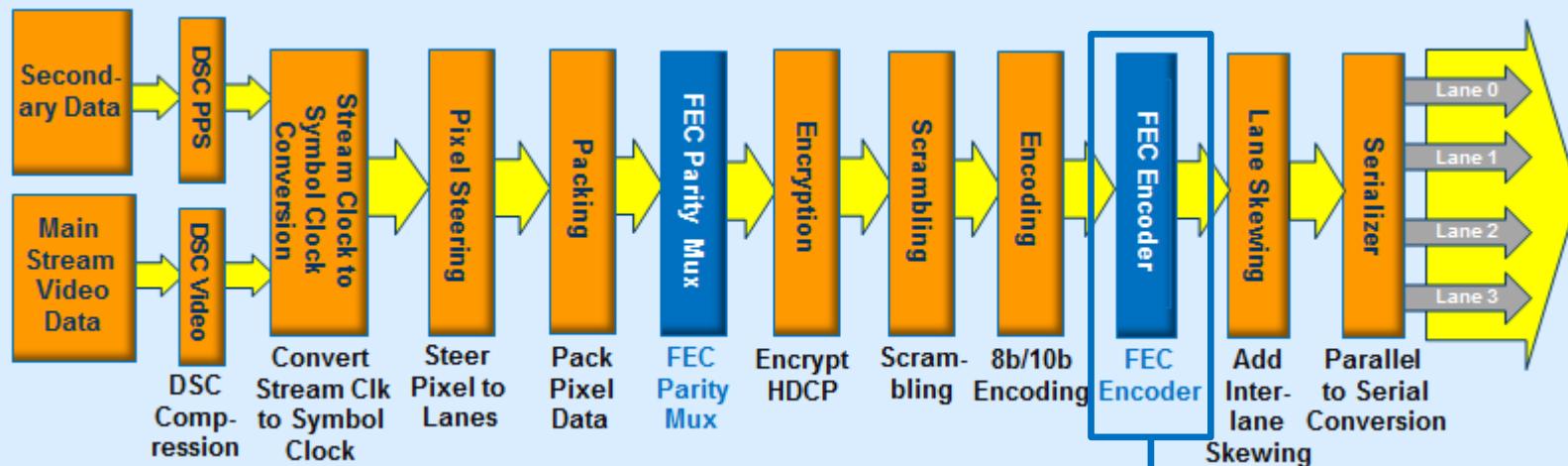
DP Main Link Transmitter Functional Blocks – FEC Encoder – Parity Code Interleaver



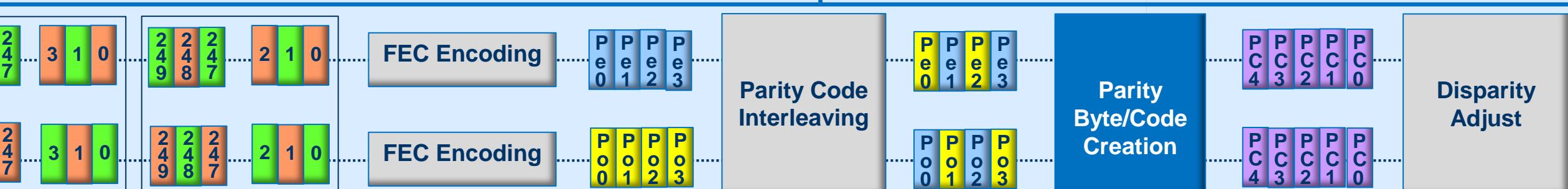
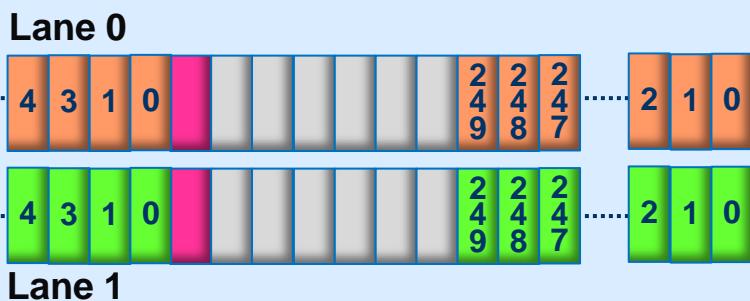
- **FEC Encoder:**
- **Parity Code Interleaving:**
 - Interleaves Parity Symbols from lane pairs.



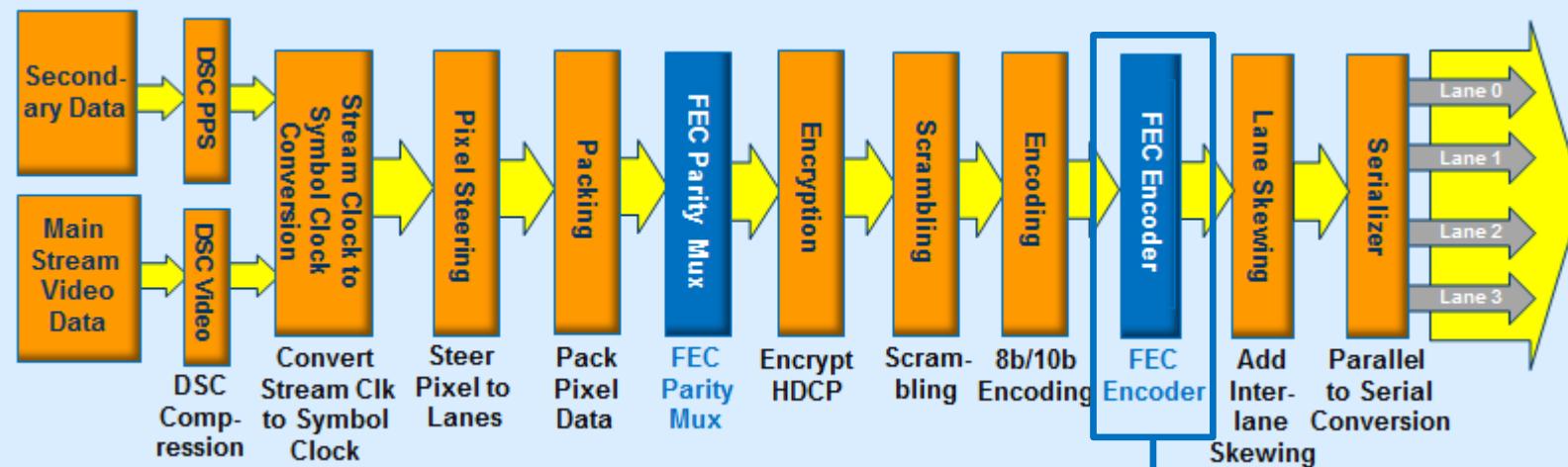
DP Main Link Transmitter Functional Blocks FEC Encoder – Parity Byte Creation



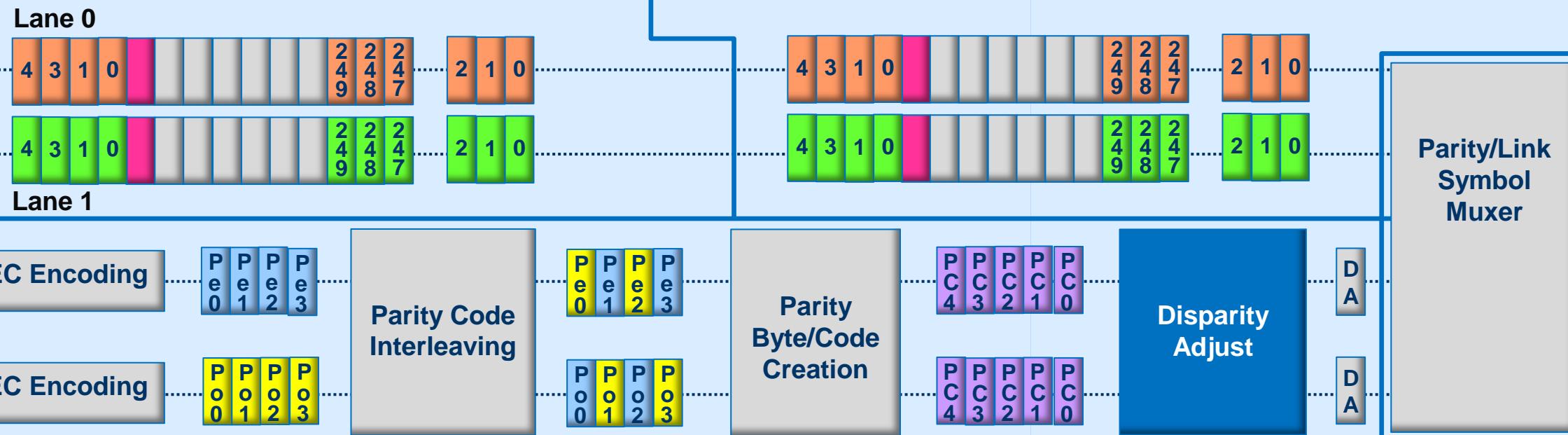
- FEC Encoder:
- Parity Byte Creation:
 - Creates 5 Parity Bytes from 4 Parity Symbols.



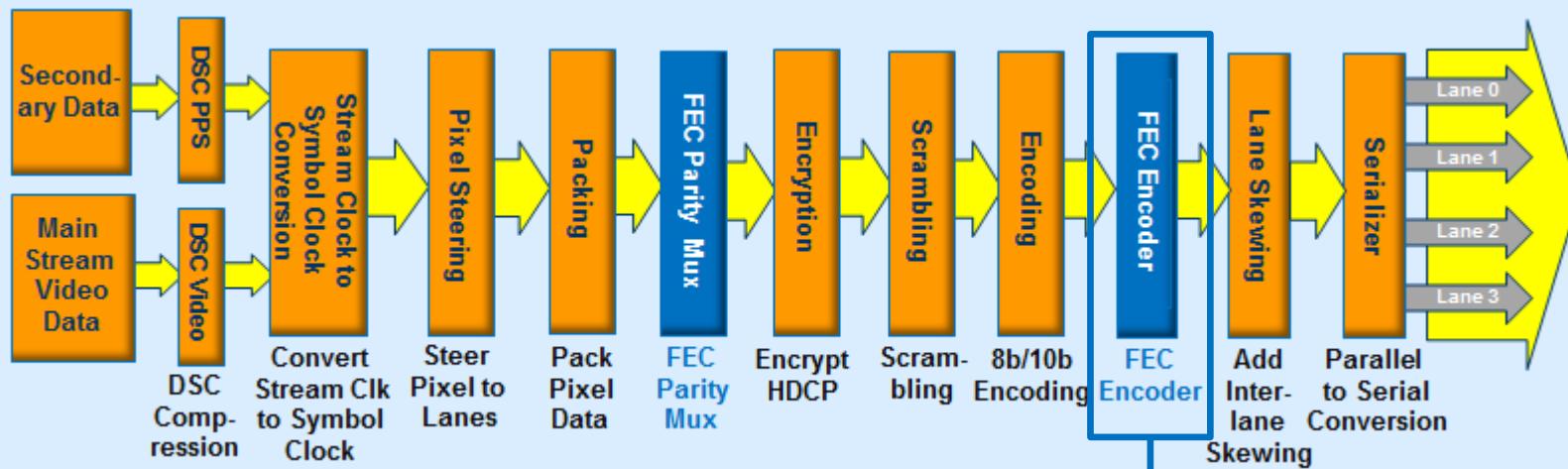
DP Main Link Transmitter Functional Blocks – FEC Encoder – Disparity Adjustment



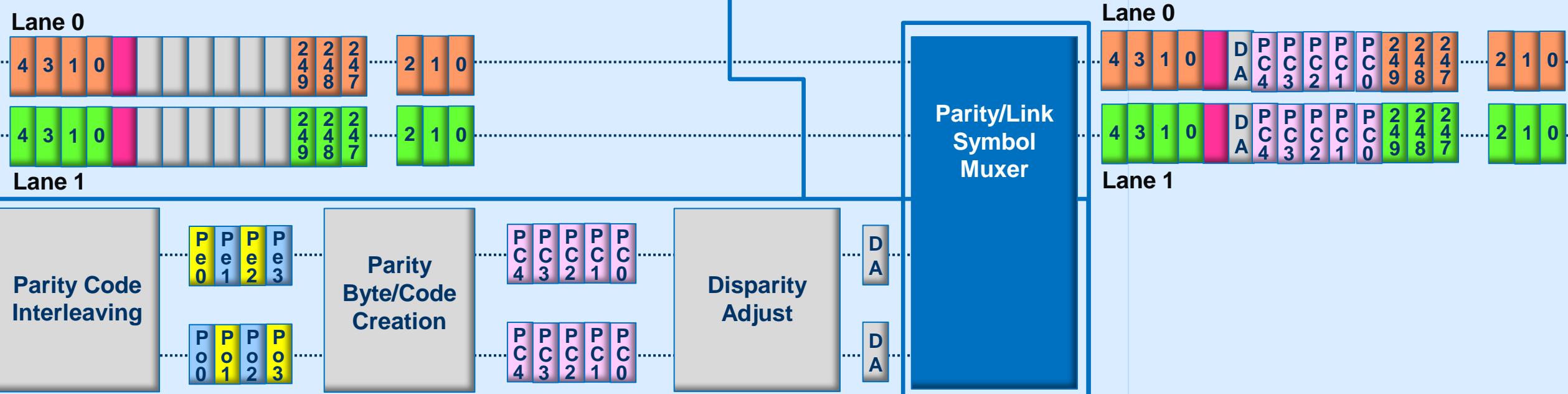
- **FEC Encoder:**
- **Running Disparity Adjustment:**
 - Adds an adjusted disparity byte to Parity Codes.



DP Main Link Transmitter Functional Blocks – FEC Encoder – Parity/Symbol Muxing



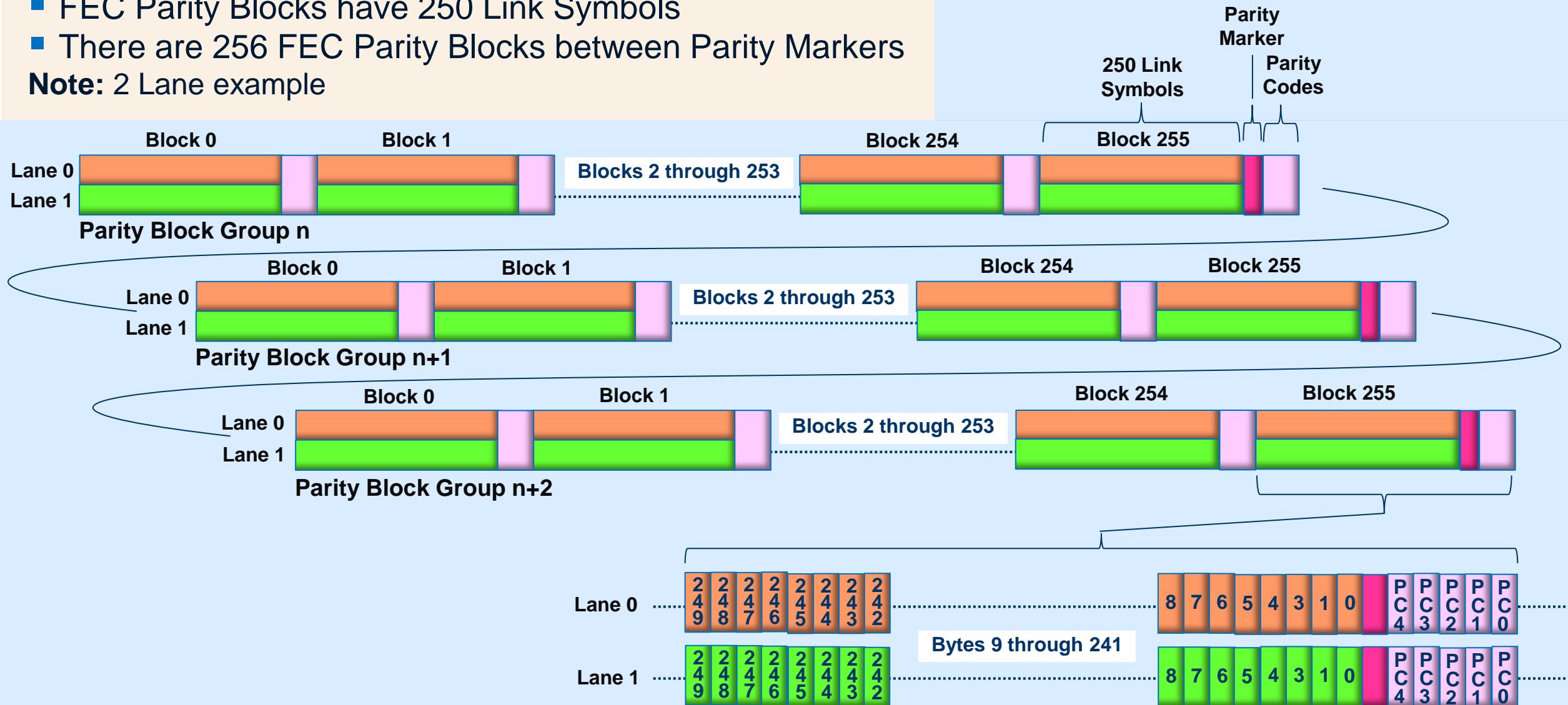
- FEC Encoder:
- Parity Code/Link Symbol Muxing:
 - Multiplexes Parity Codes into Link Symbols.



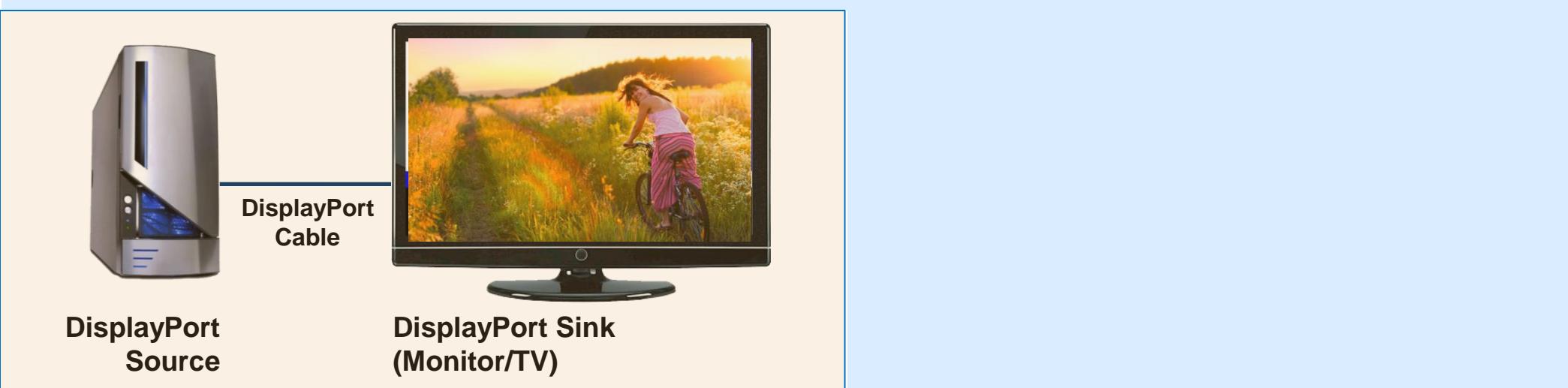
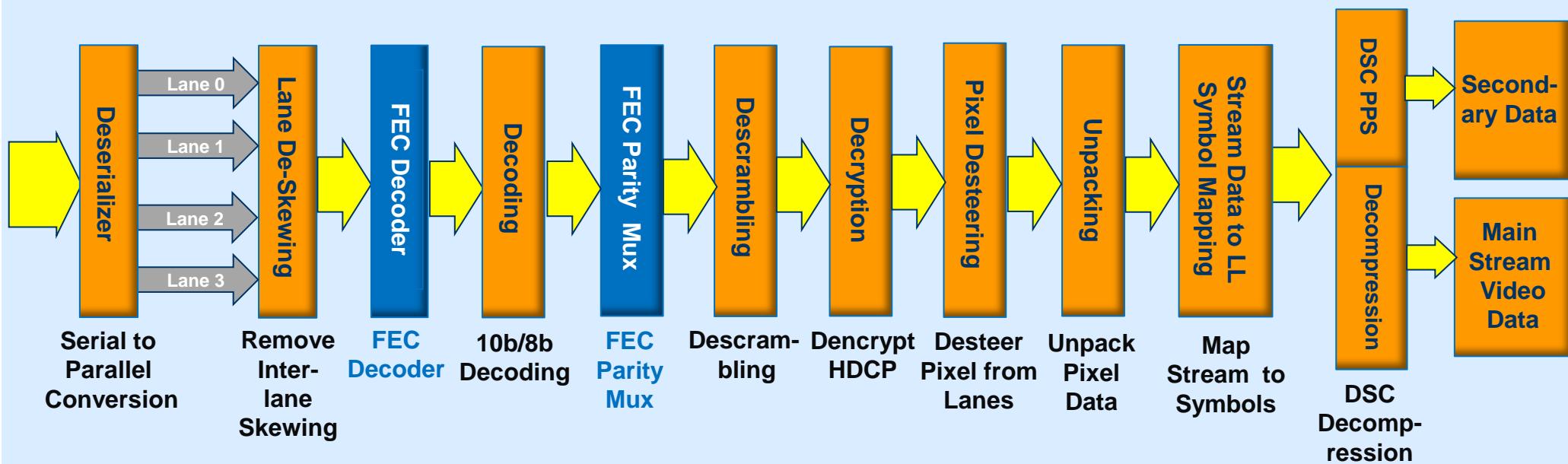
DisplayPort Main Link Transmitter – Parity Blocks & Parity Markers

- FEC Parity Blocks have 250 Link Symbols
- There are 256 FEC Parity Blocks between Parity Markers

Note: 2 Lane example



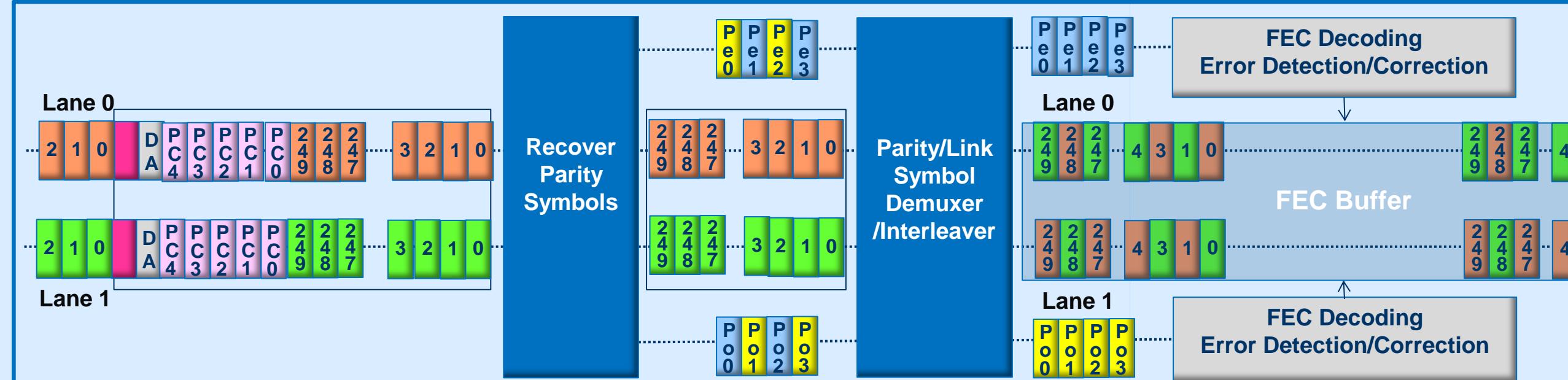
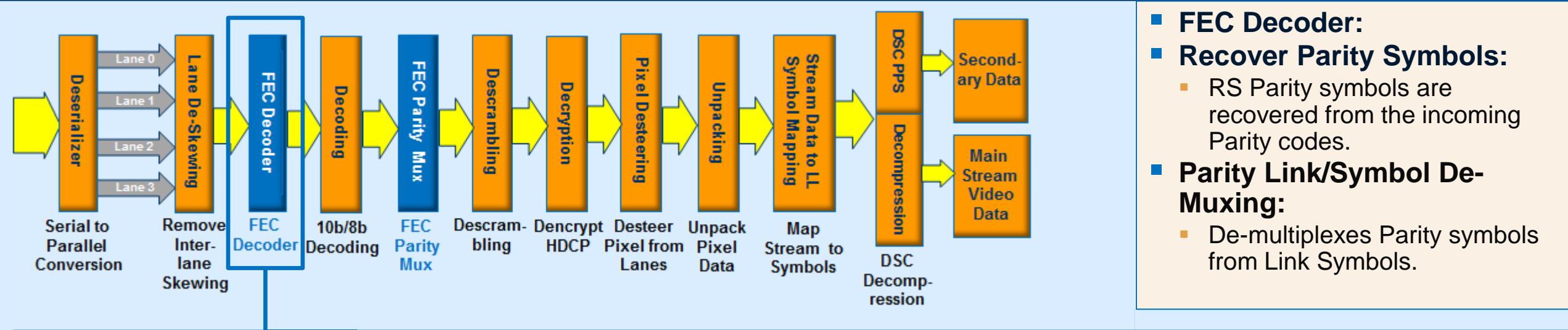
DisplayPort Main Link Receiver Functional Blocks



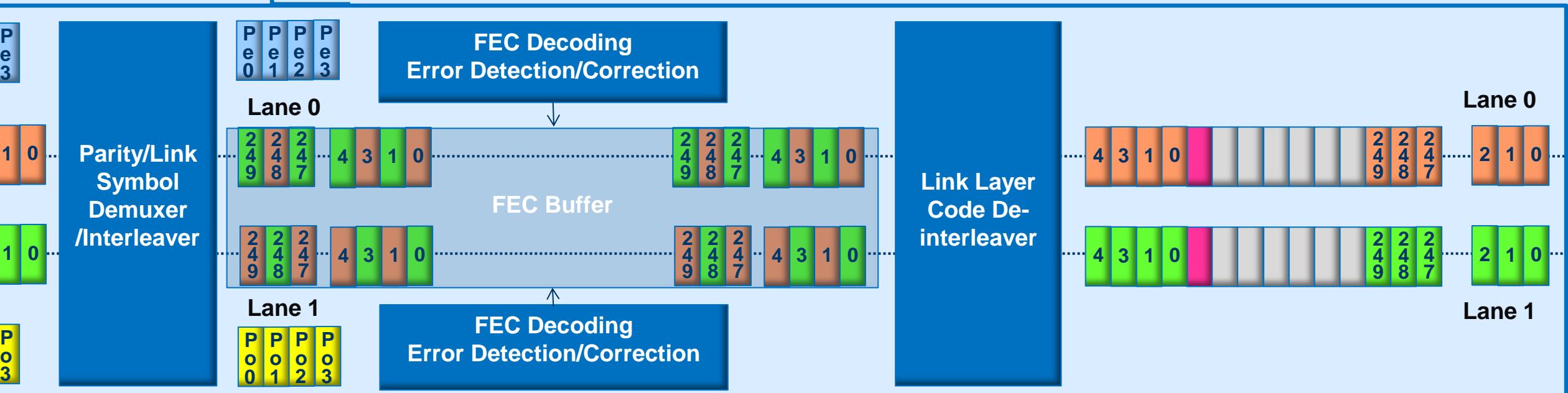
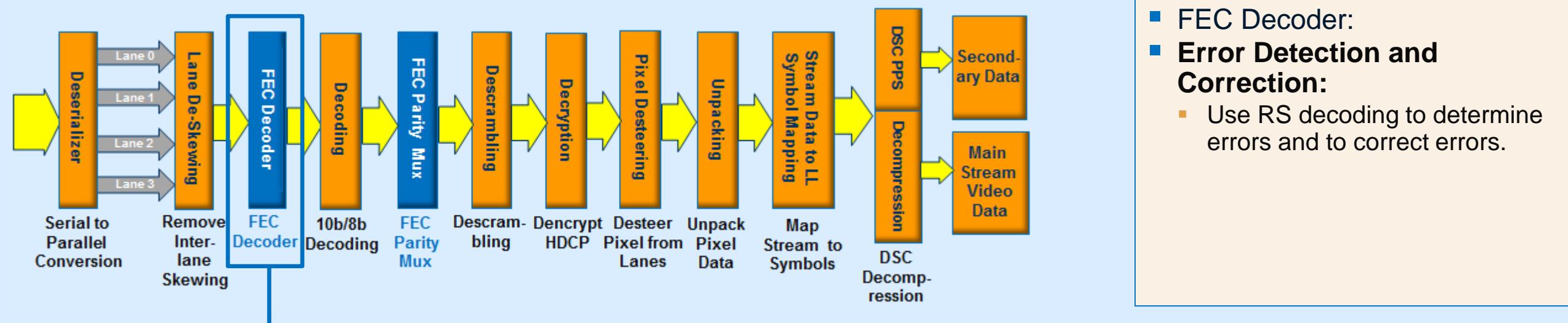
DisplayPort
Source

DisplayPort Sink
(Monitor/TV)

DisplayPort Main Link Receiver Functional Blocks – FEC Decoder



DisplayPort Main Link Receiver Functional Blocks – FEC Decoder

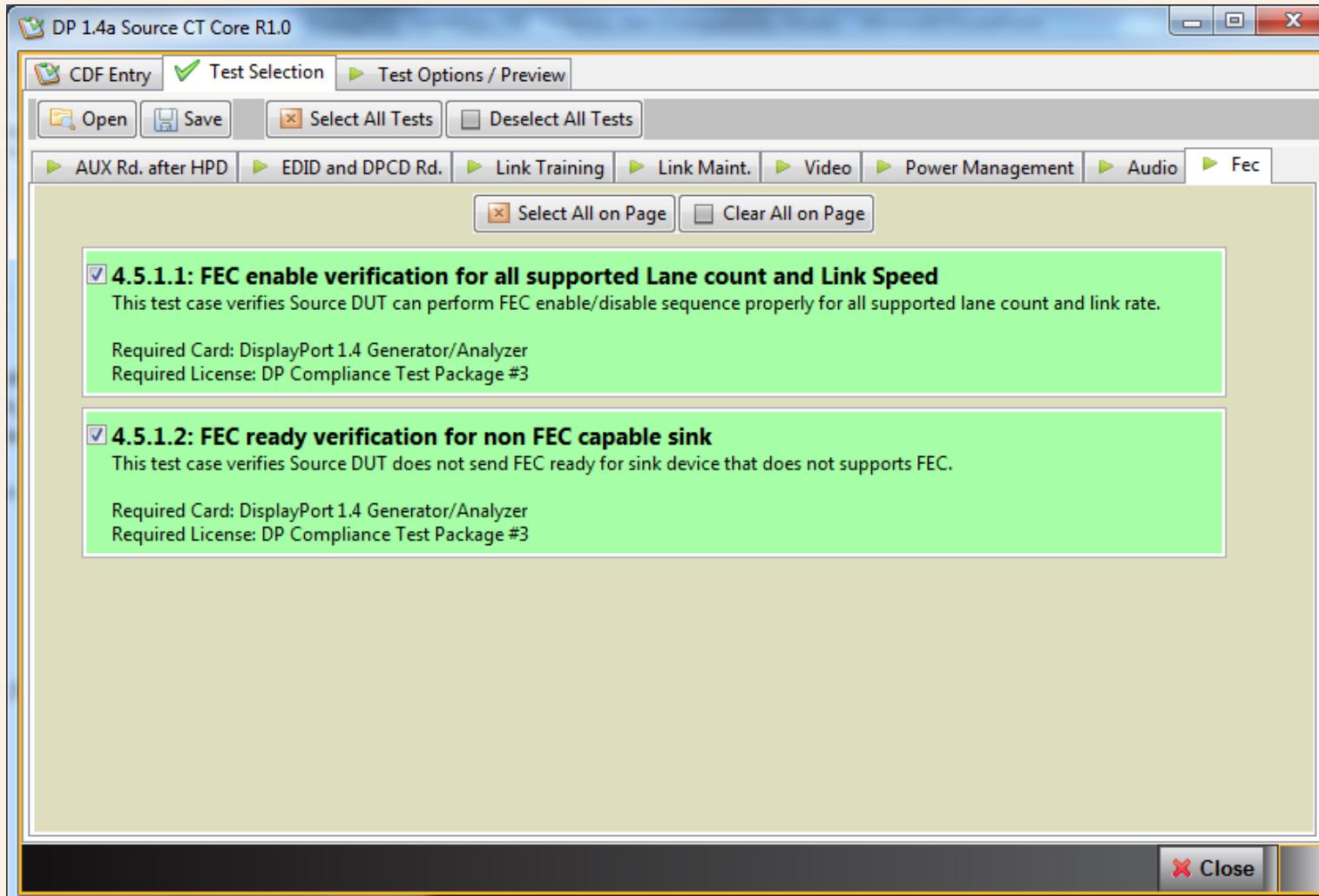


DisplayPort Forward Error Correction Compliance Testing



DisplayPort Source Forward Error Compliance Testing – List of Tests

■ List of DP FEC Source Compliance Tests



Source Forward Error Correction Compliance Test – Test ID# 4.5.1.1

Compliance Test Results Viewer

DP 1.4a Source (Core R1.0) Compliance Test Results

Results Name: 980_LB_FEC

Date Tested: October 19, 2018 9:16 AM

Overall Status: CTS Core R1.0 - Pass

Test Name / Details

4.5.1.1: FEC enable verification for all supported Lane Count

Iter 01:

- 01: [1] Test for lane count = 1 and 2 and 4 and 8 and 16 and 32 and 64 and 128 and 256 and 512 and 1024 and 2048 and 4096 and 8192 and 16384 and 32768 and 65536 and 131072 and 262144 and 524288 and 1048576 and 2097152 and 4194304 and 8388608 and 16777216 and 33554432 and 67108864 and 134217728 and 268435456 and 536870912 and 1073741824 and 2147483648 and 4294967296 and 8589934592 and 17179869184 and 34359738368 and 68719476736 and 137438953472 and 274877906944 and 549755813888 and 1099511627760 and 2199023255520 and 4398046511040 and 8796093022080 and 17592186044160 and 35184372088320 and 70368744176640 and 140737488353280 and 281474976706560 and 562949953413120 and 1125899906826240 and 2251799813652480 and 4503599627304960 and 9007199254609920 and 18014398509219840 and 36028797018439680 and 72057594036879360 and 14411518807378720 and 28823037614757440 and 57646075229514880 and 11529215045902960 and 23058430091805920 and 46116860183611840 and 92233720367223680 and 184467440734447360 and 368934881468894720 and 737869762937789440 and 1475739525875578880 and 2951479051751157760 and 5902958103502315520 and 11805916207004631040 and 23611832414009262080 and 47223664828018524160 and 94447329656037048320 and 188894659312074096640 and 377789318624148193280 and 755578637248296386560 and 151115727448593177120 and 302231454897186354240 and 604462909794372708480 and 1208925819588745416960 and 2417851639177490833920 and 4835703278354981667840 and 9671406556709963335680 and 19342813113419926671360 and 38685626226839853342720 and 77371252453679706685440 and 154742504907359413370880 and 309485009814718826741760 and 618970019629437653483520 and 1237940039258875306967040 and 2475880078517750613934080 and 4951760157035501227868160 and 9903520314071002455736320 and 19807040628142004915472640 and 39614081256284009830945280 and 79228162512568019661890560 and 15845632522513603932371120 and 31691265045027207864742240 and 63382530090054415729484480 and 126765060180108831458968960 and 253530120360217662917937760 and 507060240720435325835875520 and 1014120481440870651671751040 and 2028240962881741303343502080 and 4056481925763482606687004160 and 8112963851526965213374008320 and 16225927703053930426748016640 and 32451855406107860853496033280 and 64903710812215721706992066560 and 12980742162443144341398013120 and 25961484324886288682796026240 and 51922968649772577365592052480 and 103845937299545154731184104960 and 207691874599090309462368209920 and 415383749198180618924736419840 and 830767498396361237849472839680 and 1661534996792722475698945679360 and 3323069993585444951397891358720 and 6646139987170889902795782717440 and 13292279974341779805595565434880 and 2658455994868355961119113087760 and 5316911989736711922238226175520 and 1063382397947342384447645235040 and 2126764795894684768895290470080 and 4253529591789369537790580940160 and 8507059183578739075581161880320 and 1701411836715747815116233376640 and 3402823673431495630232466753280 and 6805647346862991260464933506560 and 13611294693735982520929667013120 and 27222589387471965041859334026240 and 54445178774943930083718668052480 and 108890357549887860167437336104960 and 217780715099775720334874672209920 and 435561430199551440669749344419840 and 871122860399102881339498688839680 and 1742245720798205762678973377679360 and 3484491441596411525357946755358720 and 6968982883192823050715893510717440 and 1393796576638564610143178702142880 and 2787593153277129220286357404285760 and 5575186306554258440572714808571520 and 11150372613108516811455496017143040 and 22300745226217033622910992034286080 and 44601490452434067245821984068572160 and 89202980904868134491643968137444320 and 17840596180973626893327936827488640 and 35681192361947253786655873654977280 and 71362384723894507573311747309954560 and 142724769447889015146623494619889120 and 285449538895778030293246989239778240 and 570898577791556060586493978479556480 and 114179715558311212117297955695912960 and 228359431116622424234595911391825920 and 456718862233244848469191822783651840 and 913437724466489696938383645567303680 and 1826875448932979393876767291134073360 and 3653750897865958787753534582268146720 and 7307501795731917575507069164536293440 and 14615003591463835151014138329072586880 and 29230007182927670302028276658145173760 and 58460014365855340604056553316290347520 and 11692002871711068120811310663258069040 and 23384005743422136241622621326516138080 and 46768011486844272483245242653032276160 and 93536022973688544966490485306064552320 and 187072045947377089932979970612129046640 and 374144091894754179865959941224258093280 and 748288183789508359731919882448516186560 and 1496576367579016719463839764897032373120 and 2993152735158033438927679529794064746240 and 5986305470316066877855359059588129488480 and 11972610940632133755710718119176258968960 and 23945221881264267511421436238352517779360 and 4789044376252853502284287247670503558880 and 9578088752505707004568574495341007117760 and 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1042958902799867559173644646640534628956976823332800 and 208

Source Forward Error Correction Compliance Test – Test ID# 5.4.1.2

The screenshot displays two windows from Teledyne LeCroy's test software. The top window is the 'Compliance Test Results Viewer' titled 'DP 1.4a Source (Core R1.0) Compliance Test Results'. It shows the results for '980_LB_FEC' tested on October 19, 2018, at 9:16 AM, with an overall status of 'CTS Core R1.0 - Pass'. The bottom window is the 'ACA Data Viewer' showing a list of events. A yellow arrow points from the 'Instrument' field in the Compliance Test Results Viewer to the 'Open ACA Data' button in the ACA Data Viewer. Another yellow arrow points from the '4.5.1.1: FEC enable verification for all supported Lane count and Link Sp...' section in the Compliance Test Results Viewer to the event list in the ACA Data Viewer. The ACA Data Viewer lists 198 events, with event 11 highlighted by a yellow box. This event is a 'Reply to Read Request' for the 'FEC_CAPABILITY' register. The register value is shown as 00090: FEC_CAPABILITY, with bit 0 set to 1 (FEC_CAPABLE). The event details show a sequence of DPHY and DNAT messages over time, with ACKs and RxE training intervals.

◆ Test verifies that a source reads the sink FEC capability register and

Instrument: SS980B [10.30.196.39]

Open ACA Data 4.5.1.1: FEC enable verification for all supported Lane count and Link Sp...

Compliance Test Results Viewer

DP 1.4a Source (Core R1.0) Compliance Test Results

Results Name: 980_LB_FEC

Date Tested: October 19, 2018 9:16 AM

Overall Status: CTS Core R1.0 - Pass

Manufacturer:

Model Name:

Port Tested: 1

HTML Report

Test Name / Details

4.5.1.1: FEC enable verification for all supported Lane count and Link Sp...

Iter 01:

- 01: [1] Test for lane count = 1 and lane rate = 1 Gbps
- 02: [2] Test for lane count = 2 and lane rate = 1 Gbps
- 03: [3] Test for lane count = 4 and lane rate = 1 Gbps
- 04: [4] Test for lane count = 1 and lane rate = 2 Gbps
- 05: [5] Test for lane count = 2 and lane rate = 2 Gbps
- 06: [6] Test for lane count = 4 and lane rate = 2 Gbps
- 07: [7] Test for lane count = 1 and lane rate = 4 Gbps
- 08: [8] Test for lane count = 2 and lane rate = 4 Gbps
- 09: [9] Test for lane count = 4 and lane rate = 4 Gbps
- 10: [10] Test for lane count = 1 and lane rate = 8 Gbps

Source DUT reads FEC CAPABILITY register 0x90h.

Source DUT sets FEC_READY before link training to F1.

Source DUT enables the FEC encoding properly.

For lane 1 Fec Uncorrected block error count is 0.

For lane 1 Fec corrected block error count is 0.

For lane 1 Fec bit error count is 0.

For lane 1 Fec parity block error count is 0.

For lane 1 Fec parity bit error count is 0.

Source DUT disables the FEC encoding properly.

11: [11] Test for lane count = 2 and lane rate = 2 Gbps

12: [12] Test for lane count = 4 and lane rate = 4 Gbps

4.5.1.2: FEC ready verification for non FEC capable lanes

Iter 01:

- 01: [1] FEC ready verification test for lane 1

Source DUT reads FEC CAPABILITY register 0x90h.

Source DUT does clear FEC_READY in FEC_CONFIGURATION register.

Open ACA Data 4.5.1.1: FEC enable verification for all supported Lane count and Link Sp...

Instrument: SS980B [10.30.196.39]

ACA Data Viewer

[ACA-4_5_1_2_01] Events: 198 (1066)

Event	Time	Type	Direction	Command	Description
0	DPHP DP-R31 +21:58:37.350145	HPD Falling Edge			
1	DPHP DP-R31 +21:58:38.330584	HPD Rising Edge			
2	DNAT DP-R31 +21:58:38.331050	> R:200 SINK_COUNT L=6	<	ACK 41 00 77 77 01 00	
3	DNAT DP-R31 +21:58:38.331122	< ACK 41 00 77 77 01 00	>	R:E TRAINING_AUX_RD_INTERVAL L=1	
4	DNAT DP-R31 +21:58:38.331260	> R:E TRAINING_AUX_RD_INTERVAL L=1	<	ACK 81	
5	DNAT DP-R31 +21:58:38.331332	< ACK 81	>	R:0 DPCD_REV L=1	
6	DNAT DP-R31 +21:58:38.331409	> R:0 DPCD_REV L=1	<	ACK 14	
7	DNAT DP-R31 +21:58:38.331482	< ACK 14	>	R:2200 DP1.3_DPCD_REV L=16	
8	DNAT DP-R31 +21:58:38.331557	> R:2200 DP1.3_DPCD_REV L=16	<	ACK 14 1E C4 81 01 00 01 80 00 20 04 08 00 02 81 00	
9	DNAT DP-R31 +21:58:38.331629	< ACK 14 1E C4 81 01 00 01 80 00 20 04 08 00 02 81 00	>	R:90 FEC_CAPABILITY L=1	
10	DNAT DP-R31 +21:58:38.331860	> R:90 FEC_CAPABILITY L=1	<	ACK 00	
11	DNAT DP-R31 +21:58:38.331933	< ACK 00	>	R:100 LINK_BW_SET L=2	
12	DPLT DP-R31 +21:58:38.475619	> R:100 LINK_BW_SET L=2	<	ACK 1E 84	
13	DPLT DP-R31 +21:58:38.475691	< ACK 1E 84	>	R:200 SINK_COUNT L=6	
14	DNAT DP-R31 +21:58:38.489205	> R:200 SINK_COUNT L=6	<	ACK 41 00 00 00 80 00	
15	DNAT DP-R31 +21:58:38.489277	< ACK 41 00 00 00 80 00	>	R:E TRAINING_AUX_RD_INTERVAL L=1	
16	DNAT DP-R31 +21:58:38.489444	< ACK 81	>	R:0 DPCD_REV L=1	
17	DNAT DP-R31 +21:58:38.489516	> R:0 DPCD_REV L=1	<	ACK 00	
18	DNAT DP-R31 +21:58:38.489618	< ACK 00	>	R:2200 DP1.3_DPCD_REV L=16	
19	DNAT DP-R31 +21:58:38.489690	< ACK 14	>	ACK 14 1E C4 81 01 00 01 80 00 20 04 08 00 02 81 00	
20	DNAT DP-R31 +21:58:38.489774	> R:2200 DP1.3_DPCD_REV L=16	<	ACK 14 1E C4 81 01 00 01 80 00 20 04 08 00 02 81 00	
21	DNAT DP-R31 +21:58:38.489846	< ACK 14 1E C4 81 01 00 01 80 00 20 04 08 00 02 81 00	>	R:90 FEC_CAPABILITY L=1	
22	DNAT DP-R31 +21:58:38.490113	> R:90 FEC_CAPABILITY L=1	<	ACK 00	
23	DNAT DP-R31 +21:58:38.490185	< ACK 00	>	R:10A eDP_CONFIGURATION_SET L=1 00	
24	DNAT DP-R31 +21:58:38.490270	> R:10A eDP_CONFIGURATION_SET L=1 00	<	ACK	
25	DNAT DP-R31 +21:58:38.490350	< ACK	>	R:201 DEVICE_SERVICE_IRQ_VECTOR L=1	
26	DNAT DP-R31 +21:58:38.490420	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1	<	ACK 00	
27	DNAT DP-R31 +21:58:38.490492	< ACK 00	>	R:E TRAINING_AUX_RD_INTERVAL L=1	
28	DNAT DP-R31 +21:58:38.549425	> R:E TRAINING_AUX_RD_INTERVAL L=1	<	ACK 81	
29	DNAT DP-R31 +21:58:38.549497	< ACK 81	>	R:E TRAINING_AUX_RD_INTERVAL L=1	
30	DNAT DP-R31 +21:58:38.549595	> R:E TRAINING_AUX_RD_INTERVAL L=1	<	ACK 81	
31	DNAT DP-R31 +21:58:38.549667	< ACK 81	>	R:0 DPCD_REV L=1	
32	DNAT DP-R31 +21:58:38.549756	> R:0 DPCD_REV L=1	<	ACK 14	
33	DNAT DP-R31 +21:58:38.549829	< ACK 14	>	R:2200 DP1.3_DPCD_REV L=16	
34	DNAT DP-R31 +21:58:38.549916	> R:2200 DP1.3_DPCD_REV L=16	<	ACK 14 1E C4 81 01 00 01 80 00 20 04 08 00 02 81 00	
35	DNAT DP-R31 +21:58:38.549989	< ACK 14 1E C4 81 01 00 01 80 00 20 04 08 00 02 81 00	>	R:90 FEC_CAPABILITY L=1	
36	DNAT DP-R31 +21:58:38.550254	> R:90 FEC_CAPABILITY L=1	<	ACK 00	
37	DNAT DP-R31 +21:58:38.550327	< ACK 00	>		

Start Time: +21:58:38.331933

Type: Native

Direction: Reply

Command: ACK

Reply to Read Request.

00090: FEC_CAPABILITY

Bit	Name	Value	Description
0	FEC_CAPABLE	N(0)	
1	UNCORRECTED_BLOCK_ERR_CNT_CAP	N(0)	
2	CORRECTED_BLOCK_ERR_CNT_CAP	N(0)	
3	BIT_ERROR_COUNT_CAPABLE	N(0)	
4		0	Reserved
5		0	Reserved
6		0	Reserved
7		0	Reserved

[0000] [00 00 -- -- -- -- --] [..] []

11: < ACK 00

Instrument: SS980B [10.30.196.39]

Open ACA Data 4.5.1.1: FEC enable verification for all supported Lane count and Link Sp...

Instrument: SS980B [10.30.196.39]

Compliance Test Results Viewer

DP 1.4a Source (Core R1.0) Compliance Test Results

Results Name: 980_LB_FEC

Date Tested: October 19, 2018 9:16 AM

Overall Status: CTS Core R1.0 - Pass

Manufacturer:

Model Name:

Port Tested: 1

HTML Report

Test Name / Details

4.5.1.1: FEC enable verification for all supported Lane count and Link Sp...

Iter 01:

- 01: [1] Test for lane count = 1 and lane rate = 1 Gbps
- 02: [2] Test for lane count = 2 and lane rate = 1 Gbps
- 03: [3] Test for lane count = 4 and lane rate = 1 Gbps
- 04: [4] Test for lane count = 1 and lane rate = 2 Gbps
- 05: [5] Test for lane count = 2 and lane rate = 2 Gbps
- 06: [6] Test for lane count = 4 and lane rate = 2 Gbps
- 07: [7] Test for lane count = 1 and lane rate = 4 Gbps
- 08: [8] Test for lane count = 2 and lane rate = 4 Gbps
- 09: [9] Test for lane count = 4 and lane rate = 4 Gbps
- 10: [10] Test for lane count = 1 and lane rate = 8 Gbps

Source DUT reads FEC CAPABILITY register 0x90h.

Source DUT sets FEC_READY before link training to F1.

Source DUT enables the FEC encoding properly.

For lane 1 Fec Uncorrected block error count is 0.

For lane 1 Fec corrected block error count is 0.

For lane 1 Fec bit error count is 0.

For lane 1 Fec parity block error count is 0.

For lane 1 Fec parity bit error count is 0.

Source DUT disables the FEC encoding properly.

11: [11] Test for lane count = 2 and lane rate = 2 Gbps

12: [12] Test for lane count = 4 and lane rate = 4 Gbps

4.5.1.2: FEC ready verification for non FEC capable lanes

Iter 01:

- 01: [1] FEC ready verification test for lane 1

Source DUT reads FEC CAPABILITY register 0x90h.

Source DUT does clear FEC_READY in FEC_CONFIGURATION register.

Open ACA Data 4.5.1.1: FEC enable verification for all supported Lane count and Link Sp...

Instrument: SS980B [10.30.196.39]

ACA Data Viewer

[ACA-4_5_1_2_01] Events: 198 (1066)

Event	Time	Type	Direction	Command	Description
0	DPHP DP-R31 +21:58:37.350145	HPD Falling Edge			
1	DPHP DP-R31 +21:58:38.330584	HPD Rising Edge			
2	DNAT DP-R31 +21:58:38.331050	> R:200 SINK_COUNT L=6	<	ACK 41 00 77 77 01 00	
3	DNAT DP-R31 +21:58:38.331122	< ACK 41 00 77 77 01 00	>	R:E TRAINING_AUX_RD_INTERVAL L=1	
4	DNAT DP-R31 +21:58:38.331260	> R:E TRAINING_AUX_RD_INTERVAL L=1	<	ACK 81	
5	DNAT DP-R31 +21:58:38.331332	< ACK 81	>	R:0 DPCD_REV L=1	
6	DNAT DP-R31 +21:58:38.331409	> R:0 DPCD_REV L=1	<	ACK 14	
7	DNAT DP-R31 +21:58:38.331482	< ACK 14	>	R:2200 DP1.3_DPCD_REV L=16	
8	DNAT DP-R31 +21:58:38.331557	> R:2200 DP1.3_DPCD_REV L=16	<	ACK 14 1E C4 81 01 00 01 80 00 20 04 08 00 02 81 00	
9	DNAT DP-R31 +21:58:38.331629	< ACK 14 1E C4 81 01 00 01 80 00 20 04 08 00 02 81 00	>	R:90 FEC_CAPABILITY L=1	
10	DNAT DP-R31 +21:58:38.331860	> R:90 FEC_CAPABILITY L=1	<	ACK 00	
11	DNAT DP-R31 +21:58:38.331933	< ACK 00	>	R:100 LINK_BW_SET L=2	
12	DPLT DP-R31 +21:58:38.475619	> R:100 LINK_BW_SET L=2	<	ACK 1E 84	
13	DPLT DP-R31 +21:58:38.475691	< ACK 1E 84	>	R:200 SINK_COUNT L=6	
14	DNAT DP-R31 +21:58:38.489205	> R:200 SINK_COUNT L=6	<	ACK 41 00 00 00 80 00	
15	DNAT DP-R31 +21:58:38.489277	< ACK 41 00 00 00 80 00	>	R:E TRAINING_AUX_RD_INTERVAL L=1	
16	DNAT DP-R31 +21:58:38.489444	< ACK 81	>	R:0 DPCD_REV L=1	
17	DNAT DP-R31 +21:58:38.489516	> R:0 DPCD_REV L=1	<	ACK 00	
18	DNAT DP-R31 +21:58:38.489618	< ACK 00	>	R:2200 DP1.3_DPCD_REV L=16	
19	DNAT DP-R31 +21:58:38.489690	< ACK 14	>	ACK 14 1E C4 81 01 00 01 80 00 20 04 08 00 02 81 00	
20	DNAT DP-R31 +21:58:38.489774	> R:2200 DP1.3_DPCD_REV L=16	<	ACK 14 1E C4 81 01 00 01 80 00 20 04 08 00 02 81 00	
21	DNAT DP-R31 +21:58:38.489846	< ACK 14 1E C4 81 01 00 01 80 00 20 04 08 00 02 81 00	>	R:90 FEC_CAPABILITY L=1	
22	DNAT DP-R31 +21:58:38.490113	> R:90 FEC_CAPABILITY L=1	<	ACK 00	
23	DNAT DP-R31 +21:58:38.490185	< ACK 00	>	R:10A eDP_CONFIGURATION_SET L=1 00	
24	DNAT DP-R31 +21:58:38.490270	> R:10A eDP_CONFIGURATION_SET L=1 00	<	ACK	
25	DNAT DP-R31 +21:58:38.490350	< ACK	>	R:201 DEVICE_SERVICE_IRQ_VECTOR L=1	
26	DNAT DP-R31 +21:58:38.490420	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1	<	ACK 00	
27	DNAT DP-R31 +21:58:38.490492	< ACK 00	>	R:E TRAINING_AUX_RD_INTERVAL L=1	
28	DNAT DP-R31 +21:58:38.549425	> R:E TRAINING_AUX_RD_INTERVAL L=1	<	ACK 81	
29	DNAT DP-R31 +21:58:38.549497	< ACK 81	>	R:E TRAINING_AUX_RD_INTERVAL L=1	
30	DNAT DP-R31 +21:58:38.549595	> R:E TRAINING_AUX_RD_INTERVAL L=1	<	ACK 81	
31	DNAT DP-R31 +21:58:38.549667	< ACK 81	>	R:0 DPCD_REV L=1	
32	DNAT DP-R31 +21:58:38.549756	> R:0 DPCD_REV L=1	<	ACK 14	
33	DNAT DP-R31 +21:58:38.549829	< ACK 14	>	R:2200 DP1.3_DPCD_REV L=16	
34	DNAT DP-R31 +21:58:38.549916	> R:2200 DP1.3_DPCD_REV L=16	<	ACK 14 1E C4 81 01 00 01 80 00 20 04 08 00 02 81 00	
35	DNAT DP-R31 +21:58:38.549989	< ACK 14 1E C4 81 01 00 01 80 00 20 04 08 00 02 81 00	>	R:90 FEC_CAPABILITY L=1	
36	DNAT DP-R31 +21:58:38.550254	> R:90 FEC_CAPABILITY L=1	<	ACK 00	
37	DNAT DP-R31 +21:58:38.550327	< ACK 00	>		

Start Time: +21:58:38.331933

Type: Native

Direction: Reply

Command: ACK

Reply to Read Request.

00090: FEC_CAPABILITY

Bit	Name	Value	Description
0	FEC_CAPABLE	N(0)	
1	UNCORRECTED_BLOCK_ERR_CNT_CAP	N(0)	
2	CORRECTED_BLOCK_ERR_CNT_CAP	N(0)	
3	BIT_ERROR_COUNT_CAPABLE	N(0)	
4		0	Reserved
5		0	Reserved
6		0	Reserved
7		0	Reserved

[0000] [00 00 -- -- -- -- --] [..] []

11: < ACK 00

Instrument: SS980B [10.30.196.39]

Open ACA Data 4.5.1.1: FEC enable verification for all supported Lane count and Link Sp...

Instrument: SS980B [10.30.196.39]

Compliance Test Results Viewer

DP 1.4a Source (Core R1.0) Compliance Test Results

Results Name: 980_LB_FEC

Date Tested: October 19, 2018 9:16 AM

Overall Status: CTS Core R1.0 - Pass

Manufacturer:

Model Name:

Port Tested: 1

HTML Report

Test Name / Details

4.5.1.1: FEC enable verification for all supported Lane count and Link Sp...

Iter 01:

- 01: [1] Test for lane count = 1 and lane rate = 1 Gbps
- 02: [2] Test for lane count = 2 and lane rate = 1 Gbps
- 03: [3] Test for lane count = 4 and lane rate = 1 Gbps
- 04: [4] Test for lane count = 1 and lane rate = 2 Gbps
- 05: [5] Test for lane count = 2 and lane rate = 2 Gbps
- 06: [6] Test for lane count = 4 and lane rate = 2 Gbps
- 07: [7] Test for lane count = 1 and lane rate = 4 Gbps
- 08: [8] Test for lane count = 2 and lane rate = 4 Gbps
- 09: [9] Test for lane count = 4 and lane rate = 4 Gbps
- 10: [10] Test for lane count = 1 and lane rate = 8 Gbps

Source DUT reads FEC CAPABILITY register 0x90h.

Source DUT sets FEC_READY before link training to F1.

Source DUT enables the FEC encoding properly.

For lane 1 Fec Uncorrected block error count is 0.

For lane 1 Fec corrected block error count is 0.

For lane 1 Fec bit error count is 0.

For lane 1 Fec parity block error count is 0.

For lane 1 Fec parity bit error count is 0.

Source DUT disables the FEC encoding properly.

11: [11] Test for lane count = 2 and lane rate = 2 Gbps

12: [12] Test for lane count = 4 and lane rate = 4 Gbps

4.5.1.2: FEC ready verification for non FEC capable lanes

Iter 01:

- 01: [1] FEC ready verification test for lane 1

Source DUT reads FEC CAPABILITY register 0x90h.

Source DUT does clear FEC_READY in FEC_CONFIGURATION register.

Open ACA Data 4.5.1.1: FEC enable verification for all supported Lane count and Link Sp...

Instrument: SS980B [10.30.196.39]

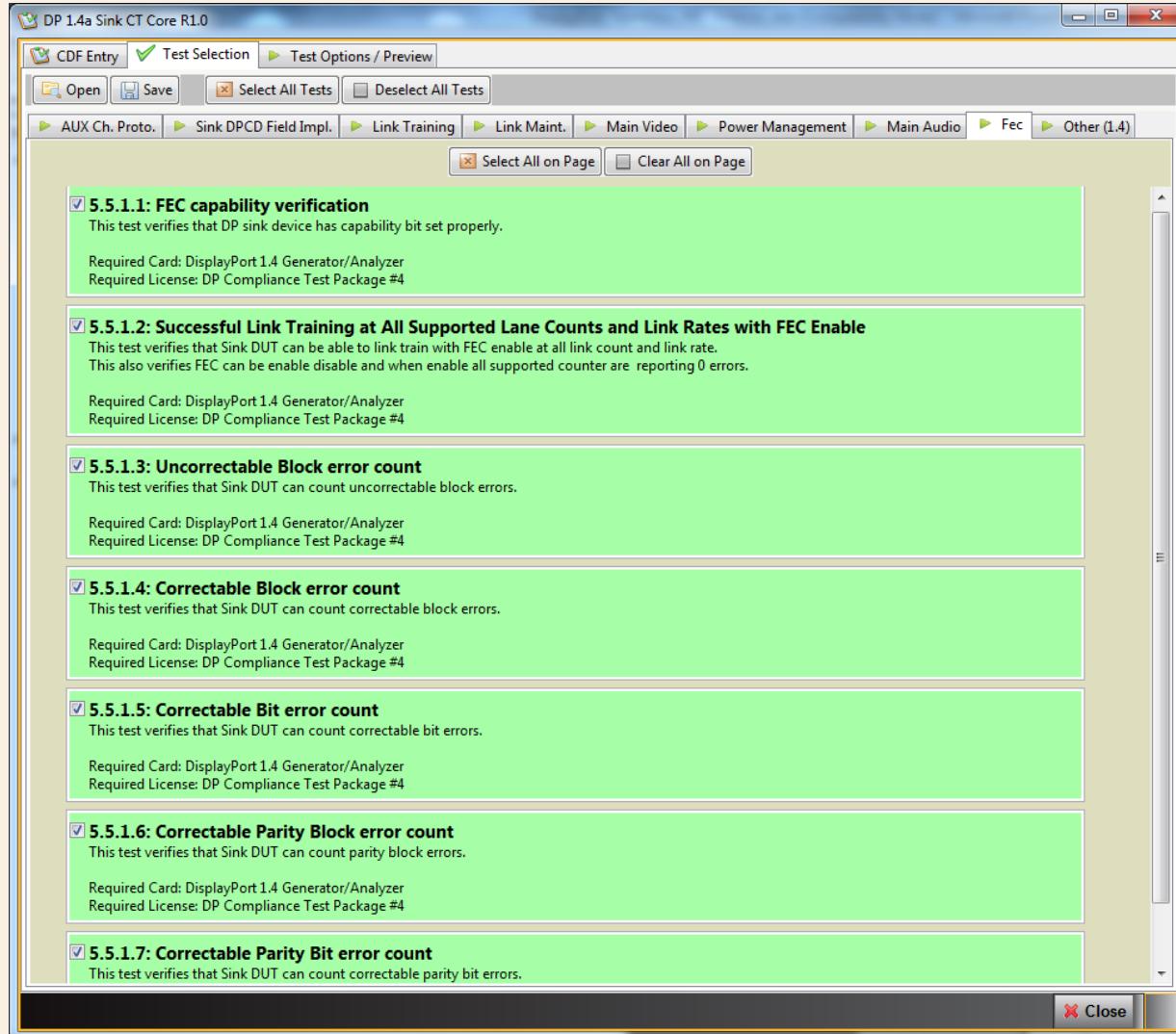
ACA Data Viewer

[ACA-4_5_1_2_01] Events: 198 (1066)

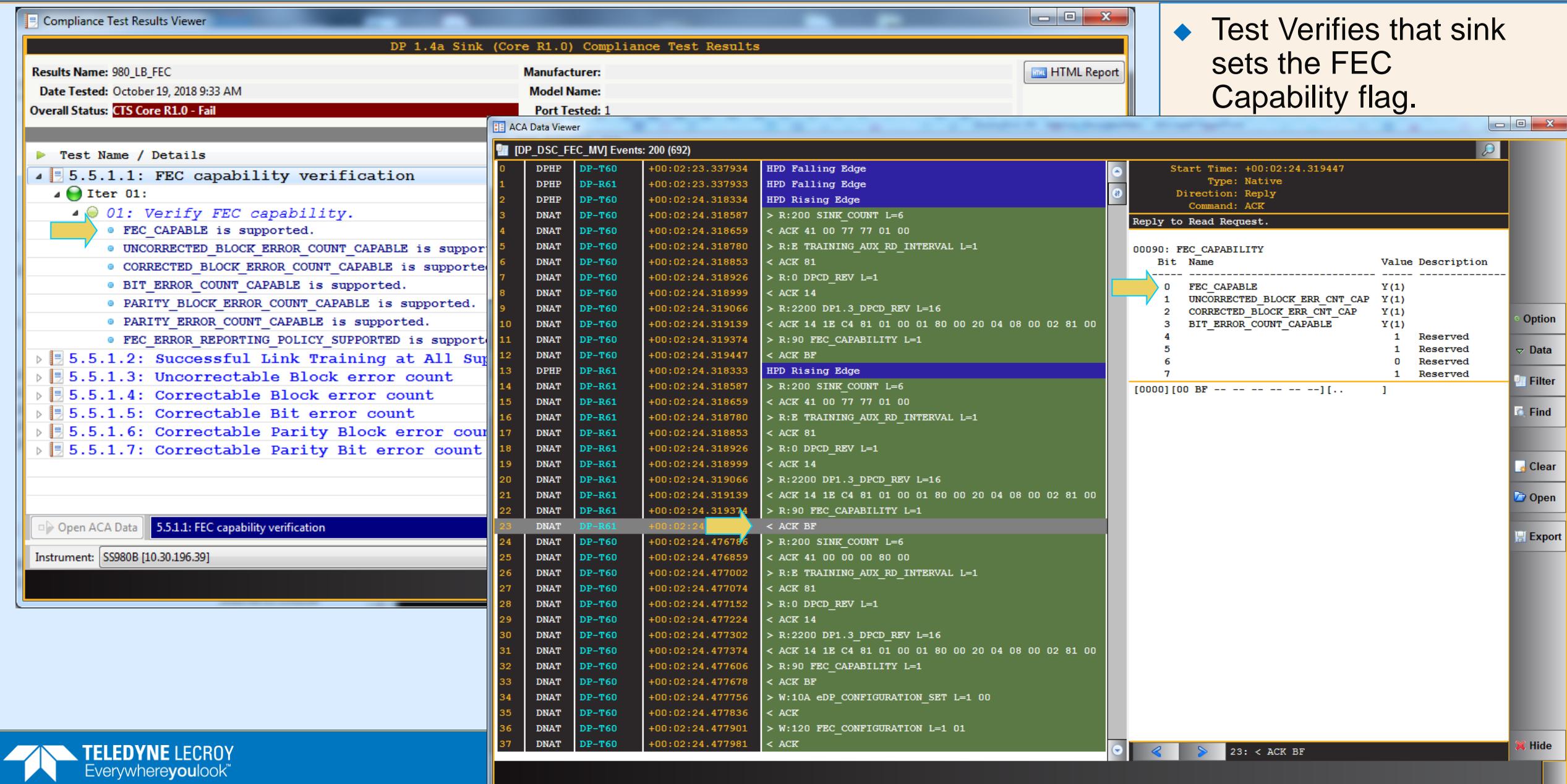
Event	Time	Type	Direction	Command	Description
0	DPHP DP-R31 +21:58:37.350145	HPD Falling Edge			
1	DPHP DP-R31 +21:58:38.330584	HPD Rising Edge			
2	DNAT DP-R31 +21:58:38.331050	> R:200 SINK_COUNT L=6	<	ACK 41 00 77 77 01 00	
3	DNAT DP-R31 +21:58:38.331122	< ACK 41 00 77 77 01 00	>	R:E TRAINING_AUX_RD_INTERVAL L=1	
4	DNAT DP-R31 +21:58:38.331260	> R:E TRAINING_AUX_RD_INTERVAL L=1	<	ACK 81	
5	DNAT DP-R31 +21:58:38.331332	< ACK 81	>	R:0 DPCD_REV L=1	
6	DNAT DP-R31 +21:58:38.331409	> R:0 DPCD_REV L=1	<	ACK 14	
7	DNAT DP-R31 +21:58:38.331482	< ACK 14	>	R:2200 DP1.3_DPCD_REV L=16	
8	DNAT DP-R31 +21:58:38.331557	> R:2200 DP1.3_DPCD_REV L=16	<	ACK 14 1E C4 81 01 00 01 80 00 20 04 08 00 02 81 00	
9	DNAT DP-R31 +21:58:38.331629	< ACK 14 1E C4 81 01 00 01 80 00 20			

DisplayPort Sink Forward Error Compliance Testing – List of Tests

■ List of DP FEC Sink Compliance Tests



Sink Forward Error Correction Compliance Test – Test ID# 5.5.1.1



Sink Forward Error Correction Compliance Test – Test ID# 5.5.1.2

- ◆ This test verifies that the Sink DUT can link train with FEC

Compliance Test Results Viewer

DP 1.4a Sink (Core R1.0) Compliance Test Results

Results Name: 980_LB_FEC
Date Tested: October 19, 2018 9:33 AM
Overall Status: CTS Core R1.0 - Fail

Manufacturer:
Model Name:
Port Tested: 1

Test Results

Test Name / Details

5.5.1.2: Successful Link Training at All Supported Lane

Iter 01:

- 01: Link Training test for lane count = 1 and lane
- 02: Link Training test for lane count = 2 and lane
- 03: Link Training test for lane count = 4 and lane
- 04: Link Training test for lane count = 1 and lane
- 05: Link Training test for lane count = 2 and lane
- 06: Link Training test for lane count = 4 and lane
- 07: Link Training test for lane count = 1 and lane
- 08: Link Training test for lane count = 2 and lane
- 09: Link Training test for lane count = 4 and lane
- 10: Link Training test for lane count = 1 and lane
- 11: Link Training test for lane count = 2 and lane
 - HPD is asserted
 - Reference Source receives AUX_ACK at 1 attempts of SET_POWER
 - Reference Source receives AUX ACK from either write request of
 - Reference Source receives AUX ACK from either write request of
 - AUX Read 0x2201 (MAX_LINK_RATE) = 0xe
 - AUX Read 0x2202 (MAX_LANE_COUNT) = 0xc4
 - Link Training at lane count 2 and link rate 8.1 successful
 - FEC Decode enable link symbol sequence detected over main link
 - For lane 1 FEC uncorrectable Block error counter reports 0
 - For lane 1 FEC correctable Block error counter reports 0
 - For lane 1 FEC correctable Bit error counter reports 0
 - For lane 1 FEC correctable parity block error counter reports
 - For lane 1 FEC correctable parity bit error counter reports 0
 - For lane 2 FEC uncorrectable Block error counter reports 0
 - For lane 2 FEC correctable Block error counter reports 0
 - For lane 2 FEC correctable Bit error counter reports 0
 - For lane 2 FEC correctable parity block error counter reports
 - For lane 2 FEC correctable parity bit error counter reports 0
 - Sink DUT reports, FEC Decode disable link symbol sequence detected
- 12: Link Training test for lane count = 4 and lane

5.5.1.3: Uncorrectable Block error count

5.5.1.1: FEC capability verification

Instrument: SS980B [10.30.196.39]

ACA Data Viewer

[ACA-5_5_1_2_01] Events: 1938 (4718)

Event Number	Transmitter	Receiver	Timestamp	Message
74	DPLT	DP-T30	+22:07:48.187419	> R:206 ADJUST_REQUEST_LANE0_1 L=2
75	DPLT	DP-T30	+22:07:48.187491	< ACK 44 44
76	DPLT	DP-T30	+22:07:48.187760	> W:103 TRAINING_LANE0_SET L=4 08 08 08 08
77	DPLT	DP-T30	+22:07:48.187864	< ACK
78	DPLT	DP-T30	+22:07:48.191880	> R:202 LANE0_1_STATUS: L=3
79	DPLT	DP-T30	+22:07:48.191952	< ACK 07 00 81
80	DPLT	DP-T30	+22:07:48.192048	> R:204 LANE_ALIGN_STATUS_UPDATED L=2
81	DPLT	DP-T30	+22:07:48.192120	< ACK 01 00
82	DPLT	DP-T30	+22:07:48.192218	> W:102 TRAINING_PATTERN_SET: L=1 00
83	DPLT	DP-T30	+22:07:48.192298	< ACK
84	DPLT	DP-T30	+22:07:48.192387	> R:102 TRAINING_PATTERN_SET: L=1 00
85	DPLT	DP-T30	+22:07:48.192467	< ACK
86	DNAT	DP-T30	+22:07:48.192543	> R:200 SINK_COUNT L=6
87	DNAT	DP-T30	+22:07:48.192616	< ACK 41 00 07 00 01 00
88	DPLT	DP-T30	+22:07:48.192814	> R:100 LINK_BW_SET L=8
89	DPLT	DP-T30	+22:07:48.192887	< ACK 06 81 00 08 08 08 08 10
90	DNAT	DP-T30	+22:07:48.193055	> R:200 SINK_COUNT L=8
91	DNAT	DP-T30	+22:07:48.193127	< ACK 41 00 07 00 01 00 88 88
92	DPLT	DP-T30	+22:07:48.270603	> R:100 LINK_BW_SET L=2
93	DPLT	DP-T30	+22:07:48.270676	< ACK 06 81
94	DPLT	DP-T30	+22:07:48.380262	> R:100 LINK_BW_SET L=2
95	DPLT	DP-T30	+22:07:48.380335	< ACK 06 81
96	DNAT	DP-T30	+22:07:48.780945	> W:280 FEC_STATUS L=1 FF
97	DNAT	DP-T30	+22:07:48.781026	< ACK
98	DPLT	DP-T30	+22:07:48.784485	> R:100 LINK_BW_SET L=2
99	DPLT	DP-T30	+22:07:48.784557	< ACK 06 81
100	DPLT	DP-T30	+22:07:48.893306	> R:100 LINK_BW_SET L=2
101	DPLT	DP-T30	+22:07:48.893379	< ACK 06 81
102	DNAT	DP-T30	+22:07:49.0000970	> R:280 FEC_STATUS L=1
103	DNAT	DP-T30	+22:07:49.0000970	< ACK 01
104	DNAT	DP-T30	+22:07:49.001049	> W:120 FEC_CONFIGURATION L=1 01
105	DNAT	DP-T30	+22:07:49.001130	< ACK
106	DNAT	DP-T30	+22:07:49.001201	> W:120 FEC_CONFIGURATION L=1 07
107	DNAT	DP-T30	+22:07:49.001281	< ACK
108	DNAT	DP-T30	+22:07:49.002387	> W:120 FEC_CONFIGURATION L=1 03
109	DNAT	DP-T30	+22:07:49.002468	< ACK
110	DNAT	DP-T30	+22:07:49.002532	> R:281 FEC_ERROR_COUNT0 L=2
111	DNAT	DP-T30	+22:07:49.002604	< ACK 00 80

Start Time: +22:07:49.0000970
Type: Native
Direction: Reply
Command: ACK
Reply to Read Request.

00280: FEC_STATUS

Bit	Name	Value	Description
0	DECODE_EN_DETECTED	Y(1)	
1	DECODE_DIS_DETECTED	N(0)	
2		0	Reserved
3		0	Reserved
4		0	Reserved
5		0	Reserved
6		0	Reserved
7		0	Reserved

[0000] [00 01 -- -- -- -- -- --] [..]

Filter

Find

Clear

Open

Export

Hide

Sink FEC Compliance – Uncorrectable Block Errors - Test ID# 5.5.1.3

Compliance Test Results Viewer

DP 1.4a Sink (Core R1.0) Compliance Test Results

Results Name: 980_LB_FEC

Date Tested: October 19, 2018 9:33 AM

Overall Status: CTS Core R1.0 - Fail

Manufacturer:

Model Name:

Port Tested: 1

[HTML Report](#)

Test Results

- ▶ Test Name / Details
- ▶ 5.5.1.2: Successful Link Training at All Supported Lane Count
- ▶ 5.5.1.3: Uncorrectable Block error count
 - Iter 01:
 - 01: Link Training test for lane count = 1 and lane rate = 100
 - 02: Link Training test for lane count = 2 and lane rate = 100
 - 03: Link Training test for lane count = 4 and lane rate = 100
 - 04: Link Training test for lane count = 1 and lane rate = 200
 - 05: Link Training test for lane count = 2 and lane rate = 200
 - 06: Link Training test for lane count = 4 and lane rate = 200
 - 07: Link Training test for lane count = 1 and lane rate = 400
 - 08: Link Training test for lane count = 2 and lane rate = 400
 - 09: Link Training test for lane count = 4 and lane rate = 400
 - 10: Link Training test for lane count = 1 and lane rate = 800
 - 11: Link Training test for lane count = 2 and lane rate = 800
 - HPD is asserted
 - Reference Source receives AUX ACK at 1 attempts of SET_POWER
 - Reference Source receives AUX ACK from either write request of SET_POWER
 - Reference Source receives AUX ACK from either write request of FEC
 - AUX Read 0x2201 (MAX_LINK_RATE) = 0x1e
 - AUX Read 0x2202 (MAX_LANE_COUNT) = 0xc4
 - Link Training at lane count 2 and link rate 8.1 successful
 - FEC Decode enable link symbol sequence detected over main link. (FEC)
 - ==> On Lane 1, after inserting 1000 FEC uncorrectable block errors (1180).
 - Lane 1 FEC uncorrectable block errors out of range (1180).
 - Lane 2 Reported FEC uncorrectable block errors (193).
 - ==> On Lane 2, after inserting 1000 FEC uncorrectable block errors (193).
 - Lane 1 Reported FEC uncorrectable block errors (3).
 - Lane 2 FEC uncorrectable block errors in range (982).
 - Sink DUT reports, FEC Decode disable link symbol sequence detected
 - 12: Link Training test for lane count = 4 and lane rate = 800
 - 5.5.1.4: Correctable Block error count
 - 5.5.1.5: Correctable Bit error count

[Open ACA Data](#)

5.5.1.1: FEC capability verification

Instrument: SS980B [10.30.196.39]

ACA Data Viewer

[ACA-5_5_1_3_01] Events: 1826 (4614)

Event ID	Source	Destination	Timestamp	Message
1588	DPLT	DP-T30	+22:10:33.947269	> R:100 LINK_BW_SET L=2
1589	DPLT	DP-T30	+22:10:33.947341	< ACK 1E 82
1590	DPLT	DP-T30	+22:10:34.056162	> R:100 LINK_BW_SET L=2
1591	DPLT	DP-T30	+22:10:34.056235	< ACK 1E 82
1592	DNAT	DP-T30	+22:10:34.165386	> R:280 FEC_STATUS L=1
1593	DNAT	DP-T30	+22:10:34.165458	< ACK 01
1594	DNAT	DP-T30	+22:10:34.165548	> W:120 FEC_CONFIGURATION L=1 01
1595	DNAT	DP-T30	+22:10:34.165628	< ACK
1596	DNAT	DP-T30	+22:10:34.165729	> W:120 FEC_CONFIGURATION L=1 07
1597	DNAT	DP-T30	+22:10:34.165809	< ACK
1598	DNAT	DP-T30	+22:10:34.167400	> W:120 FEC_CONFIGURATION L=1 01
1599	DNAT	DP-T30	+22:10:34.167481	< ACK
1600	DNAT	DP-T30	+22:10:34.167728	> W:120 FEC_CONFIGURATION L=1 07
1601	DNAT	DP-T30	+22:10:34.167809	< ACK
1602	DNAT	DP-T30	+22:10:36.271660	> W:120 FEC_CONFIGURATION L=1 03
1603	DNAT	DP-T30	+22:10:36.271741	< ACK
1604	DNAT	DP-T30	+22:10:36.271817	> R:281 FEC_ERROR_COUNTO L=2
1605	DNAT	DP-T30	+22:10:36.271889	< ACK 9C 84
1606	DNAT	DP-T30	+22:10:36.272014	> W:120 FEC_CONFIGURATION L=1 13
1607	DNAT	DP-T30	+22:10:36.272095	< ACK
1608	DNAT	DP-T30	+22:10:36.272172	> R:281 FEC_ERROR_COUNTO L=2
1609	DNAT	DP-T30	+22:10:36.272245	< ACK C1 80
1610	DNAT	DP-T30	+22:10:36.272350	> W:120 FEC_CONFIGURATION L=1 01
1611	DNAT	DP-T30	+22:10:36.272431	< ACK
1612	DNAT	DP-T30	+22:10:36.272640	> W:120 FEC_CONFIGURATION L=1 07
1613	DNAT	DP-T30	+22:10:36.272720	< ACK
1614	DNAT	DP-T30	+22:10:38.358184	> W:120 FEC_CONFIGURATION L=1 03
1615	DNAT	DP-T30	+22:10:38.358264	< ACK
1616	DNAT	DP-T30	+22:10:38.358327	> R:281 FEC_ERROR_COUNTO L=2
1617	DNAT	DP-T30	+22:10:38.358400	< ACK 03 80
1618	DNAT	DP-T30	+22:10:38.358495	> W:120 FEC_CONFIGURATION L=1 13
1619	DNAT	DP-T30	+22:10:38.358575	< ACK
1620	DNAT	DP-T30	+22:10:38.358644	> R:281 FEC_ERROR_COUNTO L=2
1621	DNAT	DP-T30	+22:10:38.358717	< ACK D6 83
1622	DNAT	DP-T30	+22:10:38.358810	> W:280 FEC_STATUS L=1 FF
1623	DNAT	DP-T30	+22:10:38.358890	< ACK
1624	DPLT	DP-T30	+22:10:38.362213	> R:100 LINK_BW_SET L=2
1625	DPLT	DP-T30	+22:10:38.362286	< ACK 1E 82

◆ Test verifies that sink can count uncorrectable errors.

Start Time: +22:10:36.272245
Type: Native
Direction: Reply
Command: ACK

Reply to Read Request.

00281: FEC_ERROR_COUNT0			
Bit	Name	Value	Description
7-0	Count7:0	193	

00282: FEC_ERROR_COUNT1

Bit	Name	Value	Description
6-0	Count14:8	0	
7	Count Valid	Y(1)	

[0000] [00 C1 80 -- -- -- -- --] [...]]

Option
Data
Filter
Find
Clear
Open
Export
Hide

Sink FEC Compliance Test – Correctable Block Errors - Test ID# 5.5.1.4

The screenshot shows the Teledyne Lecroy Compliance Test Results Viewer interface. The main window displays test results for DP 1.4a Sink (Core R1.0). Key details include:

- Results Name:** 980_LB_FEC
- Date Tested:** October 19, 2018 9:33 AM
- Overall Status:** CTS Core R1.0 - Fail
- Manufacturer:** [redacted]
- Model Name:** [redacted]
- Port Tested:** 1
- Test Results:** A large list of test cases, many of which have failed. A yellow box highlights a specific failure: "5.5.1.4: Correctable Block error count" with status "Iter 01: 11: Link Training test for lane count = 2 and lane rate 8.1 failed". Below this, a blue box highlights a series of events related to FEC errors.
- Instrument:** SS980B [10.30.196.39]

A separate window titled "ACA Data Viewer" is overlaid on the main window, showing a list of events with timestamps and types. A yellow arrow points from the highlighted test case in the main window to the corresponding event log in the ACA Data Viewer. Another yellow arrow points from the "5.5.1.4" failure in the main window to the "5.5.1.4_01" event in the ACA Data Viewer. The ACA Data Viewer log entries are as follows:

Event ID	Type	Timestamp	Details
1636	DNAT	DP-T30	+22:12:41.153312 > R:280 FEC_STATUS L=1
1637	DNAT	DP-T30	+22:12:41.153385 < ACK 01
1638	DNAT	DP-T30	+22:12:41.153455 > W:120 FEC_CONFIGURATION L=1 01
1639	DNAT	DP-T30	+22:12:41.153535 < ACK
1640	DNAT	DP-T30	+22:12:41.153601 > W:120 FEC_CONFIGURATION L=1 07
1641	DNAT	DP-T30	+22:12:41.153682 < ACK
1642	DNAT	DP-T30	+22:12:41.154738 > W:120 FEC_CONFIGURATION L=1 01
1643	DNAT	DP-T30	+22:12:41.154819 < ACK
1644	DNAT	DP-T30	+22:12:41.154995 > W:120 FEC_CONFIGURATION L=1 07
1645	DNAT	DP-T30	+22:12:41.155075 < ACK
1646	DNAT	DP-T30	+22:12:43.281084 > W:120 FEC_CONFIGURATION L=1 05
1647	DNAT	DP-T30	+22:12:43.281164 < ACK
1648	DNAT	DP-T30	+22:12:43.281234 > R:281 FEC_ERROR_COUNT0 L=2
1649	DNAT	DP-T30	+22:12:43.281306 < ACK E6 83
1650	DNAT	DP-T30	+22:12:43.281394 > W:120 FEC_CONFIGURATION L=1 15
1651	DNAT	DP-T30	+22:12:43.281474 < ACK
1652	DNAT	DP-T30	+22:12:43.281537 > R:281 FEC_ERROR_COUNT0 L=2
1653	DNAT	DP-T30	+22:12:43.281537 < ACK 02 80
1654	DNAT	DP-T30	+22:12:43.281702 > W:120 FEC_CONFIGURATION L=1 01
1655	DNAT	DP-T30	+22:12:43.281782 < ACK
1656	DNAT	DP-T30	+22:12:43.281957 > W:120 FEC_CONFIGURATION L=1 07
1657	DNAT	DP-T30	+22:12:43.282037 < ACK
1658	DNAT	DP-T30	+22:12:45.398044 > W:120 FEC_CONFIGURATION L=1 05
1659	DNAT	DP-T30	+22:12:45.398124 < ACK
1660	DNAT	DP-T30	+22:12:45.398194 > R:281 FEC_ERROR_COUNT0 L=2
1661	DNAT	DP-T30	+22:12:45.398267 < ACK 05 80
1662	DNAT	DP-T30	+22:12:45.398355 > W:120 FEC_CONFIGURATION L=1 15
1663	DNAT	DP-T30	+22:12:45.398436 < ACK
1664	DNAT	DP-T30	+22:12:45.398503 > R:281 FEC_ERROR_COUNT0 L=2
1665	DNAT	DP-T30	+22:12:45.398575 < ACK E3 83
1666	DNAT	DP-T30	+22:12:45.398666 > W:280 FEC_STATUS L=1 FF
1667	DNAT	DP-T30	+22:12:45.398746 < ACK
1668	DPLT	DP-T30	+22:12:45.402064 > R:100 LINK_BW_SET L=2
1669	DPLT	DP-T30	+22:12:45.402136 < ACK 1E 82
1670	DPLT	DP-T30	+22:12:45.510989 > R:100 LINK_BW_SET L=2
1671	DPLT	DP-T30	+22:12:45.511061 < ACK 1E 82
1672	DNAT	DP-T30	+22:12:45.618676 > R:280 FEC_STATUS L=1
1673	DNAT	DP-T30	+22:12:45.618749 < ACK 02

- ◆ Test verifies that sink can count correctable Symbol

Start Time: +22:12:43.281609
Type: Native
Direction: Reply
Command: ACK

Reply to Read Request.

00281: FEC_ERROR_COUNT0

Bit	Name	Value	Description
7-0	Count7:0	2	

00282: FEC_ERROR_COUNT1

Bit	Name	Value	Description
6-0	Count14:8	0	
7	Count Valid	Y(1)	

[0000] [00 02 80 -- -- -- --] [...]]

Option

Data

Filter

Find

Clear

Open

Export

Hide

Sink FEC Compliance Test – Correctable Bit Errors - Test ID# 5.5.1.5

Compliance Test Results Viewer

DP 1.4a Sink (Core R1.0) Compliance Test Results

Results Name: 980_LB_FEC
Date Tested: October 19, 2018 9:33 AM
Overall Status: CTS Core R1.0 - Fail

Manufacturer:
Model Name:
Port Tested: 1

Test Results

▶ **Test Name / Details**

▷ 5.5.1.2: Successful Link Training at All Supported Lane Counts and Link Rates with FEC

▷ 5.5.1.3: Uncorrectable Block error count

▷ 5.5.1.4: Correctable Block error count

▷ 5.5.1.5: Correctable Bit error count

 Iter 01:

- ▷ 01: Link Training test for lane count = 1 and lane rate = 8.1 successful
- ▷ 02: Link Training test for lane count = 2 and lane rate = 8.1 successful
- ▷ 03: Link Training test for lane count = 4 and lane rate = 8.1 successful
- ▷ 04: Link Training test for lane count = 1 and lane rate = 16.2 successful
- ▷ 05: Link Training test for lane count = 2 and lane rate = 16.2 successful
- ▷ 06: Link Training test for lane count = 4 and lane rate = 16.2 successful
- ▷ 07: Link Training test for lane count = 1 and lane rate = 32.4 successful
- ▷ 08: Link Training test for lane count = 2 and lane rate = 32.4 successful
- ▷ 09: Link Training test for lane count = 4 and lane rate = 32.4 successful
- ▷ 10: Link Training test for lane count = 1 and lane rate = 64.8 successful
- Iter 01:
 - HPD is asserted
 - Reference Source receives AUX_ACK at 1 attempts of SET_POWER
 - Reference Source receives AUX ACK from either write request of SET_POWER
 - Reference Source receives AUX ACK from either write request of FE
 - AUX Read 0x2201 (MAX_LINK_RATE) = 0xe
 - AUX Read 0x2202 (MAX_LANE_COUNT) = 0xc4
 - Link Training at lane count 2 and link rate 8.1 successful
 - FEC Decode enable link symbol sequence detected over main link. (1)
 - ⇒ On Lane 1, after inserting 1000 FEC correctable bit errors.
 - Lane 1 FEC correctable bit errors in range (998)
 - Lane 2 Reported FEC correctable bit errors (2).
 - ⇒ On Lane 2, after inserting 1000 FEC correctable bit errors.
 - Lane 2 FEC correctable bit errors in range (1000).
 - Sink DUT reports, FEC Decode disable link symbol sequence detected
- ▷ 12: Link Training test for lane count = 4 and lane rate = 64.8 successful

▷ 5.5.1.6: Correctable Parity Block error count

Open ACA Data

5.5.1.2: Successful Link Training at All Supported Lane Counts and Link Rates with FEC Enabled

Instrument: SS980B [10.30.196.39]

ACA Data Viewer

[ACA-5_5_1_5_01] Events: 18		
Event ID	Event Type	Event Description
1635	DPLT	DP-T30
1636	DNAT	DP-T30
1637	DNAT	DP-T30
1638	DNAT	DP-T30
1639	DNAT	DP-T30
1640	DNAT	DP-T30
1641	DNAT	DP-T30
1642	DNAT	DP-T30
1643	DNAT	DP-T30
1644	DNAT	DP-T30
1645	DNAT	DP-T30
1646	DNAT	DP-T30
1647	DNAT	DP-T30
1648	DNAT	DP-T30
1649	DNAT	DP-T30
1650	DNAT	DP-T30
1651	DNAT	DP-T30
1652	DNAT	DP-T30
1653	DNAT	DP-T30
1654	DNAT	DP-T30
1655	DNAT	DP-T30
1656	DNAT	DP-T30
1657	DNAT	DP-T30
1658	DNAT	DP-T30
1659	DNAT	DP-T30
1660	DNAT	DP-T30
1661	DNAT	DP-T30
1662	DNAT	DP-T30
1663	DNAT	DP-T30
1664	DNAT	DP-T30
1665	DNAT	DP-T30
1666	DNAT	DP-T30
1667	DNAT	DP-T30
1668	DPLT	DP-T30
1669	DPLT	DP-T30
1670	DPLT	DP-T30

◆ Test verifies that sink can count correctable Bit errors. Bit errors

The screenshot shows the ACA Data Viewer interface. The main window displays a list of events with details like timestamp, source, destination, and message content. A specific event, 1653, is highlighted in blue. To the right, a detailed view of this event is shown, including its type (Native), direction (Reply), command (ACK), and a note about it being a reply to a read request. Below this, two tables show FEC error counts: one for COUNT0 (value 2) and one for COUNT1 (value 0). A yellow arrow points from the event list to the COUNT0 table, indicating the correlation between the test results and the software output.

Event ID	Source	Destination	Timestamp	Message Content
1635	DPLT	DP-T30	+22:14:46.387294	< ACK 1E 82
1636	DNAT	DP-T30	+22:14:46.507891	> R:280 FEC_STATUS L=1
1637	DNAT	DP-T30	+22:14:46.507963	< ACK 01
1638	DNAT	DP-T30	+22:14:46.508034	> W:120 FEC_CONFIGURATION L=1 01
1639	DNAT	DP-T30	+22:14:46.508115	< ACK
1640	DNAT	DP-T30	+22:14:46.508184	> W:120 FEC_CONFIGURATION L=1 07
1641	DNAT	DP-T30	+22:14:46.508265	< ACK
1642	DNAT	DP-T30	+22:14:46.509326	> W:120 FEC_CONFIGURATION L=1 01
1643	DNAT	DP-T30	+22:14:46.509407	< ACK
1644	DNAT	DP-T30	+22:14:46.509582	> W:120 FEC_CONFIGURATION L=1 07
1645	DNAT	DP-T30	+22:14:46.509662	< ACK
1646	DNAT	DP-T30	+22:14:48.548895	> W:120 FEC_CONFIGURATION L=1 07
1647	DNAT	DP-T30	+22:14:48.548975	< ACK
1648	DNAT	DP-T30	+22:14:48.549036	> R:281 FEC_ERROR_COUNT0 L=2
1649	DNAT	DP-T30	+22:14:48.549109	< ACK E6 83
1650	DNAT	DP-T30	+22:14:48.549194	> W:120 FEC_CONFIGURATION L=1 17
1651	DNAT	DP-T30	+22:14:48.549275	< ACK
1652	DNAT	DP-T30	+22:14:48.549340	> R:281 FEC_ERROR_COUNT0 L=2
1653	DNAT	DP-T30	+22:14:48.549498	< ACK 02 80
1654	DNAT	DP-T30	+22:14:48.549498	> W:120 FEC_CONFIGURATION L=1 01
1655	DNAT	DP-T30	+22:14:48.549576	< ACK
1656	DNAT	DP-T30	+22:14:48.549742	> W:120 FEC_CONFIGURATION L=1 07
1657	DNAT	DP-T30	+22:14:48.549822	< ACK
1658	DNAT	DP-T30	+22:14:50.586622	> W:120 FEC_CONFIGURATION L=1 07
1659	DNAT	DP-T30	+22:14:50.586702	< ACK
1660	DNAT	DP-T30	+22:14:50.586767	> R:281 FEC_ERROR_COUNT0 L=2
1661	DNAT	DP-T30	+22:14:50.586840	< ACK 00 80
1662	DNAT	DP-T30	+22:14:50.586925	> W:120 FEC_CONFIGURATION L=1 17
1663	DNAT	DP-T30	+22:14:50.587006	< ACK
1664	DNAT	DP-T30	+22:14:50.587068	> R:281 FEC_ERROR_COUNT0 L=2
1665	DNAT	DP-T30	+22:14:50.587140	< ACK E8 83
1666	DNAT	DP-T30	+22:14:50.587223	> W:280 FEC_STATUS L=1 FF
1667	DNAT	DP-T30	+22:14:50.587303	< ACK
1668	DPLT	DP-T30	+22:14:50.590684	> R:100 LINK_BW_SET L=2
1669	DPLT	DP-T30	+22:14:50.590756	< ACK 1E 82
1670	DPLT	DP-T30	+22:14:50.699524	> R:100 LINK_BW_SET L=2
1671	DPLT	DP-T30	+22:14:50.699597	< ACK 1E 82
1672	DNAT	DP-T30	+22:14:50.809877	> R:280 FEC_STATUS L=1

Sink FEC Compliance Test – Correctable Parity Block Errors - Test ID# 5.5.1.6

Compliance Test Results Viewer

DP 1.4a Sink (Core R1.0) Compliance Test Results

Results Name: 980_LB_FEC
Date Tested: October 19, 2018 9:33 AM
Overall Status: CTS Core R1.0 - Fail

Manufacturer:
Model Name:
Port Tested: 1

HTML Report

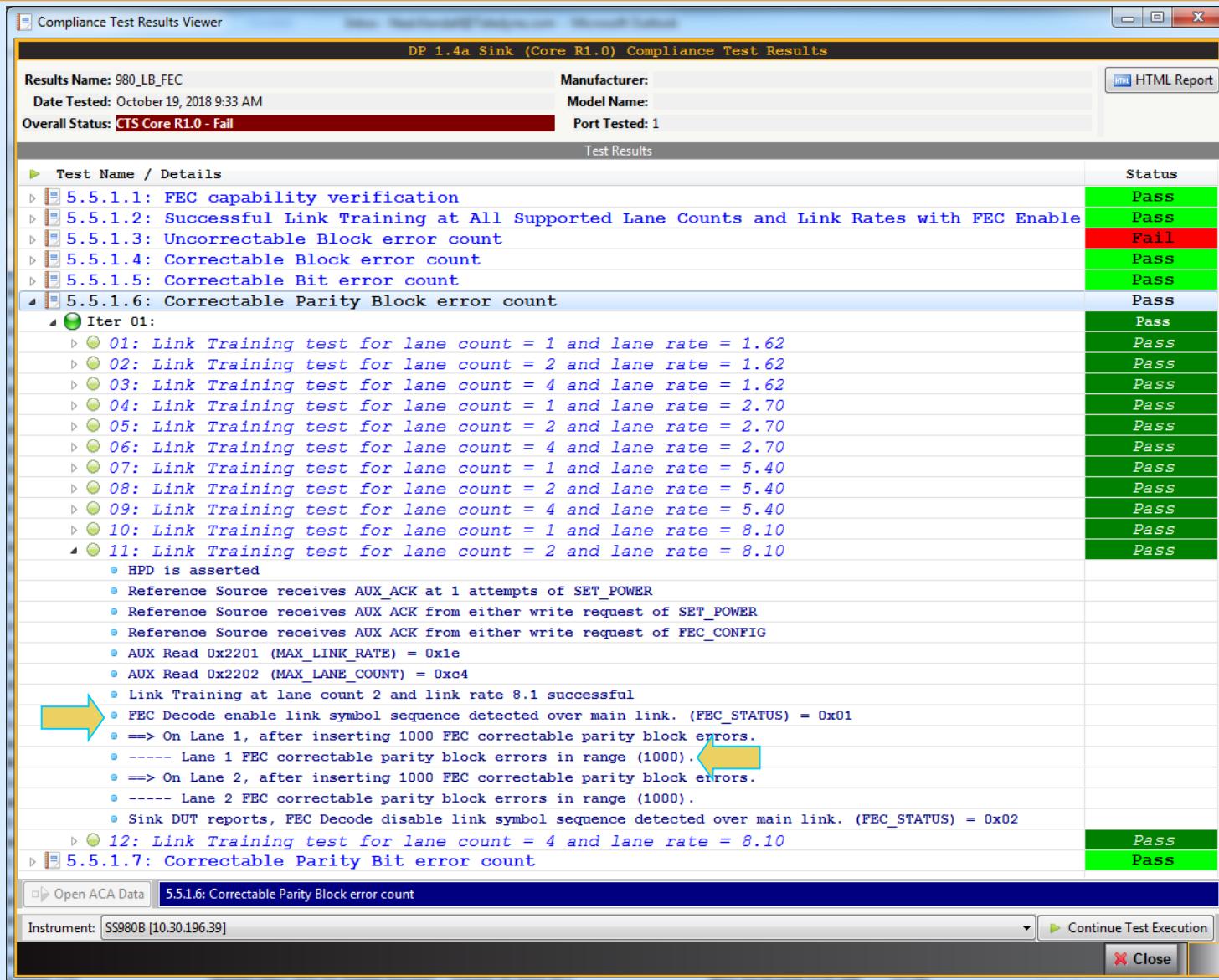
Test Results

Test Name / Details	Status
5.5.1.1: FEC capability verification	Pass
5.5.1.2: Successful Link Training at All Supported Lane Counts and Link Rates with FEC Enable	Pass
5.5.1.3: Uncorrectable Block error count	Fail
5.5.1.4: Correctable Block error count	Pass
5.5.1.5: Correctable Bit error count	Pass
5.5.1.6: Correctable Parity Block error count	Pass
Iter 01:	
01: Link Training test for lane count = 1 and lane rate = 1.62	Pass
02: Link Training test for lane count = 2 and lane rate = 1.62	Pass
03: Link Training test for lane count = 4 and lane rate = 1.62	Pass
04: Link Training test for lane count = 1 and lane rate = 2.70	Pass
05: Link Training test for lane count = 2 and lane rate = 2.70	Pass
06: Link Training test for lane count = 4 and lane rate = 2.70	Pass
07: Link Training test for lane count = 1 and lane rate = 5.40	Pass
08: Link Training test for lane count = 2 and lane rate = 5.40	Pass
09: Link Training test for lane count = 4 and lane rate = 5.40	Pass
10: Link Training test for lane count = 1 and lane rate = 8.10	Pass
11: Link Training test for lane count = 2 and lane rate = 8.10	Pass
HPD is asserted	
Reference Source receives AUX_ACK at 1 attempts of SET_POWER	
Reference Source receives AUX ACK from either write request of SET_POWER	
Reference Source receives AUX ACK from either write request of FEC_CONFIG	
AUX Read 0x2201 (MAX_LINK_RATE) = 0x1e	
AUX Read 0x2202 (MAX_LANE_COUNT) = 0xc4	
Link Training at lane count 2 and link rate 8.1 successful	
FEC Decode enable link symbol sequence detected over main link. (FEC_STATUS) = 0x01	
==> On Lane 1, after inserting 1000 FEC correctable parity block errors.	
----- Lane 1 FEC correctable parity block errors in range (1000).	
==> On Lane 2, after inserting 1000 FEC correctable parity block errors.	
----- Lane 2 FEC correctable parity block errors in range (1000).	
Sink DUT reports, FEC Decode disable link symbol sequence detected over main link. (FEC_STATUS) = 0x02	
12: Link Training test for lane count = 4 and lane rate = 8.10	Pass
5.5.1.7: Correctable Parity Bit error count	Pass

Open ACA Data 5.5.1.6: Correctable Parity Block error count

Instrument: SS980B [10.30.196.39]

Continue Test Execution Close



- ◆ Test verifies that sink can count parity block errors. Parity block errors are the errors within the parity blocks themselves.
- ◆ Test equipment injects a known number of errors and verifies by reading counters.
- ◆ Test is run at all lane rates and all lane count configurations.

Thank you for your Attention Questions?

Please contact me, Neal Kendall at:
neal.kendall@teledyne.com
If you have any questions.



980B Test Platform
equipped with
980 DisplayPort 1.4
Video Generator /
Protocol Analyzer
module

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