

# DisplayPort Protocol Compliance Testing

## Part 2 – Protocol Testing

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Webinar – September – 2019



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quantum data<sup>TM</sup>

980B w/ DP 1.4 Video Generator /  
Protocol Analyzer module



# About the Presenter



**Neal Kendall - Marketing Manager  
Teledyne LeCroy - quantumdata Product Family**

- ◆ Neal Kendall Marketing Manager Teledyne LeCroy for the quantumdata family of products.
- ◆ 15 years in the Video Protocols industry.

Please feel free to contact me, Neal Kendall at:  
[neal.kendall@teledyne.com](mailto:neal.kendall@teledyne.com)  
If you have any questions.

# Agenda – Cover a Broad Range of DisplayPort 1.4 Compliance Tests

- DisplayPort Brief Overview
- DisplayPort Link Layer Protocols
  - ◆ Link Training Protocols and Compliance
  - ◆ Main Link Protocols and Compliance
- DP Display Stream Compression (DSC)
  - ◆ DP DSC Operation
  - ◆ DP DSC Compliance
- DP Forward Error Correction (FEC)
  - ◆ DP FEC Operation
  - ◆ DP FEC Compliance
- DP High-Bandwidth Content Protection (HDCP) Protocols
  - ◆ DP HDCP Operation
  - ◆ DP HDCP Compliance

- ◆ Please Check out our other DisplayPort “Essentials of” Webinars available at:  
[https://www.quantumdata.com/980\\_dp\\_14\\_usb.html](https://www.quantumdata.com/980_dp_14_usb.html):
  - ◆ Essentials of DisplayPort Protocols
  - ◆ Essentials of HDCP 2.2 Protocols
  - ◆ Essentials of DisplayPort Link Layer Protocols Compliance Test Webinar
  - ◆ Essentials of Display Stream Compression (DSC) Protocols Webinar
  - ◆ Essentials of DisplayPort Forward Error Correction (FEC) Protocols Webinar
  - ◆ Essentials of **USB-C DisplayPort Alt Mode** Power Delivery Protocols Webinar

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[neal.kendall@teledyne.com](mailto:neal.kendall@teledyne.com)  
If you have any questions.

# DisplayPort Protocol Compliance Testing - Overview

- DisplayPort Compliance Tests are **“Normative” i.e. required** to obtain the DP logo.
- DisplayPort Link Layer Protocols
  - ◆ Link Training Protocols and Compliance
  - ◆ Main Link Protocols and Compliance
  - ◆ Source and Sink
- DP Display Stream Compression (DSC)
  - ◆ DP DSC Compliance (**Not yet Normative**)
  - ◆ Source and Sink
- DP Forward Error Correction (FEC)
  - ◆ DP FEC Compliance
  - ◆ Source and Sink
  - ◆ Required for DSC
- DP HDCP Protocols
  - ◆ DP HDPC Compliance
  - ◆ Source, Sink and Repeaters

- ◆ DP Compliance Test Process:
  - ◆ Select the type of compliance test you wish to run (left).
  - ◆ Complete the Capabilities Declaration Form (CDF).
  - ◆ Select the specific tests in the test suite (for source or sink).
  - ◆ Keep or de-select specific test iterations.
  - ◆ Initiate the test suite; monitor results in real time.
  - ◆ View the detailed test results and note specific cause of failures.
  - ◆ View the associated capture logs used by the test to determine compliance to pinpoint failures.
  - ◆ Save test results as HTML or QD format.
  - ◆ Disseminate results to colleagues at other locations.

# DisplayPort – Brief Overview

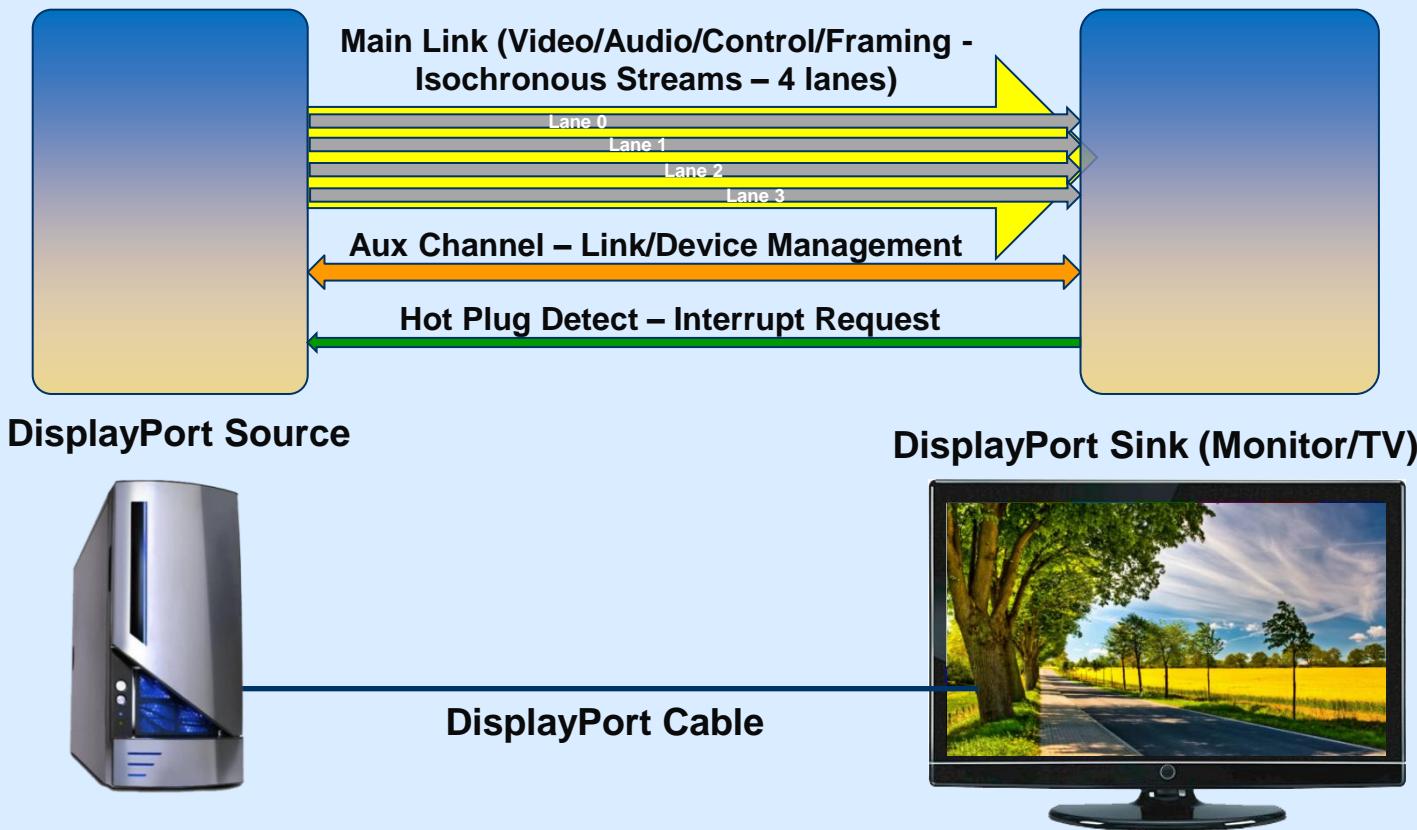
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980B w/ DP 1.4 Video Generator /  
Protocol Analyzer module



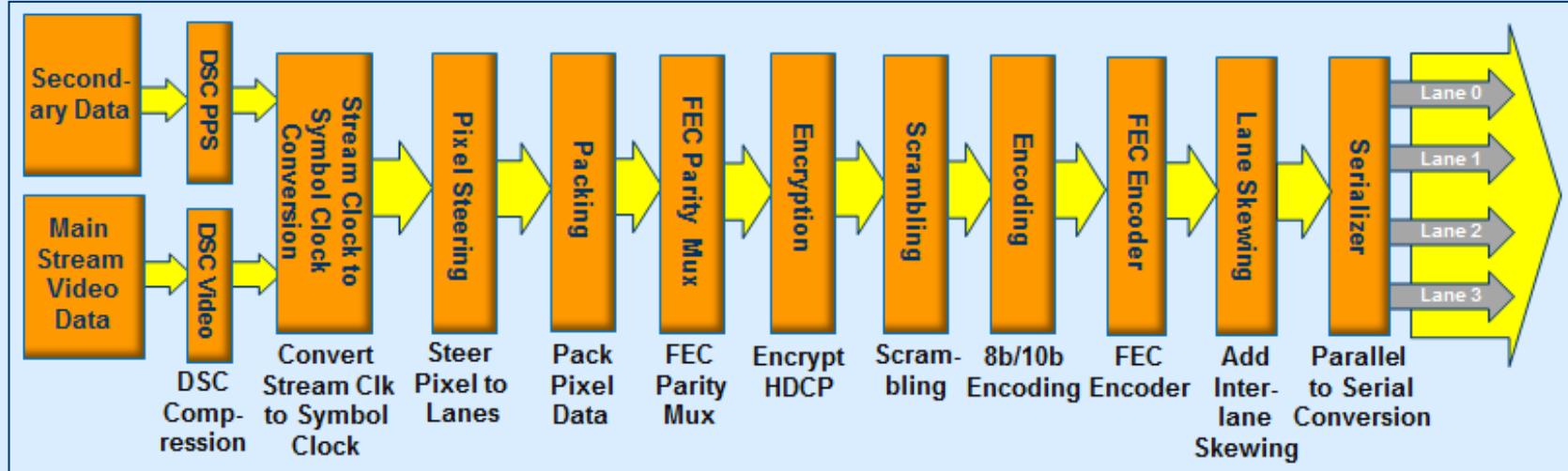
# DisplayPort Anatomy



- ◆ Main Link: Unidirectional, high-bandwidth channel used to transport video, audio, metadata and protocol control elements.
- ◆ Main Link 1, 2 or 4 Lane Configurations.
- ◆ Main Link 4 link rates:
  - ◆ 1.62Gbps (Reduced Bit Rate)
  - ◆ 2.7Gbps (High Bit Rate)
  - ◆ 5.4Gbps (High Bit Rate 2)
  - ◆ 8.1Gbps (High Bit Rate 3)
- ◆ No clock channel. Sink recovers clock using link transitions.
- ◆ Aux Channel: Bidirectional, half duplex channel at 1Mbps. Link Training, DSC and FEC Configuration, DPCD Register status, HDCP authentication & EDID exchange.
- ◆ Hot plug:
  - ◆ Connection Detection.
  - ◆ Interrupt mechanism for link failures.

# DisplayPort Main Link Functional Blocks

DisplayPort Transmitter Block



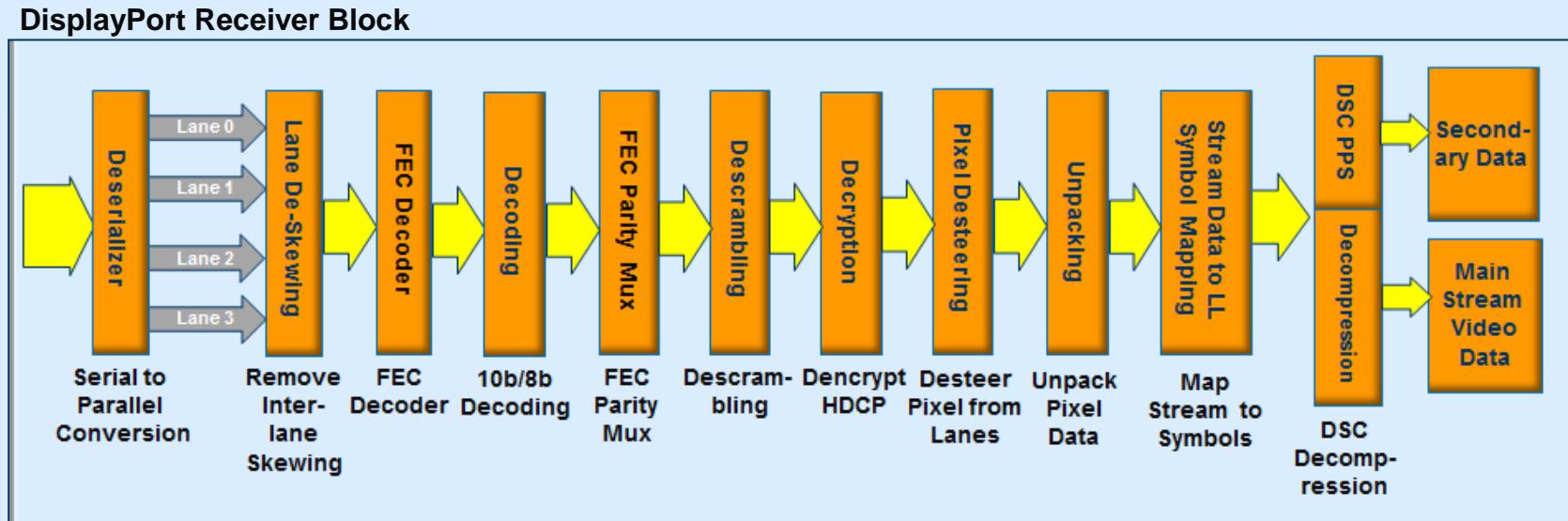
■ DisplayPort Transmitter Functional Block Diagram



DisplayPort Cable

DisplayPort Sink (Monitor/TV)

■ DisplayPort Receiver Functional Block Diagram



DisplayPort Source



DisplayPort Cable

# DisplayPort Main Link Protocol – One Video Frame



- Video packets occur during the active video period.
- Metadata: Main Stream Attributes (MSA) and Secondary Data Packets (SDP) occur during the vertical blanking period and are identified with Framing control characters.
- Fill characters used to stuff the unused link symbols.
- DSC slices used to partition video frame.

	Video		Fill Characters
	Metadata MSA, IF		Control Symbols
	Audio (SDP)		Control VBID w/ Compression Flag Set
	PPS		EoC

# DisplayPort Link Layer Protocol

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Protocol Analyzer module



# Link Layer Source Compliance Tests

DisplayPort Source  
(DUT)

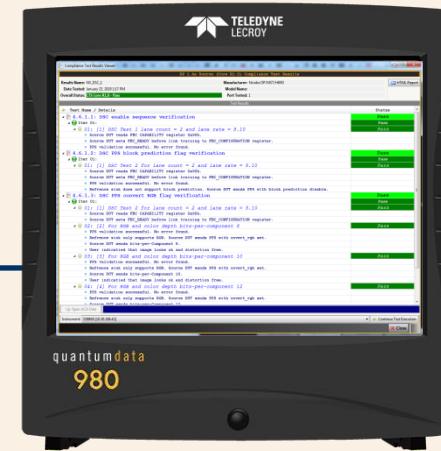


DisplayPort Cable

Other Webinars:

[https://www.quantumdata.com/980\\_dp\\_14\\_usb.html](https://www.quantumdata.com/980_dp_14_usb.html):

- ◆ Essentials of DisplayPort Protocols
- ◆ Essentials of DisplayPort Link Layer Protocols Compliance Test



DP 1.4 Reference Sink  
Example: Teledyne LeCroy  
quantumdata 980 Test Platform  
with DP 1.4 Protocol Analyzer /  
Video Generator

# Source Link Layer Compliance – List of Tests

DP 1.4a Source CT Core R1.0

Instrument: SS980B [10.30.196.70]

CDF Entry Test Selection Test Options / Preview Connect Cards...

Test List

All Count Options

Category / Test Name

- AUX Rd. after HPD
  - 4.2.1.1: Source DUT Retry on No-Reply During AUX Read after HPD Plug Event
  - 4.2.1.2: Source DUT Read After HPD Plug Event
  - 4.2.1.3: Source DUT Read After HPD Plug Event
  - 4.2.1.4: Source DUT Read After HPD Plug Event
  - 4.2.1.5: Source DUT Read After HPD Plug Event
- EDID and DPCD
  - 4.2.2.1: DPCD
  - 4.2.2.2: DPCD
  - 4.2.2.3: EDID
  - 4.2.2.4: EDID
  - 4.2.2.5: EDID
  - 4.2.2.6: EDID
  - 4.2.2.7: Branch
  - 4.2.2.8: EDID
  - 4.2.2.9: E-DD
  - 4.2.2.10: Link
- Link Training
  - 4.3.1.1: Success
  - 4.3.1.2: Success
  - 4.3.1.3: Success
  - 4.3.1.4: Success
  - 4.3.1.5: Success
  - 4.3.1.6: Success
  - 4.3.1.7: Success
  - 4.3.1.8: Unsuccessful
  - 4.3.1.9: Unsuccessful
  - 4.3.1.10: Unsuccessful
  - 4.3.1.11: Success
  - 4.3.1.12: Success
  - 4.3.1.13: Success

DP 1.4a Source CT Core R1.0

Instrument: SS980B [10.30.196.70]

CDF Entry Test Selection Test Options / Preview Connect Cards...

Test List

All Count Options

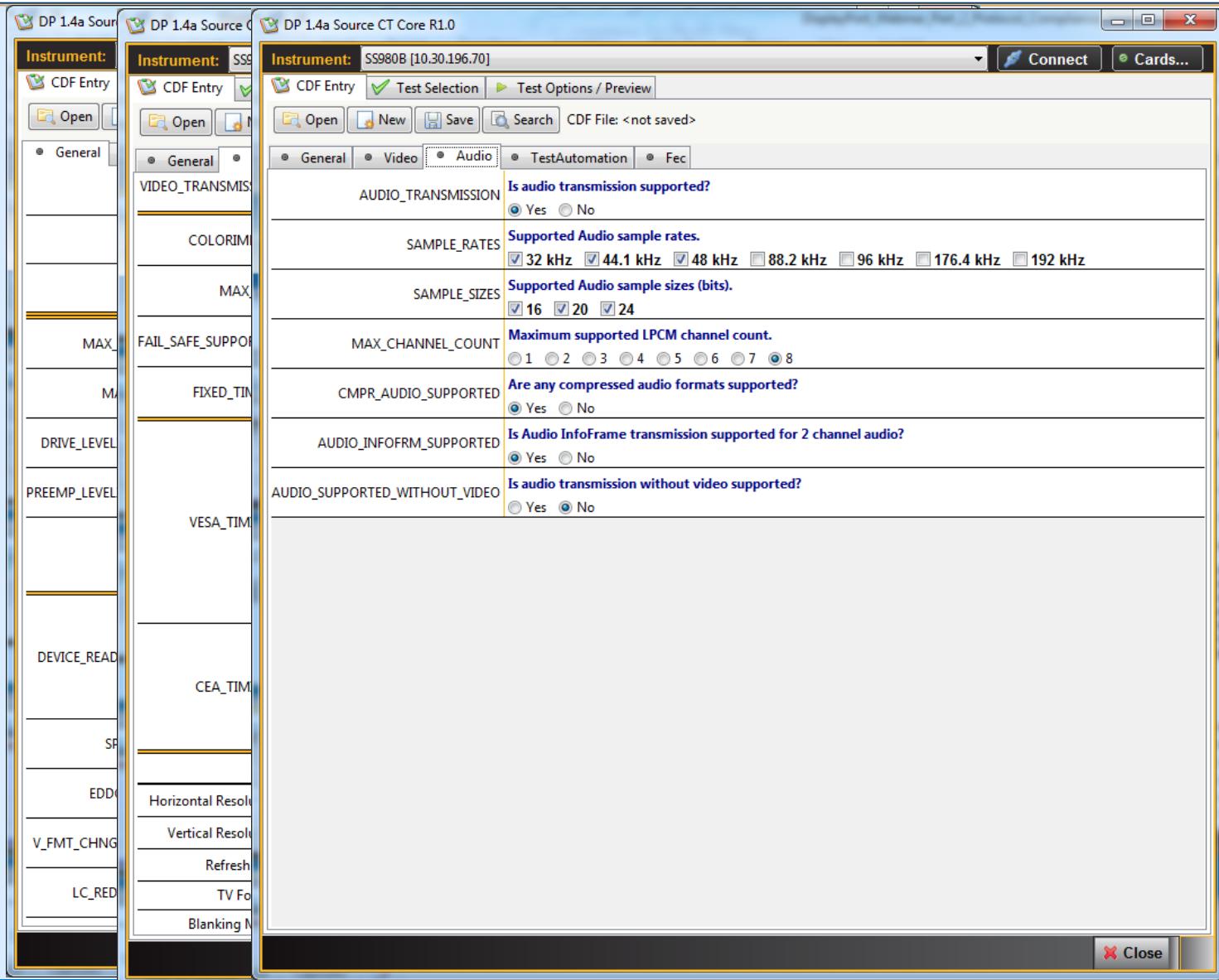
Category / Test Name

- Link Maint.
  - 4.3.2.1: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock.
  - 4.3.2.2: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Clock Recovery Lock.
  - 4.3.2.3: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock
  - 4.3.2.4: Handling of IRQ HPD Pulse with No Error Status Bits Set
  - 4.3.2.5: Lane Count Reduction
- Video
  - 4.3.3.1: Video Time Stamp Generation
  - 4.4.1.1: Pixel Data Packing and Steering
  - 4.4.1.2: Main Stream Data Packing and Stuffing Least Packed TU
  - 4.4.1.3: Main Stream Data Packing and Stuffing Most Packed TU
  - 4.4.2: Main Video Stream Format Change Handling
- Power Management
  - 4.4.3: Power Management
- Audio
  - 4.4.4.2: Audio Stream Header Synchronization
  - 4.4.4.3: Audio Time Stamp Generation
  - 4.4.4.4: Audio InfoFrame Packet
  - 4.4.4.5: Audio Stream Transmission
  - 4.4.4.6: Audio Start Sequence

Execute Tests

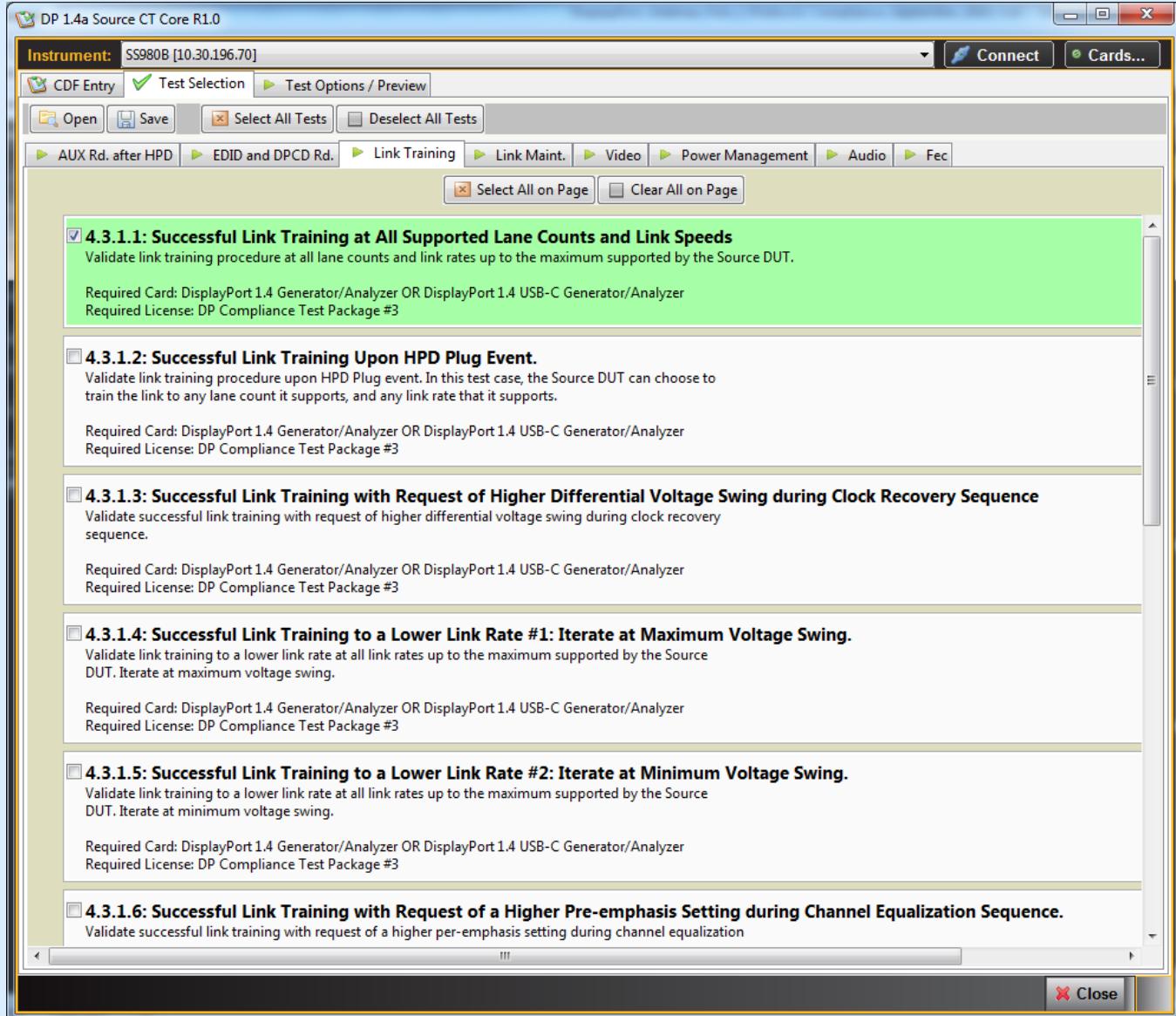
Close

# Source Link Layer Compliance - Entering the CDF Information



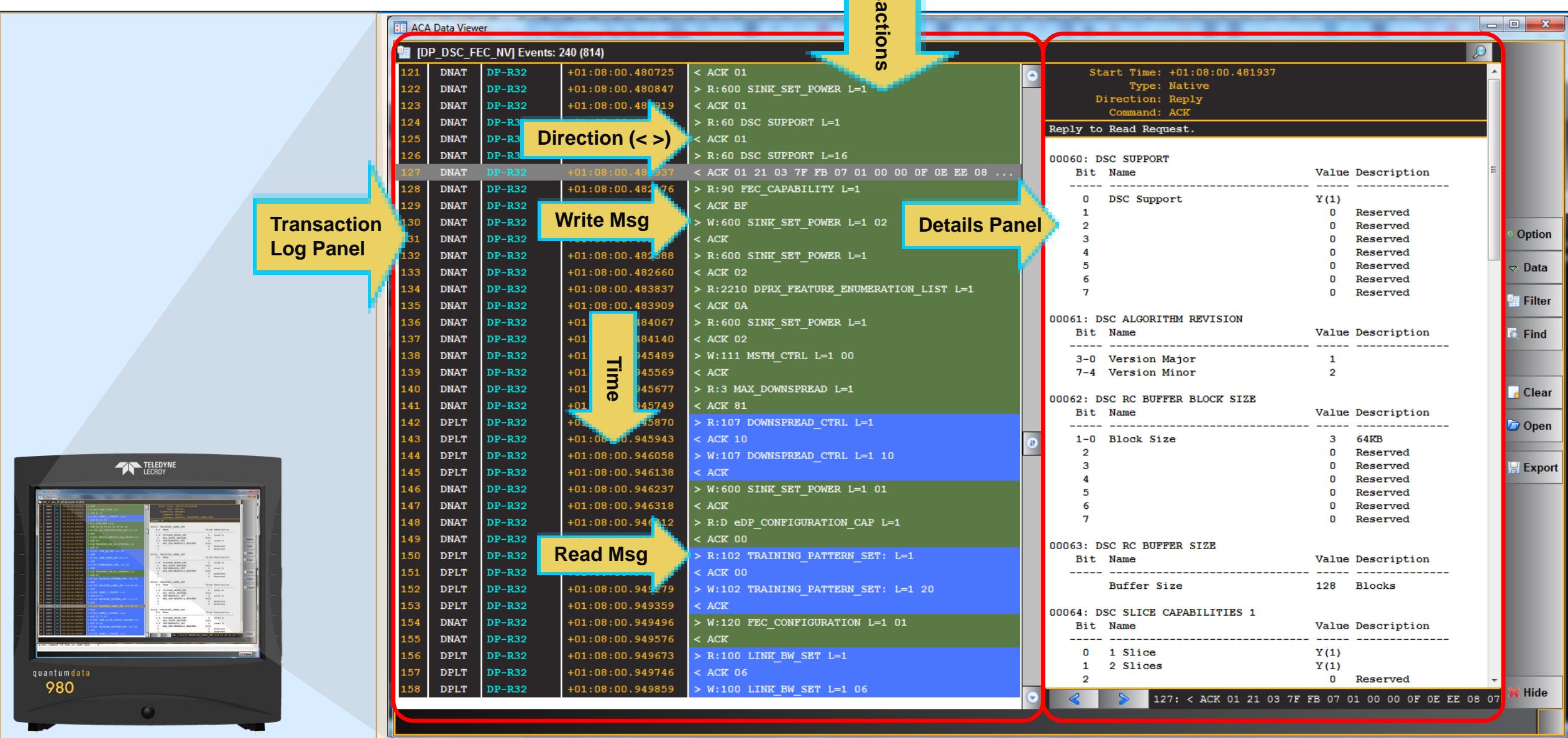
- Capabilities Declaration Form (CDF) must be filled out prior to the running the test.
- CDF is used by the reference sink to know which Link Layer related sink features to test.
- Video – Described video capabilities of the sink device.
- Audio – Described audio capabilities of the sink device.

# Source Link Layer Compliance - Test 4.3.1.1 Successful Link Training



- Select the desired test(s)

# 980 Auxiliary Channel Analyzer (ACA)

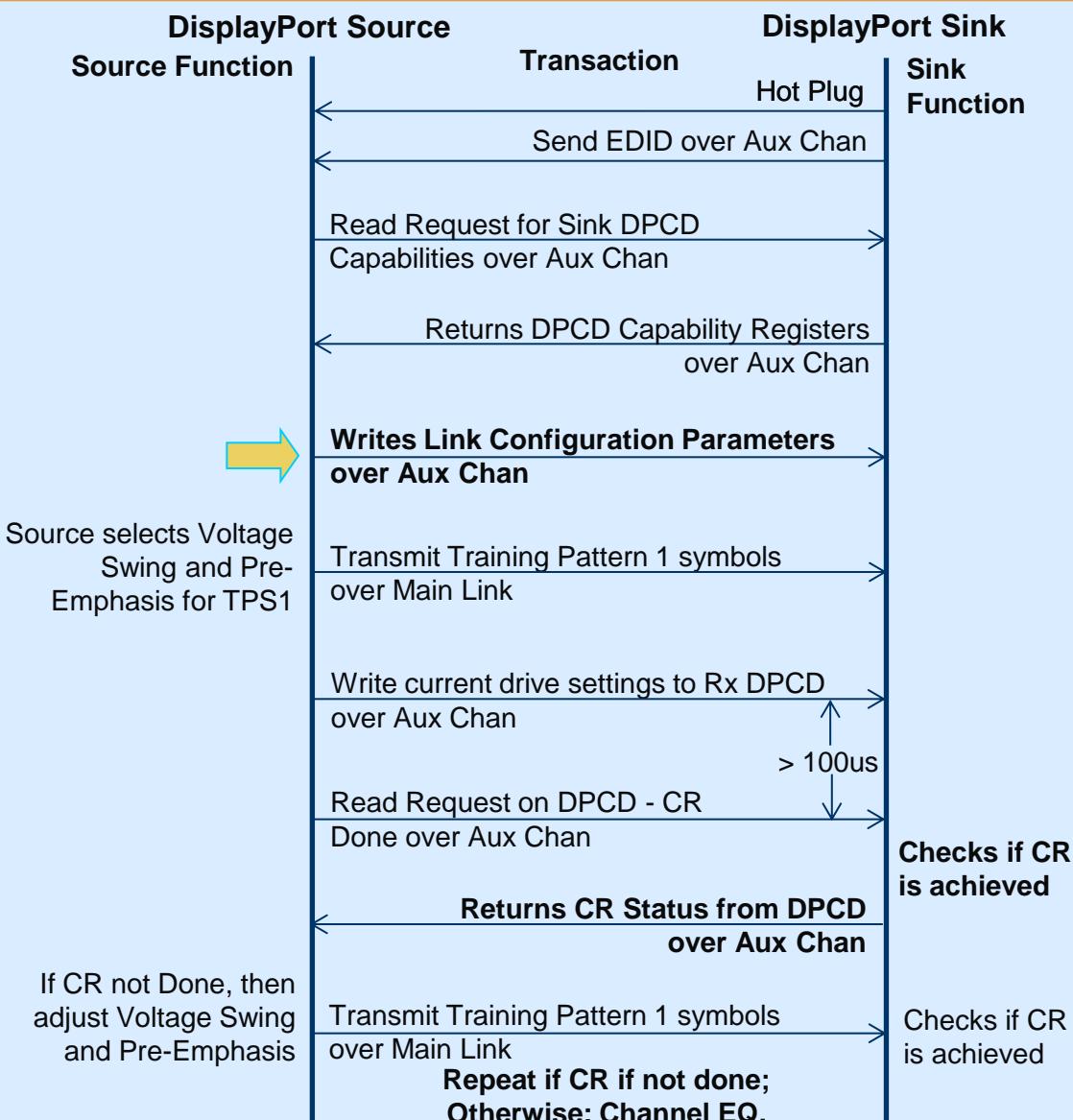


quantumdata



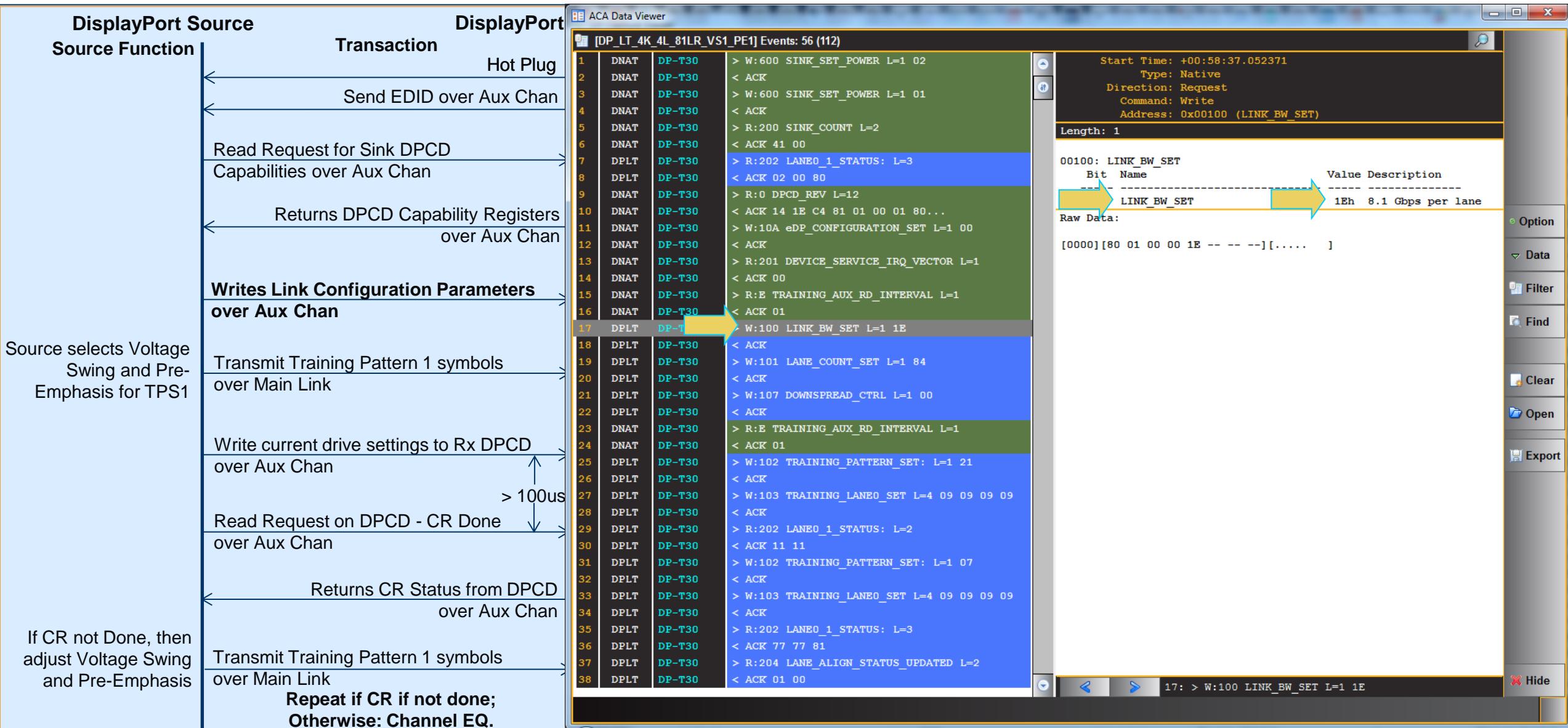
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Everywhereyoulook™

# Connection Sequence – Link Training Clock Recovery Sequence

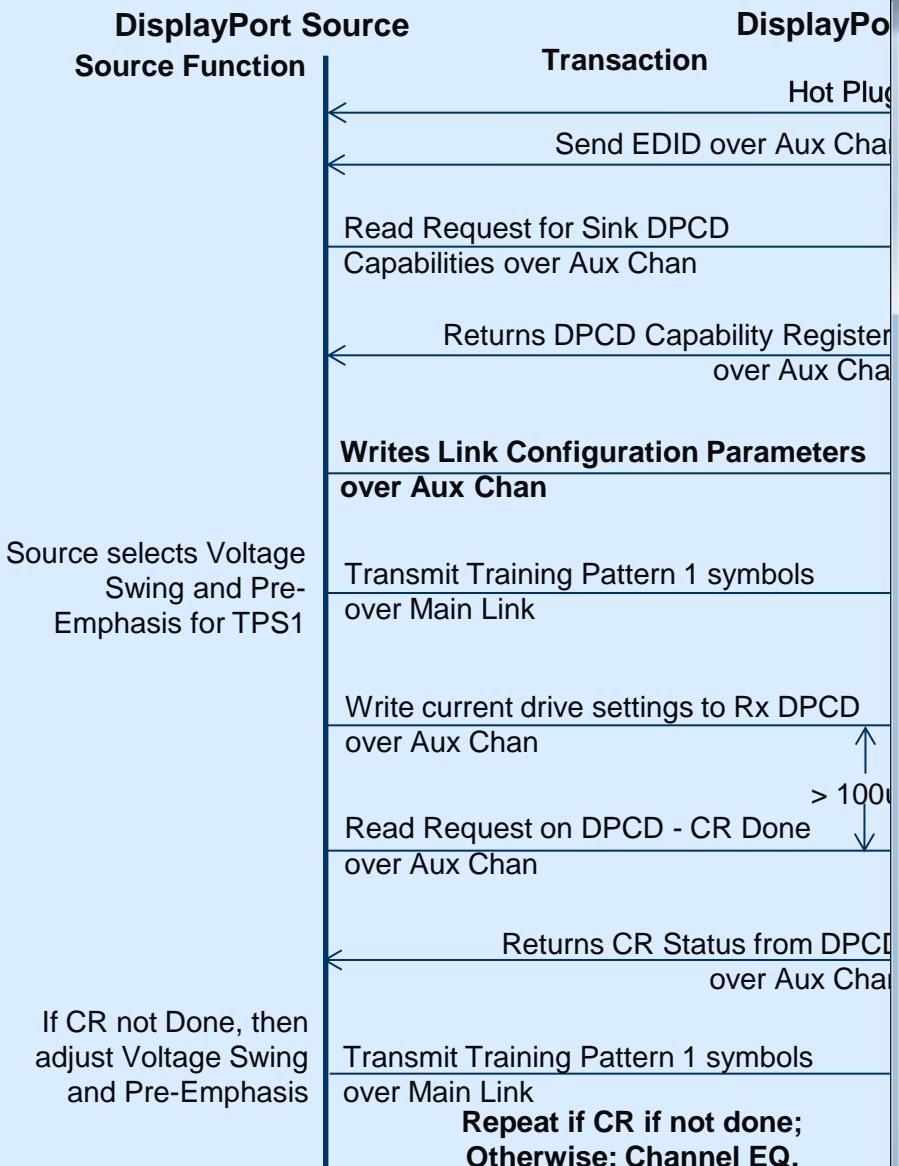


- ◆ Clock Recover needed because DisplayPort, like most high speed serial interfaces, **does not have a separate clock channel**—the clock is derived from the bit stream.
- ◆ Receiver needs a reference clock of its own at approximately the same frequency.
- ◆ Very difficult to have two clocks—one on the transmitter and one on the receiver—that have the same clock frequency.
- ◆ Receiver has to align its clock to the edge transitions of the incoming data stream using a PLL.
- ◆ An unscrambled **special sequence of bits** has to be used (“training sequence”) to optimize edge sampling for clock alignment.
- ◆ Clock recovery typically begins with the following settings:
  - Lowest drive levels, i.e. voltage swing and pre-emphasis (unless embedded applications).
  - Maximum Link Rate supported, typically HBR2 5.4Gb/s/lane or HBR3 at 8.1Gb/s/lane.
  - Maximum number of lanes supported, typically 2 or 4.

# Connection Sequence – Link Training Clock Recovery Sequence



# Connection Sequence – Link Training Clock Recovery Sequence



**ACA Data Viewer**

[DP\_LT\_4K\_4L\_81LR\_VS1\_P1] Events: 56 (112)

Start Time: +00:58:37.052516  
 Type: Native  
 Direction: Request  
 Command: Write  
 Address: 0x00101 (LANE\_COUNT\_SET)  
 Length: 1

00101: LANE\_COUNT\_SET

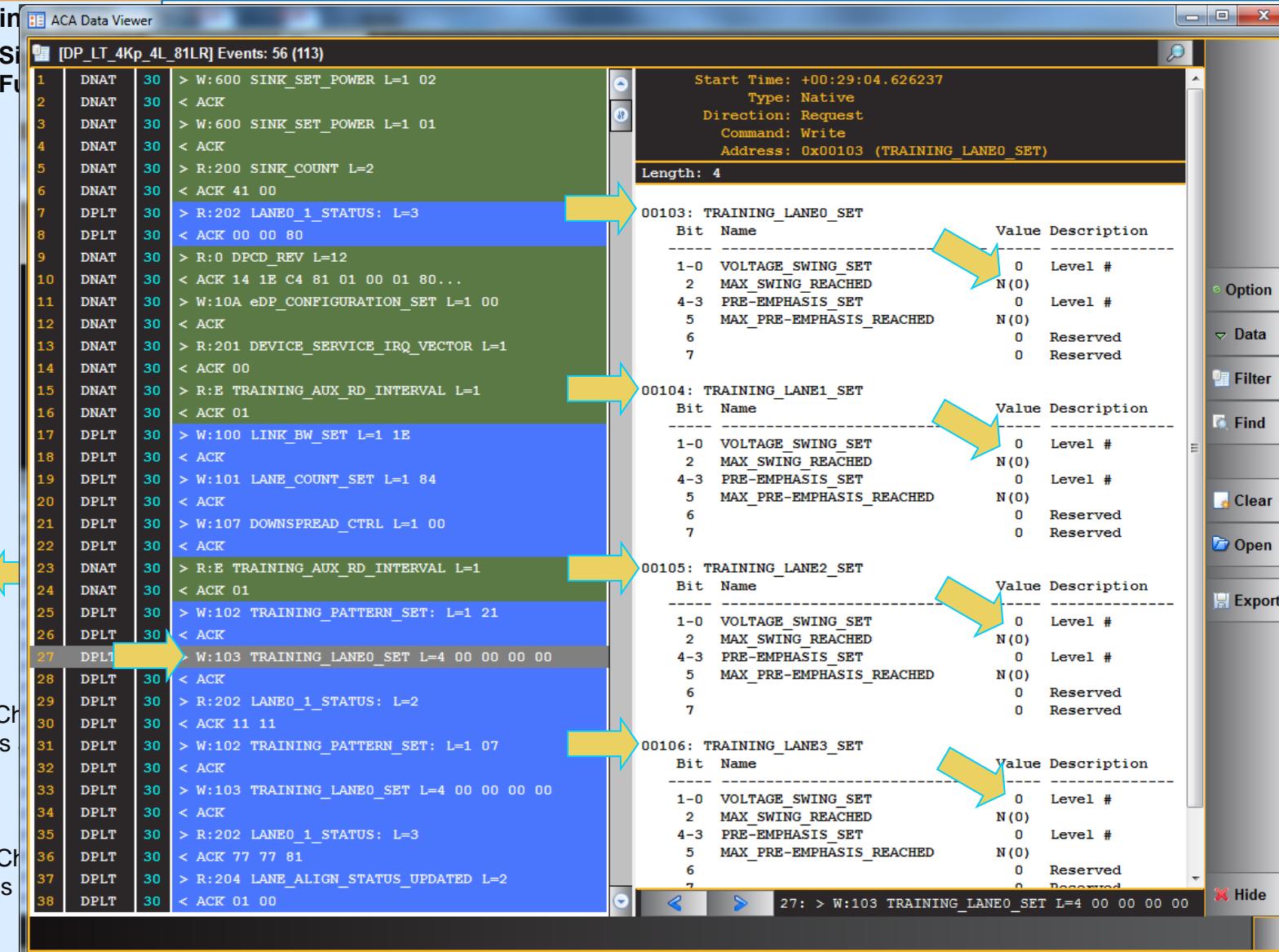
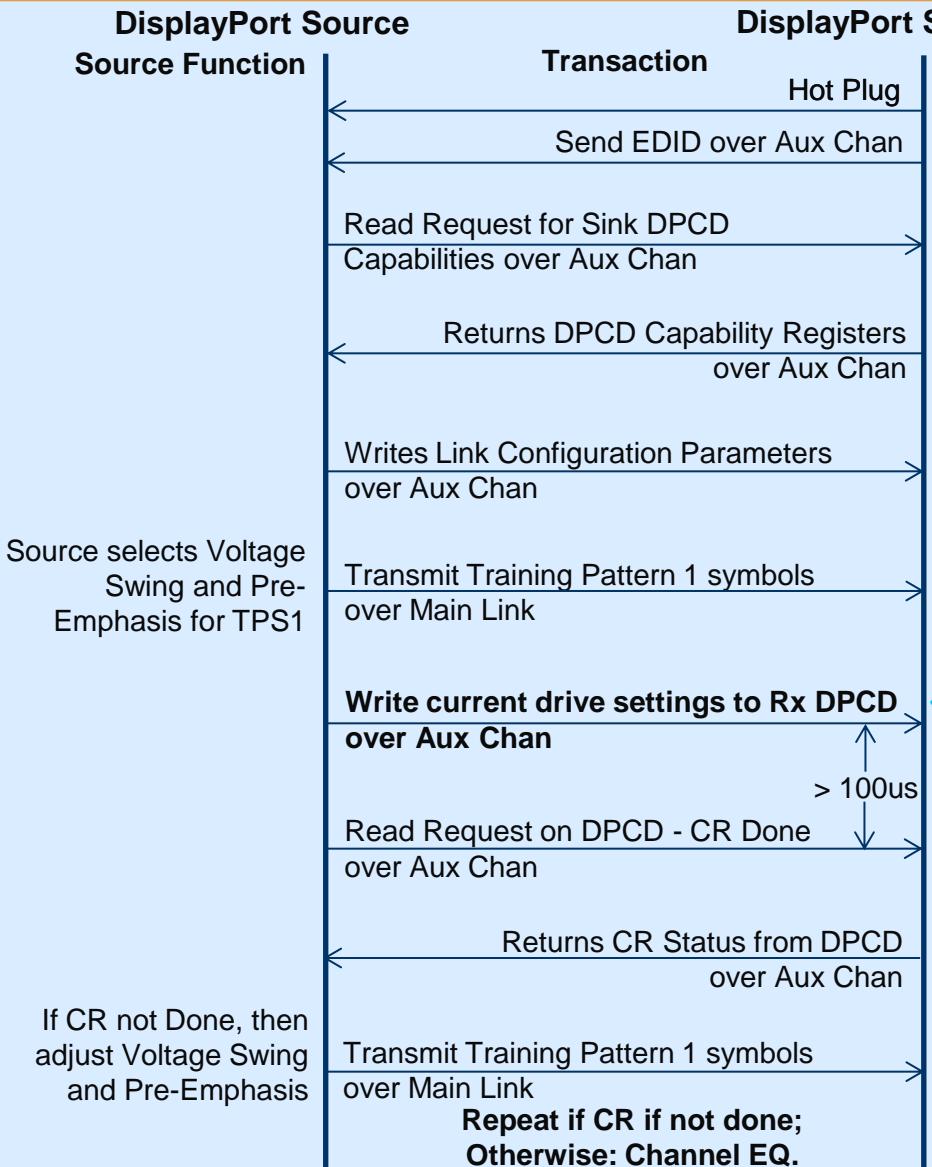
Bit	Name	Value Description
4-0	LANE_COUNT_SET	4 lanes
5	POST_LT_ADJ_REQ_GRANTED	N(0)
6		Reserved
7	ENHANCED_FRAME_CAP	Y(1)

Raw Data:

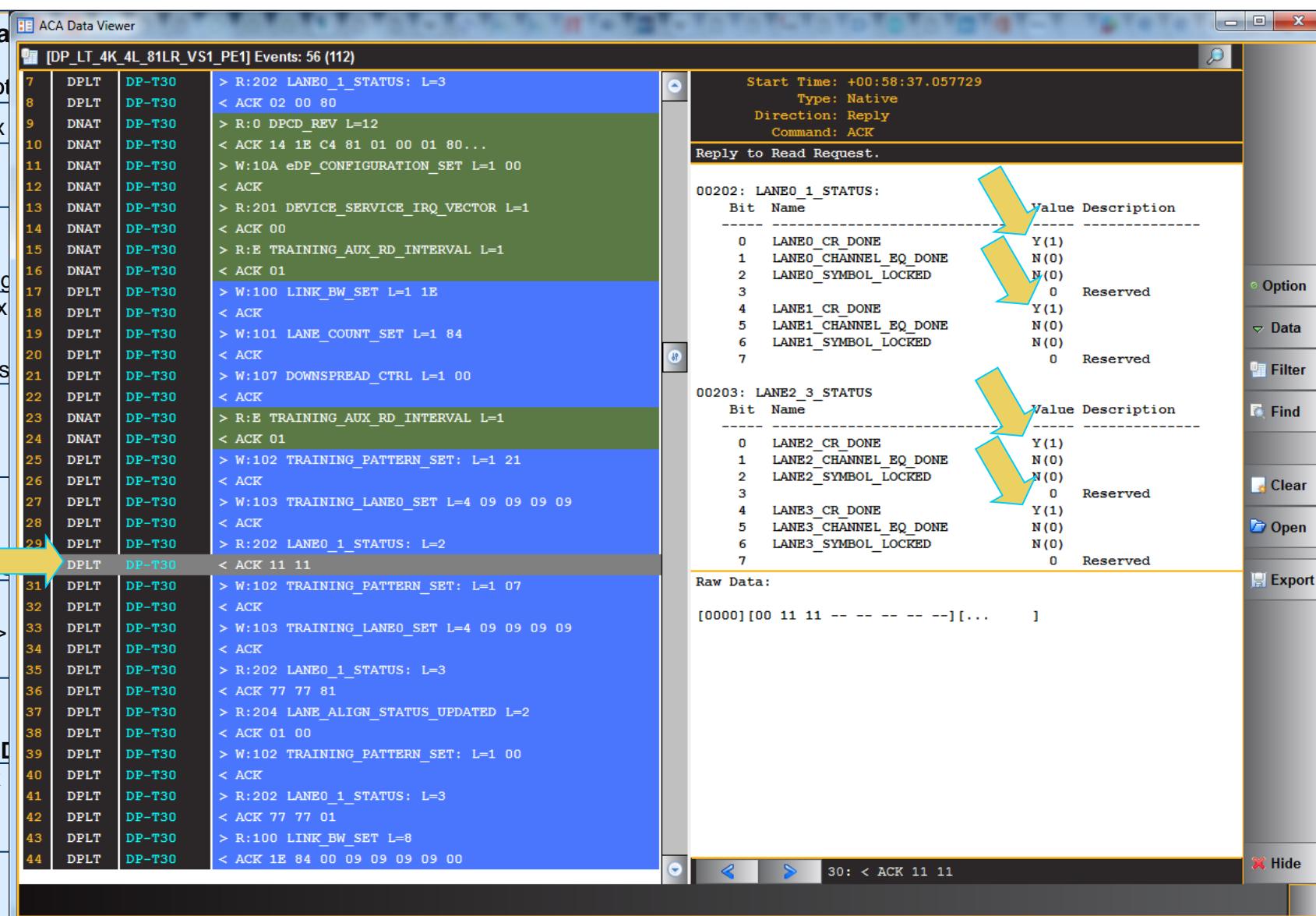
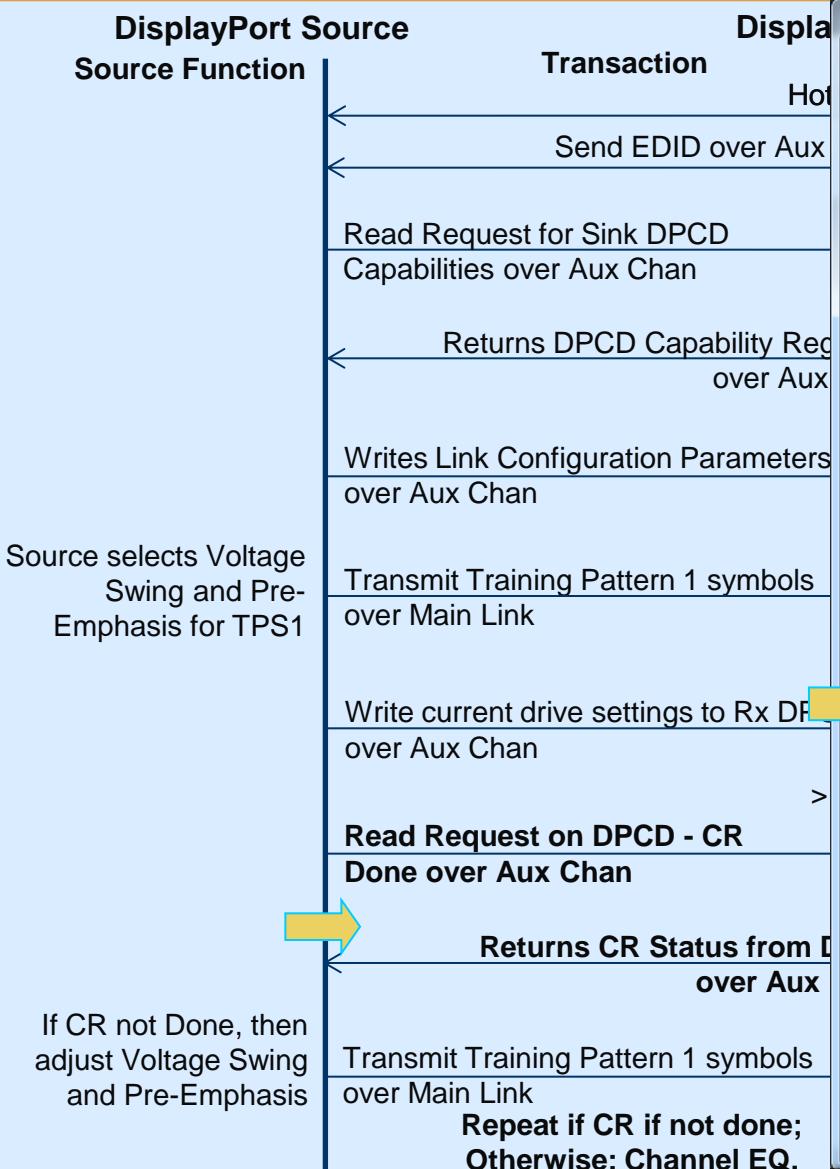
[0000][80 01 01 00 84 -- -- --][.....]

19: > W:101 LANE\_COUNT\_SET L=1 84

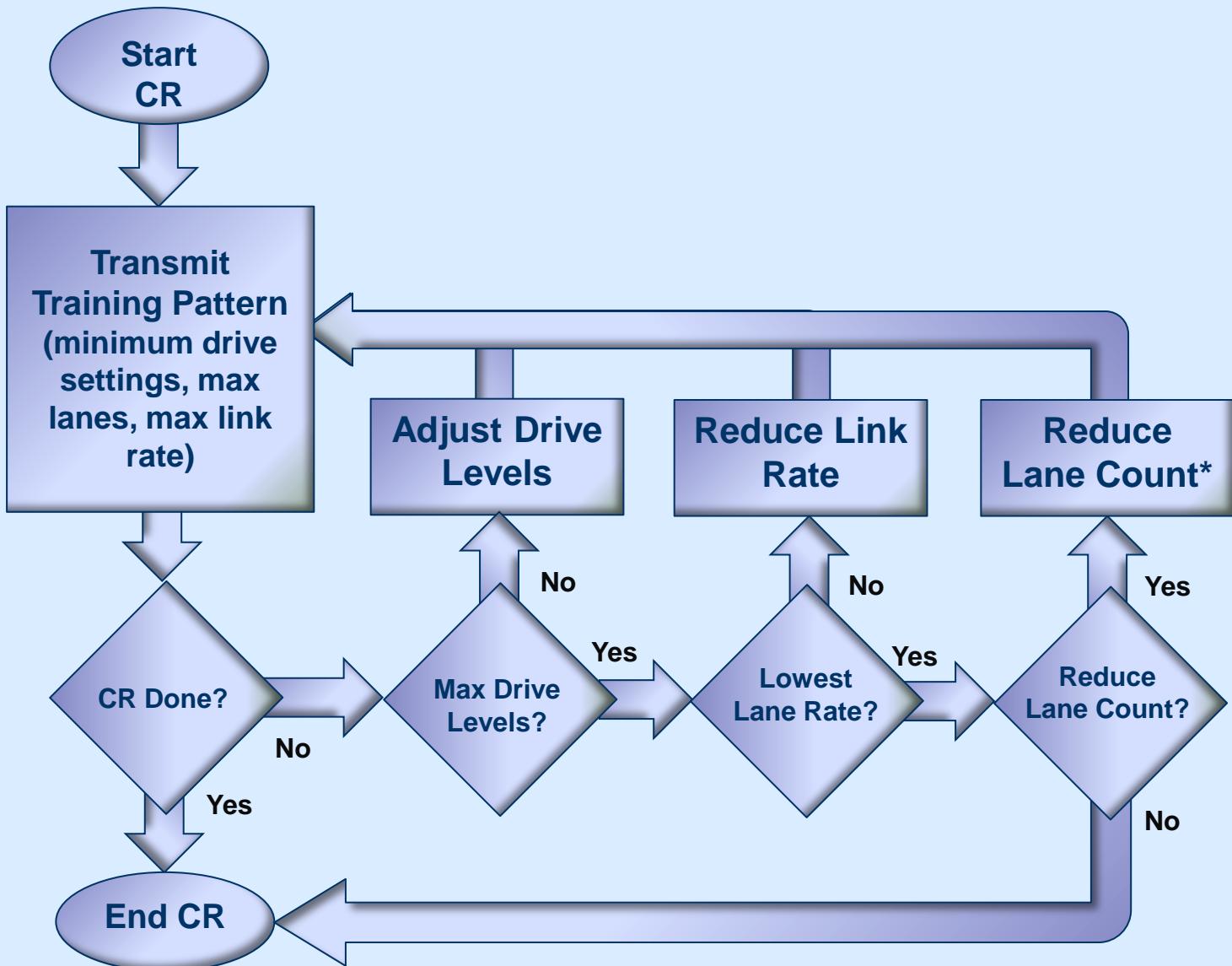
# Connection Sequence – Link Training Clock Recovery Sequence



# Connection Sequence – Link Training Clock Recovery Sequence

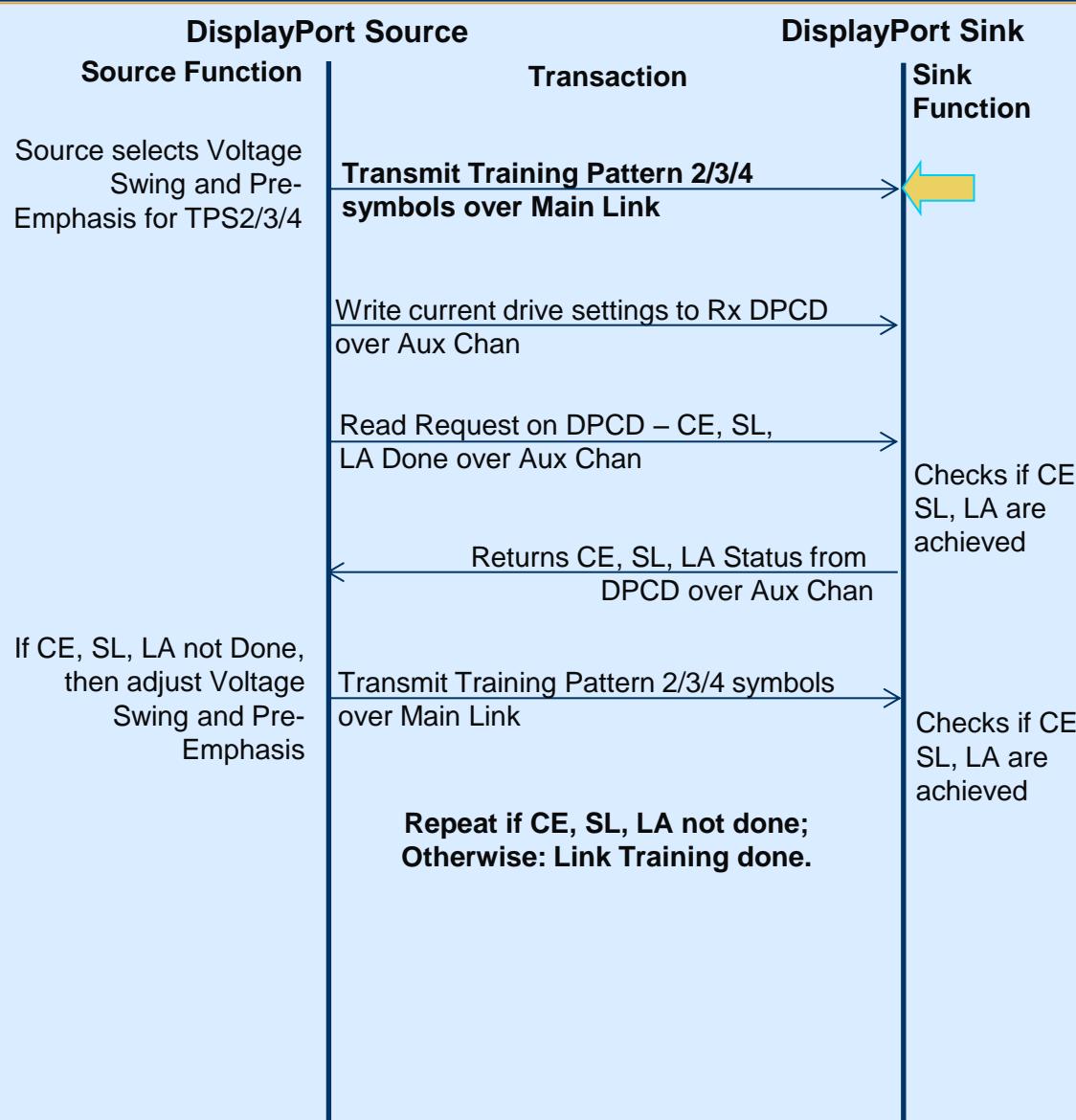


# Connection Sequence – Link Training Clock Recovery

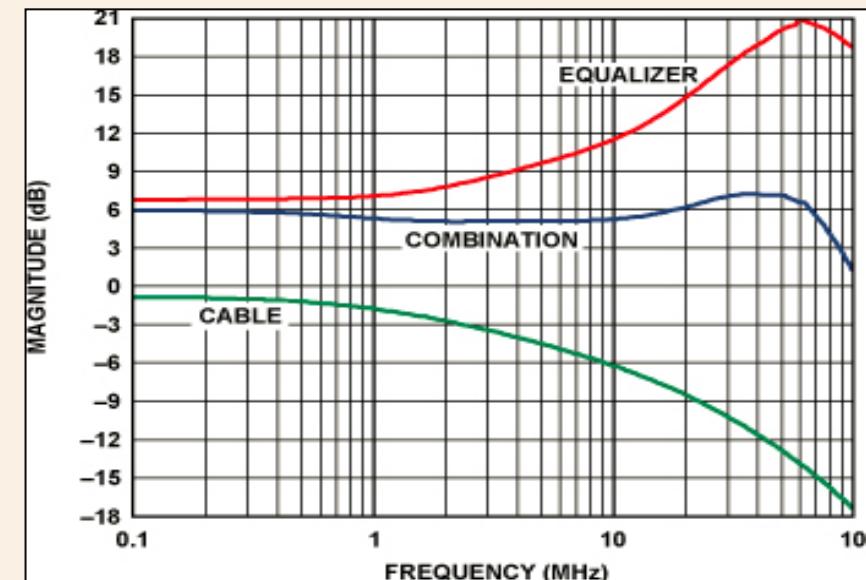


- ◆ Link Training Clock Recovery.
- ◆ There are 3 things that can be changed while still meeting the requirements of the video format being transmitted; listed in priority order:
  - Drive levels, i.e. voltage swing and pre-emphasis.
  - Link Rate, i.e. RBR at 1.62 Gb/s/lane through HBR3 at 8.1Gb/s/lane.
  - Number of lanes. **Lanes can be reduced if the Clock Recovery shows that the lower lanes were successfully locked.**

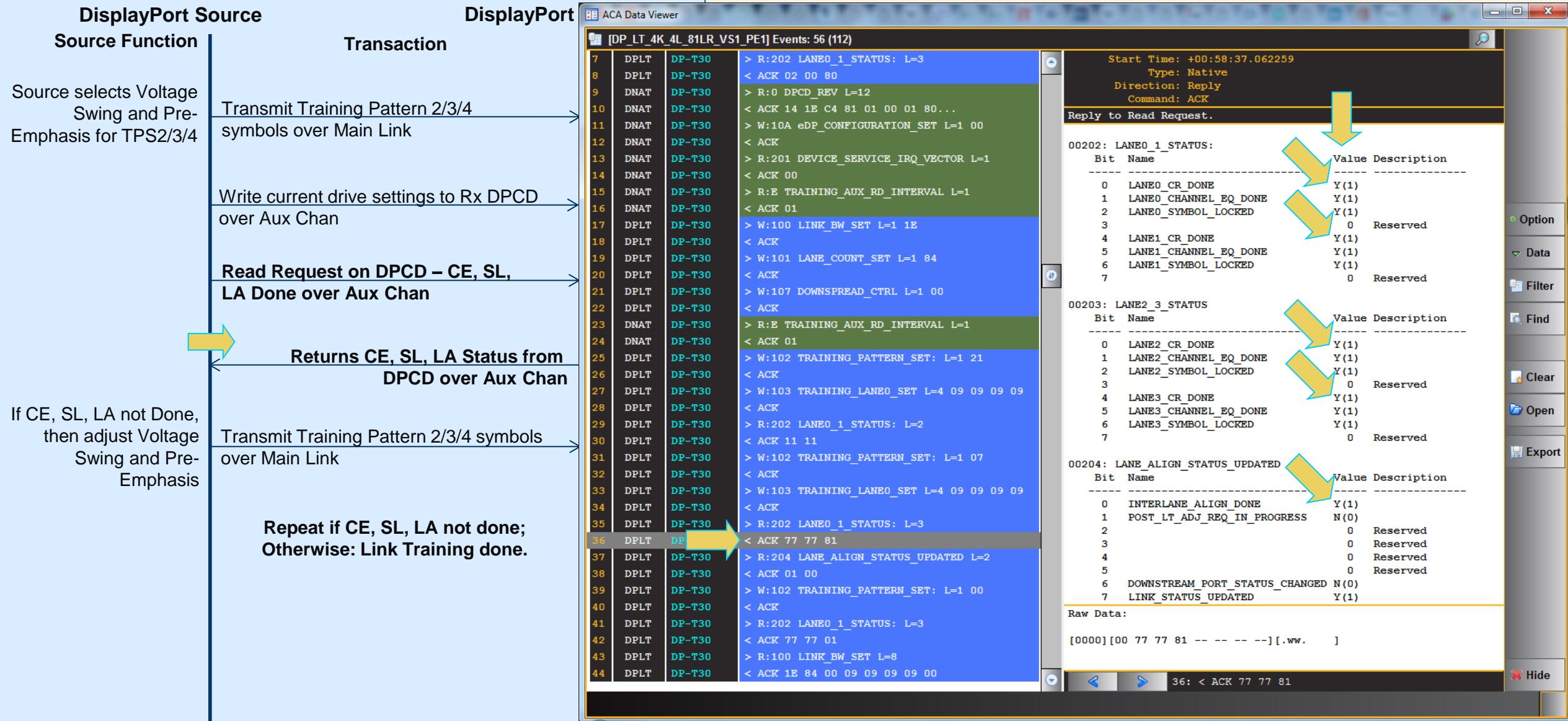
# Connection Sequence – Link Training Channel EQ, Symbol Lock, Interlane Alignment



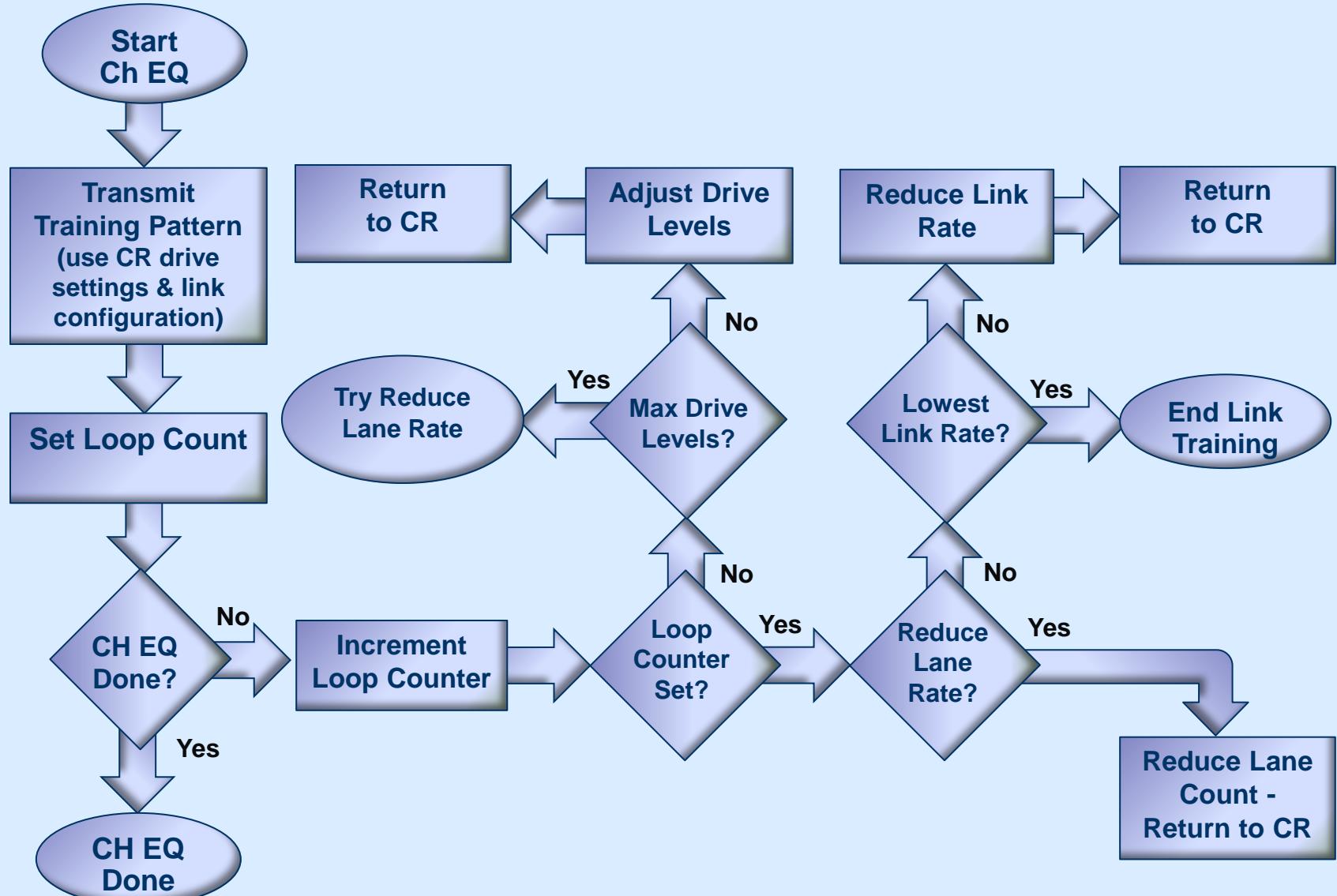
- ◆ **Symbol Lock and Equalization.**
  - Starts with **same link configuration and drive settings** used for Clock Recovery. But different Training Patterns.
  - Symbol Lock is achieved when the receiver has **identified and aligned on the 8b/10b symbol boundaries**.
  - Cable acts like a low pass filter attenuating the harmonics of the fundamental frequency and smearing out the bits resulting in inter-symbol interference.
  - Cable equalization is the process of **altering the frequency response of a video amplifier to compensate for high frequency losses in a cable**.



# Connection Sequence – Link Training Channel EQ, Symbol Lock, Interlane Alignment



# Connection Sequence – Channel EQ, Symbol Lock and Interlane Alignment



- ◆ There are 3 things that can be changed while still meeting the requirements of the video format being transmitted; listed in priority order:
  - Drive levels, i.e. voltage swing and pre-emphasis.
  - Link Rate, i.e. RBR at 1.62 Gb/s/lane through HBR3 at 8.1Gb/s/lane.
  - Number of lanes. Lanes can be reduced if the CR shows that the lower lanes were successfully locked.

# Source Link Layer Compliance – Test 4.3.1.1 Successful Link Training

Compliance Test Results Viewer

DP 1.4a Source (1.4 Core R1.0) Compliance Test Results

Results Name: AA\_Link\_Training\_Sample1  
Date Tested: April 23, 2018 11:25 AM  
Overall Status: CTS 1.4 Core R1.0 - Pass

Manufacturer: Model Name: Port Tested: 1

HTML Report

Test Results

Test Name / Details

4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds

Iter 01:

- 01: [1] Link Training test for lane count = 1 and lane rate = 1.62 Pass
- 02: [2] Link Training test for lane count = 2 and lane rate = 1.62 Pass
- 03: [3] Link Training test for lane count = 4 and lane rate = 1.62 Pass
- 04: [4] Link Training test for lane count = 1 and lane rate = 2.70 Pass
- 05: [5] Link Training test for lane count = 2 and lane rate = 2.70 Pass
- 06: [6] Link Training test for lane count = 4 and lane rate = 2.70 Pass
- 07: [7] Link Training test for lane count = 1 and lane rate = 5.40 Pass
- 08: [8] Link Training test for lane count = 2 and lane rate = 5.40 Pass
- 09: [9] Link Training test for lane count = 4 and lane rate = 5.40 Pass
- 10: [10] Link Training test for lane count = 1 and lane rate = 8.10 Pass
- 11: [11] Link Training test for lane count = 2 and lane rate = 8.10 Pass

Source DUT start link training.  
Source DUT sets link bandwidth and lane count before TP1 is set.  
Source DUT sets same link bandwidth for link rate under test.  
Source DUT sets correct lane count for lane count under test.  
Source DUT sets TP1 on all active lanes.  
Source DUT starts with voltage swing 0 on all active lanes.  
Source DUT starts with pre-emphasis 0 on all active lanes.  
CR Lock succeeded on all active lanes.  
Training pattern 2 or 3 or 4 detected after Training pattern 1.  
For HBR3 Source Training pattern 4 detected.  
Equalization succeeded on all active lanes.  
Symbol lock succeeded on all active lanes.  
All Lanes are Aligned and skewed.  
Link compliance training test completed successfully.

Link training completed in 21.50 ms, which exceeds the 10ms guideline.

- 12: [12] Link Training test for lane count = 4 and lane rate = 8.10 Pass

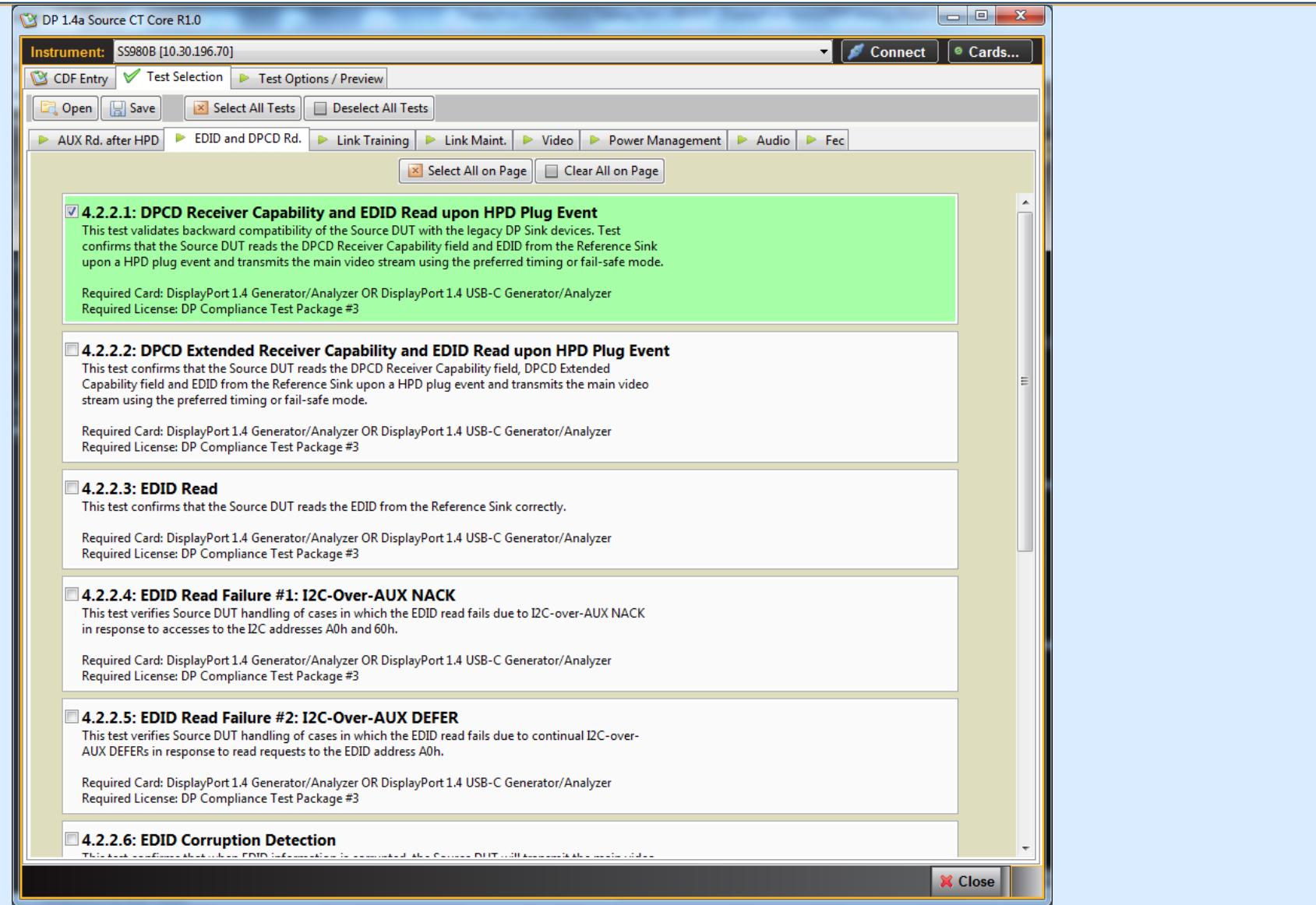
4.3.1.2: Successful Link Training Upon HPD Plug Event.  
4.3.1.3: Successful Link Training with Request of Higher Differential Voltage Swing during Clock Recovery Sequence.  
4.3.1.4: Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing.

Open ACA Data Iter 01: Continue Test Execution Close

Instrument: SS980B [10.30.196.70]

- Example shows sample test results.
- Test run at various lane configurations.
- Shows details of subtest 12 for link training at 8.1 Gb/s link rate on four (4) lanes.
- Warning shown.

# Source Link Layer Compliance – Test Selection - Test 4.2.2.1 DPCD Receiver Cap. & EDID Read



- Select the desired test(s)

## Source Link Layer Compliance – Test 4.2.2.1 DPCD Receiver Capability & EDID Read

DP 1.4a Source (1.4 Core R1.0) Compliance Test Results		HTML Report
Results Name: AA_DP_Source_LL_Compliance2 Date Tested: May 4, 2018 2:55 PM Overall Status: CTS 1.4 Core R1.0 - Canceled		Manufacturer: ACME Model Name: XYZ Port Tested: 1
Test Results		
▶ Test Name / Details		Status
4.2.1.1: Source DUT Retry on No-Reply During AUX Read after HPD Plug Event	Iter 01:	Pass
▶ 01: Within 1ms, time between 2 AUX requests is at least 400us		Pass
▶ 02: After 1ms, time between 2 AUX requests is at least 400us		Pass
4.2.1.2: Source Retry on Invalid Reply During AUX Read after HPD Plug Event	Iter 01:	Pass
▶ 01: After invalid reply, time between 2 AUX requests is at least 400us		Pass
4.2.1.3: Source Device HPD Event Pulse Length Test	Iter 01:	Pass
▶ 01: Source DUT begins link training within 5 sec. after HPD assert		Pass
▶ 02: Source DUT should complete link training		Pass
4.2.1.4: Source Device IRQ HPD Pulse Length Test	Iter 01:	Pass
▶ 01: Source DUT reads IRQ VECTOR when IRQ HPD in the range of 510 usec to 520 usec		Pass
▶ 02: Source DUT reads IRQ VECTOR when IRQ HPD in the range of 980 usec to 990 usec		Pass
▶ 03: Source DUT does NOT read IRQ VECTOR when IRQ HPD in the range of 230 usec to 240 usec		Pass
4.2.1.5: Source Device Inactive HPD / Inactive AUX Test	Iter 01:	Pass
▶ 01: Source DUT begins link training within 5 sec after HPD		Pass
▶ 02: Source DUT NOT attempt AUX transactions while HPD is low		Pass
4.2.2.1: DPCD Receiver Capability and EDID Read upon HPD Plug Event	Iter 01:	Fail
▶ 01: Verify information after test 1a		Fail
● Reference sink config DPCD_REV(0h)=11,MAX_LINK_RATE(1h)=06h,TPS3_SUPPORTED = 0,TPS4_SUPPORTED = 0, ExtCap not supported		Fail
● Source DUT read the DPCD Receiver Capability field (DPCD: 00000h:0000Fh) through AUX CH before link training.		Fail
● Source DUT failed to read the entire EDID block through AUX CH before transmission of the video stream.		Fail
● Source DUT performs link training to its maximum capability.		Fail
● Source DUT transmits video stream using preferred timing 720x480p		Fail
▶ 02: Verify information after test 1b		Fail
▶ 03: Verify information after test 1c		Fail
▶ 04: Verify information after test 1d		Fail
▶ Open ACA Data		
Instrument: SS980B [10.30.196.70]	Continue Test Execution	Close

- ◆ Example shows sample test results.
  - ◆ This test validates backward compatibility of the Source DUT with the legacy DP Sink devices.

# Sink Link Layer Compliance Tests

DP 1.4 Reference Source  
Example: Teledyne LeCroy  
quantumdata 980 Test Platform  
with DP 1.4 Video Generator /  
Protocol Analyzer



DisplayPort Cable

DisplayPort Sink (Monitor/TV - DUT)



# Sink Link Layer Compliance Tests

The image shows two identical software windows side-by-side, both titled "DP 1.4a Sink CT Core R1.0". Each window has a toolbar at the top with "Instrument: SS980B [10.30.196.70]", "Connect", and "Cards..." buttons. Below the toolbar are tabs: "CDF Entry" (selected), "Test Selection" (highlighted with a green checkmark), and "Test Options / Preview". The main area is a "Test List" grid with columns for "Category / Test Name" and "Status" (indicated by a green checkmark). The left window displays the "AUX Ch. Proto." category, which includes tests 5.2.1.1 through 5.2.1.6. The right window displays the "Main Video" category, which includes tests 5.4.1.1 through 5.4.4.6.

**DP 1.4a Sink CT Core R1.0**

Instrument: SS980B [10.30.196.70]

CDF Entry  Test Selection  Test Options / Preview

Test List

Category / Test Name	Status
AUX Ch. Proto.	✓
5.2.1.1: Read One Byte from Valid DPCD Address	✓
5.2.1.2: DPCD Receiver Capability Read (Read 12 Bytes from Valid DPCD Address)	✓
5.2.1.3: Write One Byte to Valid DPCD Address	✓
5.2.1.4: Write Nine Bytes to Valid DPCD Addresses	✓
5.2.1.5: Write EDID Offset (One Byte I2C-Over-AUX Write)	✓
5.2.1.6: Read One EDID Byte (One Byte I2C-Over-AUX Read)	✓

**DP 1.4a Sink CT Core R1.0**

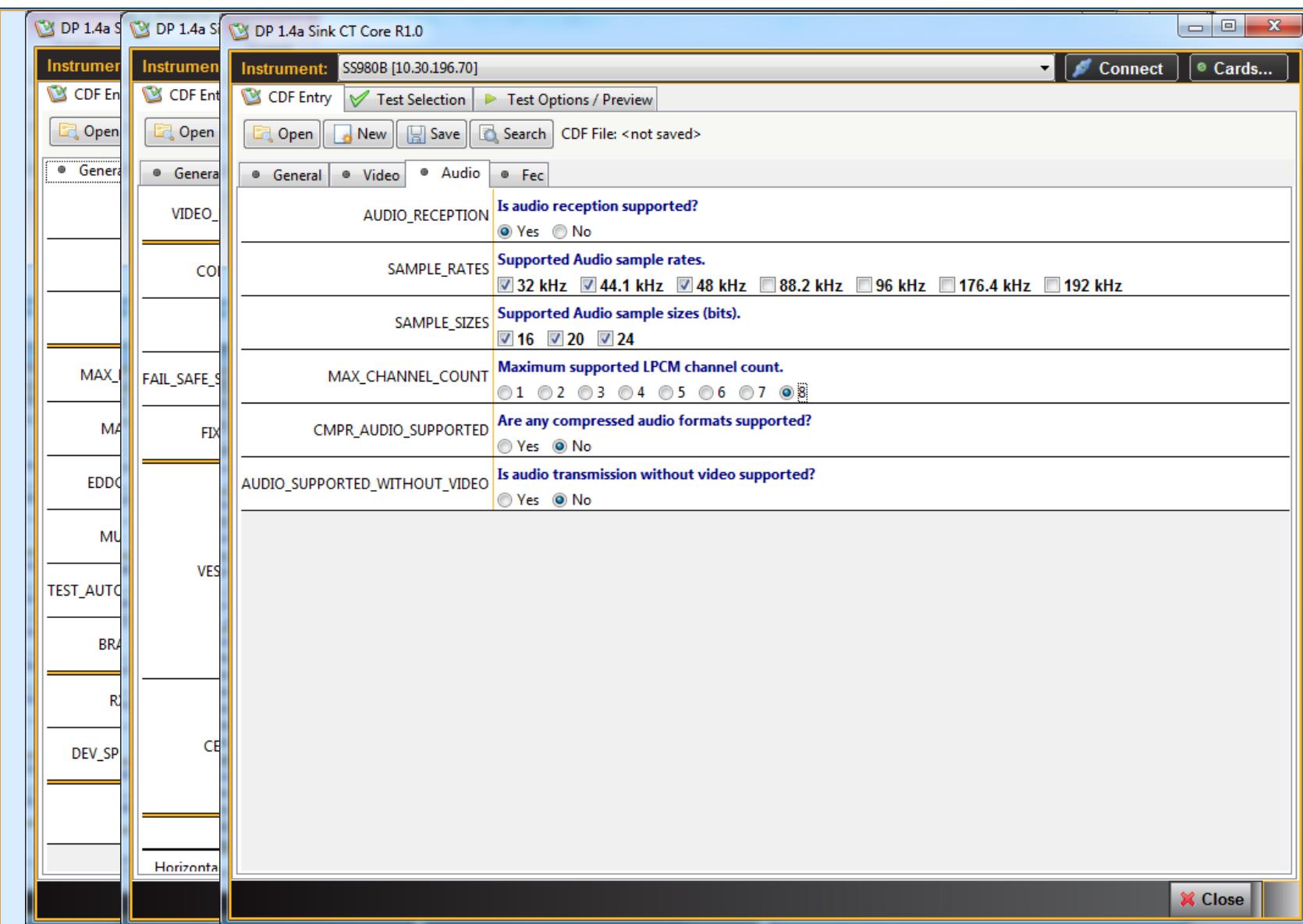
Instrument: SS980B [10.30.196.70]

CDF Entry  Test Selection  Test Options / Preview

Test List

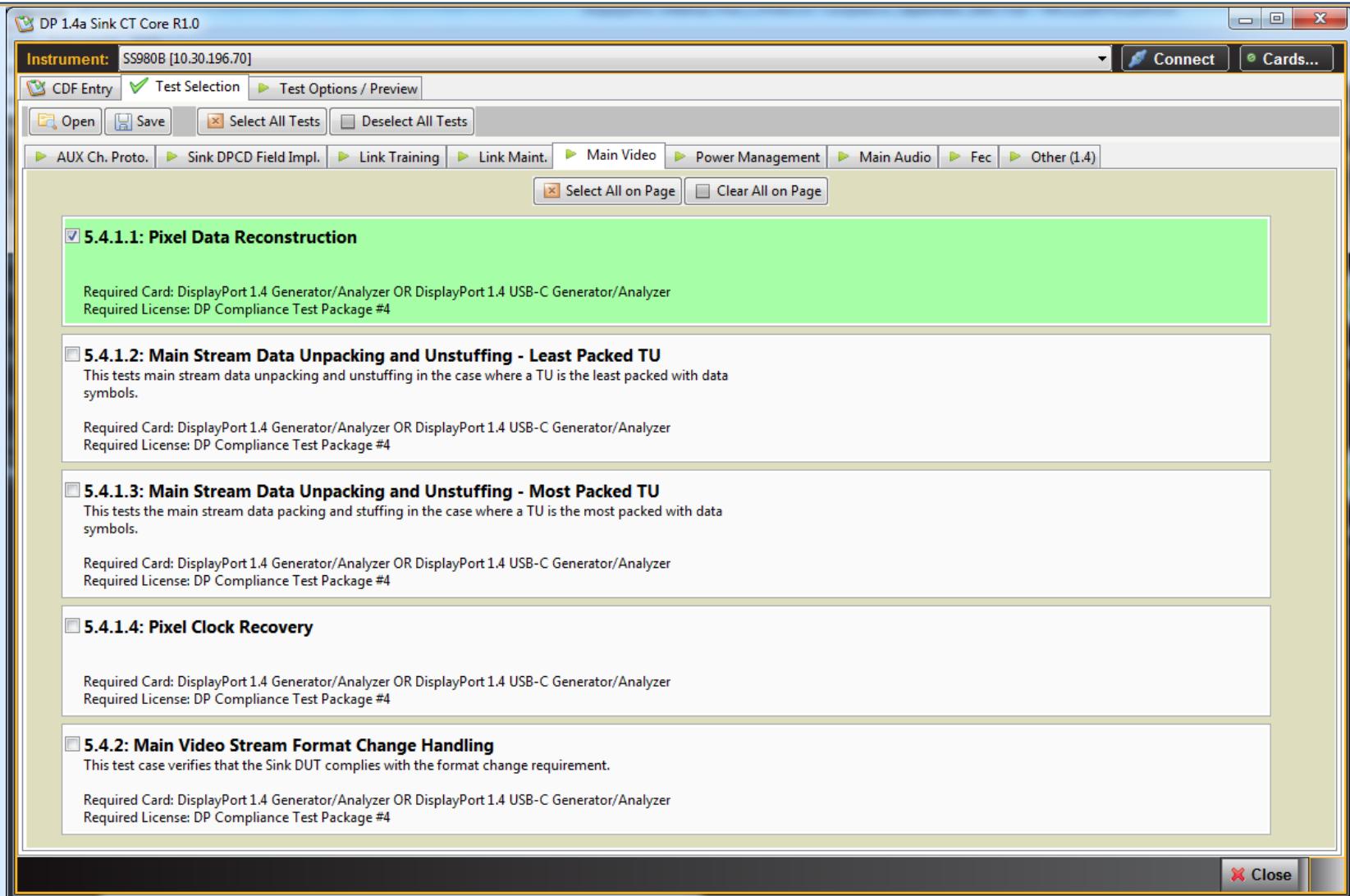
Category / Test Name	Status
Link Maint.	✓
5.3.2.1: IRQ HPD Pulse Due to Loss of Symbol Lock and Clock Recovery Lock.	✓
5.3.2.2: IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock	✓
Main Video	✓
5.4.1.1: Pixel Data Reconstruction	✓
5.4.1.2: Main Stream Data Unpacking and Unstuffing - Least Packed TU	✓
5.4.1.3: Main Stream Data Unpacking and Unstuffing - Most Packed TU	✓
5.4.1.4: Pixel Clock Recovery	✓
5.4.2: Main Video Stream Format Change Handling	✓
Power Management	✓
5.4.3.1: Entering and Exiting Power Save Mode	✓
5.4.3.2: Resumption of Main Link Activity After Extended Idle	✓
Main Audio	✓
5.4.4.2: Audio Startup and Format Change	✓
5.4.4.3: RS Error Correction	✓
5.4.4.4: Audio InfoFrame Packet	✓
5.4.4.5: Audio Clock Recovery	✓
5.4.4.6: Audio Stream Reception	✓
FEC	

# Entering the CDF Information – Sink Link Layer Capabilities



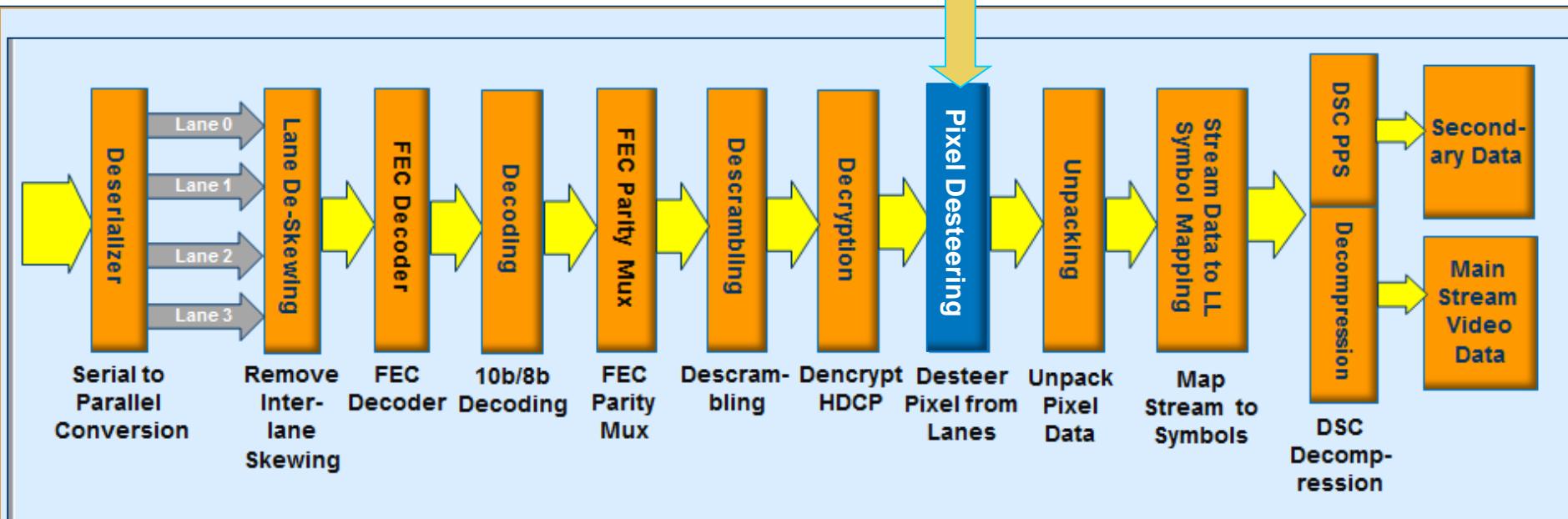
- ◆ Capabilities Declaration Form (CDF) must be filled out prior to the running the test.
- ◆ CDF is used by the reference sink to know which Link Layer related sink features to test.
- ◆ Video Tab – Described video capabilities of the sink device.
- ◆ Audio Tab – Described audio capabilities of the sink device.

# Sink Link Layer Compliance – Test 5.4.1.1 Pixel Data Reconstruction



- ◆ Select the desired test.

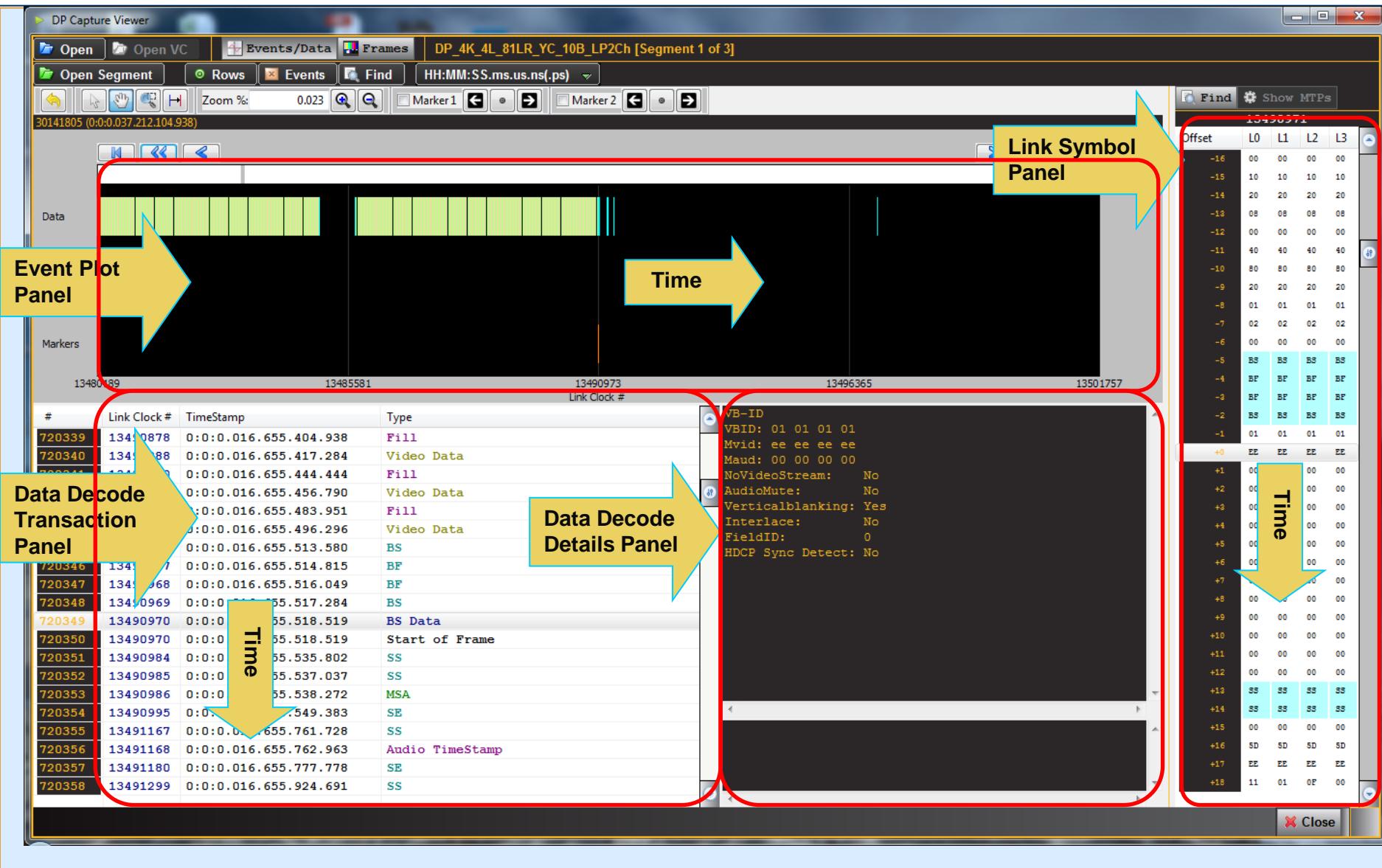
# DisplayPort Main Link Stream Generation – Desteering



- ◆ Two types of link symbols:
  - **Data symbols** (e.g. pixel, metadata)
  - **Control symbols** (K-Chars) to frame the data symbols.
- ◆ Pixel Steering/Desterring – The process of mapping the pixel data to each of the 2 or 4 lanes.

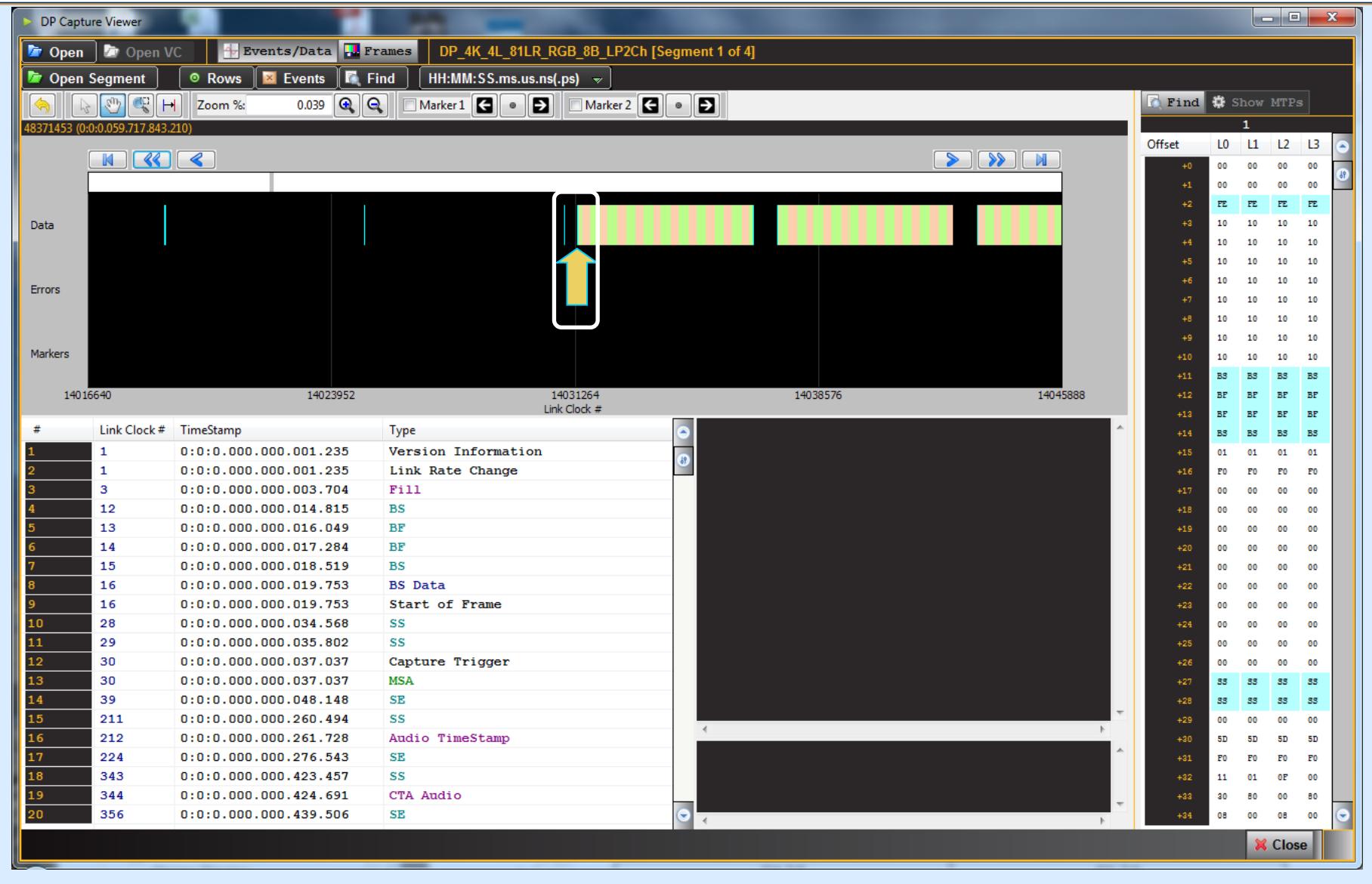


# DisplayPort Protocol Analyzer



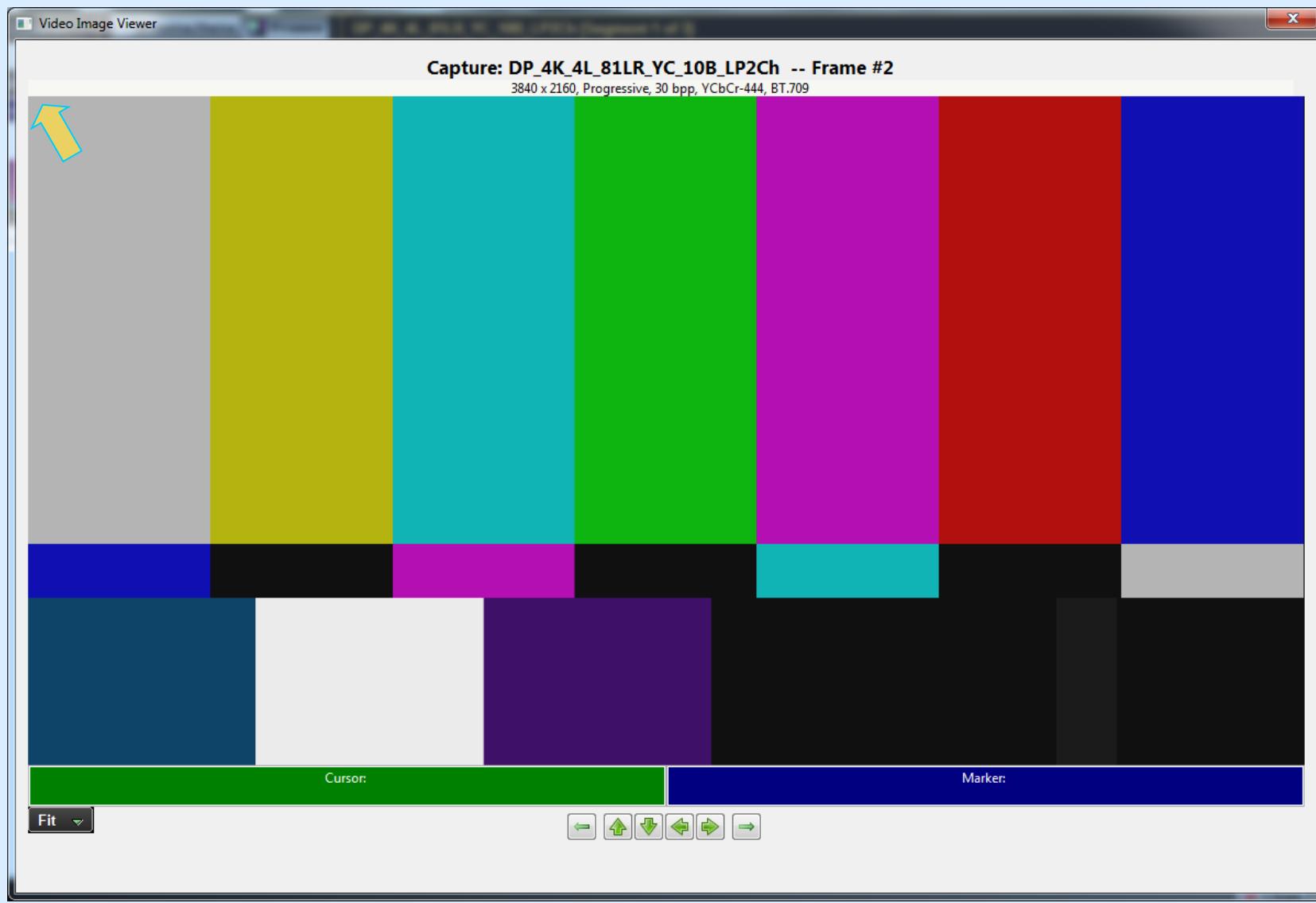
- ◆ DisplayPort Capture Viewer.
- ◆ Three Panels:
  - ◆ Event Plot (GUI)
  - ◆ Data Decode (Table) with Details subpanel.
  - ◆ Link Symbol panel. Shows raw 8 bit hex for all for lanes.
- ◆ All Panels are in sync.

# DisplayPort Main Link Protocol – Pixel Desteering (8 bit)



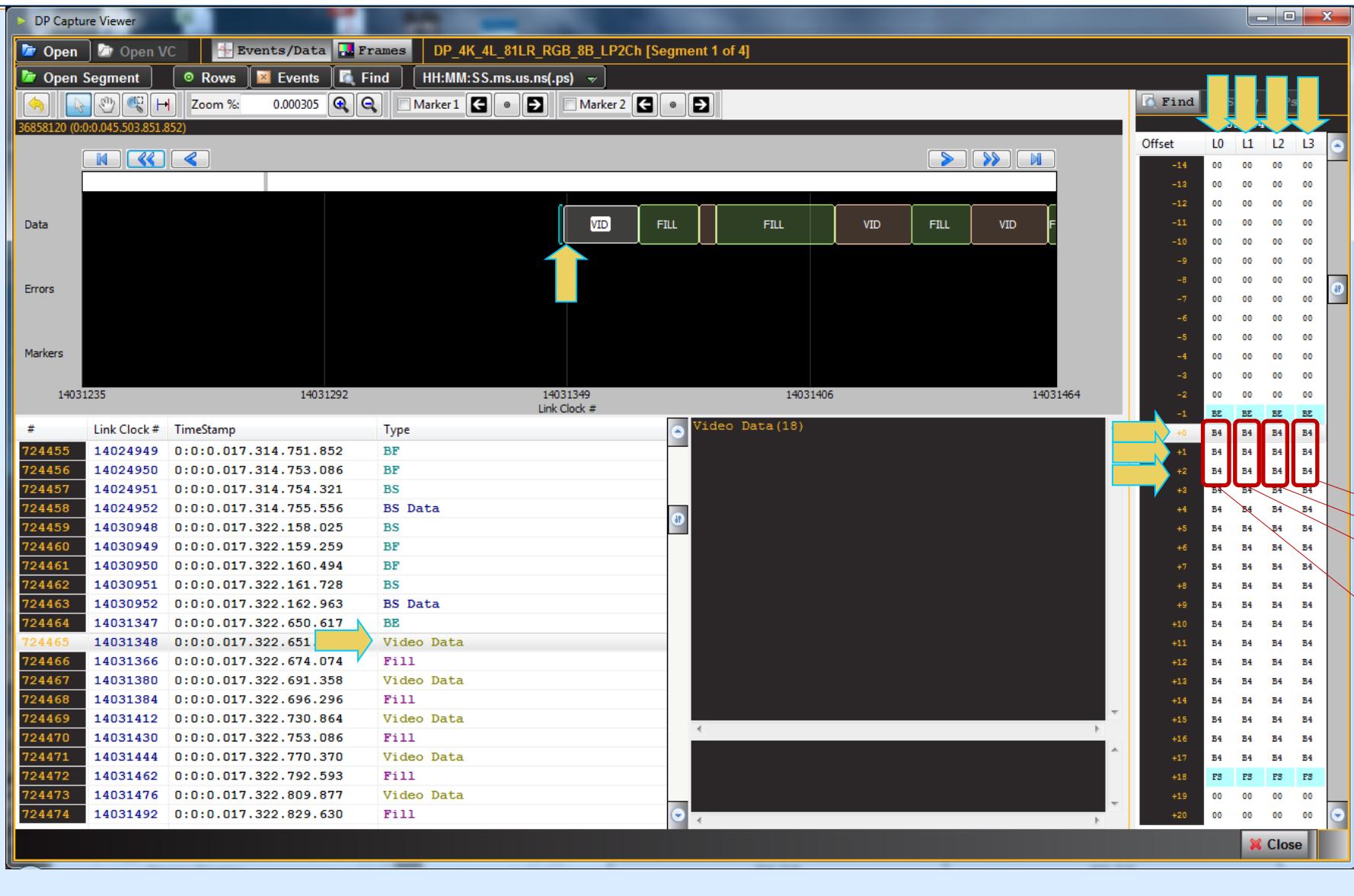
- ◆ Looking at the first pixel of a frame on a 4K video resolution with a link rate of 8.1Gb/s using four lanes using a color depth of 8 bits per component.

# DisplayPort Main Link Protocol – Pixel Desteering



- ◆ Pixels data values are mapped “steered” on the lanes that are used.
- ◆ The video frame is a test pattern SMPTEbar.
- ◆ We will look at the first pixel of the video frame.

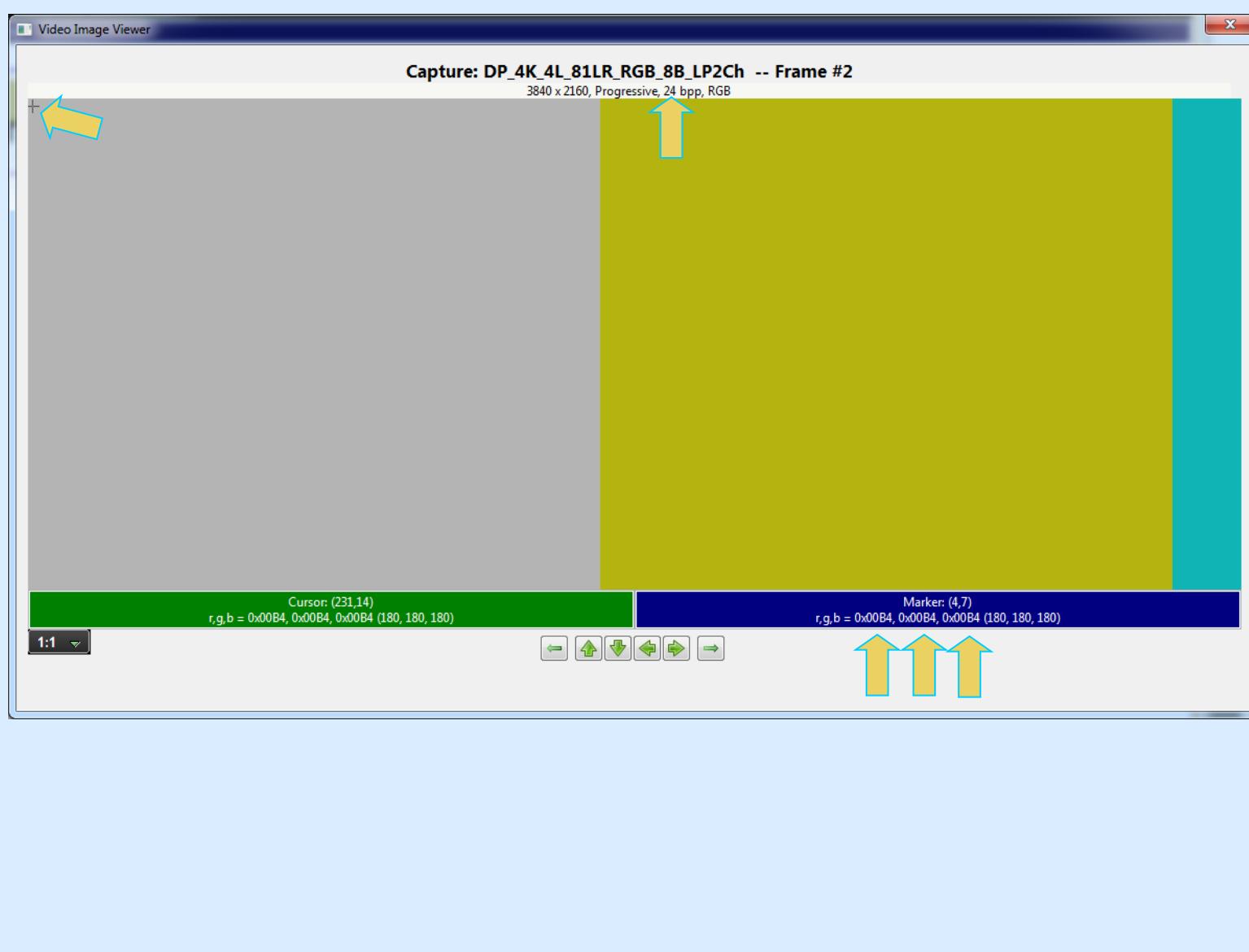
# DisplayPort Main Link Protocol – Pixel Desteering (8 bit)



- ◆ Looking at the first video transfer unit in a frame.
- ◆ Notice that the RGB values are uniform across the lanes with a pixel value of B4 representing the color of the first set of pixels in the frame:
- ◆ Example: Pixel 0 is all in Lane 0.

Lane0	Lane1	Lane2	Lane3
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-7:0	B1-7:0	B2-7:0	B3-7:0
Lane0	Lane1	Lane2	Lane3
R0-B4	R1-B4	R2-B4	R3-B4
G0-B4	G1-B4	G2-B4	G3-B4
B0-B4	B1-B4	B2-B4	B3-B4

# DisplayPort Main Link Protocol – Pixel Desteering (8 bit)



- ◆ Looking at the first video transfer unit in a frame.
- ◆ Notice that the RGB values are uniform across the lanes with a pixel value of B4 representing the color of the first set of pixels in the frame:

Lane0	Lane1	Lane2	Lane3
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R0-B4	R1-B4	R2-B4	R3-B4
G0-B4	G1-B4	G2-B4	G3-B4
B0-B4	B1-B4	B2-B4	B3-B4

B	4						
1011	0100	1011	0100	1011	0100	1011	0100
B	4						
1011	0100	1011	0100	1011	0100	1011	0100
B	4						
1011	0100	1011	0100	1011	0100	1011	0100

# Sink Link Layer Compliance – Test 5.4.1.1 Pixel Data Reconstruction

Compliance Test Results Viewer

DP 1.4 Sink (1.4 Core R1.0) Compliance Test Results

Results Name: 03\_27\_2018\_16\_07\_26\_sink  
Date Tested: March 27, 2018 4:07 PM  
Overall Status: CTS 1.4 Core R1.0 - Pass

Manufacturer:  
Model Name:  
Port Tested: 1

HTML Report

Test Results

Test Name / Details	Status
5.4.1.1: Pixel Data Reconstruction	Pass
Iter 01:	Pass
01: Link Training at lane count = 1 and low lane rate	Pass
02: Test validation when lane count = 1 and 6 bpc	Pass
03: Test validation when lane count = 1 and 8 bpc	Pass
04: Test validation when lane count = 1 and 10 bpc	Pass
05: Test validation when lane count = 1 and 12 bpc	Pass
06: Test validation when lane count = 1 and 16 bpc	Pass
07: Link Training at lane count = 2 and low lane rate	Pass
08: Test validation when lane count = 2 and 6 bpc	Pass
09: Test validation when lane count = 2 and 8 bpc	Pass
10: Test validation when lane count = 2 and 10 bpc	Pass
11: Test validation when lane count = 2 and 12 bpc	Pass
12: Test validation when lane count = 2 and 16 bpc	Pass
13: Link Training at lane count = 4 and low lane rate	Pass
14: Test validation when lane count = 4 and 6 bpc	Pass
15: Test validation when lane count = 4 and 8 bpc	Pass
• TEST_CRC_R_Cr field equals to the Reference Source's internal CRC calculations (0xF58C).	
• TEST_CRC_G_Y field equals to the Reference Source's internal CRC calculations (0xA3D3).	
• TEST_CRC_B_Cb field equals to the Reference Source's internal CRC calculations (0x0720).	
16: Test validation when lane count = 4 and 10 bpc	Pass
17: Test validation when lane count = 4 and 12 bpc	Pass
18: Test validation when lane count = 4 and 16 bpc	Pass
5.4.1.2: Main Stream Data Unpacking and Unstuffing - Least Packed TU	Pass
Iter 01:	Pass
01: Initial Link Training at maximum link rate and lane count success	Pass
• HPD is asserted	
• Reference Source receives AUX_ACK at 1 attempts	
• Reference Source receives AUX ACK from either write request	

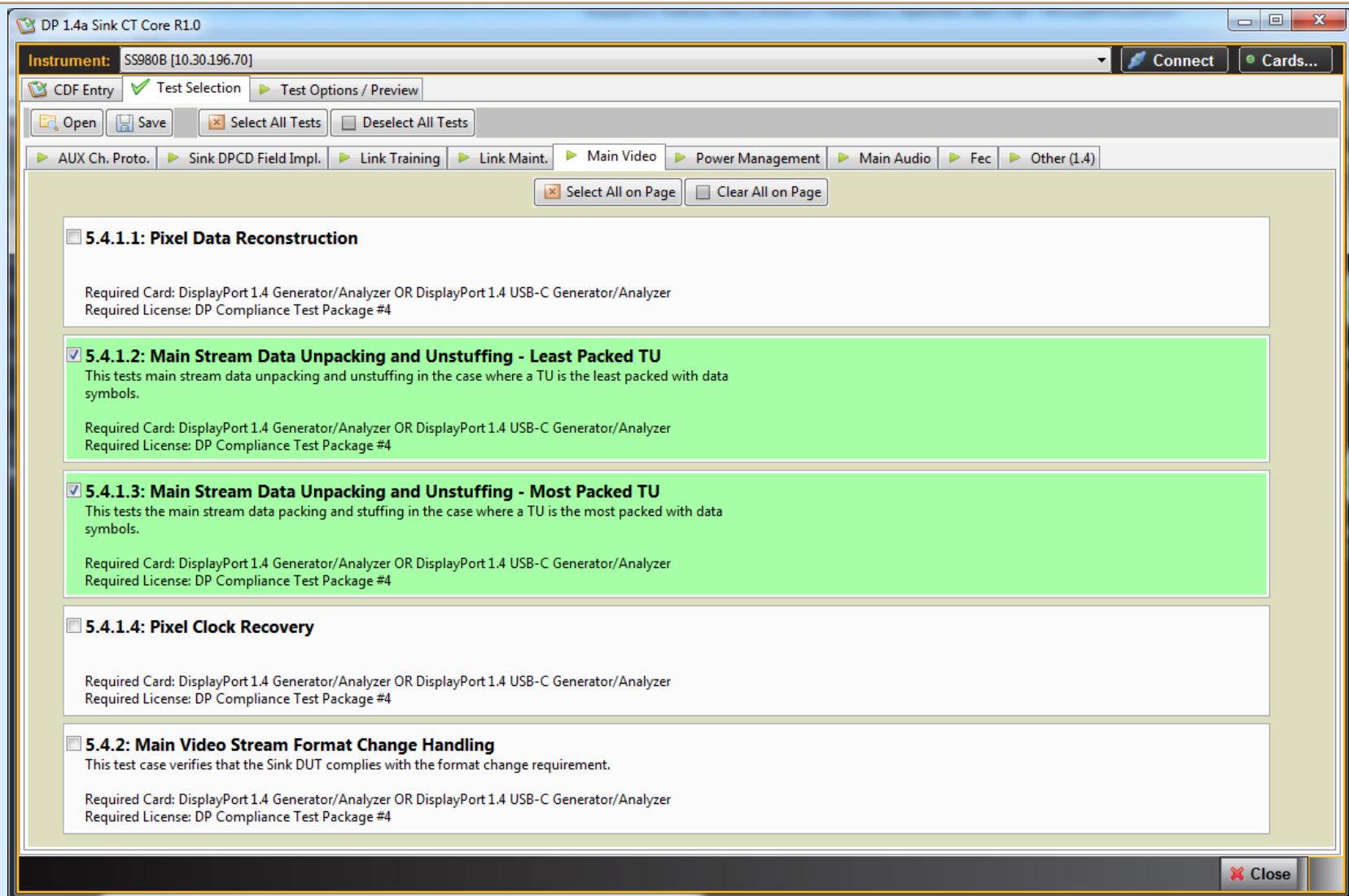
Open ACA Data 5.4.1.1: Pixel Data Reconstruction

Instrument: SS980B [10.30.196.39]

Continue Test Execution Close

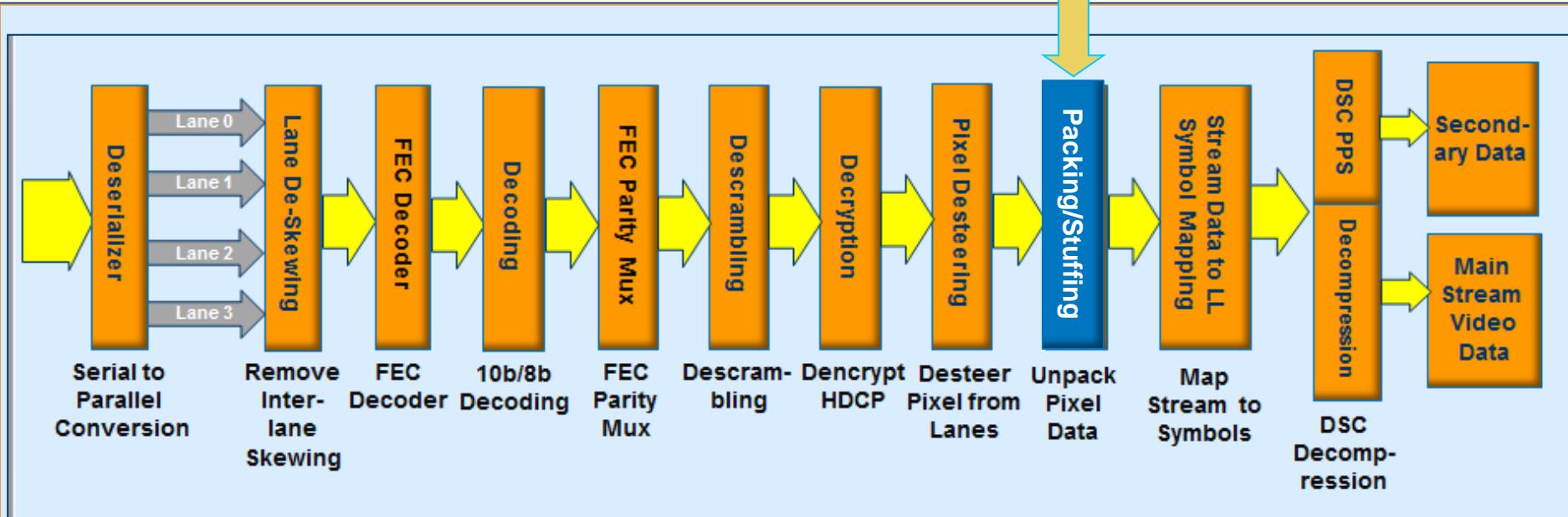
- ◆ Example test results for pixel data reconstruction.
- ◆ CRC check and visual check of received video data.
- ◆ Read CRC values in DPCD registers.
- ◆ Details show subtest with Lane count of 4 with 8 bits per component.

# Sink Link Layer Compliance – Test Selection - Test 5.4.1.2/3 Stream Unpacking/Unstuffing

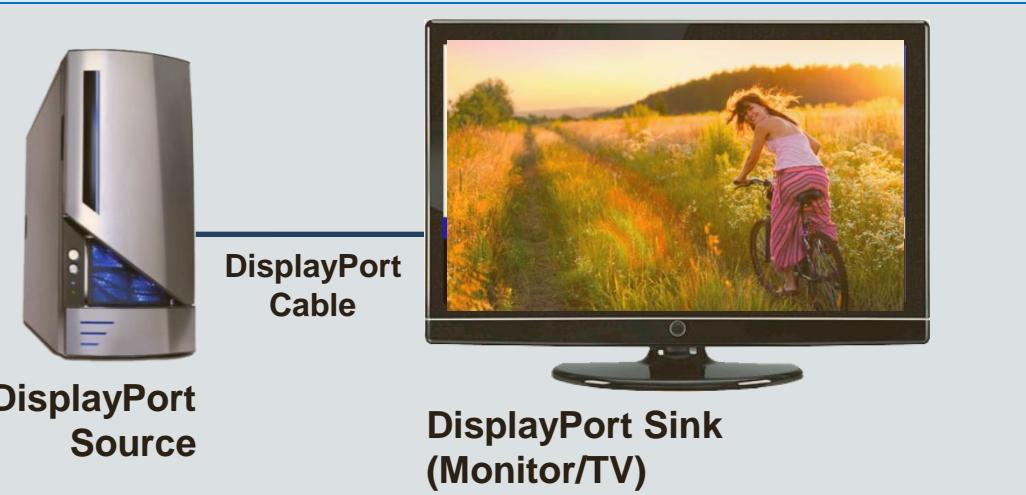


- ◆ Example shows Main Stream Data Unpacking Test Results.
- ◆ **Least Packed** means less video than fill characters per transfer unit.
- ◆ Uses 480p on 4 Lanes at 8.1Gb/s.

# DisplayPort Main Link Stream Generation – Packing and Stuffing



- ◆ Two types of link symbols:
  - **Data symbols** (e.g. pixel, metadata)
  - **Control symbols** (K-Chars) to frame the data symbols.
- ◆ Example shows Main Stream Data Unpacking Test Results.
- ◆ **Least Packed** means less video than fill characters per transfer unit.
- ◆ Uses 480p on 4 Lanes at 8.1Gb/s.



# Sink Link Layer Compliance – Test 5.4.1.2 Stream Unpacking/Unstuffing

Compliance Test Results Viewer

DP 1.4 Sink (1.4 Core R1.0) Compliance Test Results

Results Name: 04\_23\_2018\_11\_55\_18\_sink  
Date Tested: April 23, 2018 11:55 AM  
Overall Status: CTS 1.4 Core R1.0 - Pass

Manufacturer:  
Model Name:  
Port Tested: 1

HTML Report

Test Results

Test Name / Details	Status
5.4.1.2: Main Stream Data Unpacking and Unstuffing - Least Packed TU	Pass
Iter 01:	
01: Initial Link Training at maximum link rate and lane count success <ul style="list-style-type: none"><li>HPD is asserted</li><li>Reference Source receives AUX_ACK at 1 attempts</li><li>Reference Source receives AUX ACK from either write request</li><li>AUX Read 0x2201 (MAX_LINK_RATE) = 0x1e</li><li>AUX Read 0x2202 (MAX_LANE_COUNT) = 0xc4</li><li>Link Training at lane count 4 and link rate 8.1 successful</li></ul>	Pass
02: CRC check or Visual check <ul style="list-style-type: none"><li>TEST_CRC_R_Cr field equals to the Reference Source's internal CRC calculations (0x731C).</li><li>TEST_CRC_G_Y field equals to the Reference Source's internal CRC calculations (0x0A08).</li><li>TEST_CRC_B_Cb field equals to the Reference Source's internal CRC calculations (0x352B).</li></ul>	Pass
5.4.1.3: Main Stream Data Unpacking and Unstuffing - Most Packed TU	Pass

Open ACA Data

5.4.1.2: Main Stream Data Unpacking and Unstuffing - Least Packed TU

Instrument: SS980B [10.30.196.39]

Continue Test Execution

Close

The screenshot shows the Compliance Test Results Viewer interface. At the top, it displays the results for a DP 1.4 Sink (1.4 Core R1.0) with a results name of 04\_23\_2018\_11\_55\_18\_sink, tested on April 23, 2018, at 11:55 AM, with an overall status of CTS 1.4 Core R1.0 - Pass. The manufacturer, model name, and port tested are listed as well, along with a link to an HTML report.

The main area shows the test results for two main categories: 5.4.1.2 and 5.4.1.3. Under 5.4.1.2, there is an 'Iter 01' section containing two test cases: 'Initial Link Training' and 'CRC check or Visual check'. The 'Initial Link Training' case includes several sub-points about link rates and counts. The 'CRC check or Visual check' case includes points about TEST\_CRC fields. Both of these test cases are marked as 'Pass'. The 5.4.1.3 category also has a 'Pass' status.

At the bottom, there are buttons for 'Open ACA Data', 'Continue Test Execution', and 'Close'.

- ◆ Example shows Main Stream Data Unpacking Test Results.
- ◆ **Least Packed** means less video than fill characters per transfer unit.
- ◆ Uses 480p on 4 Lanes at 8.1Gb/s.

# Sink Link Layer Compliance – Test 5.4.1.3 Stream Unpacking/Unstuffing

Compliance Test Results Viewer

DP 1.4 Sink (1.4 Core R1.0) Compliance Test Results

Results Name: 04\_23\_2018\_11\_55\_18\_sink  
Date Tested: April 23, 2018 11:55 AM  
Overall Status: CTS 1.4 Core R1.0 - Pass

Manufacturer:  
Model Name:  
Port Tested: 1

HTML Report

Test Results

	Status
5.4.1.2: Main Stream Data Unpacking and Unstuffing - Least Packed TU	Pass
5.4.1.3: Main Stream Data Unpacking and Unstuffing - Most Packed TU	Pass
Iter 01:	
01: Link Training at lane count = 1 and low lane rate	Pass
HPD is asserted	Pass
Reference Source receives AUX_ACK at 1 attempts	Pass
Reference Source receives AUX ACK from either write request	Pass
AUX Read 0x2201 (MAX_LINK_RATE) = 0x1e	Pass
AUX Read 0x2202 (MAX_LANE_COUNT) = 0xc4	Pass
Link Training at lane count 1 and link rate 1.62 successful	Pass
02: Test validation when lane count = 1	Pass
03: Link Training at lane count = 2 and low lane rate	Pass
04: Test validation when lane count = 2	Pass
05: Link Training at lane count = 4 and low lane rate	Pass
HPD is asserted	Pass
Reference Source receives AUX_ACK at 1 attempts	Pass
Reference Source receives AUX ACK from either write request	Pass
AUX Read 0x2201 (MAX_LINK_RATE) = 0x1e	Pass
AUX Read 0x2202 (MAX_LANE_COUNT) = 0xc4	Pass
Link Training at lane count 4 and link rate 1.62 successful	Pass
06: Test validation when lane count = 4	Not Judged

Open ACA Data

5.4.1.3: Main Stream Data Unpacking and Unstuffing - Most Packed TU

Instrument: SS980B [10.30.196.39]

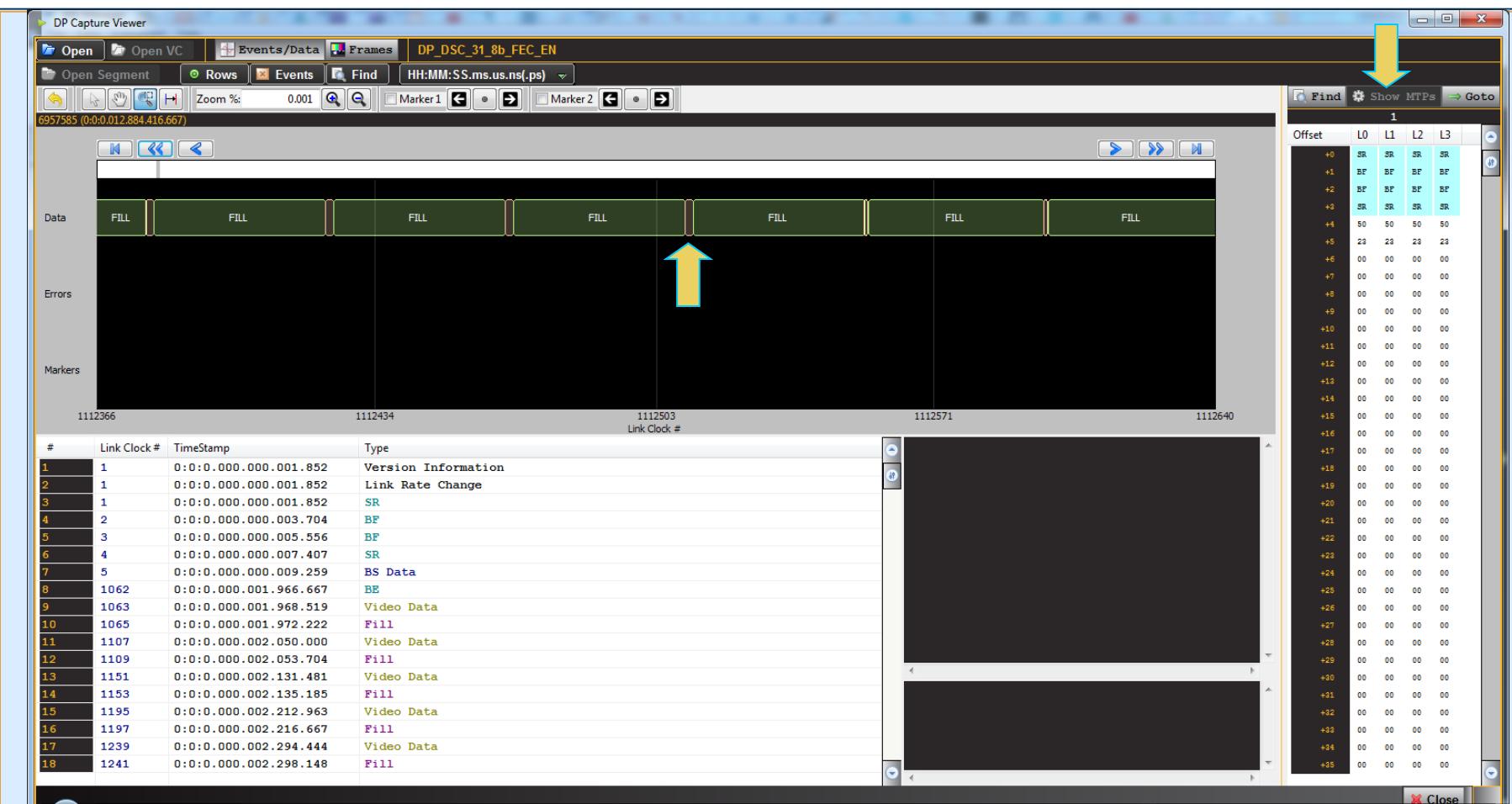
Continue Test Execution

Close



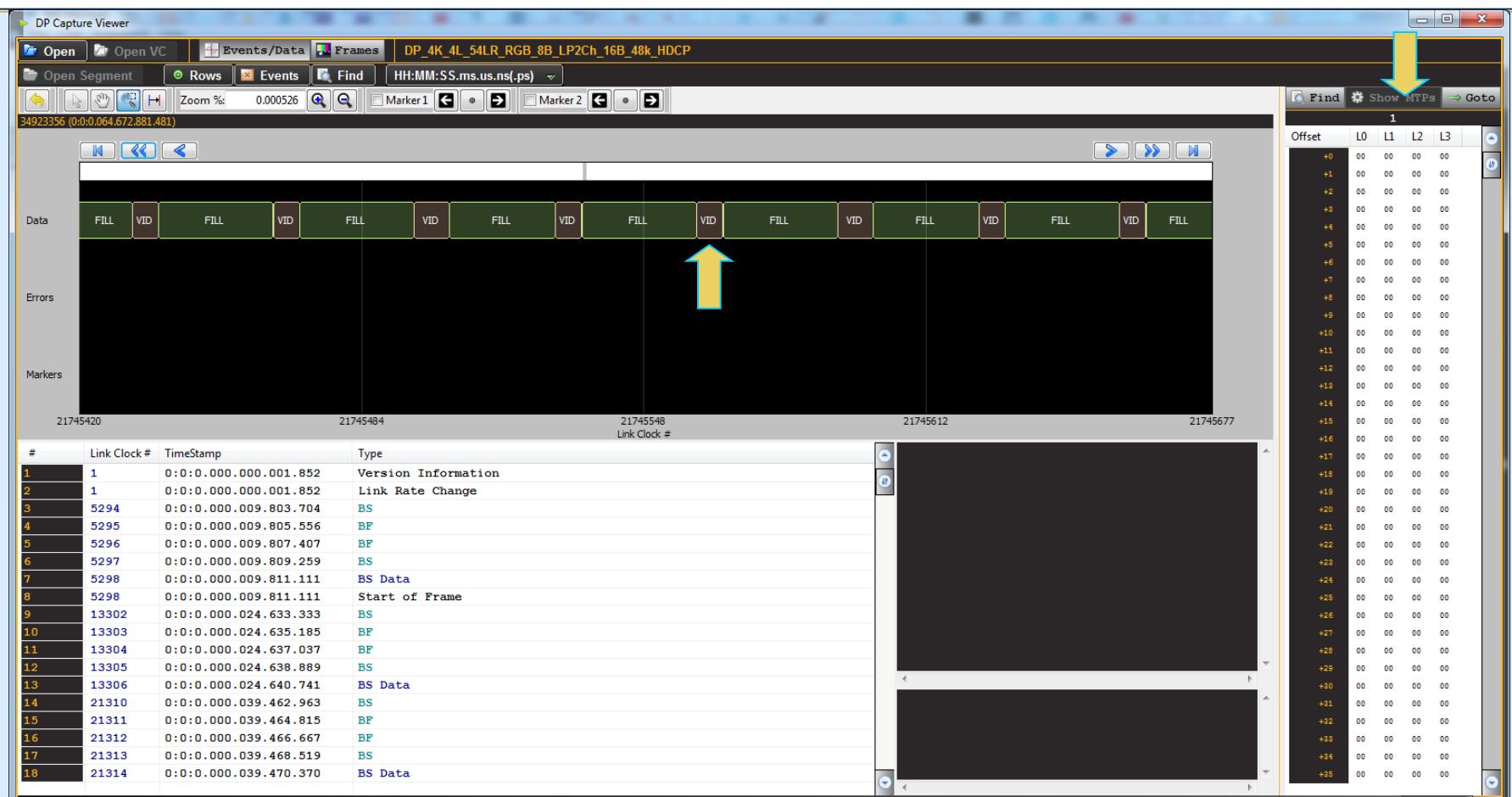
- ◆ Example shows Main Stream Data Unpacking Test Results.
- ◆ **Most Packed** means more video than fill characters per transfer unit.
- ◆ Test uses high resolution format on 4 lanes at 1.62Gb/s link rate.

# DisplayPort Main Link Protocol – Transfer Unit (Least Packed)



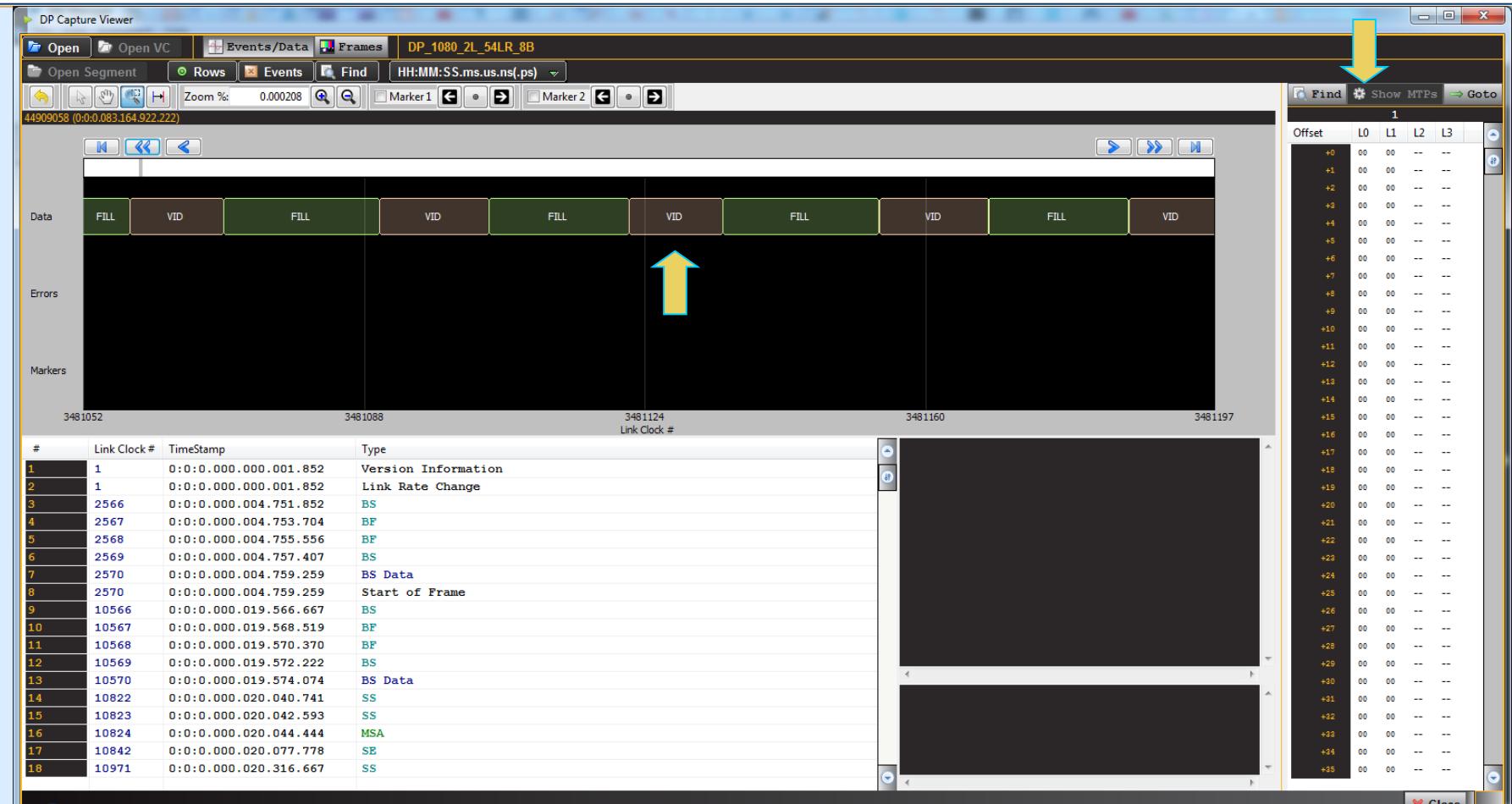
- ◆ Example shows **4 lane** example at **8.1Gb/s** link rate with a **480p** format at 8 bit color depth.
- ◆ Transfer units are composed of almost entirely fill characters.

# DisplayPort Main Link Protocol – Transfer Unit (More Packed)



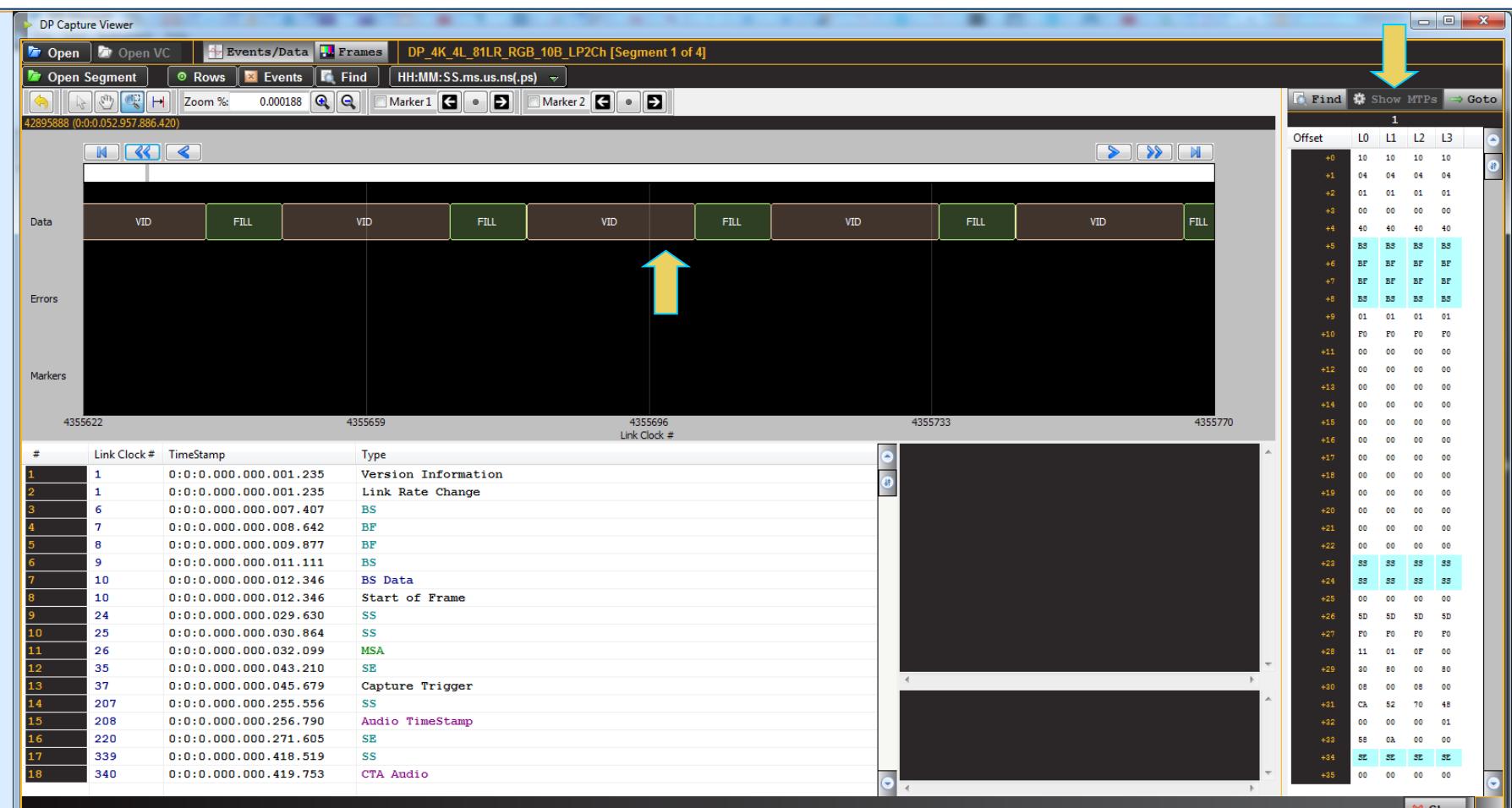
- ◆ Example shows **4 lane** example at **5.4Gb/s** link rate with a **4K** format at 8 bit color depth.
- ◆ Transfer units are predominantly fill characters for stuffing.

# DisplayPort Main Link Protocol – Transfer Unit (Even More Packed)



- ◆ Example shows **2 lane** example at **5.4Gb/s** link rate with a **1080p** format with 8 bit color depth.
- ◆ Transfer units are nearly equal amounts of video and fill characters.

# DisplayPort Main Link Protocol – Transfer Unit (Most Packed)



- ◆ Example shows **4 lane** example at **8.1Gb/s** link rate with a **4K format** with **10 bit** color depth.
- ◆ Transfer units are mostly video.

# DisplayPort Display Stream Compression (DSC) Overview

Webinar – September – 2019



Other Webinars for DSC:

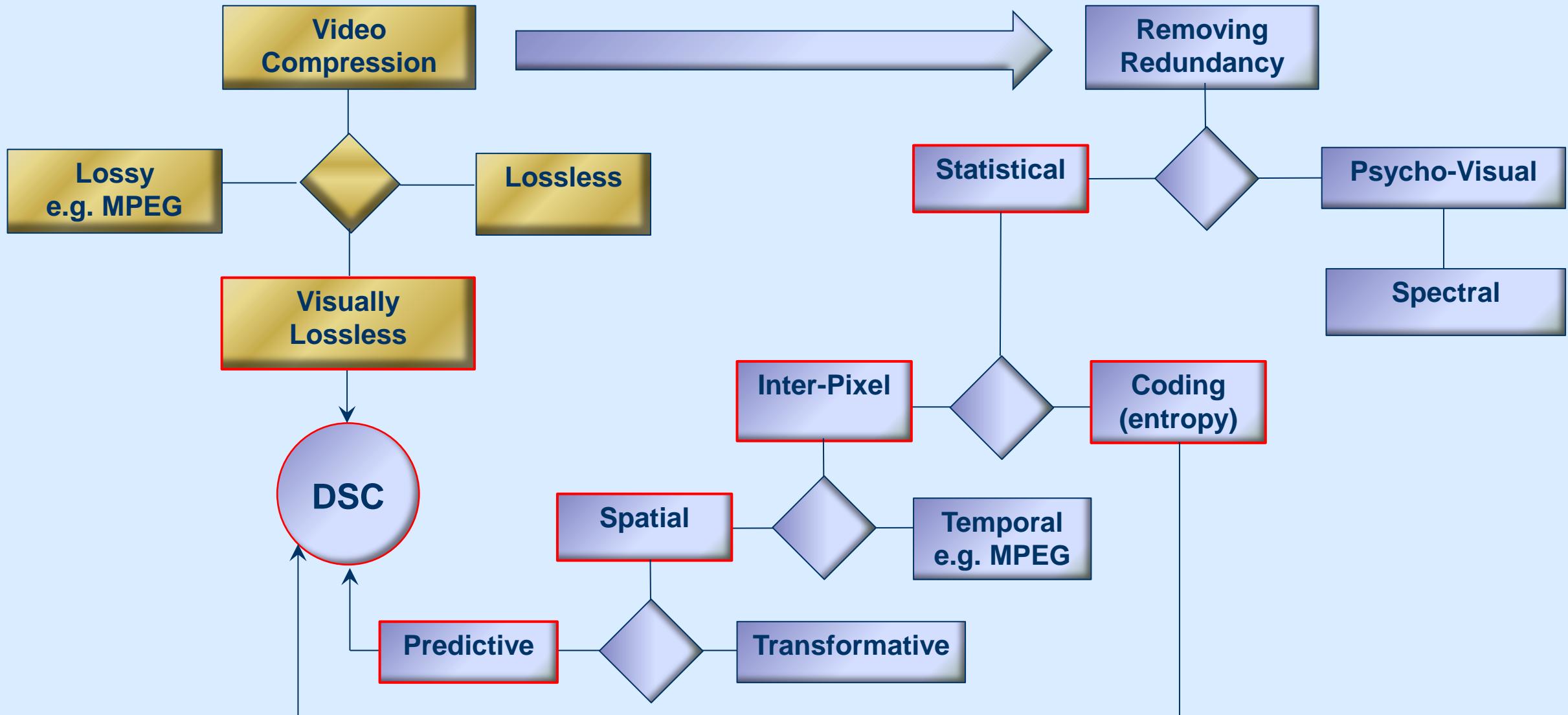
[https://www.quantumdata.com/980\\_dp\\_14\\_usb.html](https://www.quantumdata.com/980_dp_14_usb.html):

- ◆ Essentials of Display Stream Compression (DSC) Protocols Webinar

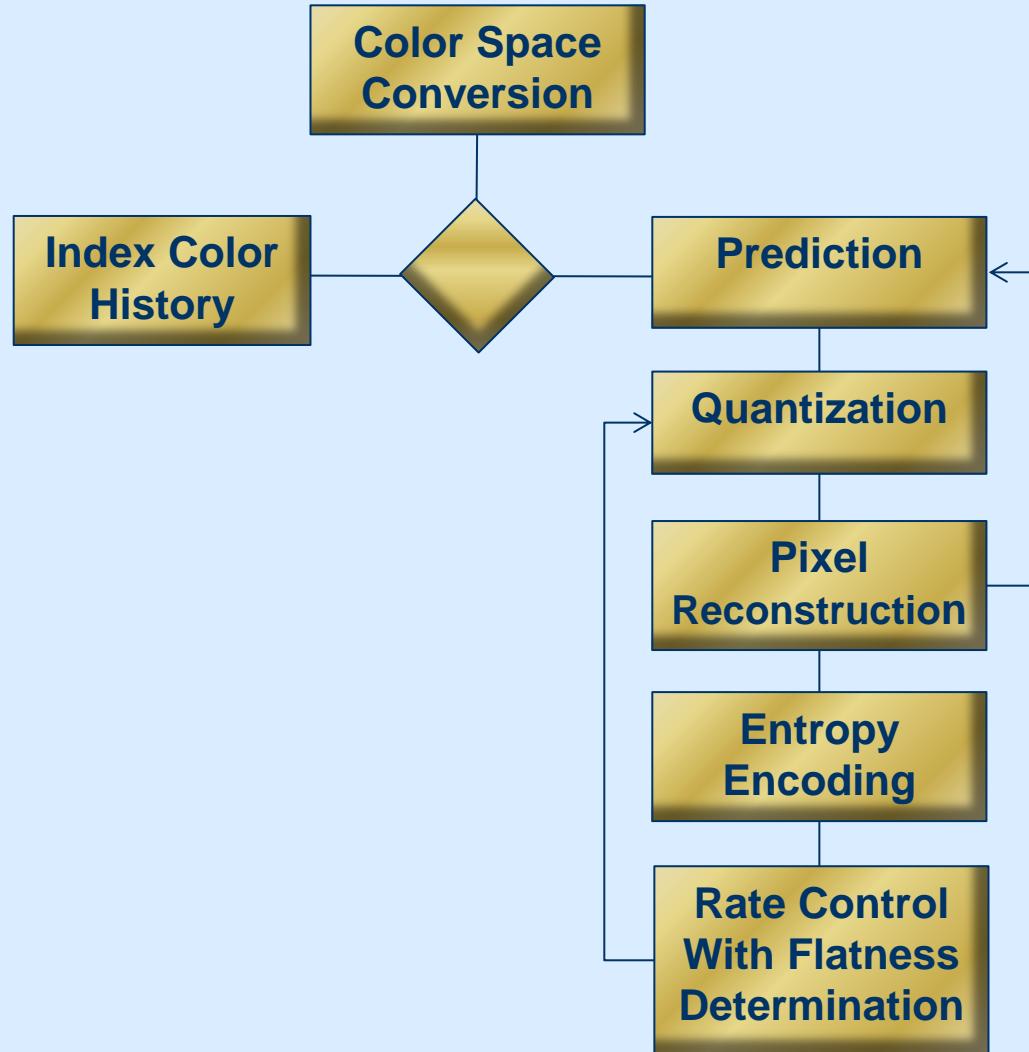
980B w/ DP 1.4 Video Generator /  
Protocol Analyzer module



# Video Compression Principles – Video Compression Taxonomy

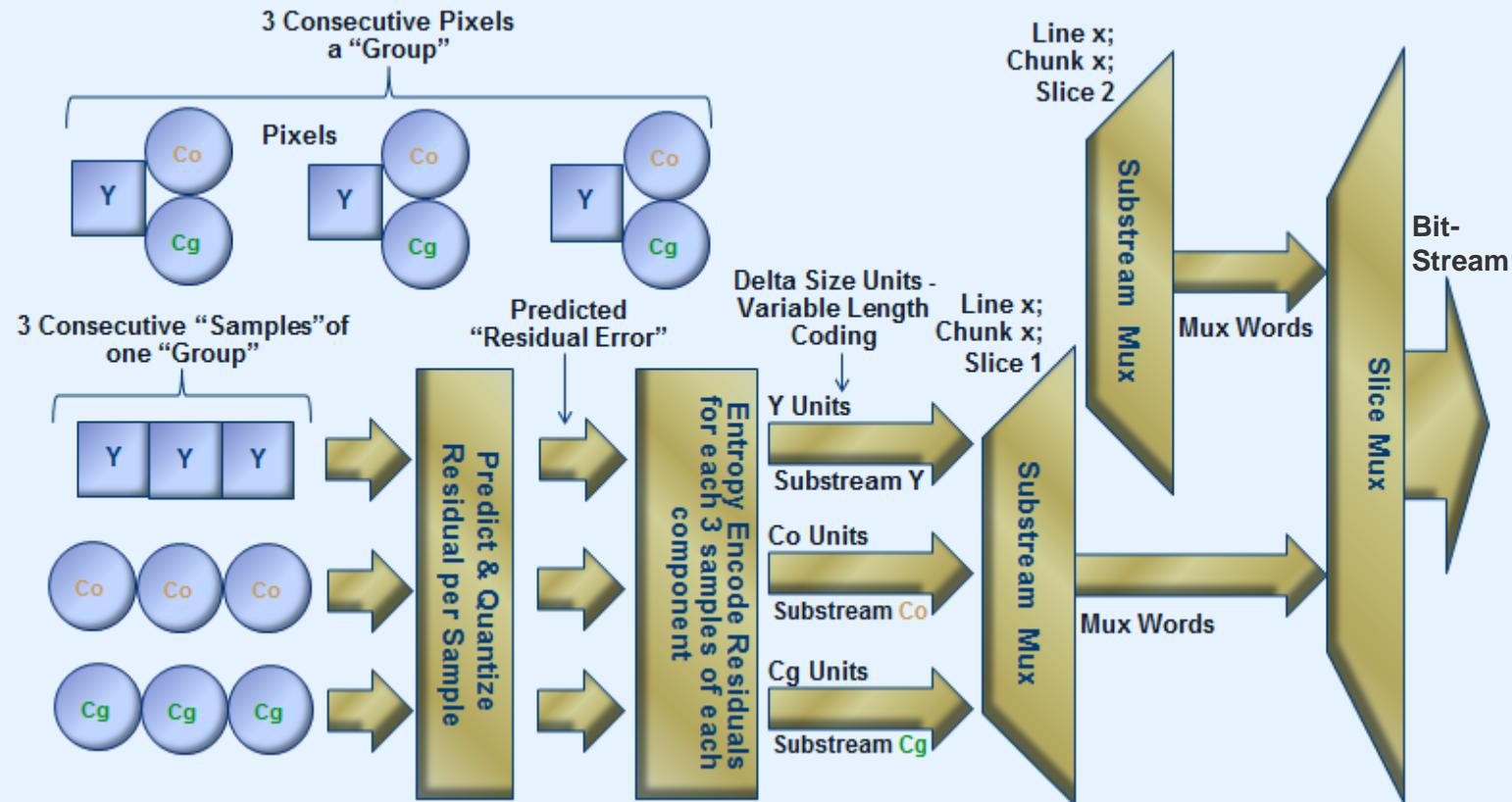


# Display Stream Compression – How Does DSC Compression Work?



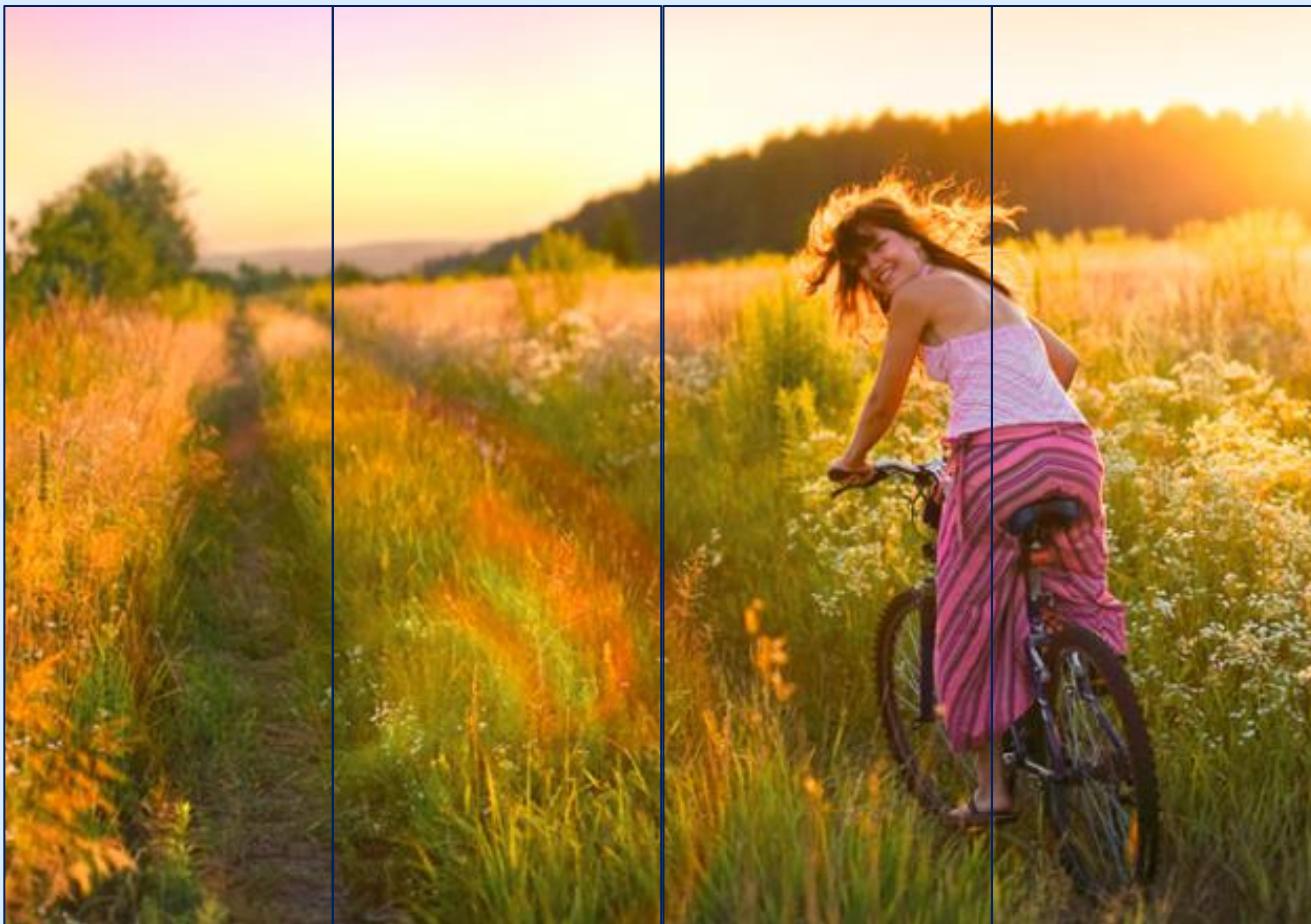
- Display Stream Compression – How it Works:
  1. **Color Space Conversion** – RGB inputs are converted to YCoCg-R.
  2. **Prediction** – One of three (3) models: 1) **Median-Adaptive**, 2) Block, 3) Midpoint.
  3. **Indexed Color History** – An alternative to Prediction where recently used pixel values are stored and available to be referenced.
  4. **Quantization** – Assigns bit values to a residual sample producing some level of error, i.e. lossy component.
  5. **Pixel Reconstruction** – Recreating the pixels in the encoder using the same method used in the decoder.
  6. **Entropy Encoding** – A way of encoding values such that the more frequently occurring values are encoded with fewer bits than less frequently occurring values. (Morse Code is an example of Entropy Encoding.)
  7. **Rate Control** – Process to ensure proper bitstream flow. Manages buffer fullness to ensure that it is not underflowed or overflowed. Controls quantization in association to flatness.
  8. **Flatness determination** – Flatness is the constancy of pixel values or “smoothness” in an area of the video.

# Display Stream Compression – Terminology



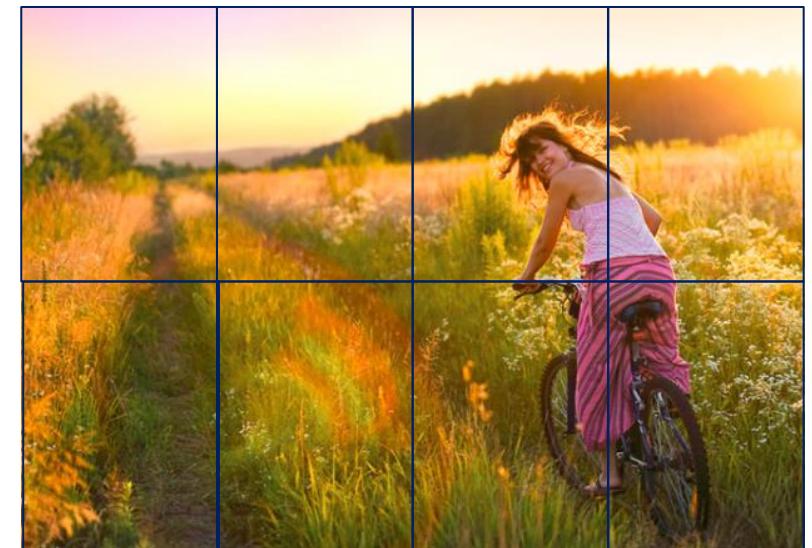
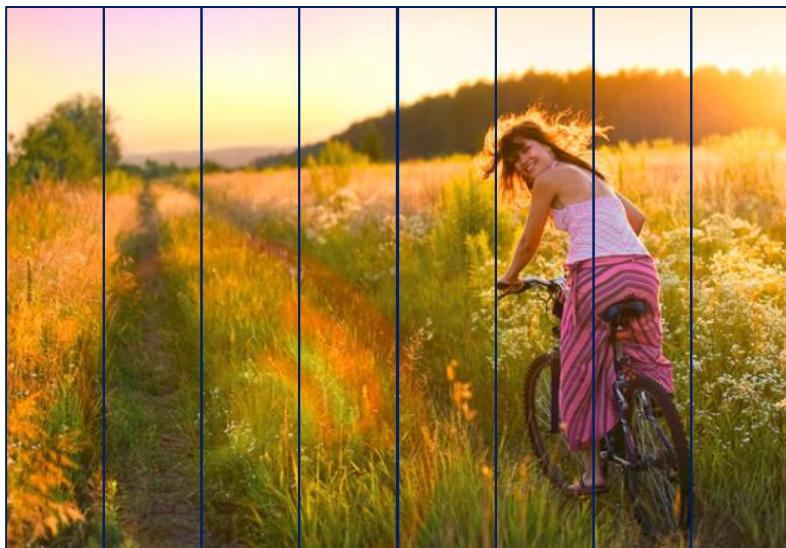
- Important DSC Terminology
  - **Pixel** – A single controllable distinct visual element on a video frame.
  - **Sample** – One component of one pixel. A distinct component value within a pixel Unit, e.g. Y, Co, Cg.
  - **Group** – A logical element set composed of three (3) consecutive pixels (in raster scan order) in a line on a video "Picture".
  - **Unit "Delta-Sized Units"** – A variable length encoded element of the prediction based residual representing a single Sample's (component) within a group.
  - **Substream** – A stream of component bits for one component, i.e. from one Unit.
  - **Mux Word** – A fixed number of bits **for a specific substream component** (Y, Co, Cg). Mux words (48 bit words) from different substreams are multiplexed in the Slice Mux.
  - **Substream Mux** – Multiplexes multiple component substreams in to the "Mux Words" for each component.
  - **Slice** – A rectangular partition of a video "Picture" that's encoded/decoded independently of other slices within the Picture. All slices within a Picture are the same size.
  - **Slice Mux** – Used when there are multiple slices per line (which is most of the time). Chunks for each line are muxed together.
  - **Chunk** – Portion of encoded bitstream that comprises a line of compressed video.

# Display Stream Compression – Slices

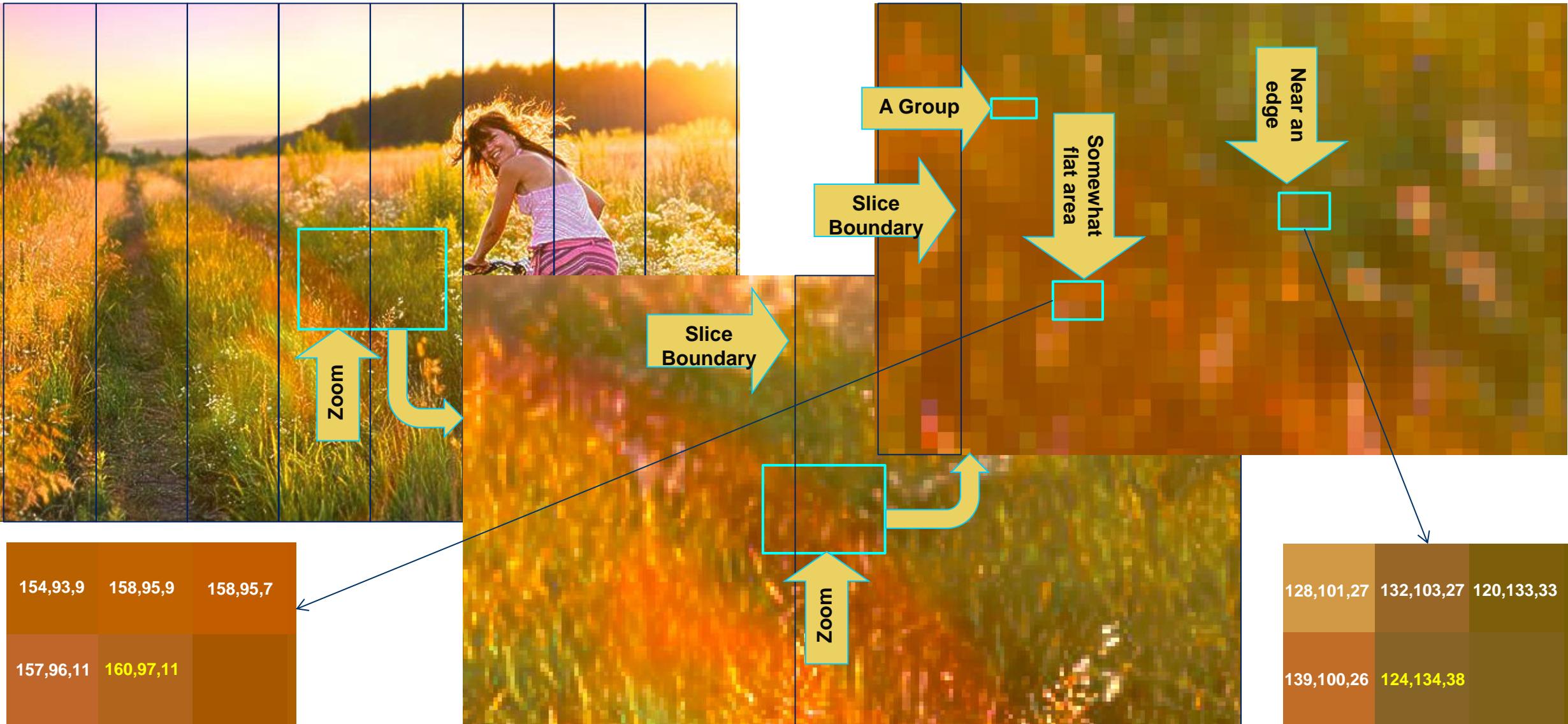


- DSC Slices – Quick Facts.
  - A slice is a rectangular partition of a video frame.
  - Each slice is **encoded independently** of other slices within the frame.
  - There can be one or multiple slices per line.
  - When there are multiple slices per line, the “Slice Multiplexing” function is used to multiplex the slice data into the bit stream.
  - All **slices within a frame are the same size**.
  - **Slice configuration** is transmitted from a source encoder to a sink decoder in **metadata (Picture Parameter Set [PPS])**.
- Why use slices...why partition the video frame?
  - Partitioning the video into slices to ensure transmission **errors aren't propagated** across the slices.
  - Slice partitioning allows or facilitates parallel processing of slices.

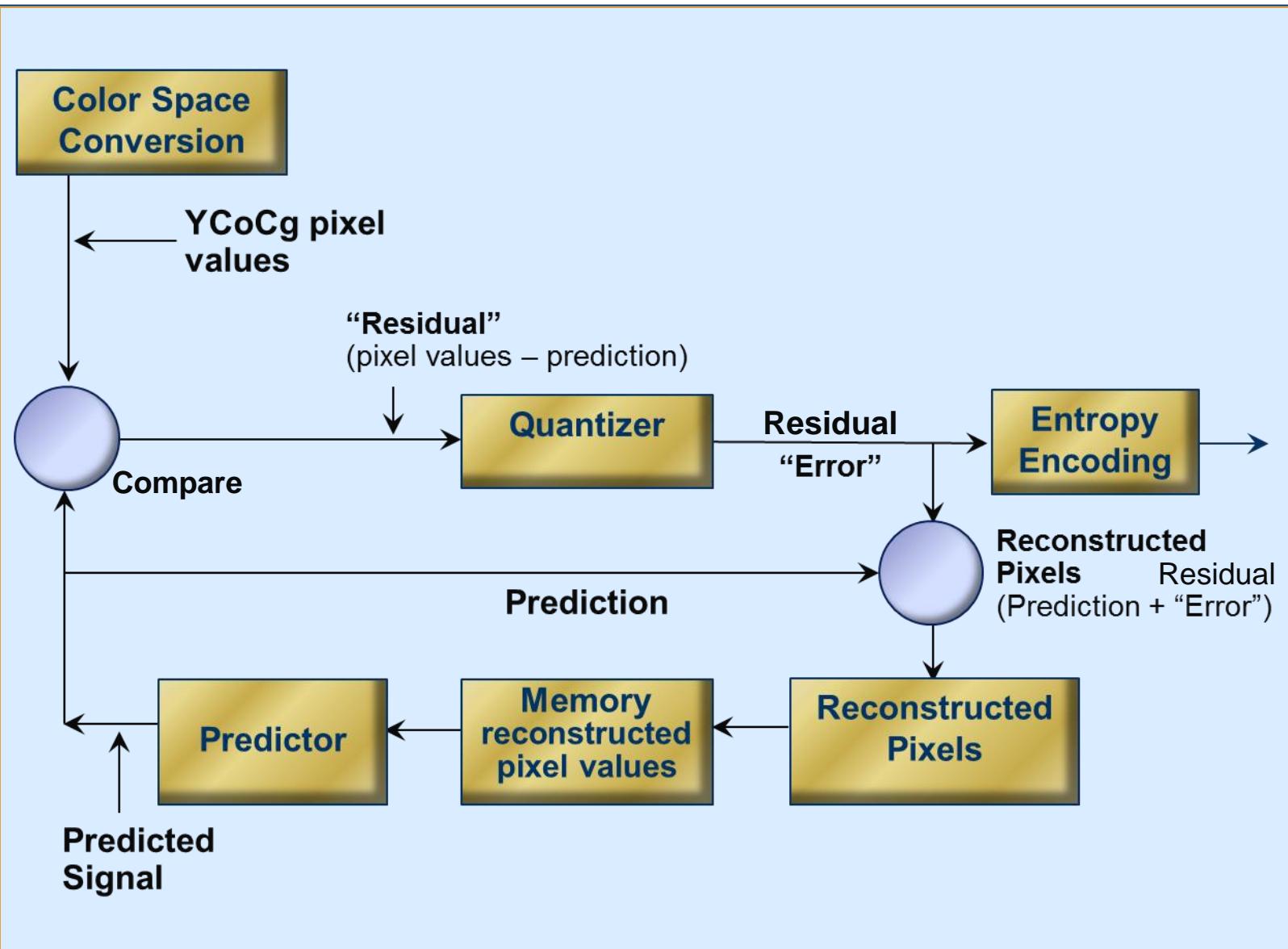
# Display Stream Compression – Slice Configurations



# Display Stream Compression – MMAP Prediction Method

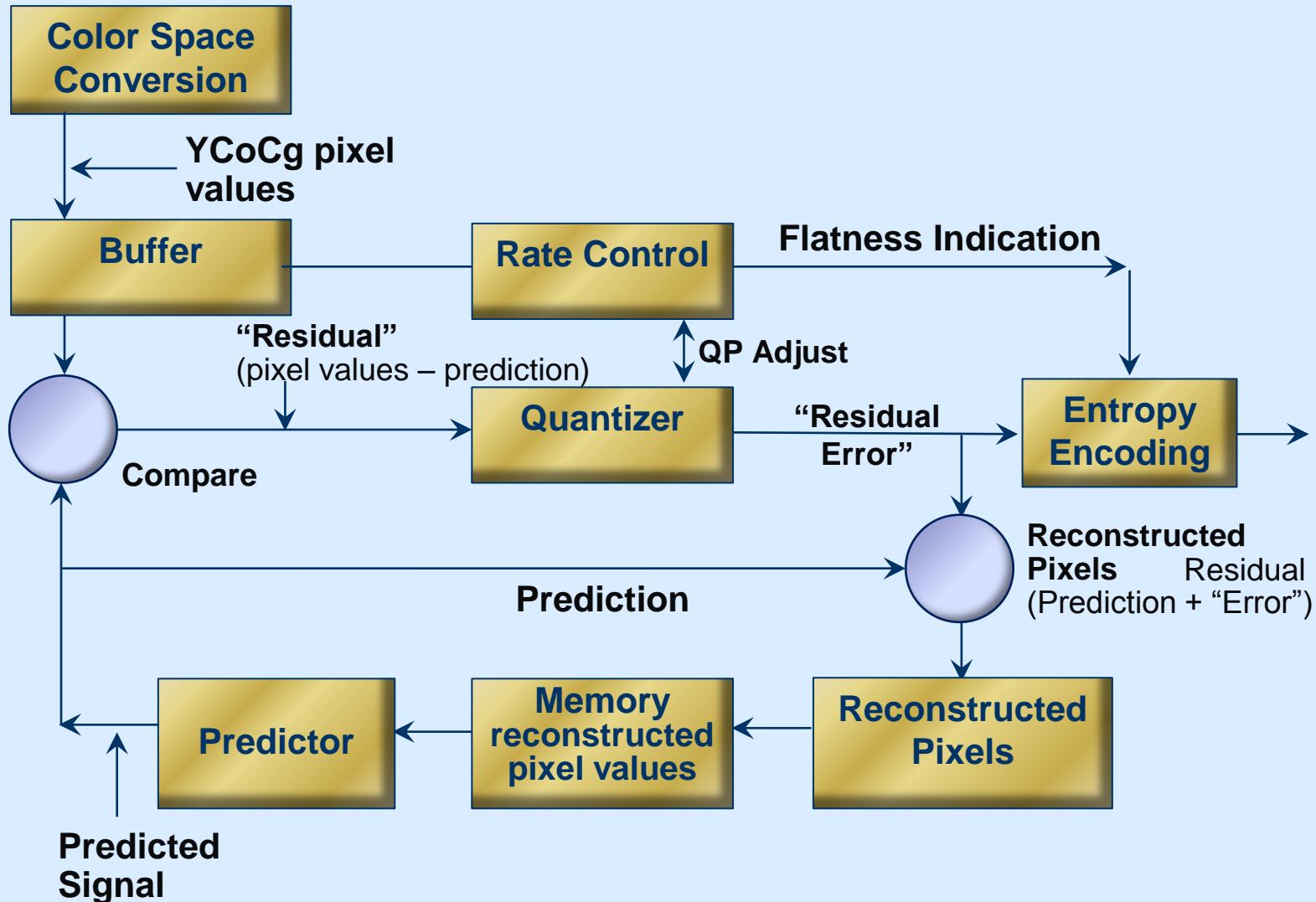


# Display Stream Compression – Encoder Prediction Operation



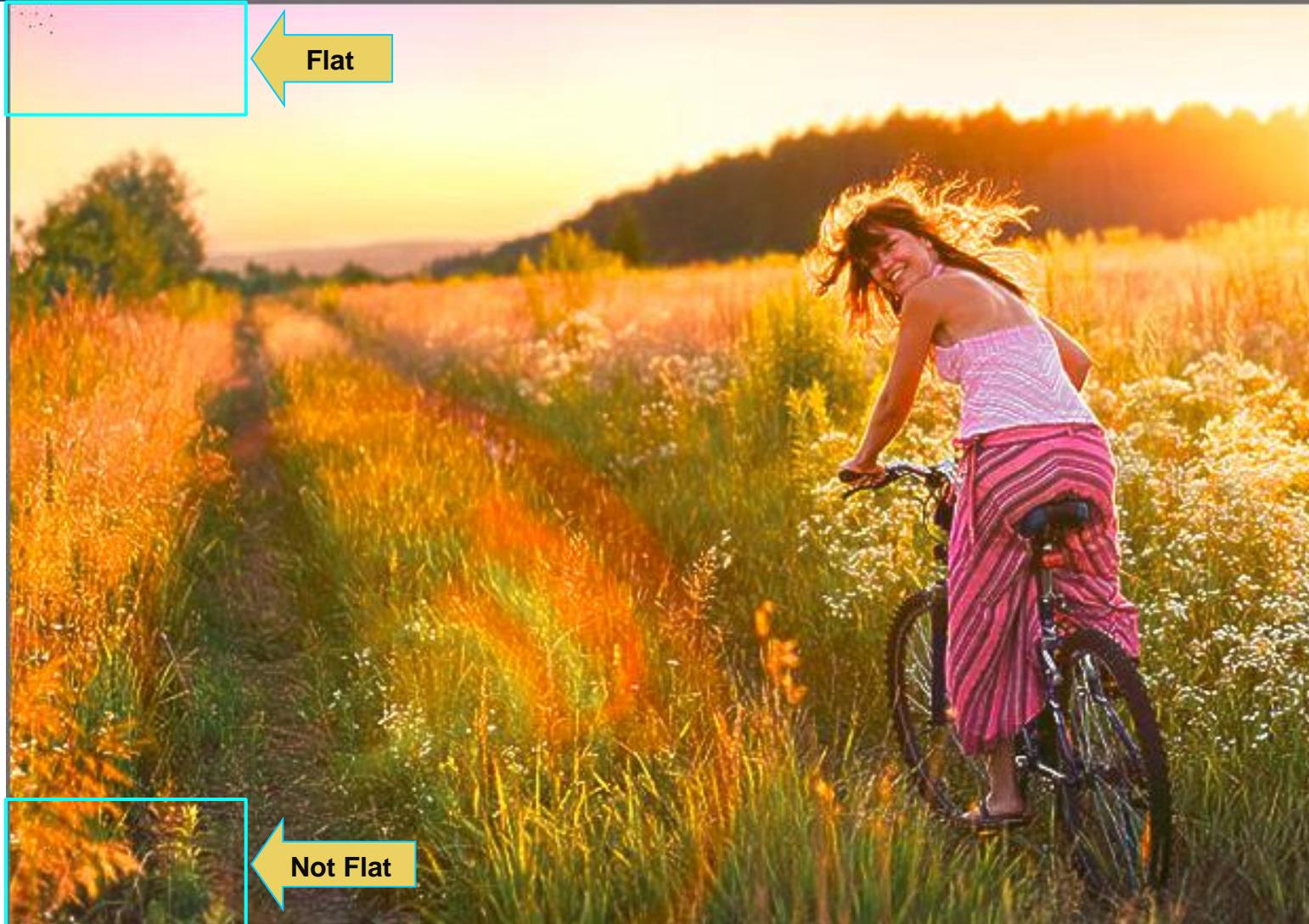
- DSC compression is based on Differential Pulse Code Modulation (DPCM) methods to predict the current pixel from adjacent pixels and encodes the difference between the original pixel values and predicted pixel values to produce a **"Residual."**
- A quantizer converts the Residual into a quantized (**a "Residual "Error"**). It is the prediction residual with the quantized error (not the original pixel values) that is transmitted to the decoder over the display link.
- However, the **Predictor uses "reconstructed pixels"** in the prediction, not the actual pixel values. Why?:
  - Use of the reconstructed (decoded) pixels ensures that the prediction signal is identical in the encoder and decoder.
  - Because the original pixels are not available in the decoder side, the use of.
  - If the encoder used the original pixels for prediction, there would be an accumulation of error "Error Drift."

# Display Stream Compression – Encoder Flatness Indication & QP Adjustment



- “Flatness” is a **measure of smoothness** or similarity in pixel values throughout a region in the video.
- Flatness is used by the Rate Controller to adjust the “**Quantization Parameter**” (QP) which allows the quantization to introduce more or less error depending on the flatness.
- There are two (2) levels of flatness: 1) Very Flat and 2) Somewhat Flat.
- The **flatter the region the less errors that can be tolerated** because they are far more noticeable than “busy” areas.
- Flatness determination uses a “**Super Group**” which is four groups.
- The **indication of flatness** occurs every four groups (Super Group) and is **transmitted** using a code sequence **in the first luma subplot** in the Super Group.
- The original uncompressed pixels are used in the flatness determination.

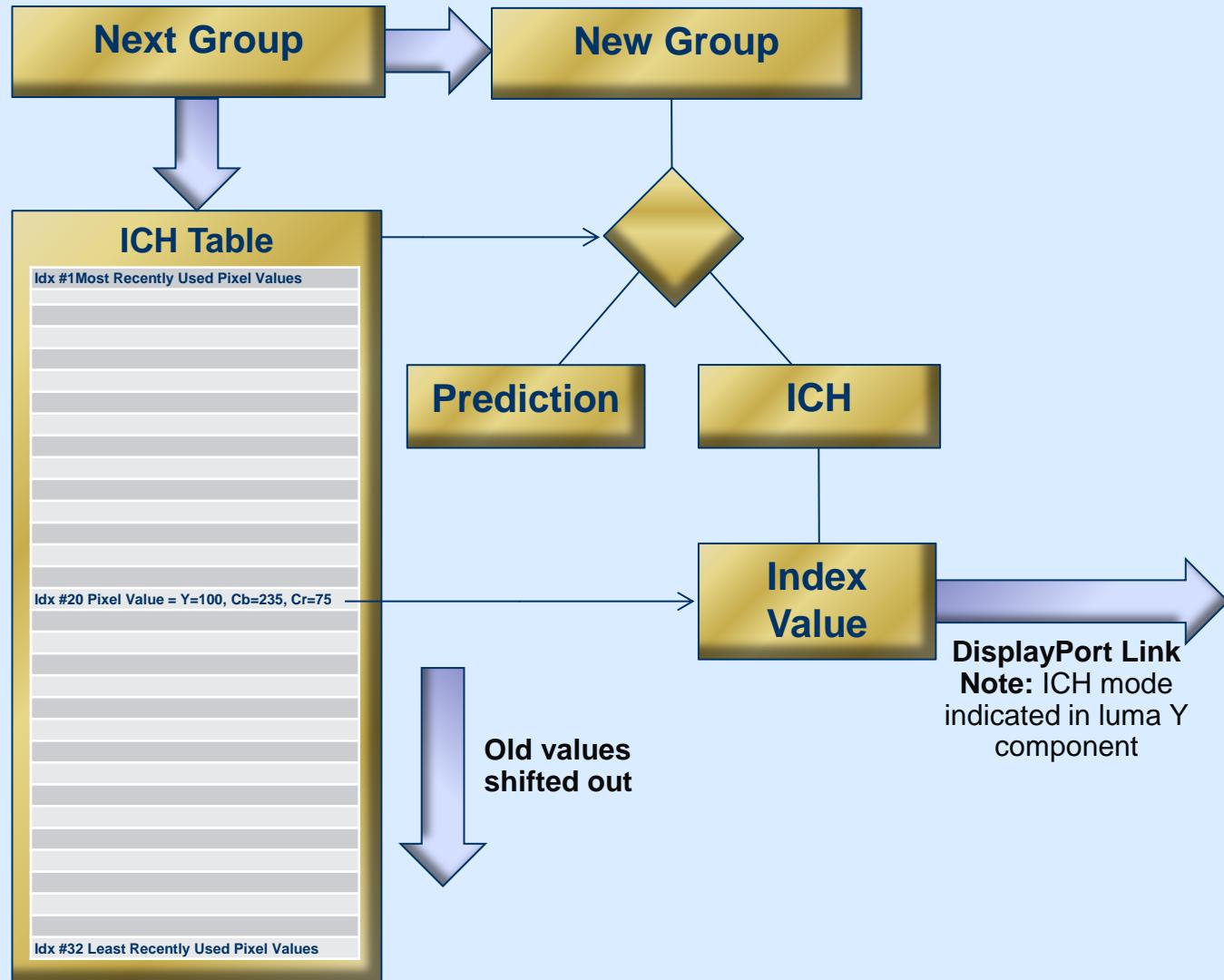
# Display Stream Compression – Encoder Flatness Indication & QP Adjustment



- Flatness / QP – Quick Facts.
  - Flatness is detected and used by the Rate Controller to adjust the “Quantization Parameter” (QP) which allows the quantization to introduce more or less error depending on the flatness.
  - The more flat an area of the image, the lower the QP.
  - Image to right has pixel errors introduced in both the “Flat” region and the “Not Flat” region.

**Note:** The pixel errors are only noticeable in the Flat region.

# Display Stream Compression – Indexed Color History (ICH) Operation



- DSC Indexed Color History - Quick Facts:
  - ICH mode is an alternative DSC compression mechanism to Prediction.
  - The DSC encoder determines whether to use the ICH mode on a **pixel group by pixel group basis**.
  - ICH is useful on **computer graphics where certain pixel values occur very commonly**.
  - ICH uses a “Storage Unit”, i.e. a dynamic table with the recent history of reconstructed pixel values.
  - There are 32 values in the Index Color History storage unit.
  - The ICH process assigns a **5 bit “Index Value”** that points to a location in the table.
  - It is these 5 bit Index Values that are transmitted over the DisplayPort link to the decoder.
  - The **encoder and decoder have the same ICH table of values**.
  - The **encoder signals over the bitstream** to the decoder that it will use ICH by a special bit sequence **in the luma (Y) substream**.

# DisplayPort Display Stream Compression (DSC) Protocol Operation

Webinar – September – 2019



Other Webinars for DSC:

[https://www.quantumdata.com/980\\_dp\\_14\\_usb.html](https://www.quantumdata.com/980_dp_14_usb.html):

- ◆ Essentials of Display Stream Compression (DSC) Protocols Webinar

980B w/ DP 1.4 Video Generator / Protocol Analyzer module

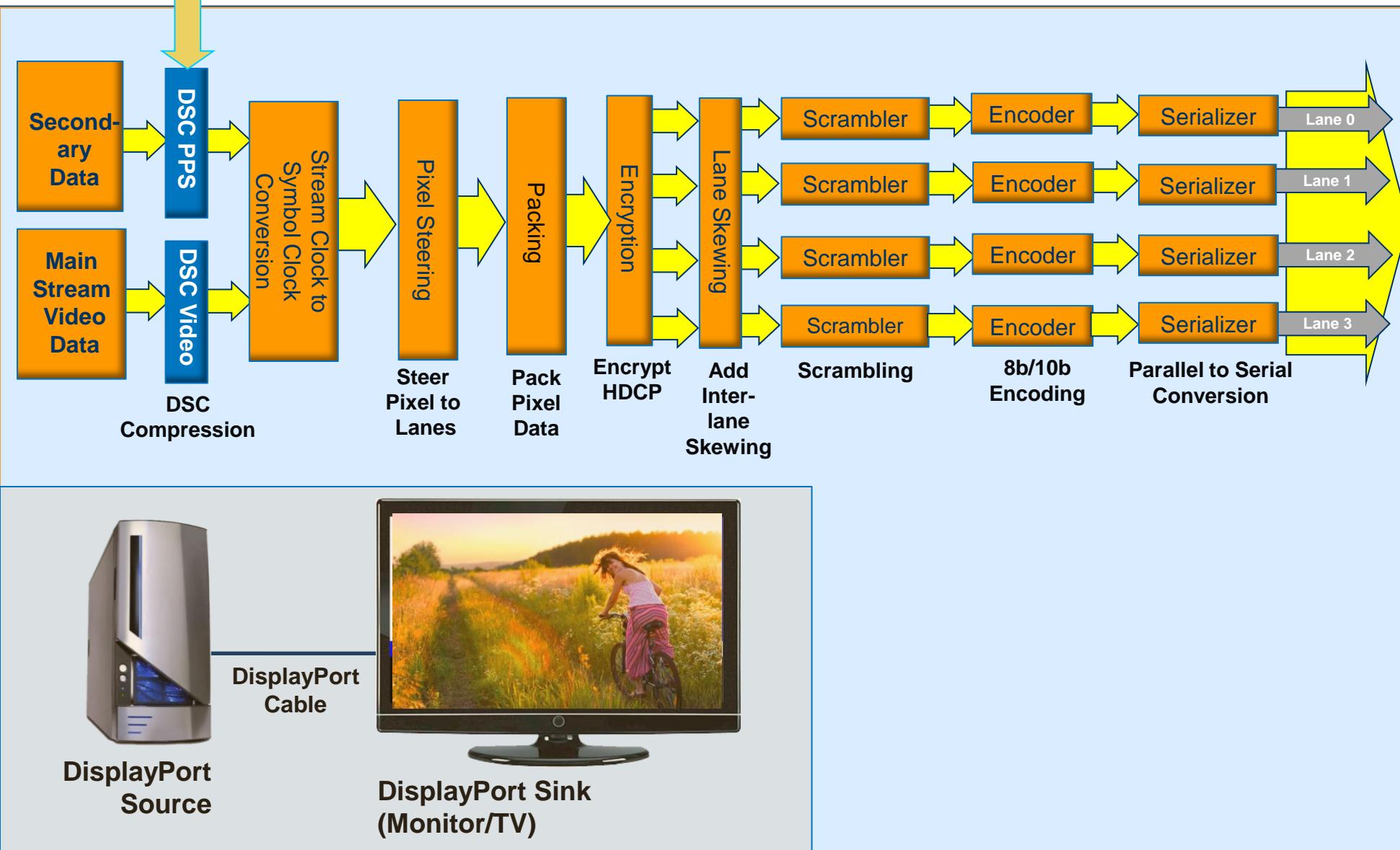


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# DisplayPort DSC Protocols

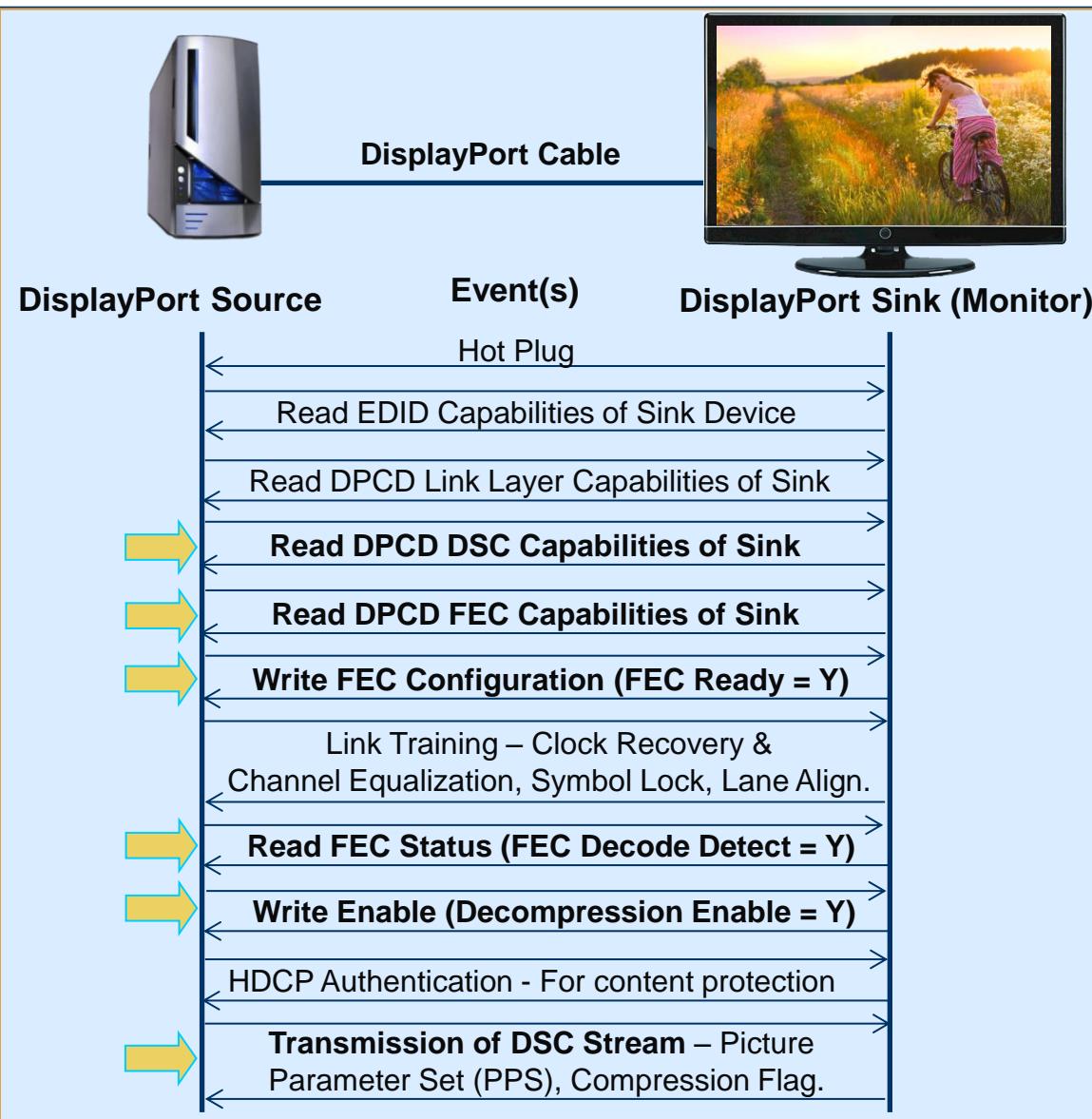
## Configuration, Discovery, Enabling/Disabling

# DisplayPort Main Link Stream Generation – DSC PPS and Video



- ◆ Two types of link symbols:
  - **Data symbols** (e.g. pixel, metadata)
  - **Control symbols** (K-Chars) to frame the data symbols.
- ◆ Example shows Main Stream Data Unpacking Test Results.
- ◆ **Least Packed** means less video than fill characters per transfer unit.
- ◆ Uses 480p on 4 Lanes at 8.1Gb/s.

# Display Stream Compression – Configuration, Discovery, Enabling



- **Hot Plug.** Indication to a Source that a Display is connected.
- **Read EDID.** EDID is a data structure provided by a DP display that describes its capabilities to a DP video source.
- **Read DPCD Link Capabilities.** DPCD is a data structure in a DP sink device that describes its link capabilities.
- **Read DPCD registers for DSC Capability.** Source reads to verify the DSC Support flag is set indicating DSC support.
- **Read DPCD registers for FEC.** Source reads to verify the FEC Capability flag is set indicating FEC capability.
- **Set FEC Configuration registers.** Source writes to set the FEC Ready flag (enable).
- **Link Training.** Link training establishes the physical link parameters (number of lanes, link rate, voltage swing, pre-emphasis, equalization) used for transmission of video and audio over the main link. **Two phases:**
  - Clock Recovery
  - Channel Equalization, Symbol Lock, Inter-Lane alignment.
- **Read FEC Status.** Verify sink detects the FEC Decode enable sequence is detected.
- **Enable DSC.** Source sets (enables) Decompression Enable Flag.
- If the video/audio content is flagged for content protection, the **HDCP authentication** protocol is used.
- **Transmit compressed**, encrypted video with Picture Parameter (PPS) metadata.

# Display Stream Compression – Picture Parameter Set (PPS)



- Picture Parameter Set (PPS)
  - Source **sends PPS** after it receives an acknowledgement from the sink that the **Decompression Enable bit has been set** in the DPCD register.
  - The PPS is transmitted **over the main link during the vertical blanking** in a DisplayPort **Secondary Data** packet.
  - The parameter data that is transmitted in the **PPS** is necessary to inform the sink how to decode the compressed data.
  - Sink uses the last PPS transmitted before the Blanking Start (BS) symbol sequence of the scan line prior to where the active region starts.
  - Compression **parameters can be changed between compressed frames by transmitting a new PPS**. The PPS values apply to all subsequent frames.

# DisplayPort Display Stream Compression (DSC) - Compliance Testing

Webinar – September – 2019



Other Webinars for DSC:

[https://www.quantumdata.com/980\\_dp\\_14\\_usb.html](https://www.quantumdata.com/980_dp_14_usb.html):

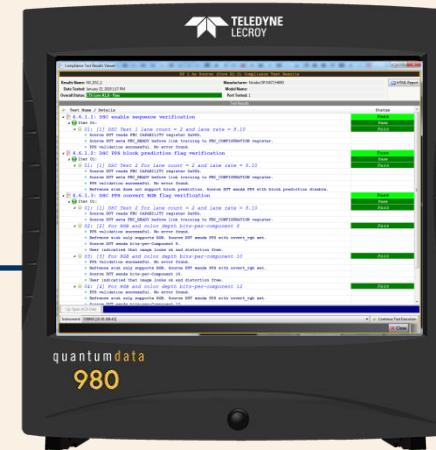
- ◆ Essentials of Display Stream Compression (DSC) Compliance Test Protocols

# DisplayPort DSC Compliance Basic Interop – DSC Transport Source Testing

DisplayPort  
Source DUT



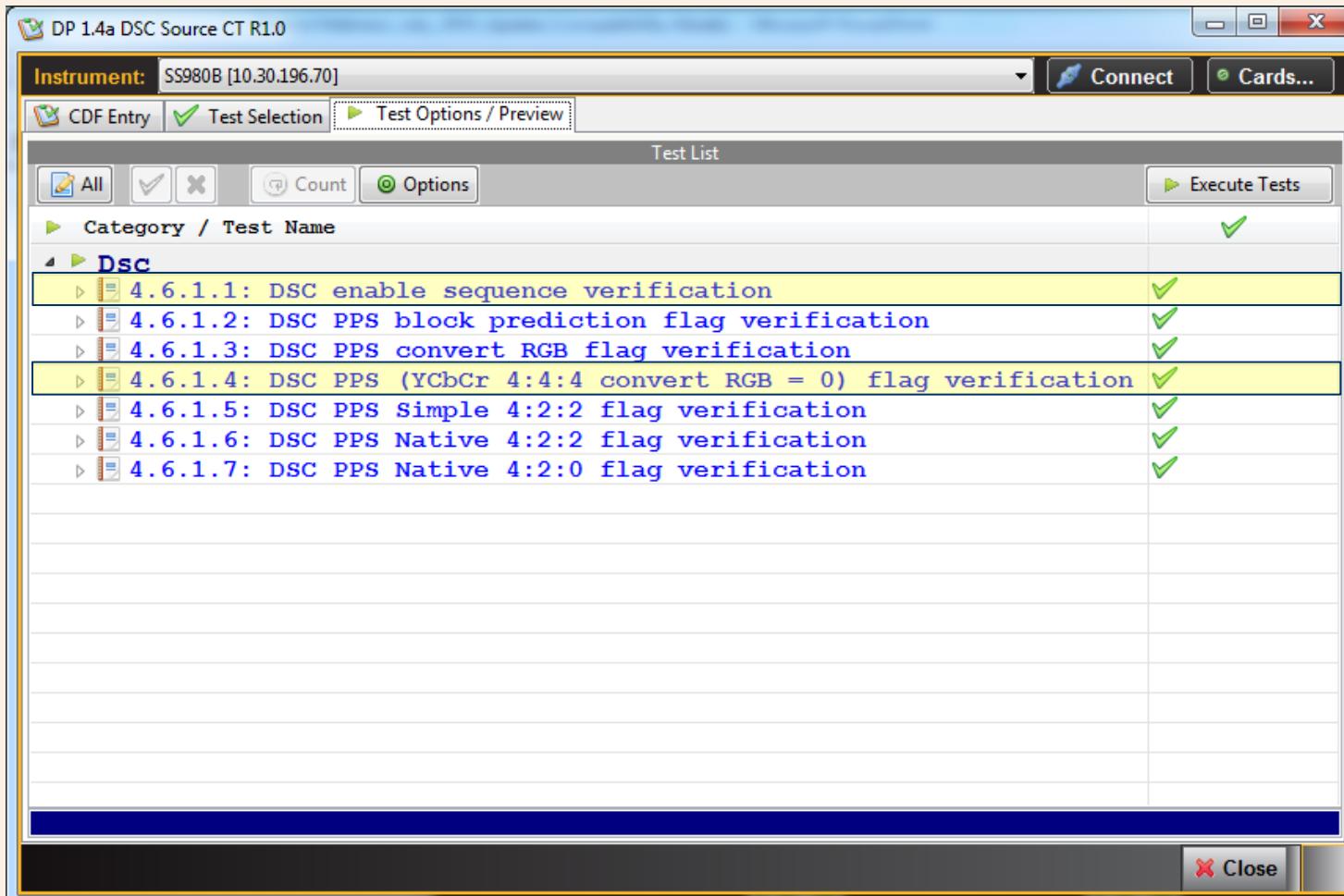
DisplayPort Cable



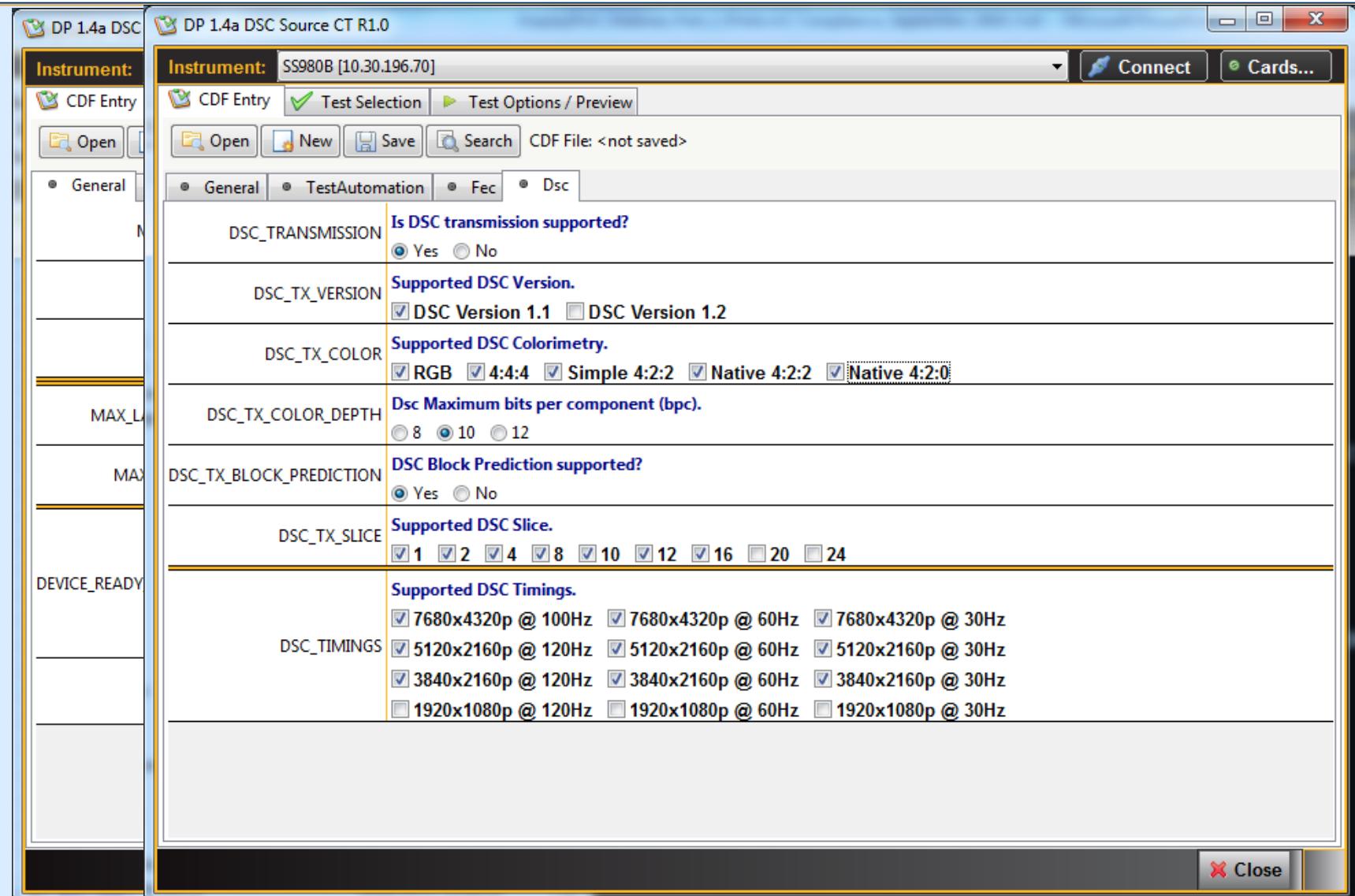
DP 1.4 Reference Sink  
Example: Teledyne LeCroy  
quantumdata 980 Test Platform  
with DP 1.4 Protocol Analyzer /  
Video Generator

# DisplayPort Source DSC Compliance Testing – List of Tests

- List of DP DSC Source Compliance Tests.
- First Phase of DSC Compliance testing covers Basic Interoperability for DSC Transport.

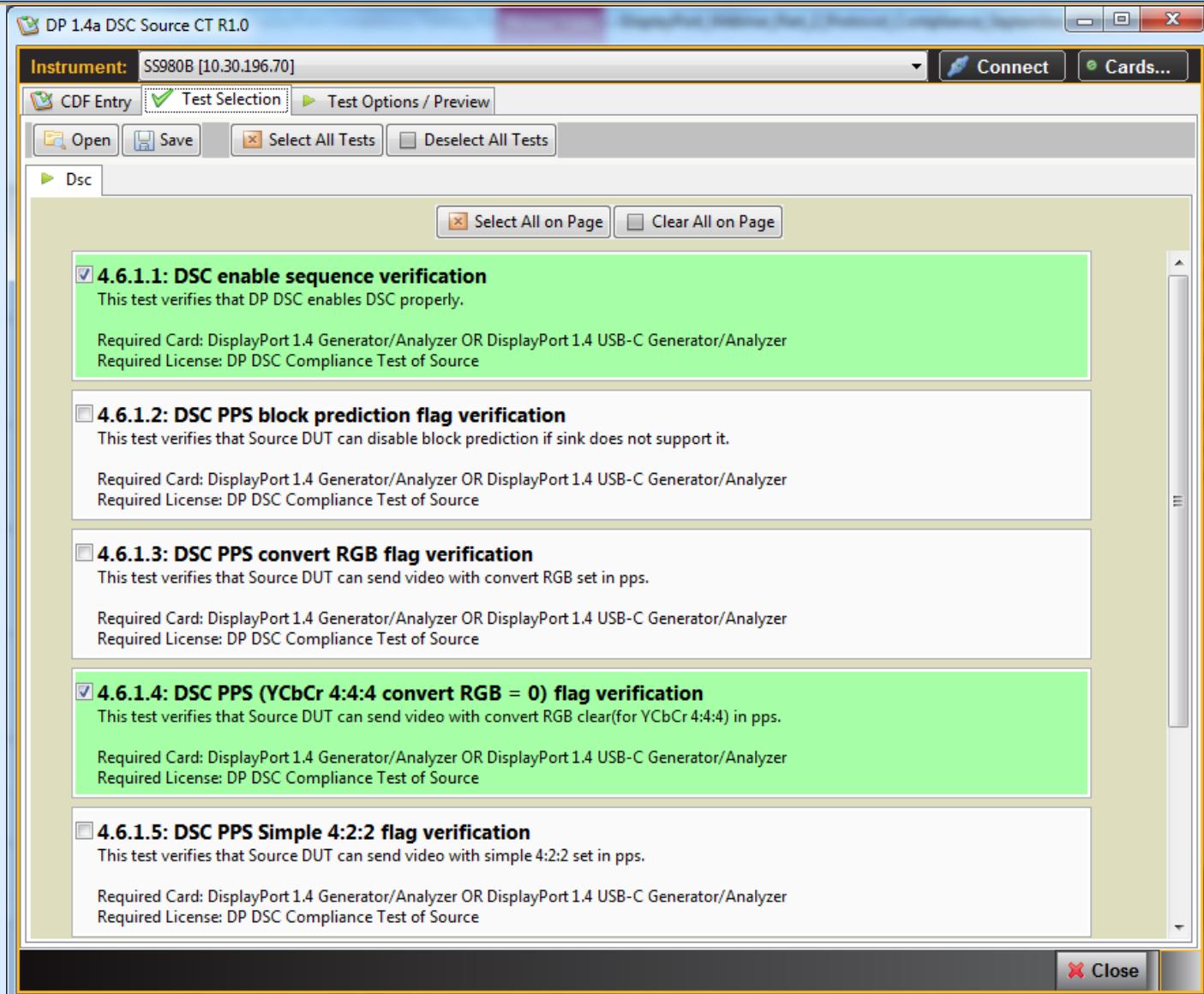


# Entering the CDF Information – Source DSC Capabilities



- ◆ Capabilities Declaration Form (CDF) must be filled out prior to the running the test.
- ◆ CDF is used by the reference sink to know which Link Layer related sink features to test.
- ◆ DSC – Described DSC capabilities of the source device.

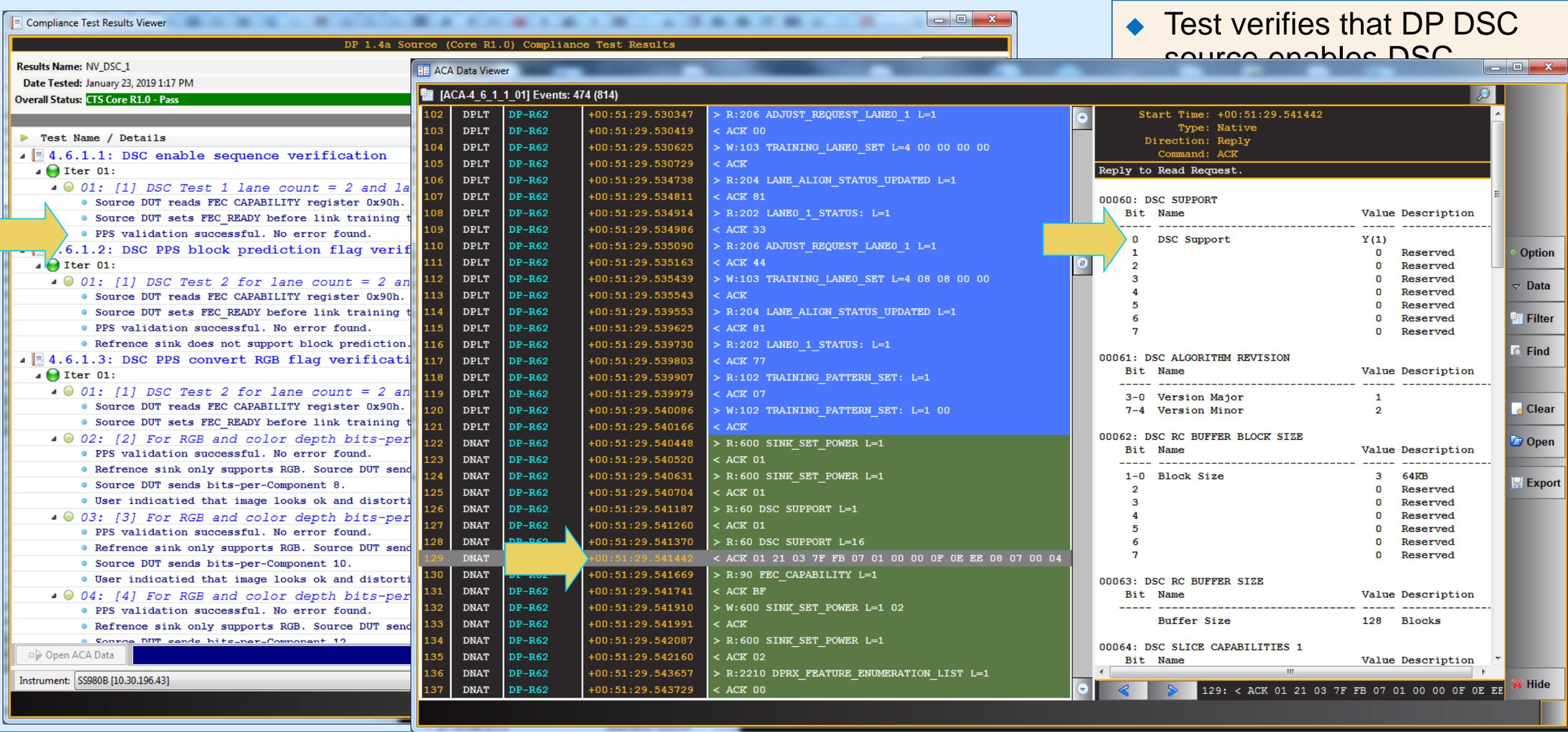
# DSC Source Compliance – Test Selection - Test 4.5.1.1 DSC Enable Sequence



- ◆ Selecting the DSC Source tests to run.

# Source Display Stream Compression Compliance Test – Test 4.6.1.1 - 1

- ◆ Test verifies that DP DSC source enables DSC



# **Source Display Stream Compression Compliance Test – Test 4.6.1.1 - 2**

- ◆ Test verifies that DP DSC enables DSC properly

The figure shows two windows from a test results viewer. The main window is titled "DP 1.4a Source (Core R1.0) Compliance Test Results" and displays test results for "NV\_DSC\_1" tested on January 23, 2019, at 1:17 PM, with an overall status of "CTS Core R1.0 - Pass". The left pane lists test cases for DSC enable sequence verification, PPS block prediction flag verification, and RGB conversion. The right pane, titled "ACA Data Viewer", shows a timeline of events. A yellow arrow points from the "DSC enable sequence verification" section in the main window to event 216 in the ACA Data Viewer, which is a "R:206 ADJUST\_REQUEST\_LANE0\_1 L=1" message. Another yellow arrow points from the "DSC ENABLE" row in the ACA Data Viewer details panel to event 230, which is a "W:160 DSC\_ENABLE L=1 01" message. The ACA Data Viewer also includes a details panel for the selected event, showing fields like Start Time, Type, Direction, Command, Address, Length, Bit Name, Value, and Description.

# Source Display Stream Compression Compliance Test – Test 4.6.1.1 - 3

◆ Test verifies that DP DSC enables DSC properly.

The screenshot displays two windows related to DP 1.4a Source Compliance Test Results:

- Compliance Test Results Viewer:** Shows the results for NV\_DSC\_1, tested on January 23, 2019, at 1:17 PM. The overall status is CTS Core R1.0 - Pass. It lists test cases for DSC enable sequence verification, DSC PPS block prediction flag verification, and DSC PPS convert RGB flag verification, all of which pass.
- DP Capture Viewer:** Shows a timeline of frames (BS, BF, SS) and a Picture Parameter Set (PPS) structure. The timeline includes markers for Link Clock # 1476516, 1476531, 1476547, 1476563, and 1476579. A yellow arrow points from the viewer's timeline to the PPS structure. Another yellow arrow points from the PPS structure to the detailed list of frame types and their timestamps.
- Detailed Frame List:** A table below the timeline lists frame details by Link Clock # and TimeStamp. It includes columns for #, Link Clock #, TimeStamp, and Type. The table shows various frame types (SS, SE, BS, BF, BS Data) and their corresponding timestamps.
- Picture Parameter Set (PPS) Details:** A detailed view of the PPS structure, listing parameters such as Packet ID, dsc\_version major, dsc\_version minor, pps\_identifier, bits\_per\_component, linebuf\_depth, block\_pred\_enable, convert\_rgb, simple\_422, vbr\_enable, native\_420, native\_422, and bits\_per\_pixel.
- Hex Dump:** A hex dump of the PPS structure, showing byte values for Lane 0 through Lane 3.

# DisplayPort DSC Compliance Basic Interop – DSC Transport Sink Testing

DP 1.4 Reference Source  
Example: Teledyne LeCroy  
quantumdata 980 Test Platform  
with DP 1.4 Video Generator /  
Protocol Analyzer



DisplayPort DSC-Capable  
Sink DUT (Monitor/TV)



DisplayPort Cable

# DSC Sink Compliance Testing – List of Tests

DP 1.4a DSC Sink CT R1.0

Instrument: SS980B [10.30.196.70]

CDF Entry  Test Selection

Test List

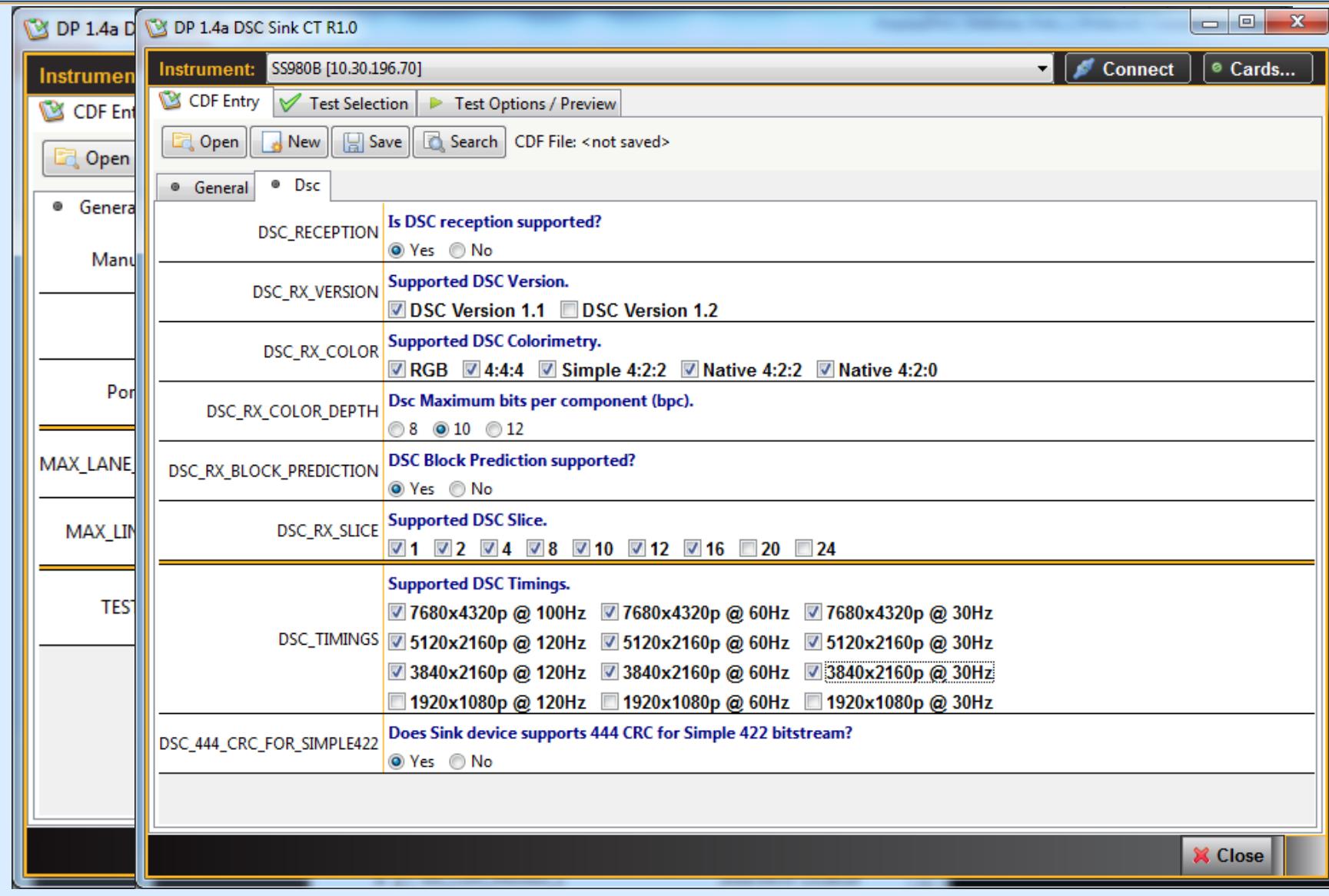
All  Count  Options

Category / Test Name

Dsc

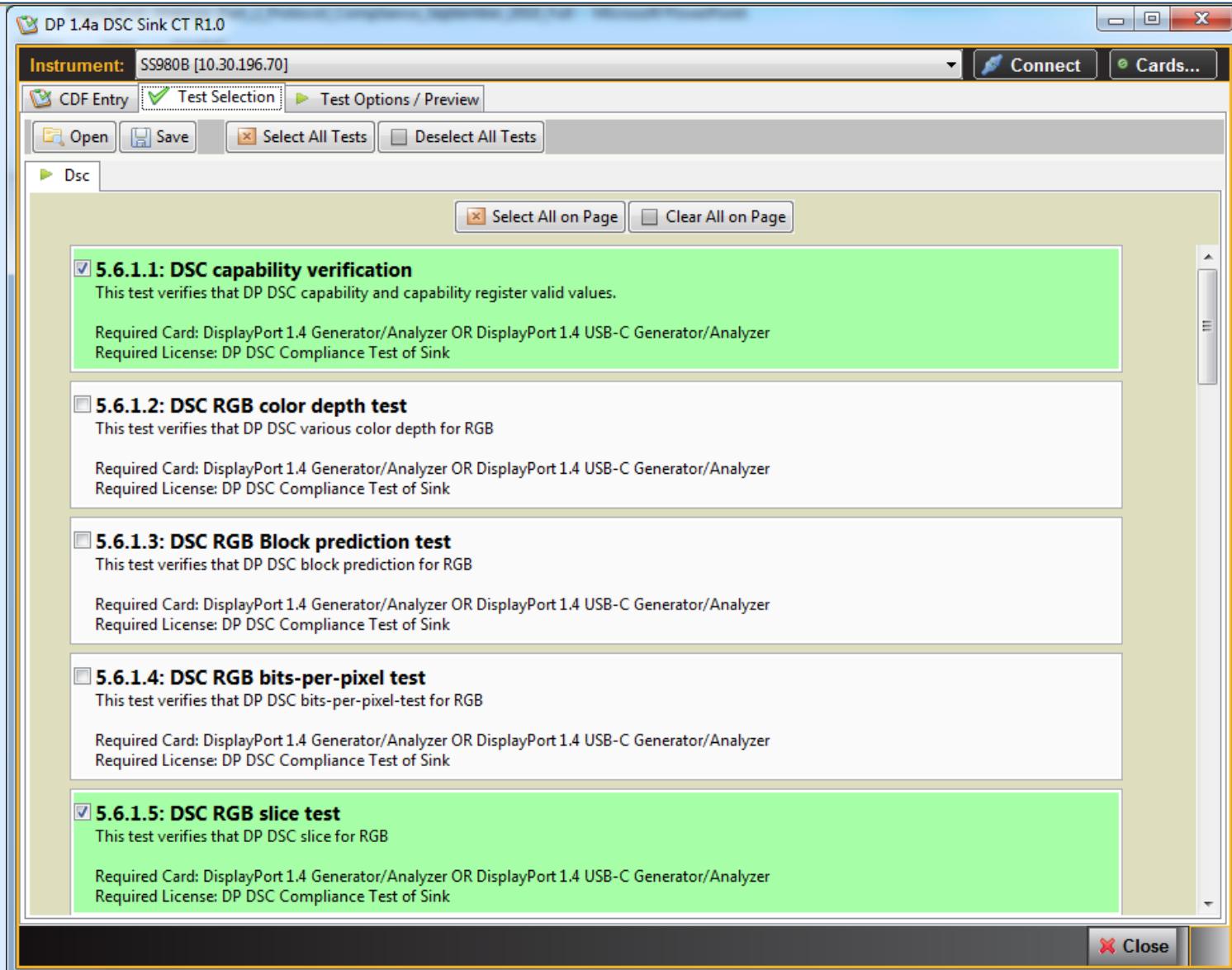
Test Description	Status
5.6.1.1: DSC capability verification	✓
5.6.1.2: DSC RGB color depth test	✓
5.6.1.3: DSC RGB Block prediction test	✓
5.6.1.4: DSC RGB bits-per-pixel test	✓
5.6.1.5: DSC RGB slice test	✓
5.6.1.6: DSC RGB lanes test	✓
5.6.1.7: DSC YCbCr 4:4:4 color depth test	✓
5.6.1.8: DSC YCbCr 4:4:4 Block prediction test	✓
5.6.1.9: DSC YCbCr 4:4:4 bits-per-pixel test	✓
5.6.1.10: DSC YCbCr 4:4:4 slice test	✓
5.6.1.11: DSC YCbCr 4:4:4 lanes test	✓
5.6.1.12: DSC Simple 4:2:2 color depth test	✓
5.6.1.13: DSC Simple 4:2:2 Block prediction test	✓
5.6.1.14: DSC Simple 4:2:2 bits-per-pixel test	✓
5.6.1.15: DSC Simple 4:2:2 slice test	✓
5.6.1.16: DSC Simple 4:2:2 lanes test	✓
5.6.1.17: DSC Native 4:2:2 color depth test	✓
5.6.1.18: DSC Native 4:2:2 Block prediction test	✓
5.6.1.19: DSC Native 4:2:2 bits-per-pixel-test	✓
5.6.1.20: DSC Native 4:2:2 slice test	✓
5.6.1.21: DSC Native 4:2:2 lanes test	✓
5.6.1.22: DSC Native 4:2:0 color depth test	✓
5.6.1.23: DSC Native 4:2:0 Block prediction test	✓
5.6.1.24: DSC Native 4:2:0 bits-per-pixel test	✓
5.6.1.25: DSC Native 4:2:0 slice test	✓
5.6.1.26: DSC Native 4:2:0 lanes test	✓

# Entering the CDF Information – Source DSC Capabilities



- ◆ Capabilities Declaration Form (CDF) must be filled out prior to the running the test.
- ◆ CDF is used by the reference sink to know which Link Layer related sink features to test.
- ◆ DSC – Described DSC capabilities of the source device.

# DSC Source Compliance – Test Selection - Test 5.6.1.1 DSC Enable Sequence



- ◆ Selecting the DSC Source tests to run.

# Sink Display Stream Compression Compliance Test – Test 5.6.1.1 - 1

The screenshot displays two windows from a test environment:

- Compliance Test Results Viewer:** Shows the "DP 1.4a DSC Sink (R1.0) Compliance Test Results".
  - Results Name: DSC\_sink\_test
  - Date Tested: May 21, 2019 4:26 PM
  - Overall Status: CTS R1.0 - Pass
- ACA Data Viewer:** Shows a timeline of events and a detailed view of a specific event.
  - Timeline View:** [ACA-5\_1\_1\_01] Events: 4 (68)

Index	DNAT	DP-T30	Time	Message
0	DNAT	DP-T30	+02:00	> R:90 FEC_CAPABILITY L=1
1	DNAT	DP-T30	+02:00	< ACK BF
2	DNAT	DP-T30	+02:00:52.21886	> R:60 DSC SUPPORT L=16
3	DNAT	DP-T30	+02:00:52.219132	< ACK 01 21 00 02 2B 04 01 00 00 1F 0E 61 08 00 ...
  - Detailed View:** Event 00090: FEC\_CAPABILITY
    - Start Time: +02:00:52.218735
    - Type: Native
    - Direction: Reply
    - Command: ACK
    - Description: Reply to Read Request.
    - Bit Description Table:

Bit	Name	Value	Description
0	FEC_CAPABLE	Y(1)	
1	UNCORRECTED_BLOCK_ERR_CNT_CAP	Y(1)	
2	CORRECTED_BLOCK_ERR_CNT_CAP	Y(1)	
3	BIT_ERROR_COUNT_CAPABLE	Y(1)	
4		1	Reserved
5		1	Reserved
6		0	Reserved
7		1	Reserved

Yellow arrows point from the highlighted event in the timeline to the detailed view of the FEC\_CAPABILITY message.

- ◆ Test Verifies that the DP DSC sink properly sets the DSC capability bit in the DPCD registers.
- ◆ Test also verifies FEC

# Sink Display Stream Compression Compliance Test – Test 5.6.1.1 - 2

The screenshot displays two windows related to a DP 1.4a DSC Sink (R1.0) Compliance Test.

**Compliance Test Results Viewer:**

- Results Name: DSC\_sink\_test
- Date Tested: May 21, 2019 4:26 PM
- Overall Status: CTS R1.0 - Pass
- Test Name / Details:
  - 5.6.1.1: DSC capability verification
    - Iter 01:
      - 01: Verify DSC capability.
        - DSC and FEC both supported by Sink DUT.
        - All DSC capability registers (60h-6Fh) are valid and as per specification.
    - 5.6.1.2: DSC RGB color depth test
    - 5.6.1.4: DSC RGB bits-per-pixel test

- ◆ Test Verifies that the DP DSC sink properly sets the DSC capability bit in

**ACA Data Viewer:**

[ACA-5\_6\_1\_1\_01] Events: 4 (68)

Index	Event Type	Timestamp	Message
0	DNAT	DP-T30	+02:00:52.218411 > R:90 FEC_CAPABILITY L=1
1	DNAT	DP-T30	+02:00:52.218735 < ACK BF
2	DNAT	DP-T30	+02:00:52.218891 > R:60 DSC SUPPORT L=16
3	DNAT	DP-T30	+02:00:52.218913 < ACK 01 21 00 02 2B 04 01 00 00 1F 0E 61 08 00 0...

Start Time: +02:00:52.219132  
Type: Native  
Direction: Reply  
Command: ACK  
Reply to Read Request.

00060: DSC SUPPORT

Bit Name	Value Description
0 DSC Support	Y(1)
1	0 Reserved
2	0 Reserved
3	0 Reserved
4	0 Reserved
5	0 Reserved
6	0 Reserved
7	0 Reserved

00061: DSC ALGORITHM REVISION

Bit Name	Value Description
3-0 Version Major	1
7-4 Version Minor	2

00062: DSC RC BUFFER BLOCK SIZE

Bit Name	Value Description
1-0 Block Size	0 1KB
2	0 Reserved
3	0 Reserved
4	0 Reserved
5	0 Reserved
6	0 Reserved
7	0 Reserved

00063: DSC RC BUFFER SIZE

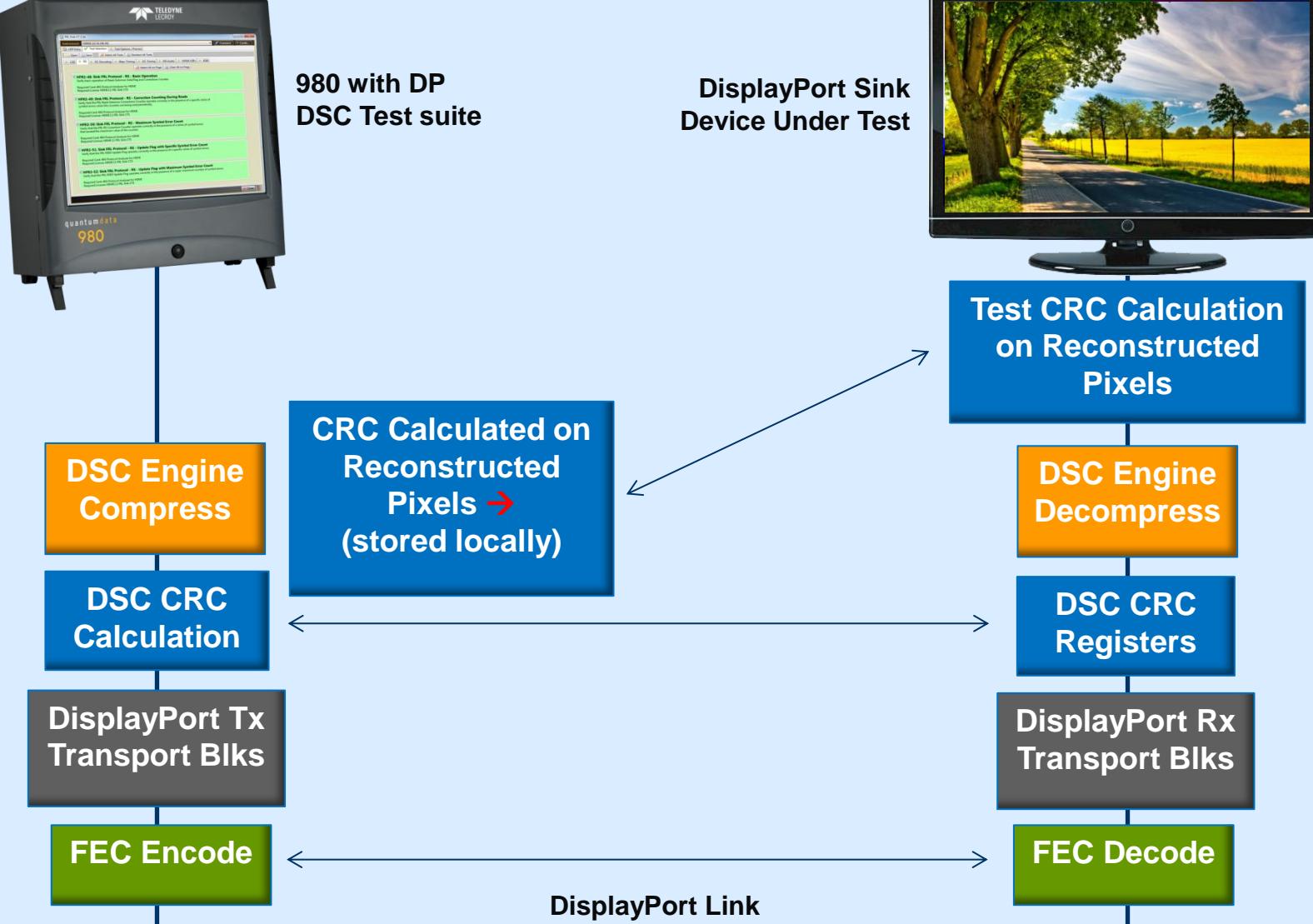
Bit Name	Value Description
Buffer Size	3 Blocks

00064: DSC SLICE CAPABILITIES 1

Bit Name	Value Description
0 1 Slice	Y(1)
1 2 Slices	Y(1)

Instrument: SS980B [10.30.196.43]

# Sink Display Stream Compression Compliance Test – CRC Checks



- ◆ DisplayPort DCS Compliance testing uses CRC checks to verify the DSC transport layer.
- ◆ FEC verifies transport across the DisplayPort link.
- ◆ DSC CRCs verify the transport through the DisplayPort functional blocks. →
- ◆ Test CRCs verify the DSC compression.
- ◆ How does CRC work?
  - ◆ CRC use a Checksum which is computed & append it to the data.
  - ◆ CRC Checksums are computed by dividing the data by a “CRC Polynomial” and using the remainder as the CRC Checksum.
  - ◆ The binary numbers of the data are the coefficients in the polynomial.
  - ◆ Finite Fields and polynomials are used to avoid duplicate remainders.

# Sink Display Stream Compression Compliance Test – Test 5.6.1.2 - 1

Compliance Test Results Viewer

DP 1.4a DSC Sink (R1.0) Compliance Test Results

Results Name: DSC\_sink\_test  
Date Tested: May 21, 2019 4:26 PM  
Overall Status: CTS R1.0 - Pass

Test Name / Details

5.6.1.1: DSC capability verification

Iter 01:

5.6.1.2: DSC RGB color depth test

Iter 01:

- 01: Initial Link Training at maximum link rate and
- 02: For Timing 1920x1080p@30Hz, Color Depth 8, CRC
- 03: For Timing 1920x1080p@30Hz, Color Depth 10, CR
- After Sending DSC image 2kClrSq.dpx, Timing 1920x1080p@30Hz,
- Slice-Width=960, Slice-Height=1080, Bits-per-component=10, Bi
- TEST\_CRC\_R\_Cr 0xBFA8 matched with expected value.
- TEST\_CRC\_G\_Y 0x714D matched with expected value.
- TEST\_CRC\_B\_Cb 0xB496 matched with expected value.
- DSC\_CRC\_0 0x0065 matched with expected value.
- DSC\_CRC\_1 0x7DD3 matched with expected value.
- DSC\_CRC\_2 0x4245 matched with expected value.
- 04: For Timing 1920x1080p@30Hz, Color Depth 12, CR
- 05: For Timing 1920x1080p@60Hz, Color Depth 8, CRC
- 06: For Timing 1920x1080p@60Hz, Color Depth 10, CR
- 07: For Timing 1920x1080p@60Hz, Color Depth 12, CR
- 08: For Timing 3840x2160p@30Hz, Color Depth 8, CRC
- 09: For Timing 3840x2160p@30Hz, Color Depth 10, CR
- 10: For Timing 3840x2160p@30Hz, Color Depth 12, CR
- 11: For Timing 3840x2160p@60Hz, Color Depth 8, CRC
- 12: For Timing 3840x2160p@60Hz, Color Depth 10, CR
- 13: For Timing 3840x2160p@60Hz, Color Depth 12, CR
- 14: For Timing 3840x2160p@120Hz, Color Depth 8, CR
- 15: For Timing 3840x2160p@120Hz, Color Depth 10, C
- 16: For Timing 3840x2160p@120Hz, Color Depth 12, C
- 17: For Timing 5120x2160p@30Hz, Color Depth 8, CRC
- 18: For Timing 5120x2160p@30Hz, Color Depth 10, CR
- 19: For Timing 5120x2160p@30Hz, Color Depth 12, CR

Open ACA Data

Instrument: SS980B [10.30.196.43]

ACA Data Viewer

[ACA-5\_6\_1\_2\_01] Events: 1612 (1676)

Event ID	Manufacturer	Port	Time	Message
1574	DNAT	DP-T30	+02:03:43.096321	> R:246 TEST_SINK_MISC L=1
1575	DNAT	DP-T30	+02:03:43.096645	< ACK 21
1576	DNAT	DP-T30	+02:03:43.096874	> R:240 TEST_CRC_R_CR L=6
1577	DNAT	DP-T30	+02:03:43.097198	< ACK C5 4A 62 66 4B 2E
1578	DNAT	DP-T30	+02:03:43.097326	> R:262 RESERVED L=6
1579	DNAT	DP-T30	+02:03:43.097650	< ACK 04 B8 27 12 30 3C
1580	DNAT	DP-T30	+02:03:43.097774	> W:270 TEST_SINK L=1 00
1581	DNAT	DP-T30	+02:03:43.098106	< ACK
1582	DPLT	DP-T30	+02:03:43.328848	> R:100 LINK_BW_SET L=2
1583	DPLT	DP-T30	+02:03:43.329171	< ACK 1E 84
1584	DPLT	DP-T30	+02:03:43.438714	> R:100 LINK_BW_SET L=2
1585	DPLT	DP-T30	+02:03:43.439038	< ACK 1E 84
1586	DNAT	DP-T30	+02:03:43.442744	> W:160 DSC_ENABLE L=1 01
1587	DNAT	DP-T30	+02:03:43.443075	< ACK
1588	DNAT	DP-T30	+02:03:47.578462	> W:270 TEST_SINK L=1 00
1589	DNAT	DP-T30	+02:03:47.578794	< ACK
1590	DNAT	DP-T30	+02:03:47.578859	> W:270 TEST_SINK L=1 01
1591	DNAT	DP-T30	+02:03:47.579191	< DEFER
1592	DNAT	DP-T30	+02:03:47.579740	> W:270 TEST_SINK L=1 01
1593	DNAT	DP-T30	+02:03:47.580071	< ACK
1594	DNAT	DP-T30	+02:03:48.560621	> R:246 TEST_SINK_MISC L=1
1595	DNAT	DP-T30	+02:03:48.560944	< ACK 21
1596	DNAT	DP-T30	+02:03:48.610148	> R:246 TEST_SINK_MISC L=1
1597	DNAT	DP-T30	+02:03:48.610471	< ACK 21
1598	DNAT	DP-T30	+02:03:48.659665	> R:246 TEST_SINK_MISC L=1
1599	DNAT	DP-T30	+02:03:48.659988	< ACK 21
1600	DNAT	DP-T30	+02:03:48.709181	> R:246 TEST_SINK_MISC L=1
1601	DNAT	DP-T30	+02:03:48.709505	< ACK 21
1602	DNAT	DP-T30	+02:03:48.758658	> R:246 TEST_SINK_MISC L=1
1603	DNAT	DP-T30	+02:03:48.758981	< ACK 21
1604	DNAT	DP-T30	+02:03:48.808171	> R:246 TEST_SINK_MISC L=1
1605	DNAT	DP-T30	+02:03:48.808473	< ACK 21
1606	DNAT	DP-T30	+02:03:48.809060	> R:240 TEST_CRC_R_CR L=6
1607	DNAT	DP-T30	+02:03:48.809188	< ACK D6 17 37 C6 ED 2F
1608	DNAT	DP-T30	+02:03:48.809188	> R:262 RESERVED L=6
1609	DNAT	DP-T30	+02:03:48.809512	< ACK E6 BA ED 07 3F D6
1610	DNAT	DP-T30	+02:03:48.809637	> W:270 TEST_SINK L=1 00
1611	DNAT	DP-T30	+02:03:48.809969	< ACK

Start Time: +02:03:48.808501  
Type: Native  
Direction: Reply  
Command: ACK  
Reply to Read Request.

00246: TEST\_SINK\_MISC

Bit	Name	Value	Description
3-0	TEST_CRC_COUNT	1	
4		0	Reserved
5	TEST_CRC_SUPPORTED	Y(1)	
6		0	Reserved
7		0	Reserved

[0000][00 21 -- -- -- -- --] [..] ]

Option

Data

Filter

Find

Clear

Open

Export

Hide

◆ Test verifies Sink DUT can render DSC images

# Sink Display Stream Compression Compliance Test – Test 5.6.1.2 - 2

Compliance Test Results Viewer

DP 1.4a DSC Sink (R1.0) Compliance Test Results

Results Name: DSC\_sink\_test  
Date Tested: May 21, 2019 4:26 PM  
Overall Status: CTS R1.0 - Pass

Manufacturer: Model Name: Port Tested: 1

Test Name / Details

5.6.1.1: DSC capability verification

5.6.1.2: DSC RGB color depth test

Iter 01:

- 01: Initial Link Training at maximum link rate and lane count.
- 02: For Timing 1920x1080p@30Hz, Color Depth 8, CRC check.
- 03: For Timing 1920x1080p@30Hz, Color Depth 10, CRC check.
- After Sending DSC image 2kClrSq.dpx, Timing 1920x1080p@30Hz, Color RGB.
- Slice-Width=960, Slice-Height=1080, Bits-per-component=10, Bits-per-pixel=30.
- TEST\_CRC\_R\_Cr 0xBFA8 matched with expected value.
- TEST\_CRC\_G\_Y 0x714D matched with expected value.
- TEST\_CRC\_B\_Cb 0xB496 matched with expected value.
- DSC\_CRC\_0 0x0065 matched with expected value.
- DSC\_CRC\_1 0x7DD3 matched with expected value.
- DSC\_CRC\_2 0x4245 matched with expected value.
- 04: For Timing 1920x1080p@30Hz, Color Depth 12, CRC check.
- 05: For Timing 1920x1080p@60Hz, Color Depth 8, CRC check.
- 06: For Timing 1920x1080p@60Hz, Color Depth 10, CRC check.
- 07: For Timing 1920x1080p@60Hz, Color Depth 12, CRC check.
- 08: For Timing 3840x2160p@30Hz, Color Depth 8, CRC check.
- 09: For Timing 3840x2160p@30Hz, Color Depth 10, CRC check.
- 10: For Timing 3840x2160p@30Hz, Color Depth 12, CRC check.
- 11: For Timing 3840x2160p@60Hz, Color Depth 8, CRC check.
- 12: For Timing 3840x2160p@60Hz, Color Depth 10, CRC check.
- 13: For Timing 3840x2160p@60Hz, Color Depth 12, CRC check.
- 14: For Timing 3840x2160p@120Hz, Color Depth 8, CRC check.
- 15: For Timing 3840x2160p@120Hz, Color Depth 10, CRC check.
- 16: For Timing 3840x2160p@120Hz, Color Depth 12, CRC check.
- 17: For Timing 5120x2160p@30Hz, Color Depth 8, CRC check.
- 18: For Timing 5120x2160p@30Hz, Color Depth 10, CRC check.
- 19: For Timing 5120x2160p@30Hz, Color Depth 12, CRC check.

Open ACA Data 5.6.1.1: DSC capability verification

Instrument: SS980B [10.30.196.43]

ACA Data Viewer

[ACA-5\_6\_1\_2\_01] Events: 1676

Event ID	Port	Event Type	Timestamp	Message
1641	DNAT	DP-T30	+02:03:43.097198	< ACK C5 4A 62 66 4B 2E
1642	DNAT	DP-T30	+02:03:43.097326	> R:262 RESERVED L=6
1643	DNAT	DP-T30	+02:03:43.097650	< ACK 04 B8 27 12 30 3C
1644	DNAT	DP-T30	+02:03:43.097774	> W:270 TEST_SINK L=1 00
1645	DNAT	DP-T30	+02:03:43.098106	< ACK
1646	DPLT	DP-T30	+02:03:43.328848	> R:100 LINK_BW_SET L=2
1647	DPLT	DP-T30	+02:03:43.329171	< ACK 1E 84
1648	DPLT	DP-T30	+02:03:43.438714	> R:100 LINK_BW_SET L=2
1649	DPLT	DP-T30	+02:03:43.439038	< ACK 1E 84
1650	DNAT	DP-T30	+02:03:43.442744	> W:160 DSC_ENABLE L=1 01
1651	DNAT	DP-T30	+02:03:43.443075	< ACK
1652	DNAT	DP-T30	+02:03:47.578462	> W:270 TEST_SINK L=1 00
1653	DNAT	DP-T30	+02:03:47.578794	< ACK
1654	DNAT	DP-T30	+02:03:47.578859	> W:270 TEST_SINK L=1 01
1655	DNAT	DP-T30	+02:03:47.579191	< DEFER
1656	DNAT	DP-T30	+02:03:47.579740	> W:270 TEST_SINK L=1 01
1657	DNAT	DP-T30	+02:03:47.580071	< ACK
1658	DNAT	DP-T30	+02:03:48.560621	> R:246 TEST_SINK_MISC L=1
1659	DNAT	DP-T30	+02:03:48.560944	< ACK 21
1660	DNAT	DP-T30	+02:03:48.610148	> R:246 TEST_SINK_MISC L=1
1661	DNAT	DP-T30	+02:03:48.610471	< ACK 21
1662	DNAT	DP-T30	+02:03:48.659665	> R:246 TEST_SINK_MISC L=1
1663	DNAT	DP-T30	+02:03:48.659988	< ACK 21
1664	DNAT	DP-T30	+02:03:48.709181	> R:246 TEST_SINK_MISC L=1
1665	DNAT	DP-T30	+02:03:48.709505	< ACK 21
1666	DNAT	DP-T30	+02:03:48.758658	> R:246 TEST_SINK_MISC L=1
1667	DNAT	DP-T30	+02:03:48.758981	< ACK 21
1668	DNAT	DP-T30	+02:03:48.808178	> R:246 TEST_SINK_MISC L=1
1669	DNAT	DP-T30	+02:03:48.808501	< ACK 21
1670	DNAT	DP-T30	+02:03:48.808737	> R:240 TEST_CRC_R_CR L=6
1671	DNAT	DP-T30	+02:03:48.809060	< ACK D6 17 37 C6 ED 2F
1672	DNAT	DP-T30	+02:03:48.809188	> R:262 RESERVED L=6
1673	DNAT	DP-T30	+02:03:48.809512	< ACK E6 BA ED 07 3F D6
1674	DNAT	DP-T30	+02:03:48.809637	> W:270 TEST_SINK L=1 00
1675	DNAT	DP-T30	+02:03:48.809969	< ACK

Start Time: +02:03:48.809060  
Type: Native  
Direction: Reply  
Command: ACK  
Reply to Read Request.

00240: TEST\_CRC\_R\_CR  
CRC: 17D6h (6102)

00242: TEST\_CRC\_G\_Y  
CRC: C637h (50743)

00244: TEST\_CRC\_B\_CB  
CRC: 2FEDh (12269)

[0000] [00 D6 17 37 C6 ED 2F --] [...] 7... ]

Option Data Filter Find Clear Open Export Hide

1671: < ACK D6 17 37 C6 ED 2F

◆ Test verifies Sink DUT

# Sink Display Stream Compression Compliance Test – Test 5.6.1.5 - 1

◆ Test verifies Sink DUT

Compliance Test Results Viewer  
DP 1.4a Sink (C)  
Results Name: AA\_DSC\_All  
Date Tested: January 24, 2019 9:02 PM  
Overall Status: CTS Core R1.0 - Incomplete

Test Name / Details  
5.6.1.5: DSC RGB slice test  
Iter 01:  
01: Initial Link Training at maximum link rate  
02: CRC check or Visual check during DSC image transfer  
03: CRC check or Visual check during DSC image transfer  
04: CRC check or Visual check during DSC image transfer  
05: CRC check or Visual check during DSC image transfer  
06: CRC check or Visual check during DSC image transfer  
07: CRC check or Visual check during DSC image transfer  
08: CRC check or Visual check during DSC image transfer  
09: CRC check or Visual check during DSC image transfer  
10: CRC check or Visual check during DSC image transfer  
11: CRC check or Visual check during DSC image transfer  
12: CRC check or Visual check during DSC image transfer  
13: CRC check or Visual check during DSC image transfer  
After Sending RGB DSC image with Color Depth 12, n  
TEST\_CRC\_R\_Cr (0x515A).  
TEST\_CRC\_G\_Y (0x7EA6).  
TEST\_CRC\_B\_Cb (0x23EB).  
DSC\_CRC\_0 (0x0000).  
DSC\_CRC\_1 (0x0000).  
DSC\_CRC\_2 (0x0000).  
User confirmed that displayed test pattern PASS

5.6.1.6: DSC RGB lanes test  
5.6.1.7: DSC YCbCr 4:4:4 color depth test  
5.6.1.8: DSC YCbCr 4:4:4 Block prediction test  
5.6.1.9: DSC YCbCr 4:4:4 bits-per-pixel-test  
5.6.1.10: DSC YCbCr 4:4:4 slice test  
5.6.1.11: DSC YCbCr 4:4:4 lanes test  
5.6.1.12: DSC Simple 4:2:2 color depth test  
5.6.1.13: DSC Simple 4:2:2 Block prediction

Open ACA Data 13: CRC check or Visual check during DSC image color Depth 12, n  
Instrument: SS980B [10.30.196.43]

ACA Data Viewer  
[ACA-5.6.1.5\_01] Events: 5848 (5976)

Event ID	Event Type	Timestamp	Event Description	
0	DNAT	DP-T60	+00:05:46.294165	> R:246 TEST_SINK_MISC L=1
1	DNAT	DP-T60	+00:05:46.294489	< ACK 21
2	DNAT	DP-T60	+00:05:46.294555	> R:60 DSC SUPPORT L=16
3	DNAT	DP-T60	+00:05:46.295111	< ACK 01 21 00 02 2B 04 01 00 00 1F 0E 61 08 00 ...
4	DNAT	DP-T60	+00:05:46.295111	> R:E TRAINING_AUX_RD_INTERVAL L=1
5	DNAT	DP-T60	+00:05:46.295436	< ACK 84
6	DNAT	DP-T60	+00:05:46.295519	> W:600 SINK_SET_POWER L=1 02
7	DNAT	DP-T60	+00:05:46.295851	< ACK
8	DNAT	DP-T60	+00:05:46.786211	> W:600 SINK_SET_POWER L=1 01
9	DNAT	DP-T60	+00:05:46.786542	< ACK
10	DNAT	DP-T60	+00:05:46.787650	> R:2201 MAX_LINK_RATE L=1
11	DNAT	DP-T60	+00:05:46.787973	< ACK 1E
12	DNAT	DP-T60	+00:05:46.788049	> R:2202 MAX_LANE_COUNT L=1
13	DNAT	DP-T60	+00:05:46.788372	< ACK C4
14	DNAT	DP-T60	+00:05:46.789531	> R:200 SINK_COUNT L=6
15	DNAT	DP-T60	+00:05:46.789855	< ACK 41 00 77 77 81 02
16	DNAT	DP-T60	+00:05:46.789996	> R:E TRAINING_AUX_RD_INTERVAL L=1
17	DNAT	DP-T60	+00:05:46.790319	< ACK 84
18	DNAT	DP-T60	+00:05:46.790388	> R:0 DPCD_REV L=1
19	DNAT	DP-T60	+00:05:46.790711	< ACK 12
20	DNAT	DP-T60	+00:05:46.790781	> R:2200 DP1.3_DPCD_REV L=16
21	DNAT	DP-T60	+00:05:46.791105	< ACK 14 1E C4 81 01 01 01 01 80 02 00 06 00 00 00 ...
22	DNAT	DP-T60	+00:05:46.791311	> R:2002 SINK_COUNT_ESI L=4
23	DNAT	DP-T60	+00:05:46.791634	< ACK 41 00 00 00
24	DNAT	DP-T60	+00:05:46.791730	> R:90 FEC_CAPABILITY L=1
25	DNAT	DP-T60	+00:05:46.792054	< ACK BF
26	DNAT	DP-T60	+00:05:46.792123	> R:60 DSC SUPPORT L=15
27	DNAT	DP-T60	+00:05:46.792447	< ACK 01 21 00 02 2B 04 01 00 00 1F 0E 61 08 00 00
28	DNAT	DP-T60	+00:05:46.792688	> W:10A eDP_CONFIGURATION_SET L=1 00
29	DNAT	DP-T60	+00:05:46.793019	< ACK
30	DNAT	DP-T60	+00:05:46.793078	> W:120 FEC_CONFIGURATION L=1 01
31	DNAT	DP-T60	+00:05:46.793410	< ACK
32	DNAT	DP-T60	+00:05:46.793470	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
33	DNAT	DP-T60	+00:05:46.793794	< DEFER
34	DNAT	DP-T60	+00:05:46.794324	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
35	DNAT	DP-T60	+00:05:46.794648	< DEFER
36	DNAT	DP-T60	+00:05:46.795171	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1

DTC Name Value Description  
0 DSC Support Y(1)  
1 Reserved 0  
2 Reserved 0  
3 Reserved 0  
4 Reserved 0  
5 Reserved 0  
6 Reserved 0  
7 Reserved 0

00061: DSC ALGORITHM REVISION  
Bit Name Value Description  
3-0 Version Major 1  
7-4 Version Minor 2

00062: DSC RC BUFFER BLOCK SIZE  
Bit Name Value Description  
1-0 Block Size 0 1KB  
2 Reserved 0  
3 Reserved 0  
4 Reserved 0  
5 Reserved 0  
6 Reserved 0  
7 Reserved 0

00063: DSC RC BUFFER SIZE  
Bit Name Value Description  
Buffer Size 3 Blocks

00064: DSC SLICE CAPABILITIES 1  
Bit Name Value Description  
0 1 Slice Y(1)  
1 2 Slices Y(1)  
2 Reserved 0  
3 4 Slices Y(1)  
4 6 Slices N(0)  
5 8 Slices Y(1)  
6 10 Slices N(0)  
7 12 Slices N(0)

Instrument: SS980B [10.30.196.43]

# Sink Display Stream Compression Compliance Test – Test 5.6.1.5 - 2

◆ Test verifies Sink DUT

The screenshot displays two windows related to a compliance test:

- Compliance Test Results Viewer (Left Window):**
  - Results Name:** AA\_DSC\_All
  - Date Tested:** January 24, 2019 9:02 PM
  - Overall Status:** CTS Core R1.0 - Incomplete
  - Test Name / Details:**
    - 5.6.1.5: DSC RGB slice test
      - Iter 01:
        - 01: Initial Link Training at maximum link
        - 02: CRC check or Visual check during DSC
        - 03: CRC check or Visual check during DSC
        - 04: CRC check or Visual check during DSC
        - 05: CRC check or Visual check during DSC
        - 06: CRC check or Visual check during DSC
        - 07: CRC check or Visual check during DSC
        - 08: CRC check or Visual check during DSC
        - 09: CRC check or Visual check during DSC
        - 10: CRC check or Visual check during DSC
        - 11: CRC check or Visual check during DSC
        - 12: CRC check or Visual check during DSC
        - 13: CRC check or Visual check during DSC
          - After Sending RGB DSC image with Color Depth 12,
          - TEST\_CRC\_R\_Cr (0x515A).
          - TEST\_CRC\_G\_Y (0x7EA6).
          - TEST\_CRC\_B\_Cb (0x23EB).
          - DSC\_CRC\_0 (0x0000).
          - DSC\_CRC\_1 (0x0000).
          - DSC\_CRC\_2 (0x0000).
          - User confirmed that displayed test pattern PASS v
    - 5.6.1.6: DSC RGB lanes test
    - 5.6.1.7: DSC YCbCr 4:4:4 color depth test
    - 5.6.1.8: DSC YCbCr 4:4:4 Block prediction tes
    - 5.6.1.9: DSC YCbCr 4:4:4 bits-per-pixel-test
    - 5.6.1.10: DSC YCbCr 4:4:4 slice test
    - 5.6.1.11: DSC YCbCr 4:4:4 lanes test
    - 5.6.1.12: DSC Simple 4:2:2 color depth test
    - 5.6.1.13: DSC Simple 4:2:2 Block prediction t
  - Open ACA Data** button
  - Instrument:** SS980B [10.30.196.43]
- ACA Data Viewer (Right Window):**
  - [ACA-5\_6\_1\_5\_01] Events: 5848 (5976)**
  - Event Log (List View):
 

Index	Source	Destination	Timestamp	Message
0	DNAT	DP-T60	+00:05:46.294165	> R:246 TEST_SINK_MISC L=1
1	DNAT	DP-T60	+00:05:46.294489	< ACK 21
2	DNAT	DP-T60	+00:05:46.294557	> R:60 DSC SUPPORT L=16
3	DNAT	DP-T60	+00:05:46.295112	< ACK 01 21 00 02 2B 04 01 00 00 1F 0E 61 08 00 ...
4	DNAT	DP-T60	+00:05:46.295436	> R:E TRAINING_AUX_RD_INTERVAL L=1
5	DNAT	DP-T60	+00:05:46.295519	< ACK 84
6	DNAT	DP-T60	+00:05:46.295851	> W:600 SINK_SET_POWER L=1 02
7	DNAT	DP-T60	+00:05:46.295851	< ACK
8	DNAT	DP-T60	+00:05:46.786211	> W:600 SINK_SET_POWER L=1 01
9	DNAT	DP-T60	+00:05:46.786542	< ACK
10	DNAT	DP-T60	+00:05:46.787650	> R:2201 MAX_LINK_RATE L=1
11	DNAT	DP-T60	+00:05:46.787973	< ACK 1E
12	DNAT	DP-T60	+00:05:46.788049	> R:2202 MAX_LANE_COUNT L=1
13	DNAT	DP-T60	+00:05:46.788372	< ACK C4
14	DNAT	DP-T60	+00:05:46.789531	> R:200 SINK_COUNT L=6
15	DNAT	DP-T60	+00:05:46.789855	< ACK 41 00 77 77 81 02
16	DNAT	DP-T60	+00:05:46.789996	> R:E TRAINING_AUX_RD_INTERVAL L=1
17	DNAT	DP-T60	+00:05:46.790319	< ACK 84
18	DNAT	DP-T60	+00:05:46.790388	> R:0 DPCD_REV L=1
19	DNAT	DP-T60	+00:05:46.790711	< ACK 12
20	DNAT	DP-T60	+00:05:46.790781	> R:2200 DP1.3_DPCD_REV L=16
21	DNAT	DP-T60	+00:05:46.791105	< ACK 14 1E C4 81 01 01 01 80 02 00 06 00 00 00 ...
22	DNAT	DP-T60	+00:05:46.791311	> R:2002 SINK_COUNT_BSI L=4
23	DNAT	DP-T60	+00:05:46.791634	< ACK 41 00 00 00
24	DNAT	DP-T60	+00:05:46.791730	> R:90 FEC_CAPABILITY L=1
25	DNAT	DP-T60	+00:05:46.792054	< ACK BF
26	DNAT	DP-T60	+00:05:46.792123	> R:60 DSC SUPPORT L=15
27	DNAT	DP-T60	+00:05:46.792447	< ACK 01 21 00 02 2B 04 01 00 00 1F 0E 61 08 00 00
28	DNAT	DP-T60	+00:05:46.792688	> W:10A eDP_CONFIGURATION_SET L=1 00
29	DNAT	DP-T60	+00:05:46.793019	< ACK
30	DNAT	DP-T60	+00:05:46.793078	> W:120 FEC_CONFIGURATION L=1 01
31	DNAT	DP-T60	+00:05:46.793410	< ACK
32	DNAT	DP-T60	+00:05:46.793470	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
33	DNAT	DP-T60	+00:05:46.793794	< DEFER
34	DNAT	DP-T60	+00:05:46.794324	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
35	DNAT	DP-T60	+00:05:46.794648	< DEFER
36	DNAT	DP-T60	+00:05:46.795171	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
  - Configuration Tables (Right Side):**
    - 0006B: Peak DSC Throughput**

Bit	Name	Value	Description
3-0	Throughput Mode 0	1	340MP/s
7-4	Throughput Mode 1	6	600MP/s
    - 0006C: DSC Maximum Slice Width**

Bit	Name	Value	Description
Max Slice Width 2560 pixels			
    - 0006D: DSC SLICE CAPABILITIES 2**

Bit	Name	Value	Description
0	16 Slices	N(0)	
1	20 Slices	N(0)	
2	24 Slices	N(0)	
3		0	Reserved
4		0	Reserved
5		0	Reserved
6		0	Reserved
7		0	Reserved
    - 0006E: DSC MIN Bits per pixel (L)**

Bit	Name	Value	Description
7-0	bits_per_pixel7:0	0	
    - 0006F: DSC MIN Bits per pixel (H)**

Bit	Name	Value	Description
1-0	bits_per_pixel9:8	0	
2		0	Reserved
3		0	Reserved
6-4	Increment	0	1/16bpp
7		0	Reserved

## Sink Display Stream Compression Compliance Test – Test 5.6.1.5 - 3

- ◆ Test verifies Sink DUT

Compliance Test Results Viewer

DP 1.4a Sink (Core AA\_DSC\_All)

Results Name: AA\_DSC\_All  
Date Tested: January 24, 2019 9:02 PM  
Overall Status: CTS Core R1.0 - Incomplete

Test Name / Details

5.6.1.5: DSC RGB slice test

- Iter 01:
  - 01: Initial Link Training at maximum link rate
  - 02: CRC check or Visual check during DSC image
  - 03: CRC check or Visual check during DSC image
  - 04: CRC check or Visual check during DSC image
  - 05: CRC check or Visual check during DSC image
  - 06: CRC check or Visual check during DSC image
  - 07: CRC check or Visual check during DSC image
  - 08: CRC check or Visual check during DSC image
  - 09: CRC check or Visual check during DSC image
  - 10: CRC check or Visual check during DSC image
  - 11: CRC check or Visual check during DSC image
  - 12: CRC check or Visual check during DSC image
  - 13: CRC check or Visual check during DSC image
    - After Sending RGB DSC image with Color Depth 12, number of bytes sent: 5848 (5976)
    - TEST\_CRC\_R\_Cr (0x515A).
    - TEST\_CRC\_G\_Y (0x7EA6).
    - TEST\_CRC\_B\_Cb (0x23EB).
    - DSC\_CRC\_0 (0x0000).
    - DSC\_CRC\_1 (0x0000).
    - DSC\_CRC\_2 (0x0000).
    - User confirmed that displayed test pattern PASS visually.
- 5.6.1.6: DSC RGB lanes test
- 5.6.1.7: DSC YCbCr 4:4:4 color depth test
- 5.6.1.8: DSC YCbCr 4:4:4 Block prediction test
- 5.6.1.9: DSC YCbCr 4:4:4 bits-per-pixel-test
- 5.6.1.10: DSC YCbCr 4:4:4 slice test
- 5.6.1.11: DSC YCbCr 4:4:4 lanes test
- 5.6.1.12: DSC Simple 4:2:2 color depth test
- 5.6.1.13: DSC Simple 4:2:2 Block prediction test

Open ACA Data | 13: CRC check or Visual check during DSC image color Depth 12, number of bytes sent: 5848 (5976)

Instrument: SS980B [10.30.196.43]

ACA Data Viewer

[ACA-5\_6\_1\_5\_01] Events: 5848 (5976)

Index	Port	Action	Time	Details
5810	DNAT	DP-T60	+00:08:50.535581	> R:246 TEST_SINK_MISC L=1
5811	DNAT	DP-T60	+00:08:50.535904	< ACK 20
5812	DNAT	DP-T60	+00:08:50.536031	> R:246 TEST_SINK_MISC L=1
5813	DNAT	DP-T60	+00:08:50.536354	< ACK 20
5814	DNAT	DP-T60	+00:08:50.536479	> R:246 TEST_SINK_MISC L=1
5815	DNAT	DP-T60	+00:08:50.536802	< ACK 20
5816	DNAT	DP-T60	+00:08:50.538759	> W:270 TEST_SINK L=1 01
5817	DNAT	DP-T60	+00:08:50.539091	< ACK
5818	DNAT	DP-T60	+00:08:50.539402	> R:246 TEST_SINK_MISC L=1
5819	DNAT	DP-T60	+00:08:50.539726	< DEFER
5820	DNAT	DP-T60	+00:08:50.540238	> R:246 TEST_SINK_MISC L=1
5821	DNAT	DP-T60	+00:08:50.540561	< ACK 20
5822	DNAT	DP-T60	+00:08:50.540687	> R:246 TEST_SINK_MISC L=1
5823	DNAT	DP-T60	+00:08:50.541010	< ACK 20
5824	DNAT	DP-T60	+00:08:50.541134	> R:246 TEST_SINK_MISC L=1
5825	DNAT	DP-T60	+00:08:50.541457	< ACK 21
5826	DNAT	DP-T60	+00:08:50.541583	> R:246 TEST_SINK_MISC L=1
5827	DNAT	DP-T60	+00:08:50.541906	< ACK 21
5828	DNAT	DP-T60	+00:08:50.542032	> R:246 TEST_SINK_MISC L=1
5829	DNAT	DP-T60	+00:08:50.542355	< ACK 21
5830	DNAT	DP-T60	+00:08:50.542480	> R:246 TEST_SINK_MISC L=1
5831	DNAT	DP-T60	+00:08:50.542803	< ACK 21
5832	DNAT	DP-T60	+00:08:50.542929	> R:246 TEST_SINK_MISC L=1
5833	DNAT	DP-T60	+00:08:50.543252	< ACK 21
5834	DNAT	DP-T60	+00:08:50.543376	> R:246 TEST_SINK_MISC L=1
5835	DNAT	DP-T60	+00:08:50.543699	< ACK 21
5836	DNAT	DP-T60	+00:08:50.543825	> R:246 TEST_SINK_MISC L=1
5837	DNAT	DP-T60	+00:08:50.544148	< ACK 21
5838	DNAT	DP-T60	+00:08:50.544274	> R:246 TEST_SINK_MISC L=1
5839	DNAT	DP-T60	+00:08:50.544597	< ACK 21
5840	DNAT	DP-T60	+00:08:51.526998	> R:240 TEST_CRC_R_CR L=6
5841	DNAT	DP-T60	+00:08:51.527322	< ACK 5A 51 A6 7E EB 23
5842	DNAT	DP-T60	+00:08:51.527465	> R:262 RESERVED L=6
5843	DNAT	DP-T60	+00:08:51.527788	< ACK 00 00 00 00 00 00
5844	DNAT	DP-T60	+00:08:51.527910	> W:270 TEST_SINK L=1 00
5845	DNAT	DP-T60	+00:08:51.528241	< ACK
5846	DNAT	DP-T60	+00:08:55.761021	> R:60 DSC SUPPORT L=16
5847	DNAT	DP-T60	+00:08:55.761344	< ACK 01 21 00 02 2B 04 01 00 00 1F 0E 61 08 00 0...

Start Time: +00:08:51.527322  
Type: Native  
Direction: Reply  
Command: ACK  
Reply to Read Request.

00240: TEST\_CRC\_R\_CR  
CRC: 515Ah (20826)

00242: TEST\_CRC\_G\_Y  
CRC: 7EA6h (32422)

00244: TEST\_CRC\_B\_CB  
CRC: 23EBh (9195)

[0000] [00 5A 51 A6 7E EB 23 --] [.ZQ.~.# ]

Option

Data

Filter

Find

Clear

Open

Export

Hide

# DisplayPort Forward Error Correction (FEC) Overview and Operation

Webinar – September – 2019



Other Webinars for FEC:

[https://www.quantumdata.com/980\\_dp\\_14\\_usb.html](https://www.quantumdata.com/980_dp_14_usb.html):

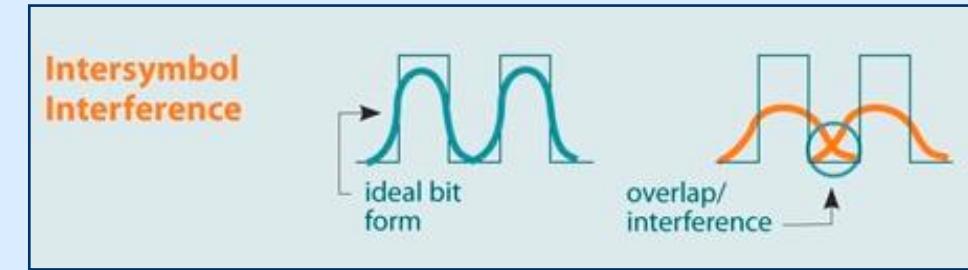
- ◆ Essentials of DisplayPort Forward Error Correction (FEC) Protocols Webinar

980B w/ DP 1.4 Video Generator /  
Protocol Analyzer module

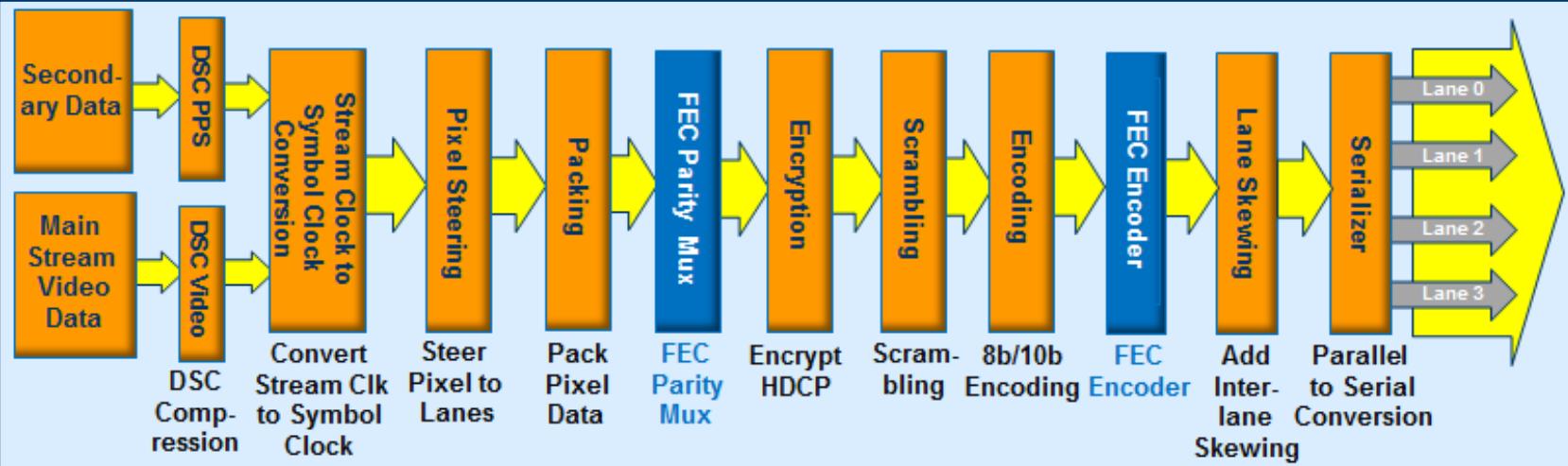


# Why is Forward Error Correction (FEC) Needed for Display Stream Compression?

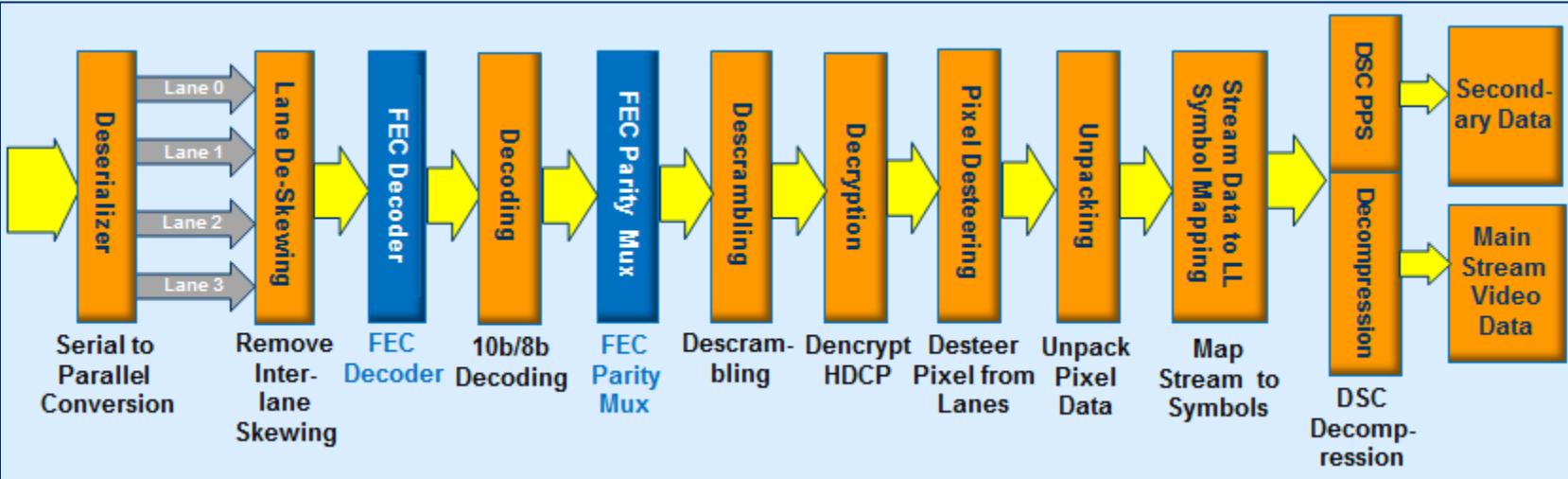
- ◆ Reed Solomon FEC is needed for DisplayPort DSC because:
  - **Higher data rates** are more prone to transmission errors.
  - Errors caused by: impulse noise, cross talk, **signal distortion** which results in Inter-Symbol interference.
  - DSC compressed streams are more susceptible to visual artifacts. A single bit error in a compressed stream results in more pervasive artifacts whether in audio or video.
- ◆ In the case of DSC, the partitioning of the DSC frame “Slices” **limits the propagation of visual artifacts** resulting from errors.
- ◆ DSC requires FEC but FEC doesn’t require DSC.
- ◆ RS FEC is well suited to the **bursty nature of errors** in high speed digital transmission.



# DisplayPort Main Link Functional Blocks – FEC Reed Solomon Encoding



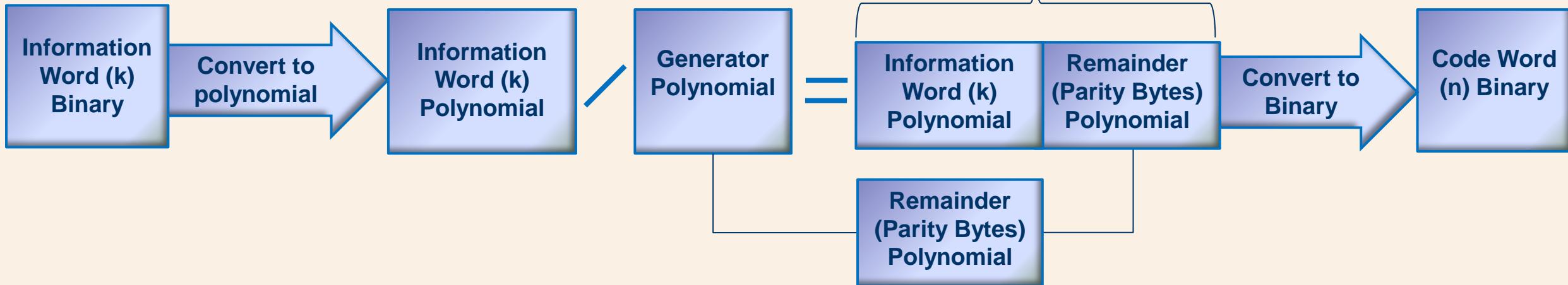
- DisplayPort Transmitter Functional Block Diagram



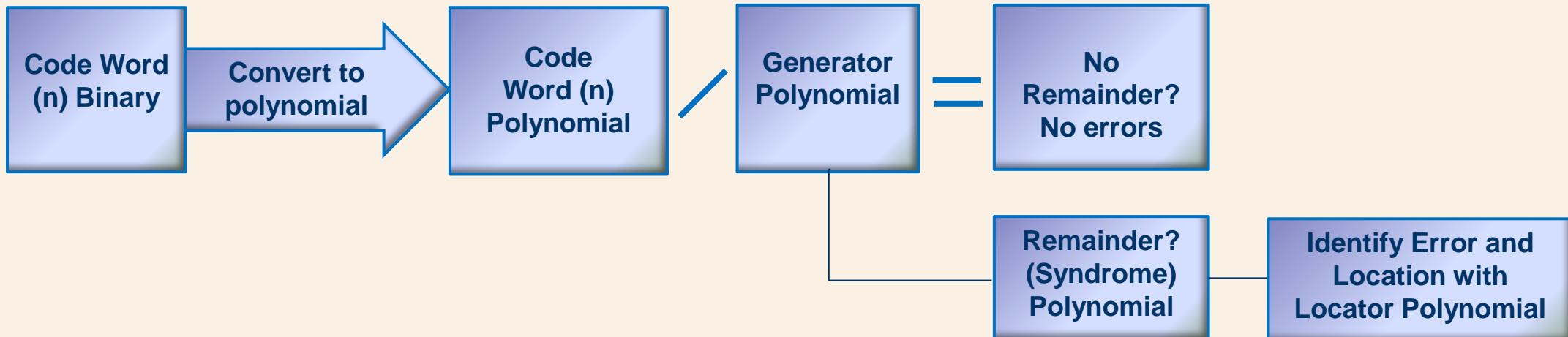
- DisplayPort Receiver Functional Block Diagram

# Reed Solomon Forward Error Correction (FEC) – In a Nutshell (continued)

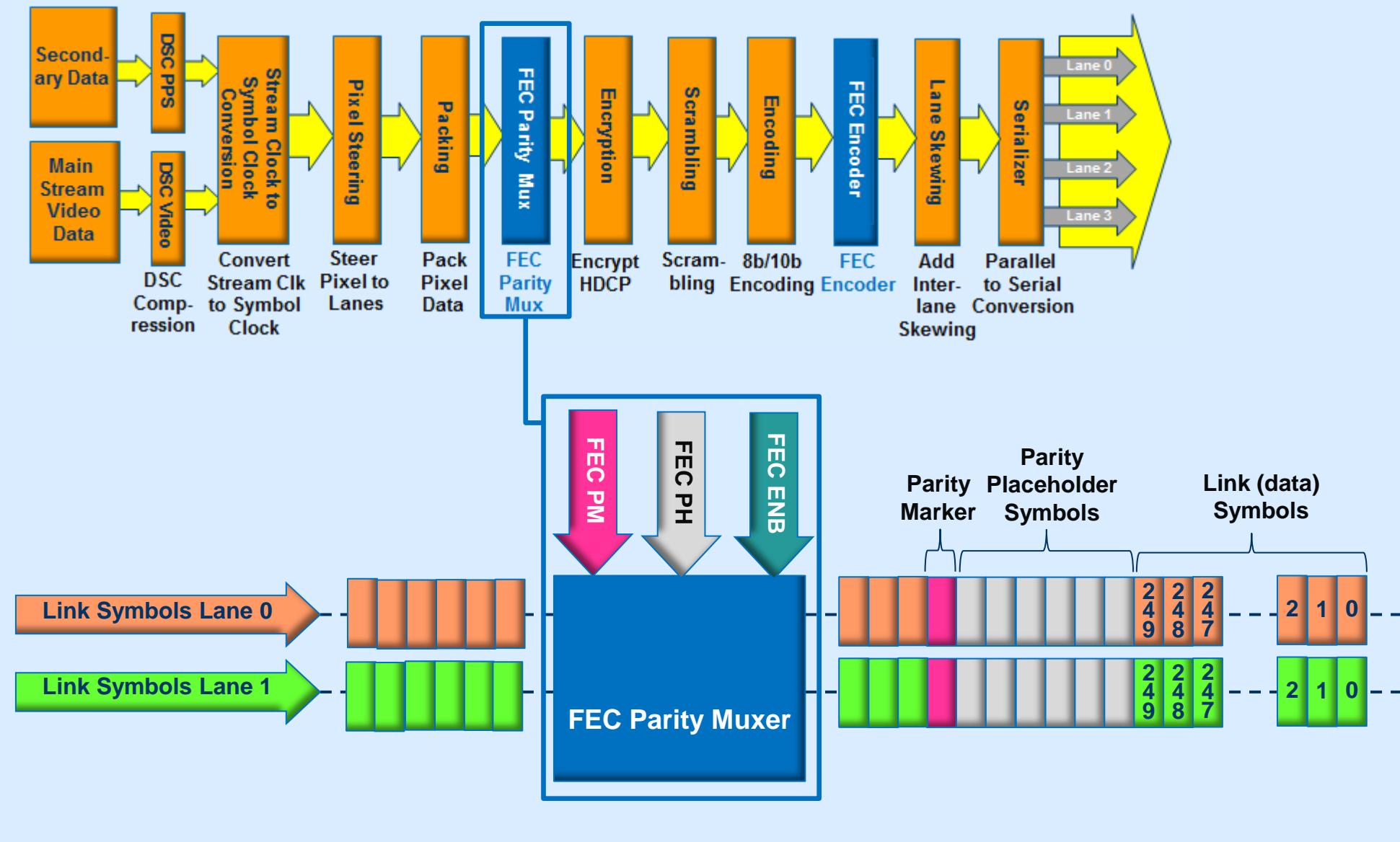
## RS-FEC Encoder



## RS-FEC Decoder

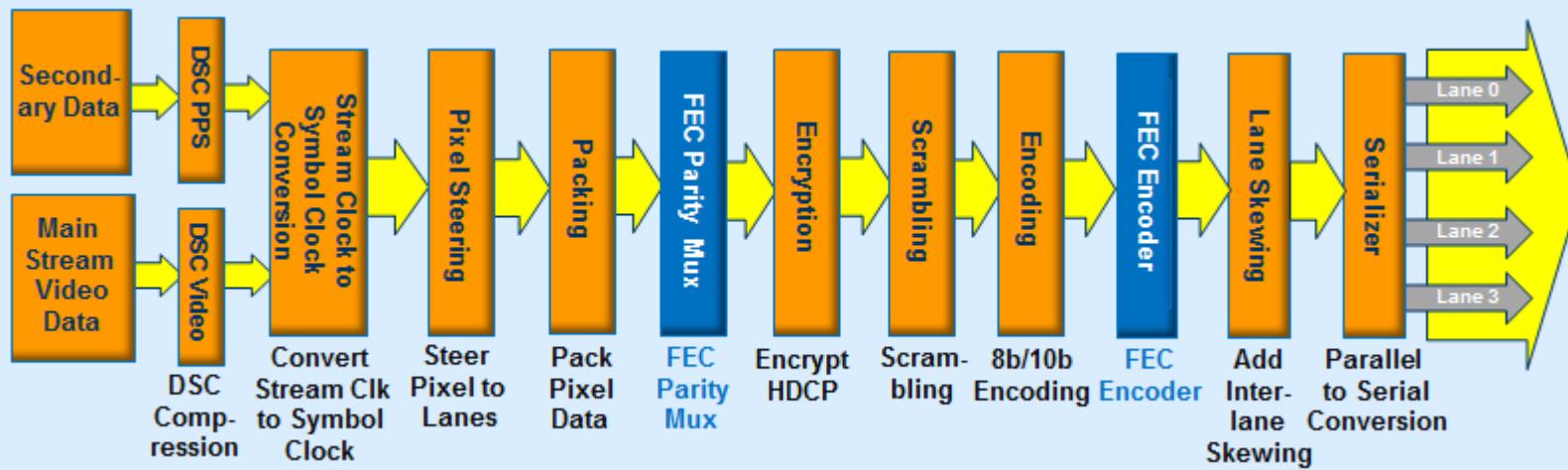


# DisplayPort Main Link Transmitter Functional Blocks (E.g. 2 lanes) – FEC Muxer

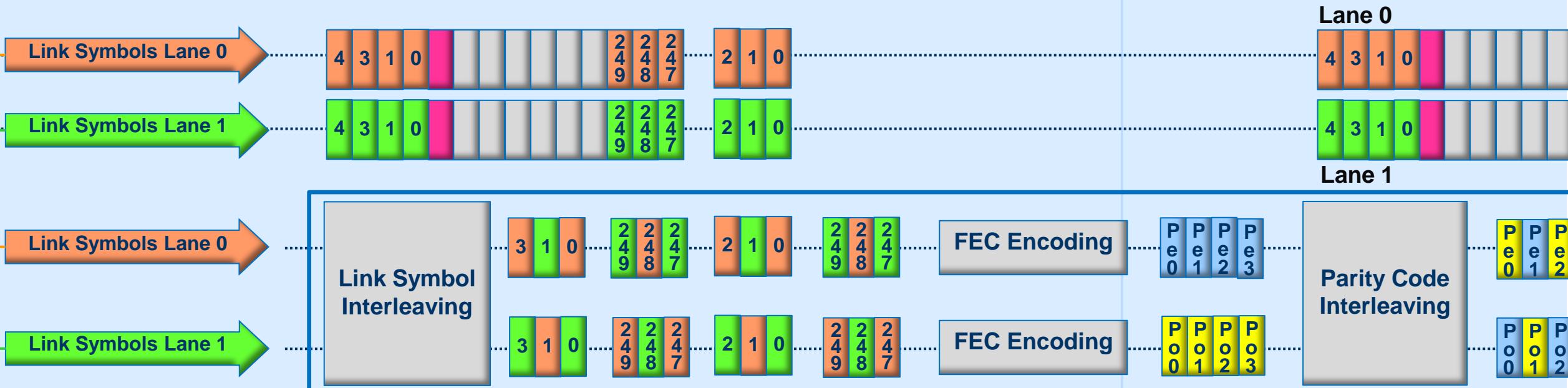


- **FEC Muxer:**
- **Insert Parity Marker:**
  - Add Parity Marker every 255 FEC blocks.
- **Initiate FEC Enable Sequence:**
  - Send K-Character sequence to enable FEC.
- **Insert Parity Placeholders:**
  - Placeholders are temporary.
  - They are removed and replace with Parity Codes by the FEC Encoder.

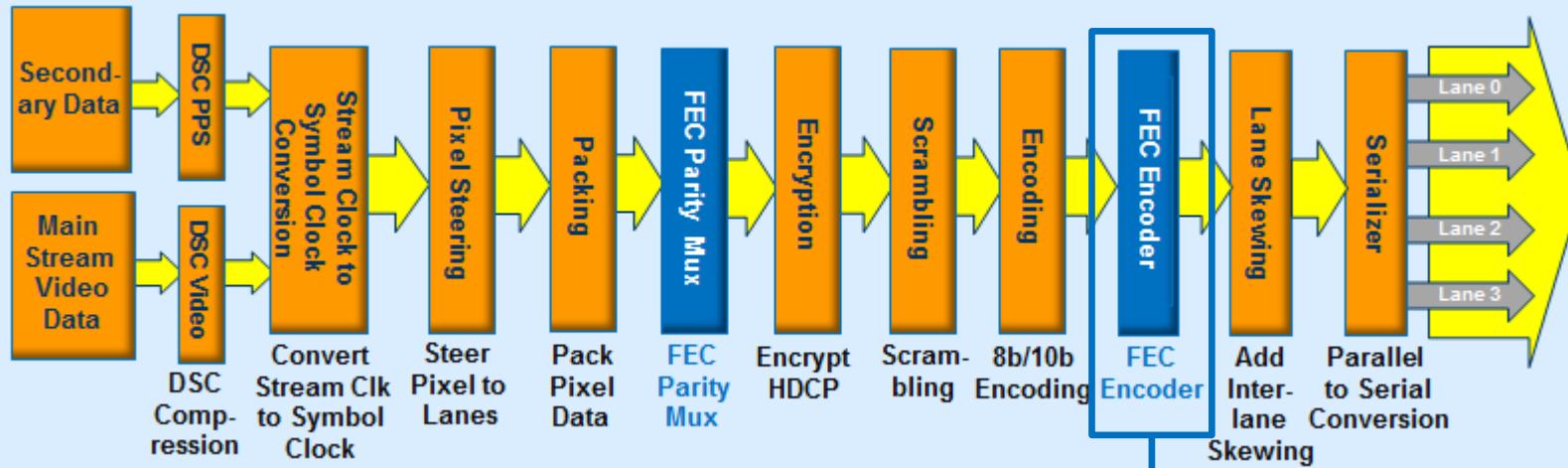
# DP Main Link Transmitter Functional Blocks – FEC Encoder – Parity/Symbol Muxing



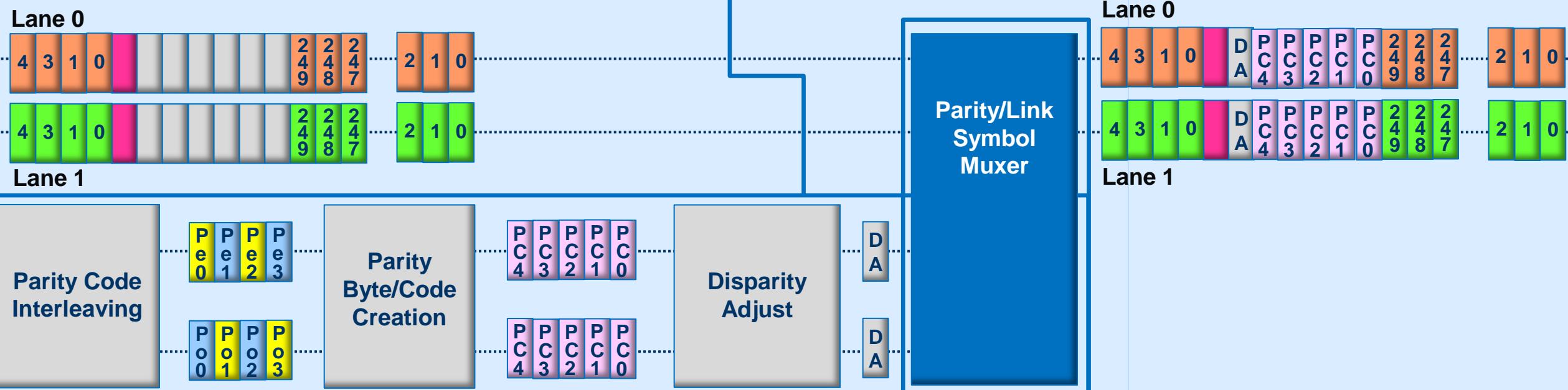
- 2 Lane Example.
- FEC Encoder:
- **Parity Code/Link Symbol Muxing:**
  - Multiplexes Parity Codes into Link Symbols.



# DP Main Link Transmitter Functional Blocks – FEC Encoder – Parity/Symbol Muxing



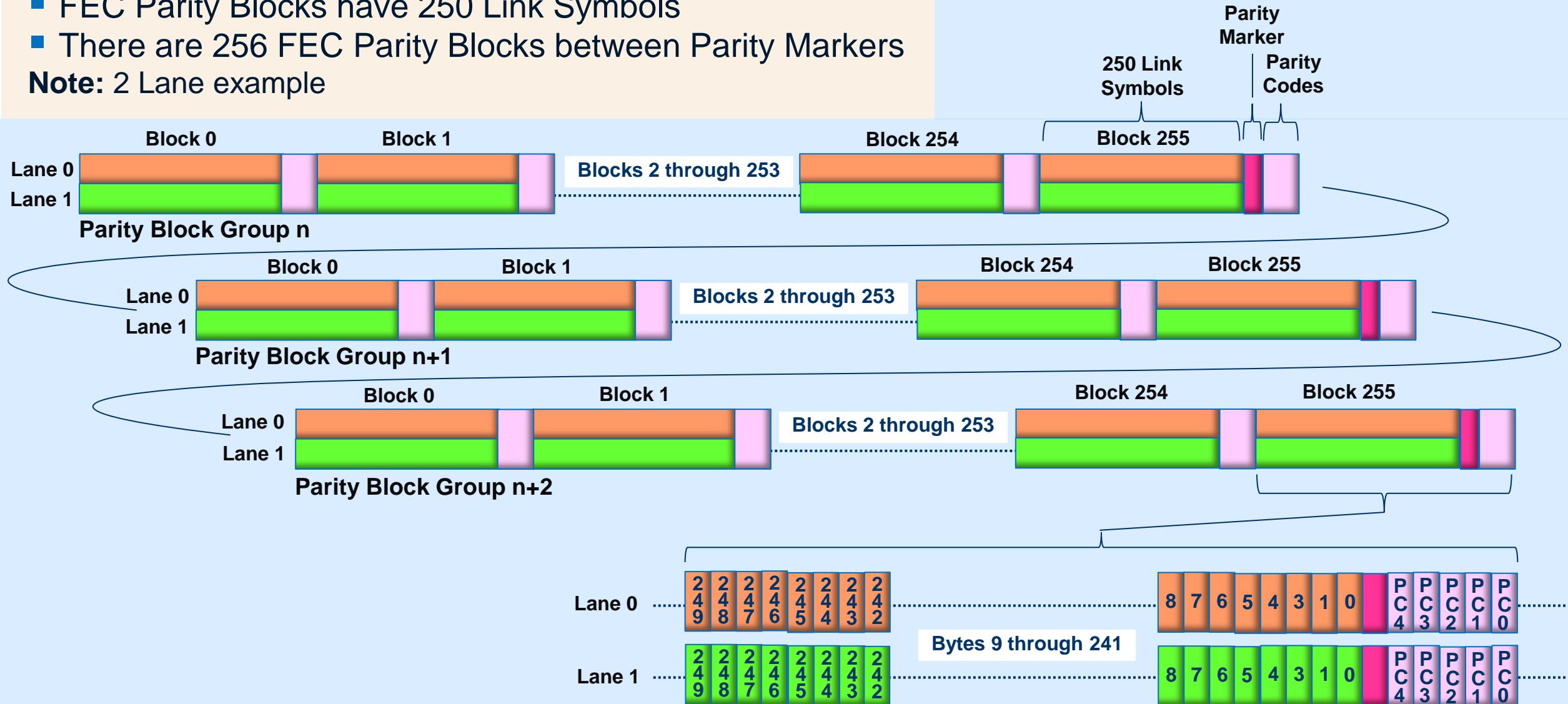
- **FEC Encoder:**
- **Parity Code/Link Symbol Muxing:**
  - Multiplexes Parity Codes into Link Symbols.



# DisplayPort Main Link Transmitter – Parity Blocks & Parity Markers

- FEC Parity Blocks have 250 Link Symbols
- There are 256 FEC Parity Blocks between Parity Markers

Note: 2 Lane example

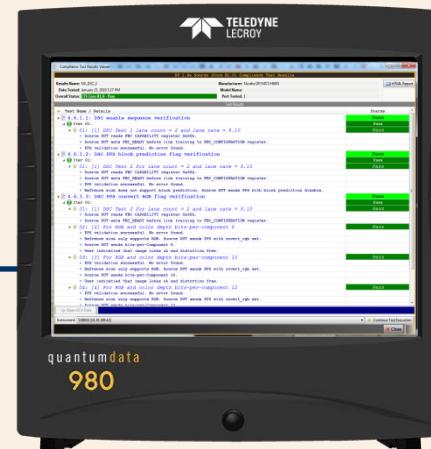


# DisplayPort FEC Compliance Source Testing

DisplayPort  
Source DUT

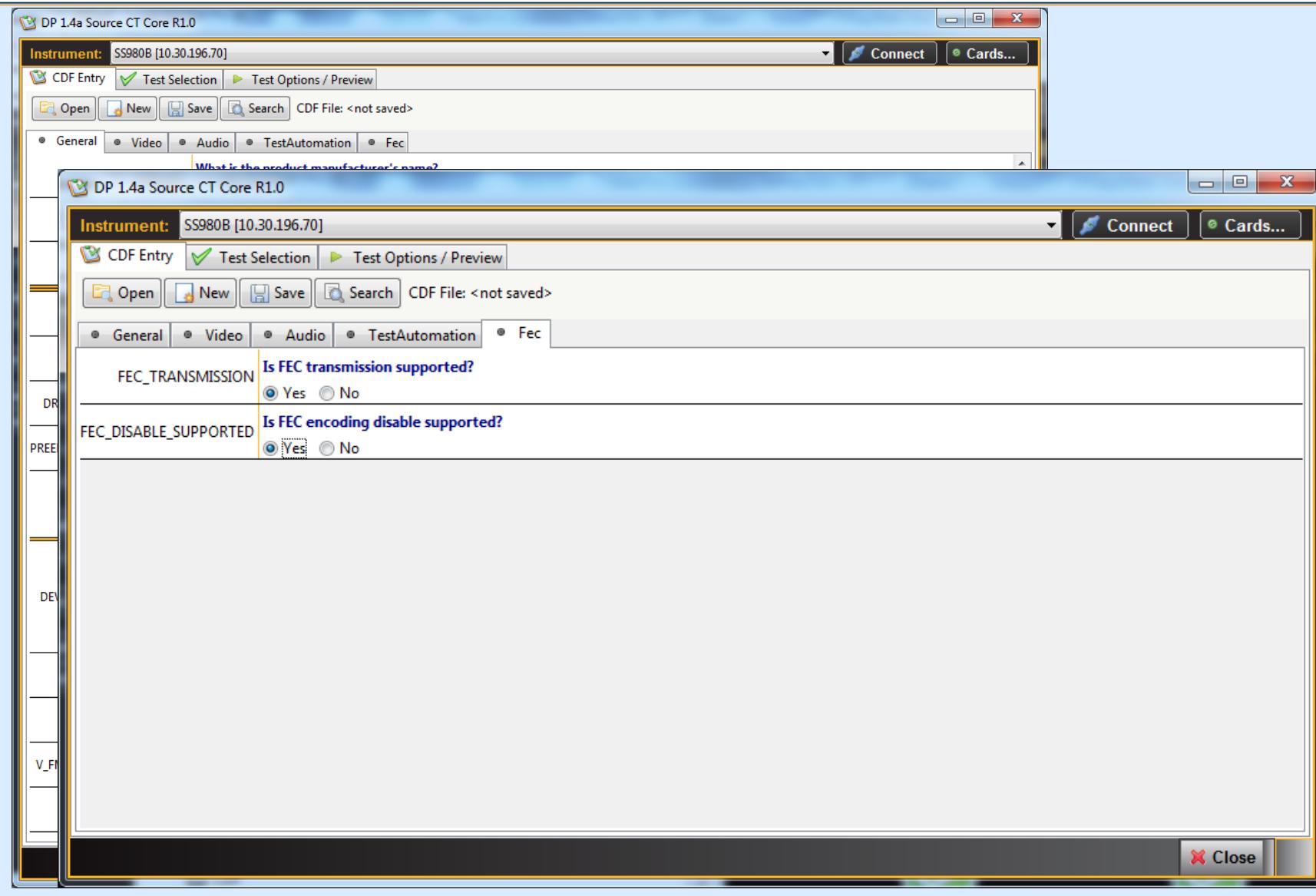


DisplayPort Cable



DP 1.4 Reference Sink  
Example: Teledyne LeCroy  
quantumdata 980 Test Platform  
with DP 1.4 Protocol Analyzer /  
Video Generator

# Source FEC Compliance - Entering the CDF Information



- Capabilities Declaration Form (CDF) must be filled out prior to the running the test.
- CDF is used by the reference sink to know which source FEC related features to test.
- FEC – Described FEC capabilities of the sink device.

# DisplayPort Source Forward Error Compliance Testing – List of Tests

DP 1.4a Source CT Core R1.0

Instrument: SS980B [10.30.196.70] Connect Cards...

CDF Entry Test Selection Test Options / Preview

All Count Options Execute Tests

Category / Test Name

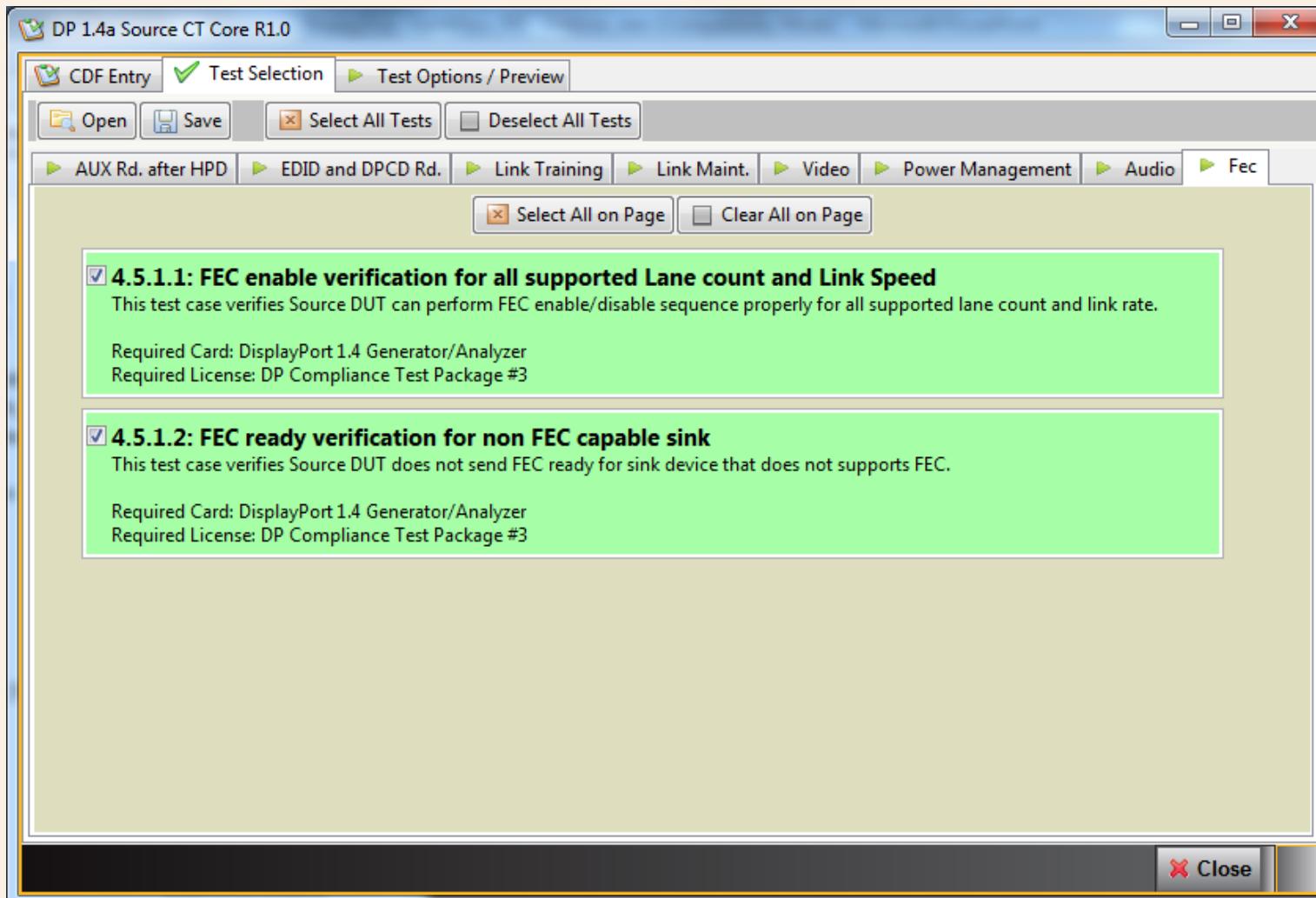
Fec

4.5.1.1: FEC enable verification for all supported Lane count and Link Speed	✓
4.5.1.2: FEC ready verification for non FEC capable sink	✓

Close

# DisplayPort Source Forward Error Compliance Testing – Test Selection

## ■ List of DP FEC Source Compliance Tests



# Source Forward Error Correction Compliance Test – Test 4.5.1.1

Compliance Test Results Viewer DP 1.4

Results Name: 980\_LB\_FEC  
Date Tested: October 19, 2018 9:16 AM  
Overall Status: CTS Core R1.0 - Pass

Test Name / Details

4.5.1.1: FEC enable verification for all supported Lane Count

Iter 01:

- 01: [1] Test for lane count = 1 and FEC ready
- 02: [2] Test for lane count = 2 and FEC ready
- 03: [3] Test for lane count = 4 and FEC ready
- 04: [4] Test for lane count = 1 and FEC error count = 0
- 05: [5] Test for lane count = 2 and FEC error count = 0
- 06: [6] Test for lane count = 4 and FEC error count = 0
- 07: [7] Test for lane count = 1 and FEC parity bit error count = 0
- 08: [8] Test for lane count = 2 and FEC parity bit error count = 0
- 09: [9] Test for lane count = 4 and FEC parity bit error count = 0
- 10: [10] Test for lane count = 1 and FEC capability = 1

Source DUT reads FEC CAPABILITY register  
Source DUT sets FEC\_READY before link training  
Source DUT enables the FEC encoding properties  
For lane 1 Fec Uncorrected block error count is 0.  
For lane 1 Fec corrected block error count is 0.  
For lane 1 Fec bit error count is 0.  
For lane 1 Fec parity block error count is 0.  
For lane 1 Fec parity bit error count is 0.  
Source DUT disables the FEC encoding properties  
11: [11] Test for lane count = 2 and FEC ready  
12: [12] Test for lane count = 4 and FEC ready

4.5.1.2: FEC ready verification for no FEC ready

Iter 01:

- 01: [1] FEC ready verification test  
Source DUT reads FEC CAPABILITY register  
Source DUT does clear FEC\_READY in FEC\_CONFIGURATION register

Open ACA Data 4.5.1.1: FEC enable verification for all supported Lane Count

Instrument: SS980B [10.30.196.39]

ACA Data Viewer [ACA-4\_5\_1\_1\_01] Events: 1458 (5016)

Event ID	Port	Device	Time	Message
117	DNAT	DP-R31	+21:51:20.142217	< ACK 81
118	DNAT	DP-R31	+21:51:20.142288	> R:0 DPDCD_REV L=1
119	DNAT	DP-R31	+21:51:20.142360	< ACK 14
120	DNAT	DP-R31	+21:51:20.142429	> R:2200 DP1.3_DPDCD_REV L=16
121	DNAT	DP-R31	+21:51:20.142502	< ACK 14 06 C2 81 01 00 01 80 00 20 04 08 00 02 81 00
122	DNAT	DP-R31	+21:51:20.142734	> R:90 FEC_CAPABILITY L=1
123	DNAT	DP-R31	+21:51:20.142807	< ACK BF
124	DNAT	DP-R31	+21:51:20.300053	> R:200 SINK_COUNT L=6
125	DNAT	DP-R31	+21:51:20.300126	< ACK 41 00 00 00 80 03
126	DNAT	DP-R31	+21:51:20.300281	> R:E TRAINING_AUX_RD_INTERVAL L=1
127	DNAT	DP-R31	+21:51:20.300354	< ACK 81
128	DNAT	DP-R31	+21:51:20.300431	> R:0 DPDCD_REV L=1
129	DNAT	DP-R31	+21:51:20.300503	< ACK 14
130	DNAT	DP-R31	+21:51:20.300583	> R:2200 DP1.3_DPDCD_REV L=16
131	DNAT	DP-R31	+21:51:20.300655	< ACK 14 06 C2 81 01 00 01 80 00 20 04 08 00 02 81 00
132	DNAT	DP-R31	+21:51:20.300886	> R:90 FEC_CAPABILITY L=1
133	DNAT	DP-R31	+21:51:20.300959	< ACK BF
134	DNAT	DP-R31	+21:51:20.301039	> W:10A eDP_CONFIGURATION_SET L=1 00
135	DNAT	DP-R31	+21:51:20.301119	< ACK
136	DNAT	DP-R31	+21:51:20.301261	> W:120 FEC_CONFIGURATION L=1 01
137	DNAT	DP-R31	+21:51:20.301261	< ACK
138	DNAT	DP-R31	+21:51:20.301334	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
139	DNAT	DP-R31	+21:51:20.301406	< ACK 00
140	DNAT	DP-R31	+21:51:20.360337	> R:E TRAINING_AUX_RD_INTERVAL L=1
141	DNAT	DP-R31	+21:51:20.360410	< ACK 81
142	DNAT	DP-R31	+21:51:20.360486	> R:E TRAINING_AUX_RD_INTERVAL L=1
143	DNAT	DP-R31	+21:51:20.360559	< ACK 81
144	DNAT	DP-R31	+21:51:20.360636	> R:0 DPDCD_REV L=1
145	DNAT	DP-R31	+21:51:20.360708	< ACK 14
146	DNAT	DP-R31	+21:51:20.360788	> R:2200 DP1.3_DPDCD_REV L=16
147	DNAT	DP-R31	+21:51:20.360861	< ACK 14 06 C2 81 01 00 01 80 00 20 04 08 00 02 81 00
148	DNAT	DP-R31	+21:51:20.361095	> R:90 FEC_CAPABILITY L=1
149	DNAT	DP-R31	+21:51:20.361167	< ACK BF
150	DPLT	DP-R31	+21:51:20.367721	> W:100 LINK_BW_SET L=1 06
151	DPLT	DP-R31	+21:51:20.367802	< ACK
152	DPLT	DP-R31	+21:51:20.367877	> W:101 LANE_COUNT_SET L=1 82
153	DPLT	DP-R31	+21:51:20.367957	< ACK
154	DPLT	DP-R31	+21:51:20.466295	> W:107 DOWNSPREAD_CTRL L=1 10

Start Time: +21:51:20.301186  
Type: Native  
Direction: Request  
Command: Write  
Address: 0x00120 (FEC\_CONFIGURATION)  
Length: 1

00120: FEC\_CONFIGURATION

Bit	Name	Value	Description
0	FEC_READY	Y(1)	
3-1	FEC_ERROR_COUNT_SEL	0	FEC_ERROR_COUNT_DISABLE
5-4	LANE_SELECT	0	
6	Reserved	0	
7	Reserved	0	

[0000][80 01 20 00 01 -- -- --][...]

ACA Data Viewer Filter Find Clear Open Export Hide

# Source Forward Error Correction Compliance Test – Test 5.4.1.2

Compliance Test Results Viewer

DP 1.4a Source (Core R1.0) Compliance Test Results

Results Name: 980\_LB\_FEC

Date Tested: October 19, 2018 9:16 AM

Overall Status: CTS Core R1.0 - Pass

Test Name / Details

4.5.1.1: FEC enable verification for all supported lane counts

Iter 01:

- 01: [1] Test for lane count = 1 and lane rate = 1 Gbps
- 02: [2] Test for lane count = 2 and lane rate = 1 Gbps
- 03: [3] Test for lane count = 4 and lane rate = 1 Gbps
- 04: [4] Test for lane count = 1 and lane rate = 2 Gbps
- 05: [5] Test for lane count = 2 and lane rate = 2 Gbps
- 06: [6] Test for lane count = 4 and lane rate = 2 Gbps
- 07: [7] Test for lane count = 1 and lane rate = 4 Gbps
- 08: [8] Test for lane count = 2 and lane rate = 4 Gbps
- 09: [9] Test for lane count = 4 and lane rate = 4 Gbps
- 10: [10] Test for lane count = 1 and lane rate = 8 Gbps
- Source DUT reads FEC\_CAPABILITY register 0x90h.
- Source DUT sets FEC\_READY before link training to F1.
- Source DUT enables the FEC encoding properly.
- For lane 1 Fec Uncorrected block error count is 0.
- For lane 1 Fec corrected block error count is 0.
- For lane 1 Fec bit error count is 0.
- For lane 1 Fec parity block error count is 0.
- For lane 1 Fec parity bit error count is 0.
- Source DUT disables the FEC encoding properly.
- 11: [11] Test for lane count = 2 and lane rate = 2 Gbps
- 12: [12] Test for lane count = 4 and lane rate = 4 Gbps

4.5.1.2: FEC ready verification for non FEC capable lanes

Iter 01:

- 01: [1] FEC ready verification test for lane 1
- Source DUT reads FEC\_CAPABILITY register 0x90h.
- Source DUT does clear FEC\_READY in FEC\_CONFIGURATION register.

Open ACA Data 4.5.1.1: FEC enable verification for all supported Lane count and Link Speed

Instrument: SS980B [10.30.196.39]

ACA Data Viewer

[ACA-4\_5\_1\_2\_01] Events: 198 (1066)

Index	Source	Destination	Time	Event Description
0	DPHP	DP-R31	+21:58:37.350145	HPD Falling Edge
1	DPHP	DP-R31	+21:58:38.330584	HPD Rising Edge
2	DNAT	DP-R31	+21:58:38.331050	> R:200 SINK_COUNT L=6
3	DNAT	DP-R31	+21:58:38.331122	< ACK 41 00 77 77 01 00
4	DNAT	DP-R31	+21:58:38.331260	> R:E TRAINING_AUX_RD_INTERVAL L=1
5	DNAT	DP-R31	+21:58:38.331332	< ACK 81
6	DNAT	DP-R31	+21:58:38.331409	> R:0 DPCD_REV L=1
7	DNAT	DP-R31	+21:58:38.331482	< ACK 14
8	DNAT	DP-R31	+21:58:38.331557	> R:2200 DP1.3_DPCD_REV L=16
9	DNAT	DP-R31	+21:58:38.331629	< ACK 14 1E C4 81 01 00 01 80 00 20 04 08 00 02 81 00
10	DNAT	DP-R31	+21:58:38.331860	> R:90 FEC_CAPABILITY L=1
11	DNAT	DP-R31	+21:58:38.331933	< ACK 00
12	DPLT	DP-R31	+21:58:38.475619	> R:100 LINK_BW_SET L=2
13	DPLT	DP-R31	+21:58:38.475691	< ACK 1B 84
14	DNAT	DP-R31	+21:58:38.489205	> R:200 SINK_COUNT L=6
15	DNAT	DP-R31	+21:58:38.489277	< ACK 41 00 00 00 80 00
16	DNAT	DP-R31	+21:58:38.489444	> R:E TRAINING_AUX_RD_INTERVAL L=1
17	DNAT	DP-R31	+21:58:38.489516	< ACK 81
18	DNAT	DP-R31	+21:58:38.489618	> R:0 DPCD_REV L=1
19	DNAT	DP-R31	+21:58:38.489690	< ACK 14
20	DNAT	DP-R31	+21:58:38.489774	> R:2200 DP1.3_DPCD_REV L=16
21	DNAT	DP-R31	+21:58:38.489846	< ACK 14 1E C4 81 01 00 01 80 00 20 04 08 00 02 81 00
22	DNAT	DP-R31	+21:58:38.490113	> R:90 FEC_CAPABILITY L=1
23	DNAT	DP-R31	+21:58:38.490185	< ACK 00
24	DNAT	DP-R31	+21:58:38.490270	> W:10A eDP_CONFIGURATION_SET L=1 00
25	DNAT	DP-R31	+21:58:38.490350	< ACK
26	DNAT	DP-R31	+21:58:38.490420	> R:201 DEVICE_SERVICE_IRQ_VECTOR L=1
27	DNAT	DP-R31	+21:58:38.490492	< ACK 00
28	DNAT	DP-R31	+21:58:38.549425	> R:E TRAINING_AUX_RD_INTERVAL L=1
29	DNAT	DP-R31	+21:58:38.549497	< ACK 81
30	DNAT	DP-R31	+21:58:38.549595	> R:E TRAINING_AUX_RD_INTERVAL L=1
31	DNAT	DP-R31	+21:58:38.549667	< ACK 81
32	DNAT	DP-R31	+21:58:38.549756	> R:0 DPCD_REV L=1
33	DNAT	DP-R31	+21:58:38.549829	< ACK 14
34	DNAT	DP-R31	+21:58:38.549916	> R:2200 DP1.3_DPCD_REV L=16
35	DNAT	DP-R31	+21:58:38.549989	< ACK 14 1E C4 81 01 00 01 80 00 20 04 08 00 02 81 00
36	DNAT	DP-R31	+21:58:38.550254	> R:90 FEC_CAPABILITY L=1
37	DNAT	DP-R31	+21:58:38.550327	< ACK 00

Start Time: +21:58:38.331933  
Type: Native  
Direction: Reply  
Command: ACK  
Reply to Read Request.

00090: FEC\_CAPABILITY

Bit	Name	Value	Description
0	FEC_CAPABLE	N(0)	
1	UNCORRECTED_BLOCK_ERR_CNT_CAP	N(0)	
2	CORRECTED_BLOCK_ERR_CNT_CAP	N(0)	
3	BIT_ERROR_COUNT_CAPABLE	N(0)	
4		0	Reserved
5		0	Reserved
6		0	Reserved
7		0	Reserved

[0000][00 00 -- -- -- -- -- --]...[1]

11: < ACK 00

◆ Test verifies that a source reads the sink FEC.

# DisplayPort FEC Compliance Sink Testing

DP 1.4 Reference Source  
Example: Teledyne LeCroy  
quantumdata 980 Test Platform  
with DP 1.4 Video Generator /  
Protocol Analyzer

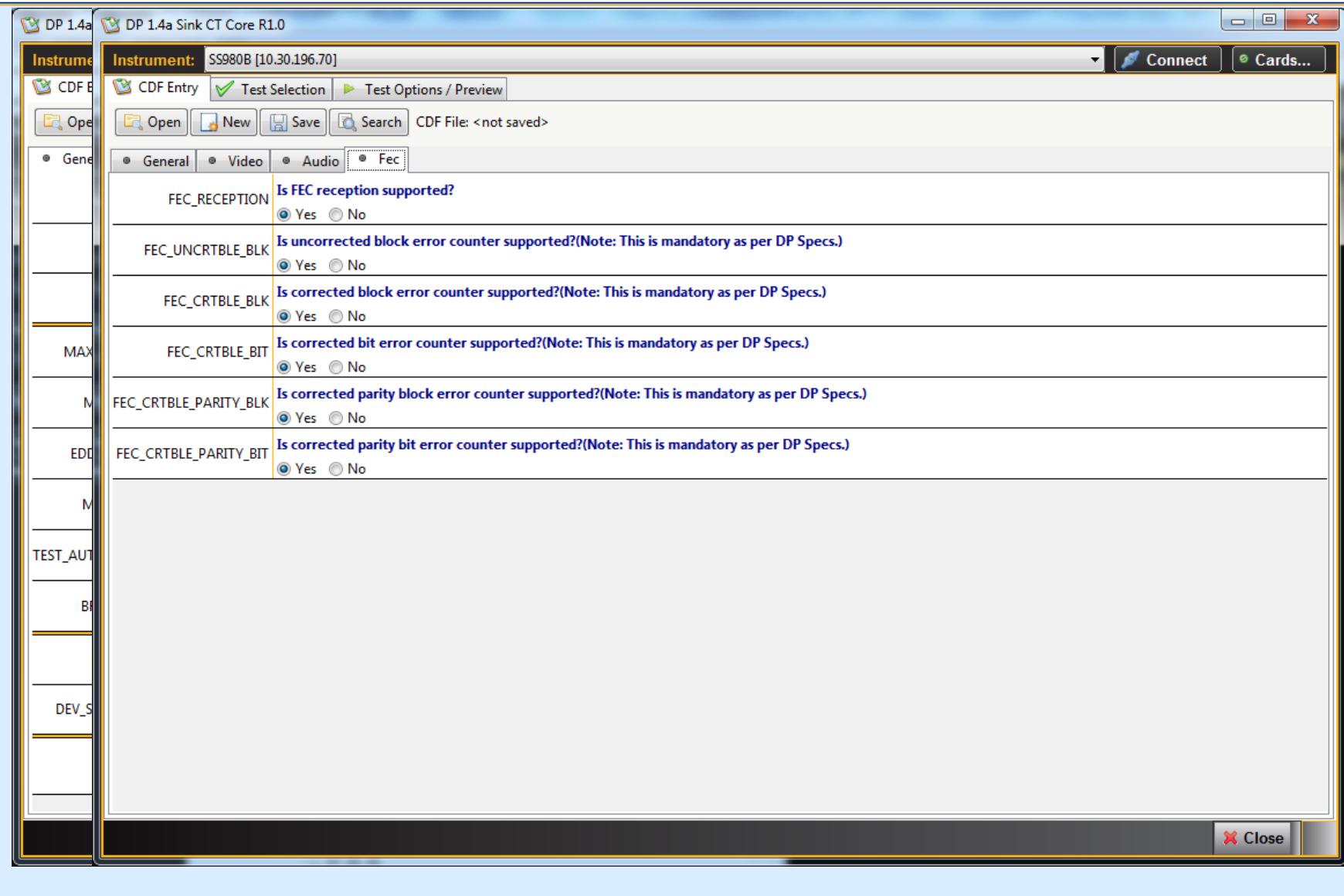


DisplayPort Sink (Monitor/TV)



DisplayPort Cable

# FEC Sink Compliance - Entering the CDF Information



- Capabilities Declaration Form (CDF) must be filled out prior to the running the test.
- CDF is used by the reference sink to know which FEC related sink features to test.
- FEC – Described FEC capabilities of the sink device.

# DisplayPort Sink Forward Error Compliance Testing – List of Tests

DP 1.4a Sink CT Core R1.0

Instrument: SS980B [10.30.196.70]

CDF Entry Test Selection Test Options / Preview

All Count Options Execute Tests

Category / Test Name

Fec

Test Name	Status
5.5.1.1: FEC capability verification	✓
5.5.1.2: Successful Link Training at All Supported Lane Counts and Link Rates with FEC Enable	✓
5.5.1.3: Uncorrectable Block error count	✓
5.5.1.4: Correctable Block error count	✓
5.5.1.5: Correctable Bit error count	✓
5.5.1.6: Correctable Parity Block error count	✓
5.5.1.7: Correctable Parity Bit error count	✓

Close

# DisplayPort Source Forward Error Compliance Testing – Test Selection

DP 1.4a Sink CT Core R1.0

Instrument: SS980B [10.30.196.70] Connect Cards...

CDF Entry Test Selection Test Options / Preview

Open Save Select All Tests Deselect All Tests

AUX Ch. Proto. Sink DPCD Field Impl. Link Training Link Maint. Main Video Power Management Main Audio Fec Other (1.4)

Select All on Page Clear All on Page

**5.5.1.1: FEC capability verification**  
This test verifies that DP sink device has capability bit set properly.  
Required Card: DisplayPort 1.4 Generator/Analyzer OR DisplayPort 1.4 USB-C Generator/Analyzer  
Required License: DP Compliance Test Package #4 or DP DSC Compliance Test of Sink

**5.5.1.2: Successful Link Training at All Supported Lane Counts and Link Rates with FEC Enable**  
This test verifies that Sink DUT can link train with FEC enable at all link count and link rate. This also verifies Sink DUT can handle FEC enable and disable by reference source. During FEC enable for 1 sec window, Sink DUT error counter are read to verify the line is error free.  
Required Card: DisplayPort 1.4 Generator/Analyzer OR DisplayPort 1.4 USB-C Generator/Analyzer  
Required License: DP Compliance Test Package #4 or DP DSC Compliance Test of Sink

**5.5.1.3: Uncorrectable Block error count**  
This test verifies that Sink DUT can count uncorrectable block errors.  
Required Card: DisplayPort 1.4 Generator/Analyzer OR DisplayPort 1.4 USB-C Generator/Analyzer  
Required License: DP Compliance Test Package #4 or DP DSC Compliance Test of Sink

**5.5.1.4: Correctable Block error count**  
This test verifies that Sink DUT can count correctable block errors.  
Required Card: DisplayPort 1.4 Generator/Analyzer OR DisplayPort 1.4 USB-C Generator/Analyzer  
Required License: DP Compliance Test Package #4 or DP DSC Compliance Test of Sink

**5.5.1.5: Correctable Bit error count**  
This test verifies that Sink DUT can count correctable bit errors.  
Required Card: DisplayPort 1.4 Generator/Analyzer OR DisplayPort 1.4 USB-C Generator/Analyzer  
Required License: DP Compliance Test Package #4 or DP DSC Compliance Test of Sink

**5.5.1.6: Correctable Parity Block error count**  
This test verifies that Sink DUT can count parity block errors.  
Required Card: DisplayPort 1.4 Generator/Analyzer OR DisplayPort 1.4 USB-C Generator/Analyzer  
Required License: DP Compliance Test Package #4 or DP DSC Compliance Test of Sink

**X Close**

# Sink Forward Error Correction Compliance Test – Test 5.5.1.2

- ◆ This test verifies that the Sink

The screenshot displays two windows side-by-side. The left window is 'Compliance Test Results Viewer' showing test results for 'DP 1.4a Sink (Core R1.0)'. It includes sections for 'Test Name / Details', 'Test Results', and a detailed log of 'Link Training test for lane count = 1 and lane rate' (Iter 01). The right window is 'ACA Data Viewer' showing a timeline of events from 'ACA-5\_5\_1\_2\_01'. A yellow arrow points from the log in the left window to the event list in the right window. The right window also shows a detailed view of the 'FEC\_STATUS' message structure.

**Compliance Test Results Viewer**

**DP 1.4a Sink (Core R1.0) Compliance Test Results**

**Results Name:** 980\_LB\_FEC    **Manufacturer:** [redacted]    **Date Tested:** October 19, 2018 9:33 AM    **Overall Status:** CTS Core R1.0 - Fail

**Test Name / Details**

**5.5.1.2: Successful Link Training at All Supported Lane Count**

**Iter 01:**

- 01: Link Training test for lane count = 1 and lane rate
- 02: Link Training test for lane count = 2 and lane rate
- 03: Link Training test for lane count = 4 and lane rate
- 04: Link Training test for lane count = 1 and lane rate
- 05: Link Training test for lane count = 2 and lane rate
- 06: Link Training test for lane count = 4 and lane rate
- 07: Link Training test for lane count = 1 and lane rate
- 08: Link Training test for lane count = 2 and lane rate
- 09: Link Training test for lane count = 4 and lane rate
- 10: Link Training test for lane count = 1 and lane rate
- 11: Link Training test for lane count = 2 and lane rate
  - HPD is asserted
  - Reference Source receives AUX\_ACK at 1 attempts of SET\_POWER
  - Reference Source receives AUX ACK from either write request of SET\_P
  - Reference Source receives AUX ACK from either write request of FEC\_C
  - AUX Read 0x2201 (MAX\_LINK\_RATE) = 0x1e
  - AUX Read 0x2202 (MAX\_LANE\_COUNT) = 0xc4
  - Link Training at lane count 2 and link rate 8.1 successful
  - FEC Decode enable link symbol sequence detected over main link. (FEC)
  - For lane 1 FEC uncorrectable Block error counter reports 0
  - For lane 1 FEC correctable Block error counter reports 0
  - For lane 1 FEC correctable Bit error counter reports 0
  - For lane 1 FEC correctable parity block error counter reports 0
  - For lane 1 FEC correctable parity bit error counter reports 0
  - For lane 2 FEC uncorrectable Block error counter reports 0
  - For lane 2 FEC correctable Block error counter reports 0
  - For lane 2 FEC correctable Bit error counter reports 0
  - For lane 2 FEC correctable parity block error counter reports 0
  - For lane 2 FEC correctable parity bit error counter reports 0
  - Sink DUT reports, FEC Decode disable link symbol sequence detected
- 12: Link Training test for lane count = 4 and lane rate

**5.5.1.3: Uncorrectable Block error count**

**Open ACA Data**    **5.5.1.1: FEC capability verification**

**Instrument:** SS980B [10.30.196.39]

**ACA Data Viewer**

**[ACA-5\_5\_1\_2\_01] Events: 1938 (4718)**

Event ID	Port	Event Type	Timestamp	Message
74	DPLT	DP-T30	+22:07:48.187419	> R:206 ADJUST_REQUEST_LANE0_1 L=2
75	DPLT	DP-T30	+22:07:48.187491	< ACK 44 44
76	DPLT	DP-T30	+22:07:48.187760	> W:103 TRAINING_LANE0_SET L=4 08 08 08 08
77	DPLT	DP-T30	+22:07:48.187864	< ACK
78	DPLT	DP-T30	+22:07:48.191880	> R:202 LANEO_1_STATUS: L=3
79	DPLT	DP-T30	+22:07:48.191952	< ACK 07 00 81
80	DPLT	DP-T30	+22:07:48.192048	> R:204 LANE_ALIGN_STATUS_UPDATED L=2
81	DPLT	DP-T30	+22:07:48.192120	< ACK 01 00
82	DPLT	DP-T30	+22:07:48.192218	> W:102 TRAINING_PATTERN_SET: L=1 00
83	DPLT	DP-T30	+22:07:48.192298	< ACK
84	DPLT	DP-T30	+22:07:48.192387	> W:102 TRAINING_PATTERN_SET: L=1 00
85	DPLT	DP-T30	+22:07:48.192467	< ACK
86	DNAT	DP-T30	+22:07:48.192543	> R:200 SINK_COUNT L=6
87	DNAT	DP-T30	+22:07:48.192616	< ACK 41 00 07 00 01 00
88	DPLT	DP-T30	+22:07:48.192814	> R:100 LINK_BW_SET L=8
89	DPLT	DP-T30	+22:07:48.192887	< ACK 06 81 00 08 08 08 08 10
90	DNAT	DP-T30	+22:07:48.193055	> R:200 SINK_COUNT L=8
91	DNAT	DP-T30	+22:07:48.193127	< ACK 41 00 07 00 01 00 88 88
92	DPLT	DP-T30	+22:07:48.270630	> R:100 LINK_BW_SET L=2
93	DPLT	DP-T30	+22:07:48.270676	< ACK 06 81
94	DPLT	DP-T30	+22:07:48.380262	> R:100 LINK_BW_SET L=2
95	DPLT	DP-T30	+22:07:48.380335	< ACK 06 81
96	DNAT	DP-T30	+22:07:48.780945	> W:280 FEC_STATUS L=1 FF
97	DNAT	DP-T30	+22:07:48.781026	< ACK
98	DPLT	DP-T30	+22:07:48.784485	> R:100 LINK_BW_SET L=2
99	DPLT	DP-T30	+22:07:48.784557	< ACK 06 81
100	DPLT	DP-T30	+22:07:48.893306	> R:100 LINK_BW_SET L=2
101	DPLT	DP-T30	+22:07:48.893379	< ACK 06 81
102	DNAT	DP-T30	+22:07:49.0	> R:280 FEC_STATUS L=1
103	DNAT	DP-T30	+22:07:49.000970	< ACK 01
104	DNAT	DP-T30	+22:07:49.001049	> W:120 FEC_CONFIGURATION L=1 01
105	DNAT	DP-T30	+22:07:49.001130	< ACK
106	DNAT	DP-T30	+22:07:49.001201	> W:120 FEC_CONFIGURATION L=1 07
107	DNAT	DP-T30	+22:07:49.001281	< ACK
108	DNAT	DP-T30	+22:07:49.002387	> W:120 FEC_CONFIGURATION L=1 03
109	DNAT	DP-T30	+22:07:49.002468	< ACK
110	DNAT	DP-T30	+22:07:49.002532	> R:281 FEC_ERROR_COUNT0 L=2
111	DNAT	DP-T30	+22:07:49.002604	< ACK 00 80

**Start Time:** +22:07:49.000970    **Type:** Native    **Direction:** Reply    **Command:** ACK

**Reply to Read Request.**

**00280: FEC\_STATUS**

Bit	Name	Value	Description
0	DECODE_EN_DETECTED	Y(1)	
1	DECODE_DIS_DETECTED	N(0)	
2		0	Reserved
3		0	Reserved
4		0	Reserved
5		0	Reserved
6		0	Reserved
7		0	Reserved

[0000] [00 01 -- -- -- -- --] [..] [1]

**Find**    **Clear**    **Open**    **Export**    **Hide**

# Sink FEC Compliance Test – Correctable Block Errors - Test 5.5.1.4

◆ Test verifies that sink can

**Compliance Test Results Viewer**

DP 1.4a Sink (Core R1.0) Compliance Test Results

Results Name: 980\_LB\_FEC  
Date Tested: October 19, 2018 9:33 AM  
Overall Status: CTS Core R1.0 - Fail

Test Name / Details

- 5.5.1.2: Successful Link Training at All Supported Lane Counts
- 5.5.1.3: Uncorrectable Block error count
- 5.5.1.4: Correctable Block error count
  - Iter 01:
    - 01: Link Training test for lane count = 1 and lane rate =
    - 02: Link Training test for lane count = 2 and lane rate =
    - 03: Link Training test for lane count = 4 and lane rate =
    - 04: Link Training test for lane count = 1 and lane rate =
    - 05: Link Training test for lane count = 2 and lane rate =
    - 06: Link Training test for lane count = 4 and lane rate =
    - 07: Link Training test for lane count = 1 and lane rate =
    - 08: Link Training test for lane count = 2 and lane rate =
    - 09: Link Training test for lane count = 4 and lane rate =
    - 10: Link Training test for lane count = 1 and lane rate =
    - 11: Link Training test for lane count = 2 and lane rate =
      - HPD is asserted
      - Reference Source receives AUX\_ACK at 1 attempts of SET\_POWER
      - Reference Source receives AUX ACK from either write request of SET\_POWER
      - Reference Source receives AUX ACK from either write request of FEC\_CONFIG
      - AUX Read 0x2201 (MAX\_LINK\_RATE) = 0x1e
      - AUX Read 0x2202 (MAX\_LANE\_COUNT) = 0xc4
      - Link Training at lane count 2 and link rate 8.1 successful
      - FEC Decode enable link symbol sequence detected over main link. (FEC\_S)
      - ==> On Lane 1, after inserting 1000 FEC correctable block errors.
      - Lane 1 FEC correctable block errors in range (998).
      - Lane 2 Reported FEC correctable block errors (2).
      - ==> On Lane 2, after inserting 1000 FEC correctable block errors.
      - Lane 1 Reported FEC correctable block errors (5).
      - Lane 2 FEC correctable block errors in range (995).
      - Sink DUT reports, FEC Decode disable link symbol sequence detected over
    - 12: Link Training test for lane count = 4 and lane rate =
  - 5.5.1.5: Correctable Bit error count

Open ACA Data

Instrument: SS980B [10.30.196.39]

**ACA Data Viewer**

[ACA-5\_5\_1\_4\_01] Events: 1870 (4658)

Event ID	Port	Direction	Timestamp	Message
1636	DNAT	DP-T30	+22:12:41.153312	> R:280 FEC_STATUS L=1
1637	DNAT	DP-T30	+22:12:41.153385	< ACK 01
1638	DNAT	DP-T30	+22:12:41.153455	> W:120 FEC_CONFIGURATION L=1 01
1639	DNAT	DP-T30	+22:12:41.153535	< ACK
1640	DNAT	DP-T30	+22:12:41.153601	> W:120 FEC_CONFIGURATION L=1 07
1641	DNAT	DP-T30	+22:12:41.153682	< ACK
1642	DNAT	DP-T30	+22:12:41.154738	> W:120 FEC_CONFIGURATION L=1 01
1643	DNAT	DP-T30	+22:12:41.154819	< ACK
1644	DNAT	DP-T30	+22:12:41.154995	> W:120 FEC_CONFIGURATION L=1 07
1645	DNAT	DP-T30	+22:12:41.155075	< ACK
1646	DNAT	DP-T30	+22:12:43.281084	> W:120 FEC_CONFIGURATION L=1 05
1647	DNAT	DP-T30	+22:12:43.281164	< ACK
1648	DNAT	DP-T30	+22:12:43.281234	> R:281 FEC_ERROR_COUNT0 L=2
1649	DNAT	DP-T30	+22:12:43.281306	< ACK E6 83
1650	DNAT	DP-T30	+22:12:43.281394	> W:120 FEC_CONFIGURATION L=1 15
1651	DNAT	DP-T30	+22:12:43.281474	< ACK
1652	DNAT	DP-T30	+22:12:43.281537	> R:281 FEC_ERROR_COUNT0 L=2
1653	DNAT	DP-T30	+22:12:43.281537	< ACK 02 80
1654	DNAT	DP-T30	+22:12:43.281702	> W:120 FEC_CONFIGURATION L=1 01
1655	DNAT	DP-T30	+22:12:43.281782	< ACK
1656	DNAT	DP-T30	+22:12:43.281957	> W:120 FEC_CONFIGURATION L=1 07
1657	DNAT	DP-T30	+22:12:43.282037	< ACK
1658	DNAT	DP-T30	+22:12:45.398044	> W:120 FEC_CONFIGURATION L=1 05
1659	DNAT	DP-T30	+22:12:45.398124	< ACK
1660	DNAT	DP-T30	+22:12:45.398194	> R:281 FEC_ERROR_COUNT0 L=2
1661	DNAT	DP-T30	+22:12:45.398267	< ACK 05 80
1662	DNAT	DP-T30	+22:12:45.398355	> W:120 FEC_CONFIGURATION L=1 15
1663	DNAT	DP-T30	+22:12:45.398436	< ACK
1664	DNAT	DP-T30	+22:12:45.398503	> R:281 FEC_ERROR_COUNT0 L=2
1665	DNAT	DP-T30	+22:12:45.398575	< ACK E3 83
1666	DNAT	DP-T30	+22:12:45.398666	> W:280 FEC_STATUS L=1 FF
1667	DNAT	DP-T30	+22:12:45.398746	< ACK
1668	DPLT	DP-T30	+22:12:45.402064	> R:100 LINK_BW_SET L=2
1669	DPLT	DP-T30	+22:12:45.402136	< ACK 1E 82
1670	DPLT	DP-T30	+22:12:45.510989	> R:100 LINK_BW_SET L=2
1671	DPLT	DP-T30	+22:12:45.511061	< ACK 1E 82
1672	DNAT	DP-T30	+22:12:45.618676	> R:280 FEC_STATUS L=1
1673	DNAT	DP-T30	+22:12:45.618749	< ACK 02

Start Time: +22:12:43.281609  
Type: Native  
Direction: Reply  
Command: ACK  
Reply to Read Request.

00281: FEC\_ERROR\_COUNT0  
Bit Name Value Description  
7-0 Count7:0 2

00282: FEC\_ERROR\_COUNT1  
Bit Name Value Description  
6-0 Count14:8 0  
7 Count Valid Y(1)  
[0000][00 02 80]... 1

1653: < ACK 02 80

Filter

Find

Clear

Open

Export

Hide

## Sink FEC Compliance Test – Correctable Bit Errors - Test ID# 5.5.1.5

The figure shows two windows from a test environment. The left window is 'Compliance Test Results Viewer' titled 'DP 1.4a Sink (Core R1.0) Compliance Test Results'. It displays test results for '5.5.1.5: Correctable Bit error count' with various sub-test details. The right window is 'ACA Data Viewer' titled '[ACA-5\_1\_5\_01] Events: 1870 (4666)'. It lists a sequence of events, including frame captures and log entries. A yellow arrow points from the '5.5.1.5' test result in the viewer to the event list in the ACA Data Viewer. Another yellow arrow points from the '5.5.1.5' test result to the 'FEC\_ERROR\_COUNT0' entry in the ACA Data Viewer, which shows a value of 2. A third yellow arrow points from the '5.5.1.5' test result to the 'FEC\_ERROR\_COUNT1' entry, which shows a value of 0.



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# DisplayPort Connection Sequence HDCP 2.2 Authentication Protocol

Webinar – September – 2019



Other Webinars for HDCP:

[https://www.quantumdata.com/980\\_dp\\_14\\_usb.html](https://www.quantumdata.com/980_dp_14_usb.html):

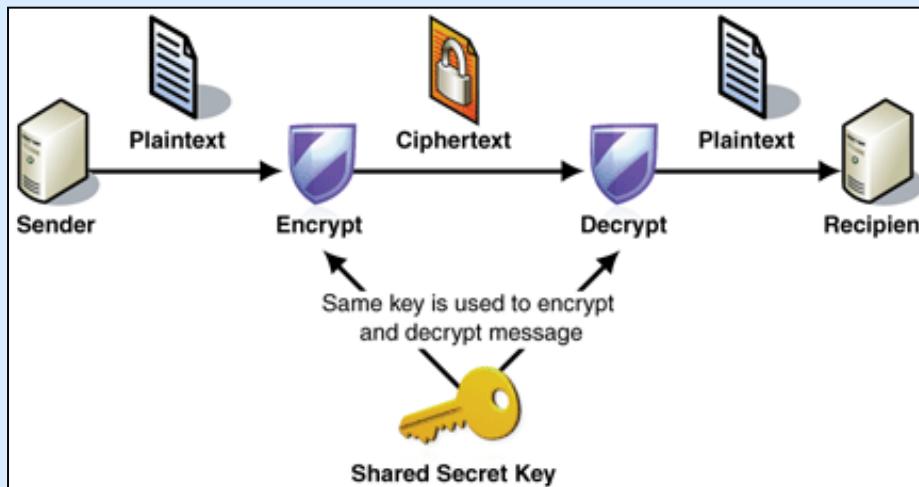
- ◆ Essentials of HDCP 2.2 Protocols

980B w/ DP 1.4 Video Generator /  
Protocol Analyzer module



# HDCP 2.2 Sequence – Cryptography – Symmetric and Asymmetric Key Encryption

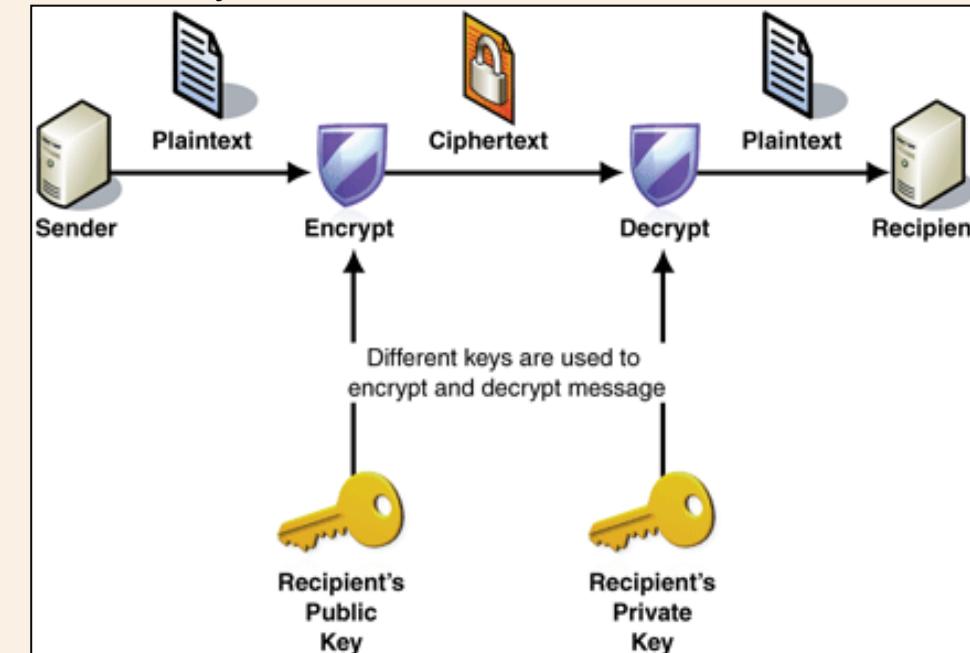
- ◆ Cryptographic systems can be categorized by the key types they use:
- ◆ **Symmetric (Private) Key Encryption (AES)**
  - ◆ Symmetric Key encryption is **much faster**.
  - ◆ Secret key needs to be **stored** securely.
  - ◆ Requires a **pre-agreed upon secret key**, or a **secure channel to exchange** the secret key.
  - ◆ Requires **separate keys for each authentication**.



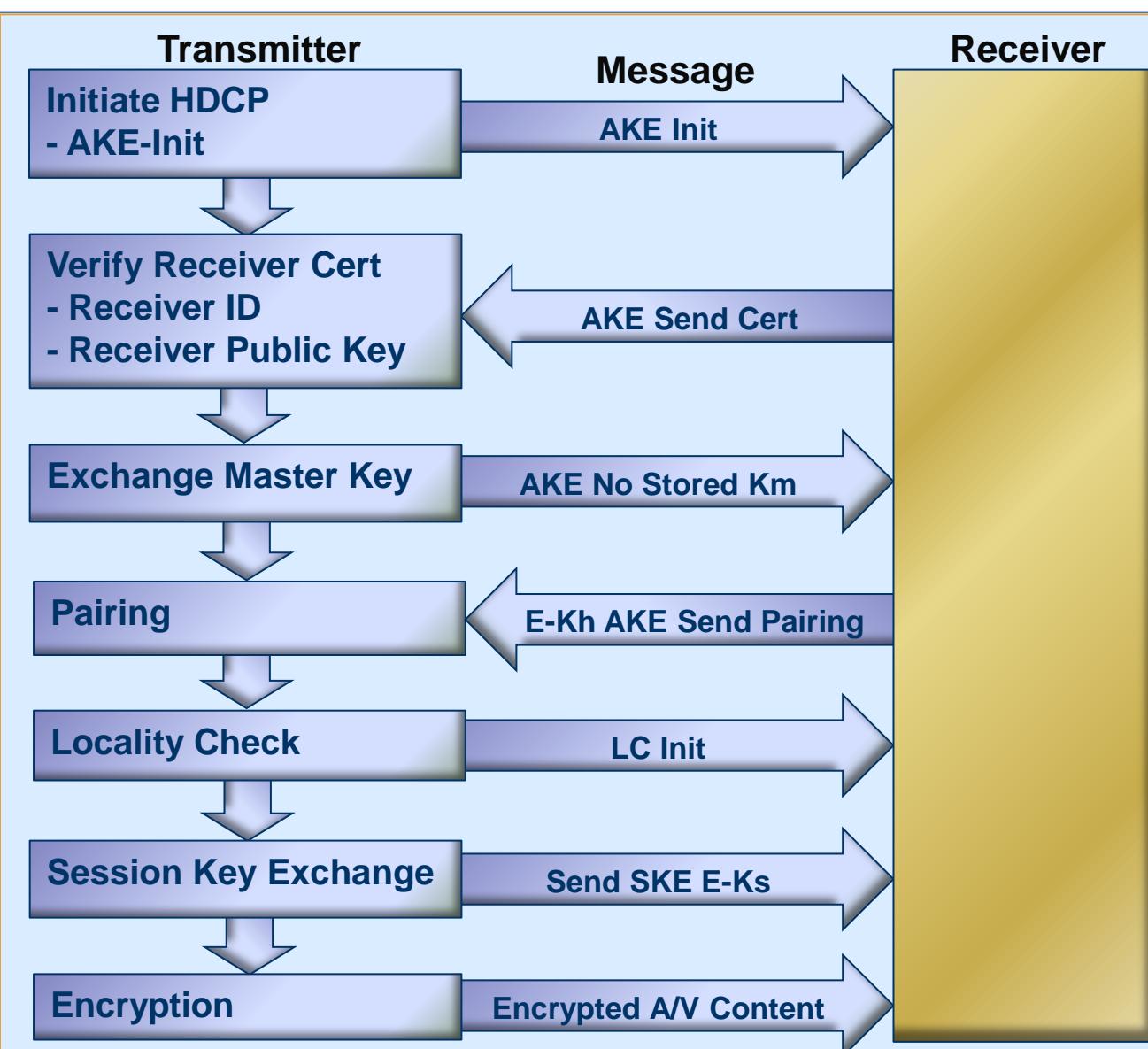
**Note:** HDCP 2.2 is a **hybrid** system using elements of both symmetric and asymmetric key encryption. **Asymmetric** key encryption is used to transfer the Master and Session keys that will be used for **symmetric** key video encryption.

- ◆ Cryptographic systems can be categorized by the key types they use:

- ◆ **Asymmetric (Public) Key Encryption (RSA)**
  - ◆ Uses pairs of keys: a **Public Key** which may be disseminated widely, and a **Private Key** which is known only to the owner—e.g. The Receiver.
  - ◆ **Invented to address the need for exchanging a secret key over an unsecured link.**
  - ◆ **Very slow** due to its computational complexity.
  - ◆ Used only for **small blocks** of data.

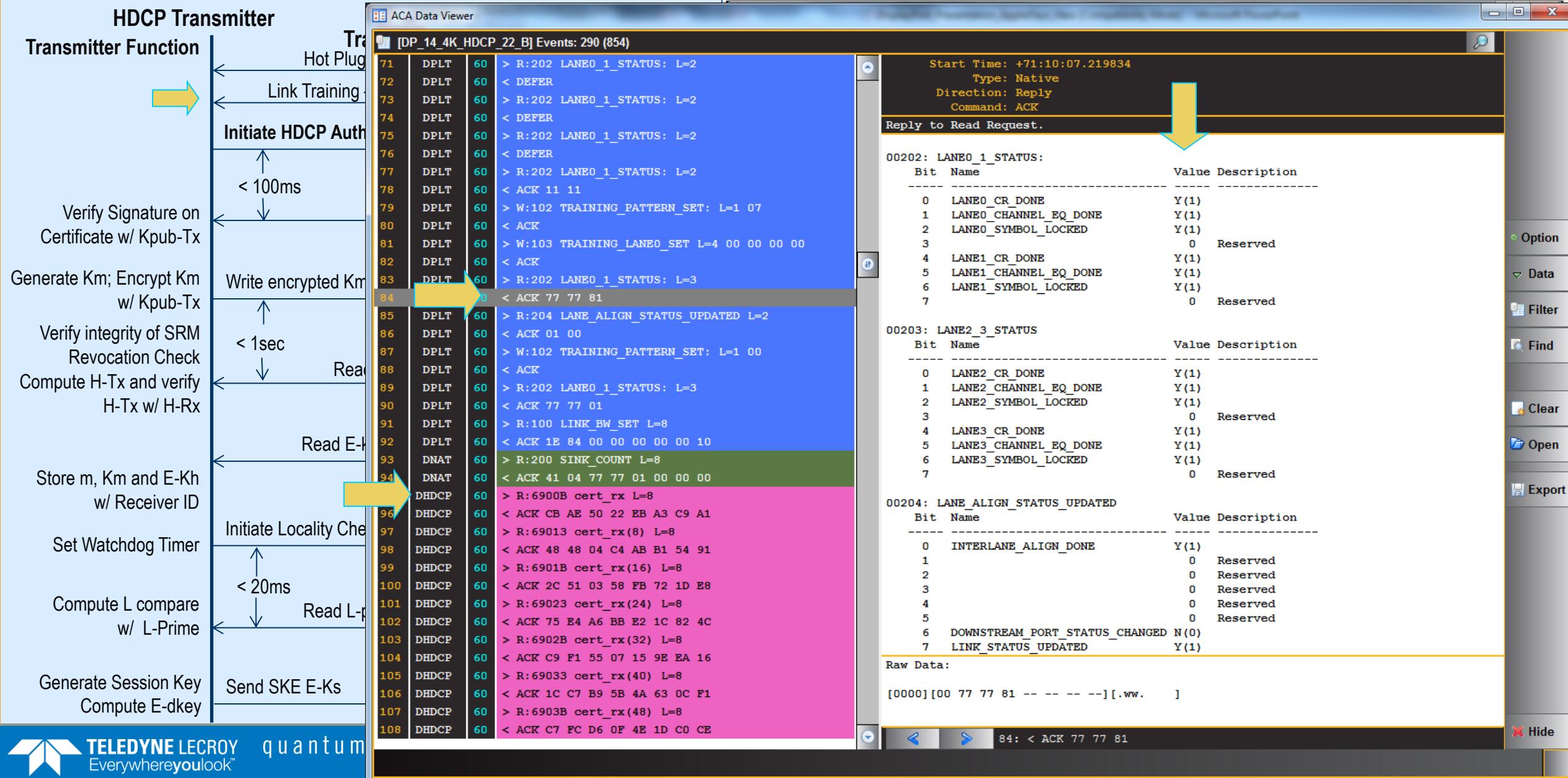


# HDCP 2.2 – Overview of HDCP 2.2 Authentication



- ◆ Overview of HDCP Authentication
- ◆ Initiate HDCP:
  - ◆ Send HDCP authentication Init message to Receiver.
- ◆ Verify Receiver Cert
  - ◆ Receiver Cert is a digital signature of Public Key and Receiver ID. Cert is RSA encrypted; verified by Hash function.
- ◆ Exchange Master key
  - ◆ Master Key is used for pairing and exchanging Session Key. Exchanged using RSA. Proper exchange verified using Hash function.
- ◆ Pairing
  - ◆ Used to reduce authentication time in subsequent authentications between same devices. Uses stored Master Key. Occurs first authentication between a unique pair of devices.
- ◆ Locality Check
  - ◆ Proximity check; uses timer to ensure colocation.
- ◆ Exchange Session Key
  - ◆ Session exchanged using the Master Key which has been previously exchanged. Exchange uses AES (since there is already a stored “secret” key (Master)).
- ◆ Encryption of A/V content
  - ◆ Uses Session Key and AES encryption.

# HDCP 2.2 Sequence – Link Training then HDCP Authentication



# HDCP 2.2 Sequence – AKE Initiation, Send Random Number and TxCaps

**HDCP Transmitter**

Transmitter Function	Transaction
Send EDID	<--
Initiate HDCP Authentication	<-- < 100ms AKE-S
Verify Signature on Certificate w/ Kpub-Tx	<--
Generate Km; Encrypt Km w/ Kpub-Tx	Write encrypted Km – AKE N
Verify integrity of SRM Revocation Check	< 1sec
Compute H-Tx and verify H-Tx w/ H-Rx	Read H – AKE
Store m, Km and E-Kh w/ Receiver ID	Read E-kh AKE-Set
Set Watchdog Timer	Initiate Locality Check – LC-Init
Compute L compare w/ L-Prime	< 20ms Read L-prime – LC
Generate Session Key Compute E-dkey	Send SKE E-Ks

**Transaction Details:**

ACA Data Viewer [HDCP\_22\_Snk\_CT\_2C\_01] Events: 216 (489)

Start Time: +25:02:58.582576  
Message: AKE\_Init (11 bytes)  
r\_tx[63..0]: BA 75 8F F9 F7 B6 EA E8  
TxCaps: 02 00 00  
VERSION: 2

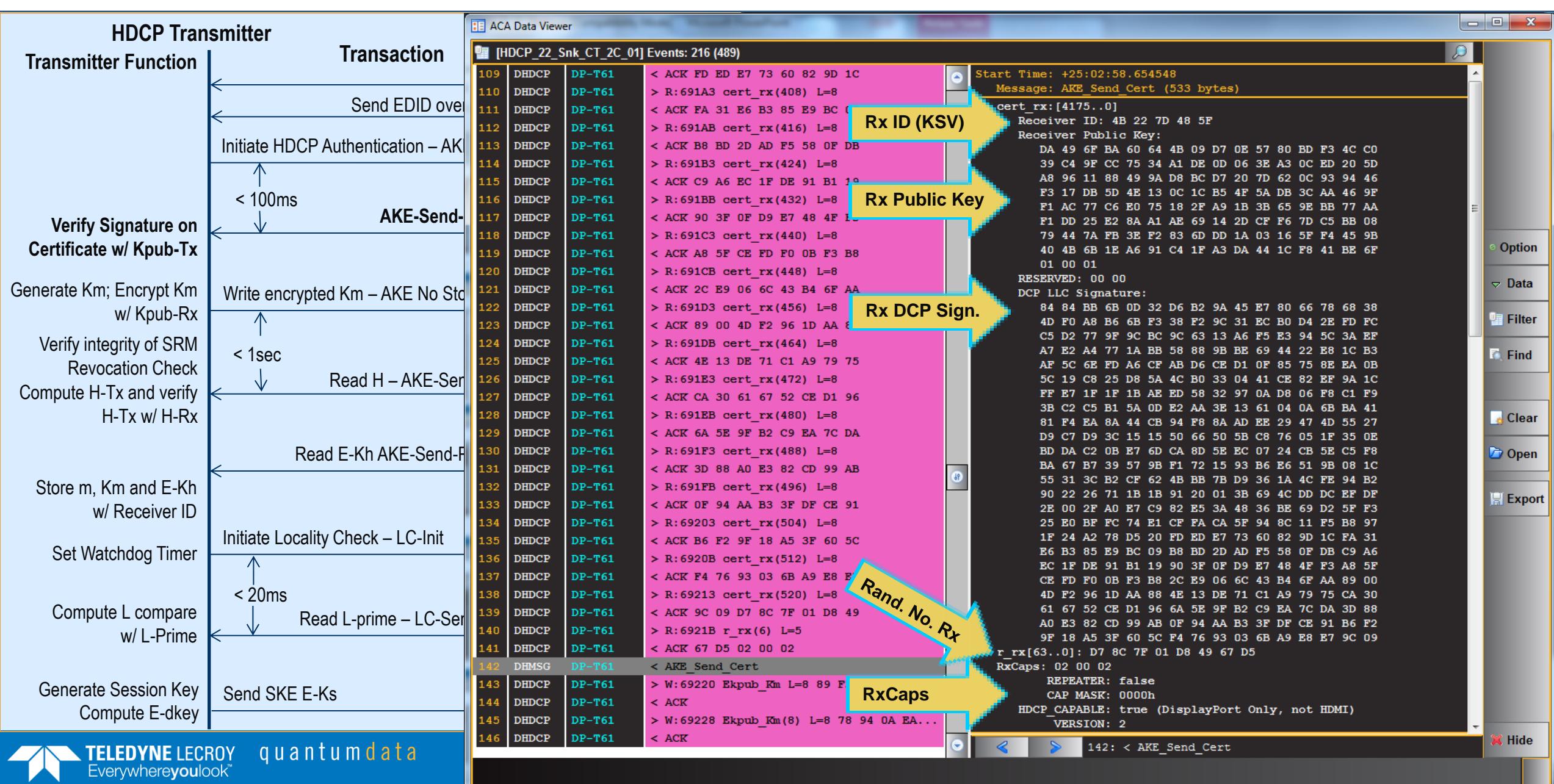
Raw Data:

```
[0000] [BA 75 8F F9 F7 B6 EA E8] [.u.....]
[0008] [02 00 00 -- -- -- -- --] [...]
```

Option  
Data  
Filter  
Find  
Clear  
Open  
Export  
Hide

7: > AKE\_Init

# HDCP 2.2 Sequence – Transmitter Reads Receiver Certificate

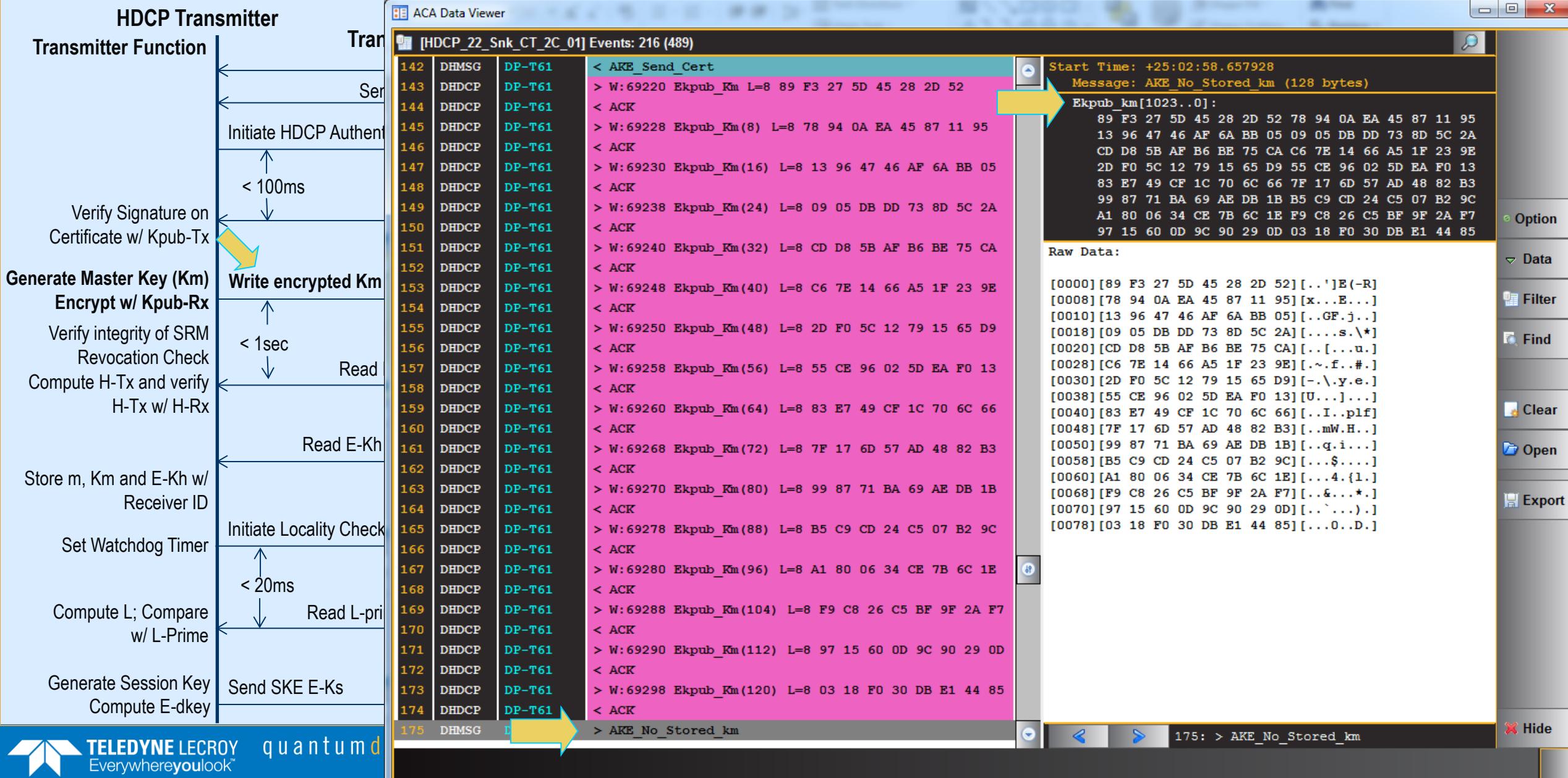


---

# **HDCP Authentication**

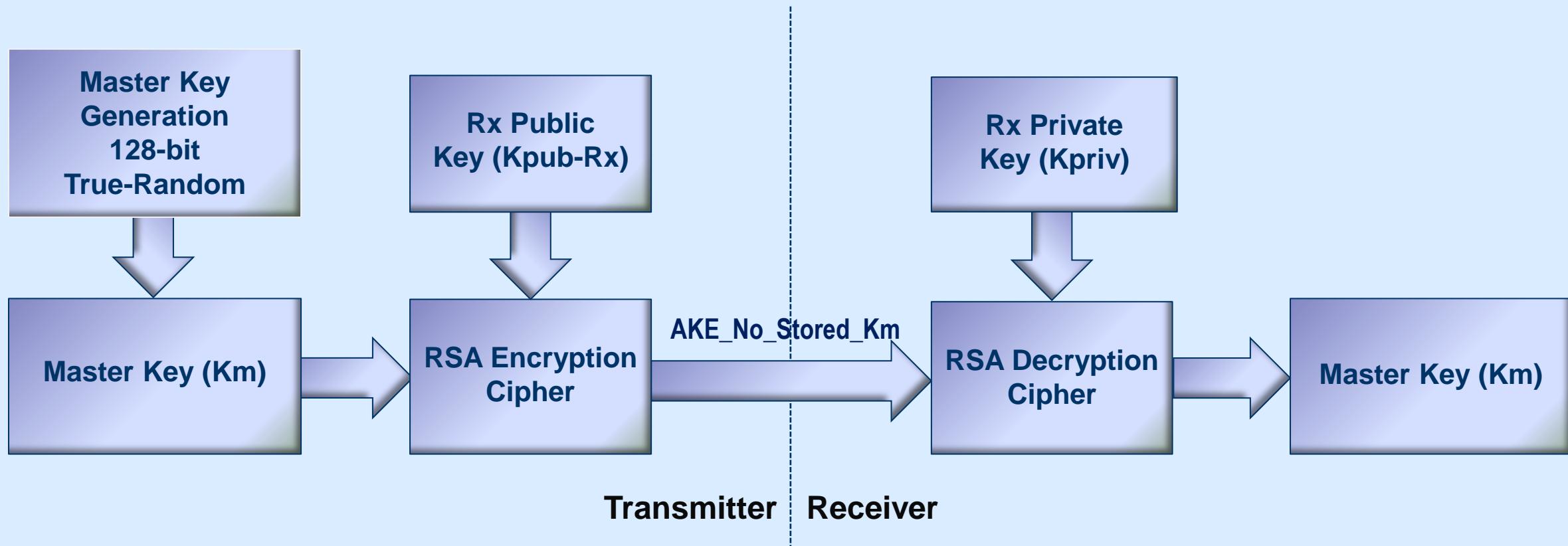
## **Generating, Exchanging the Master Key**

# HDCP 2.2 Sequence – Transmitter Sends Encrypted Master Key to Receiver



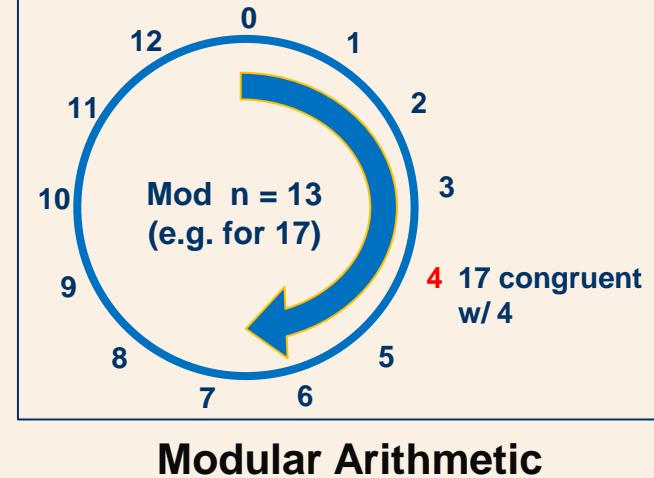
# HDCP 2.2 – Generating, Encrypting and Exchanging Master Key

- ◆ If you need to **exchange a secret key over an unsecured link** for later use in Symmetric Key encryption (AES); you **must use Asymmetric Key encryption** such as RSA to do the transfer.
- ◆ Master Key (Km) is a 128-bit key produced by the Transmitter's True-random number generator.
- ◆ Master Key is encrypted with the Receiver's public key and sent to the Receiver.



# RSA Encryption

- ◆ RSA uses the concept of a **one-way function**; Multiplying 2 prime numbers is easy but *reversing* the process to find the product's 2 prime numbers (prime factorization) is very difficult.
- ◆ Uses modular arithmetic, or “clock arithmetic.”
- ◆ The  $n$  is the product of 2 large prime numbers; it is used as the modulo in the clock arithmetic.
- ◆ Choosing values of **e** and **d** is an important factor. Calculation uses what is called a Phi function such that:  $e * d \pmod{\Phi} = 1$ .



First 1024 bits of Rx  
Public Key are the  
modulus  $n$ ;  
Next 24 bits are  $e$ .

Receiver's  
RSA Public Key  
( $n, e$ )

Unencrypted  
Content ( $m$ )  
(e.g. Master Key)

RSA Cipher  
(Encrypt)  
 $m^e \pmod{n} = c$

Sender

Receiver's  
RSA Private Key  
( $n, d$ )

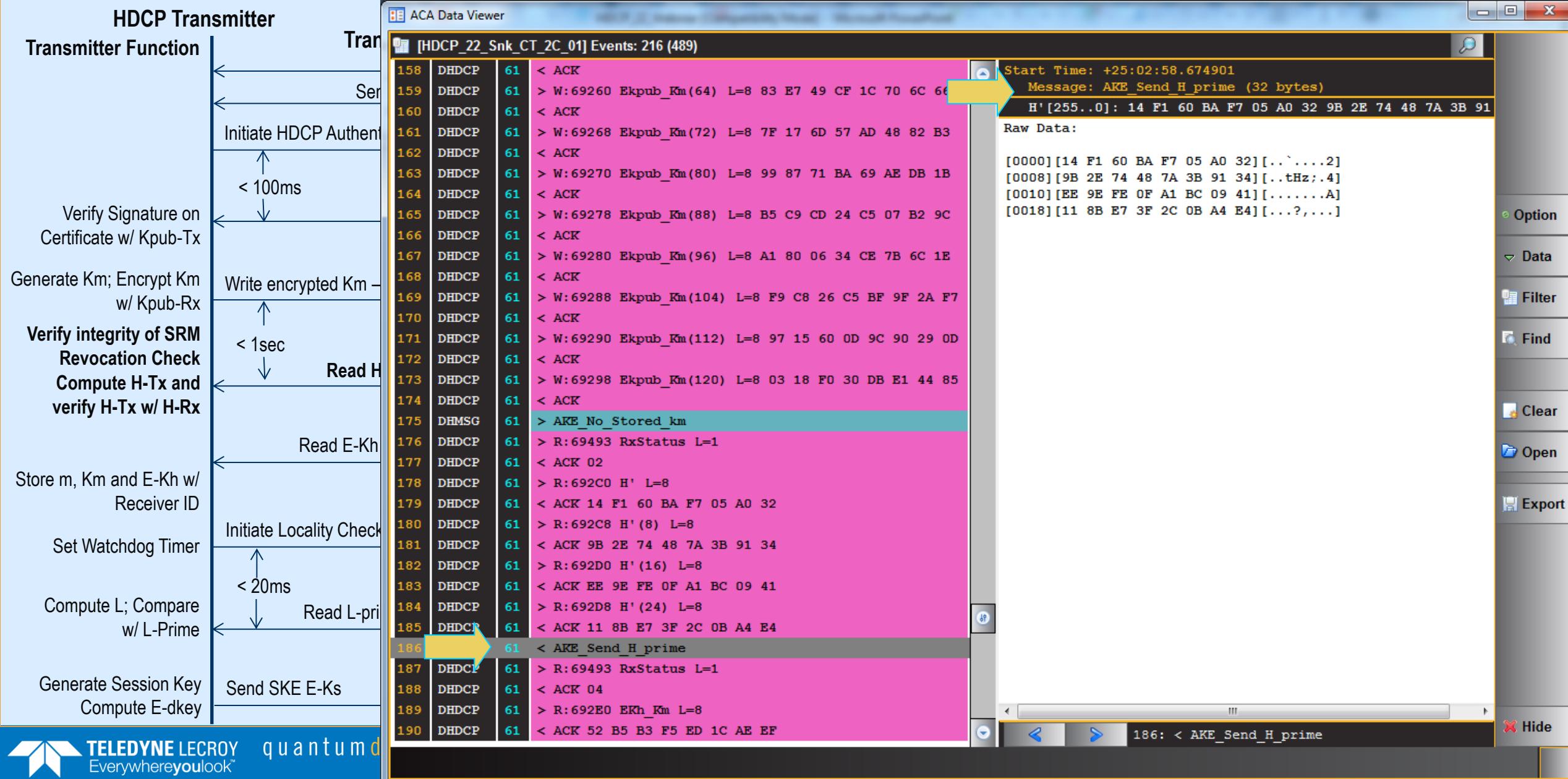
Encrypted Content ( $c$ )

Receiver

RSA Cipher  
(Decrypt)  
 $c^d \pmod{n} = m$

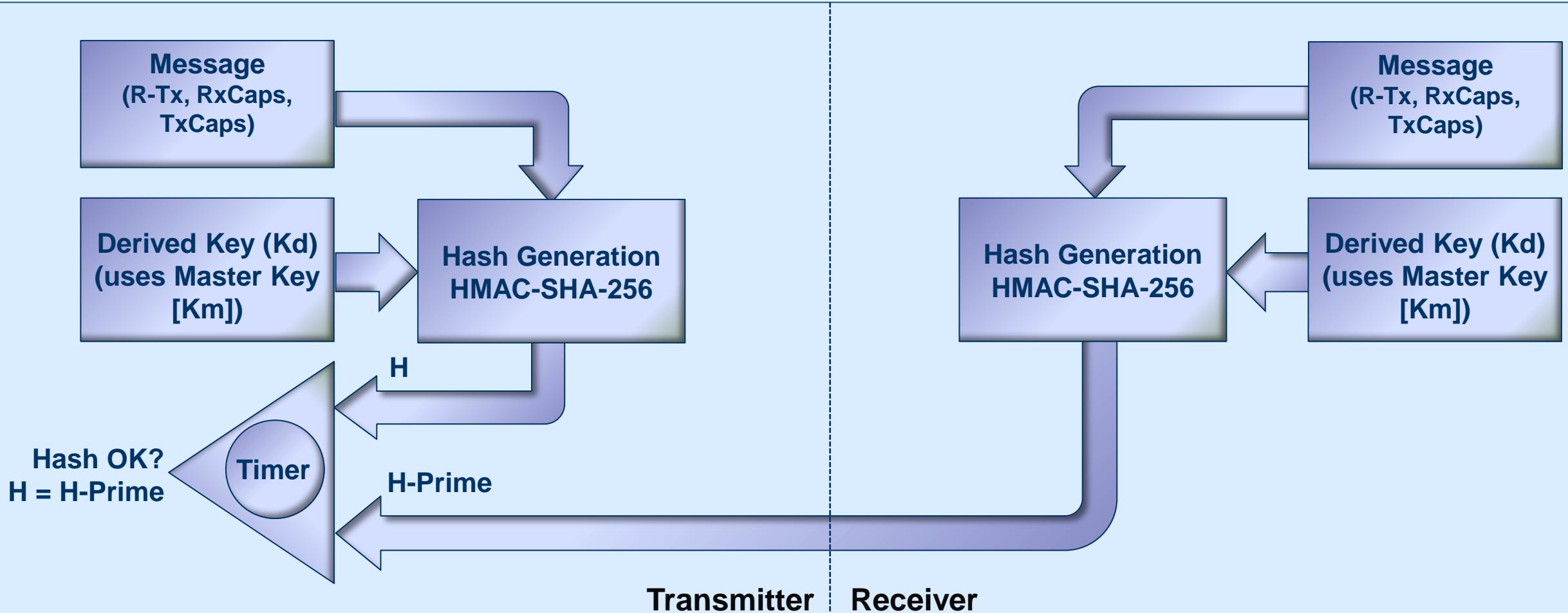
Unencrypted  
Content ( $m$ )

# HDCP 2.2 Sequence – Transmitter Reads Receiver H' to Verify Master Key Exchange



# HDCP 2.2 – Verifying Master Key Exchange & Integrity with H=H-Prime

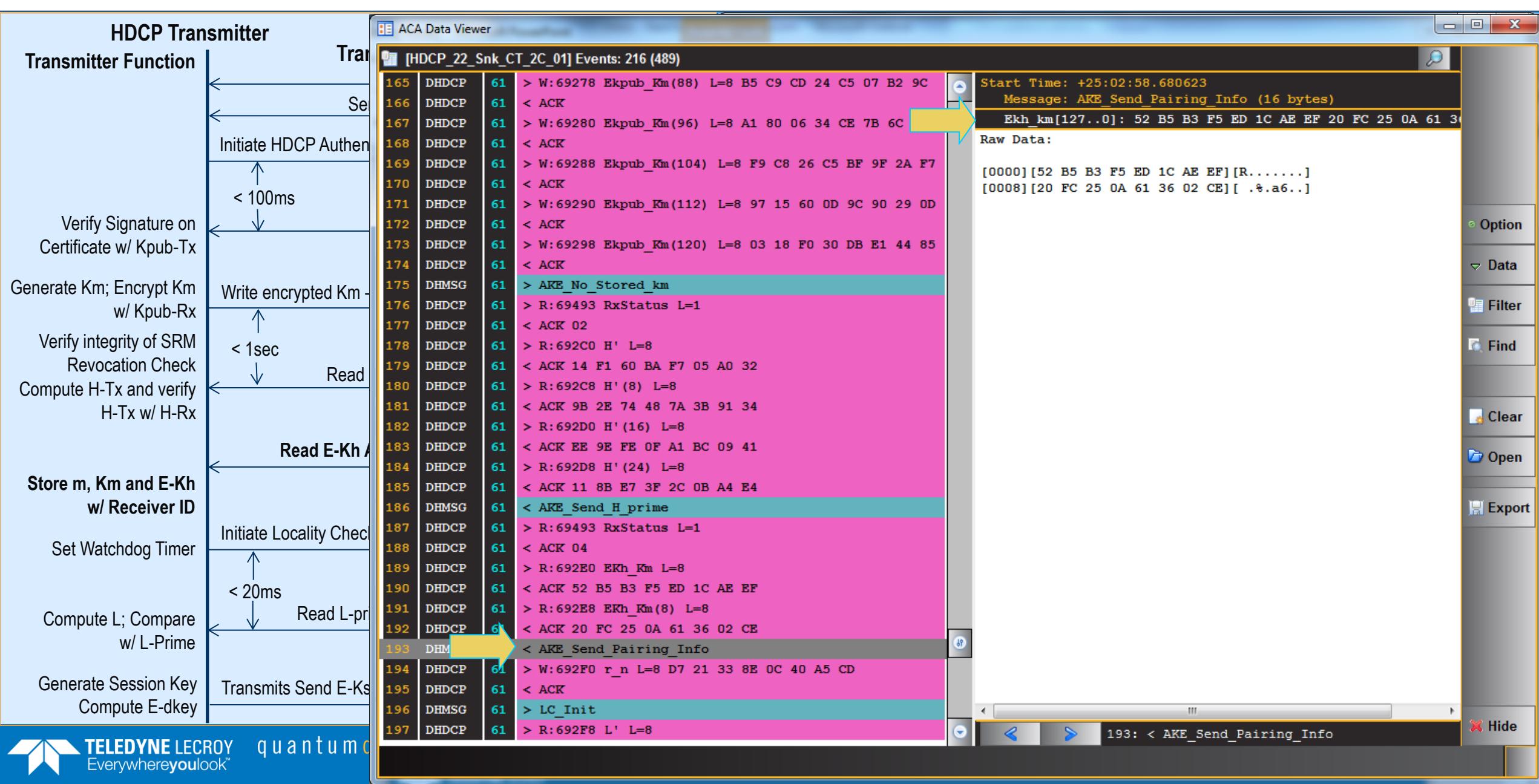
- ◆ Master Key is verified by using the Master key in a hash function by both the Transmitter and Receiver to hash a message comprised of RTx, RxCaps and TxCaps.



---

# HDCP Authentication Pairing

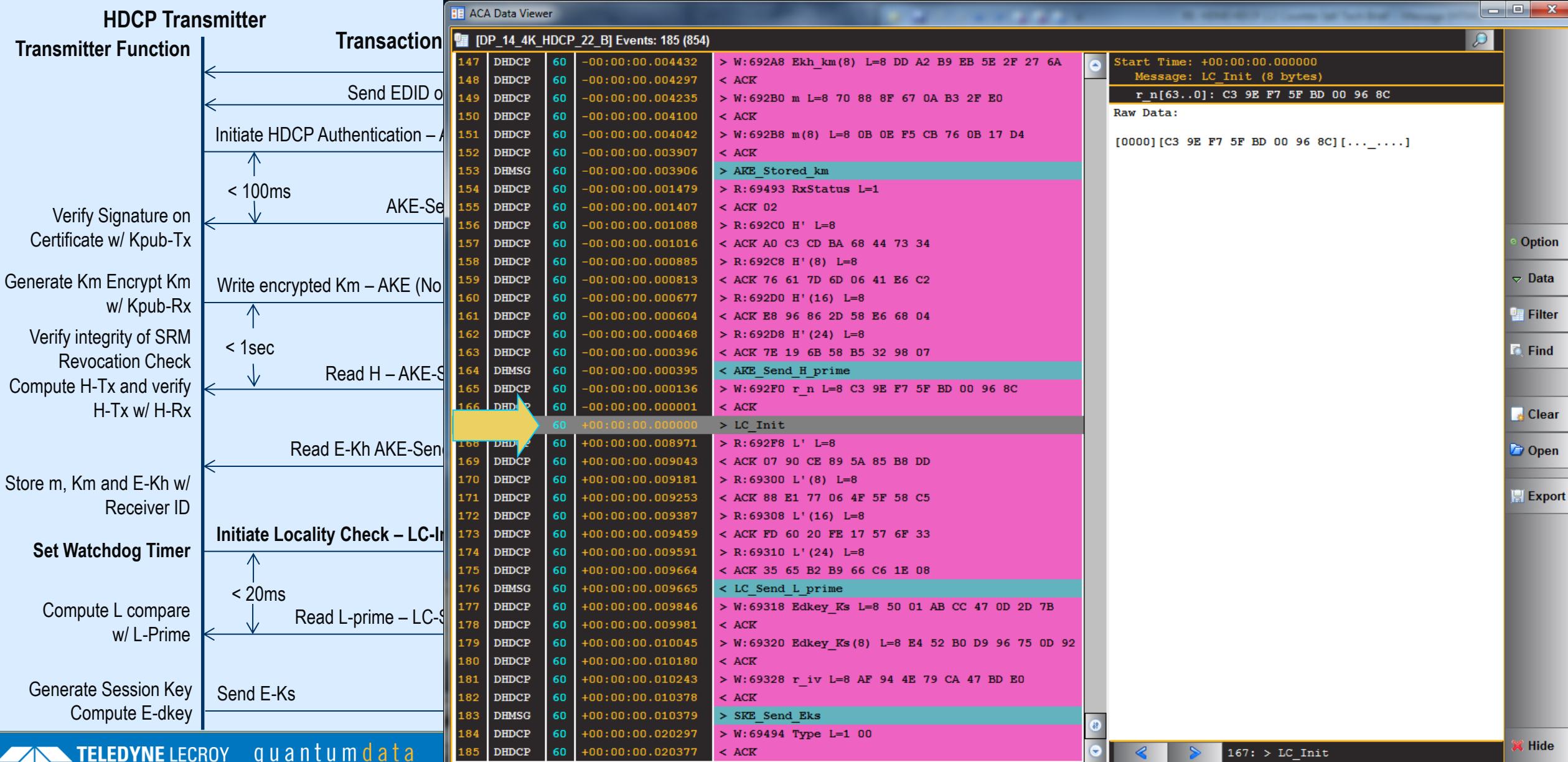
# HDCP 2.2 Sequence – Transmitter Reads Pairing Info



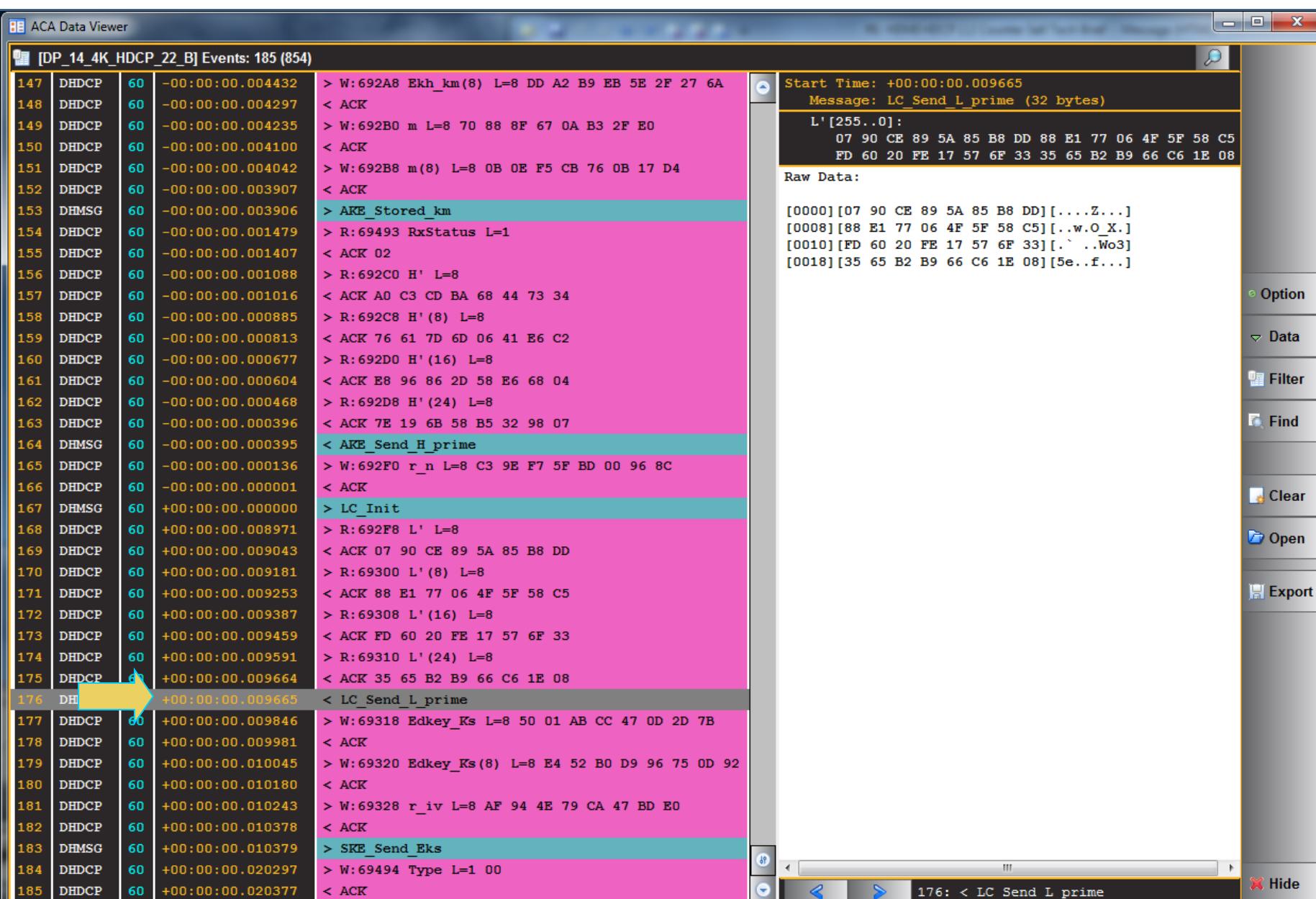
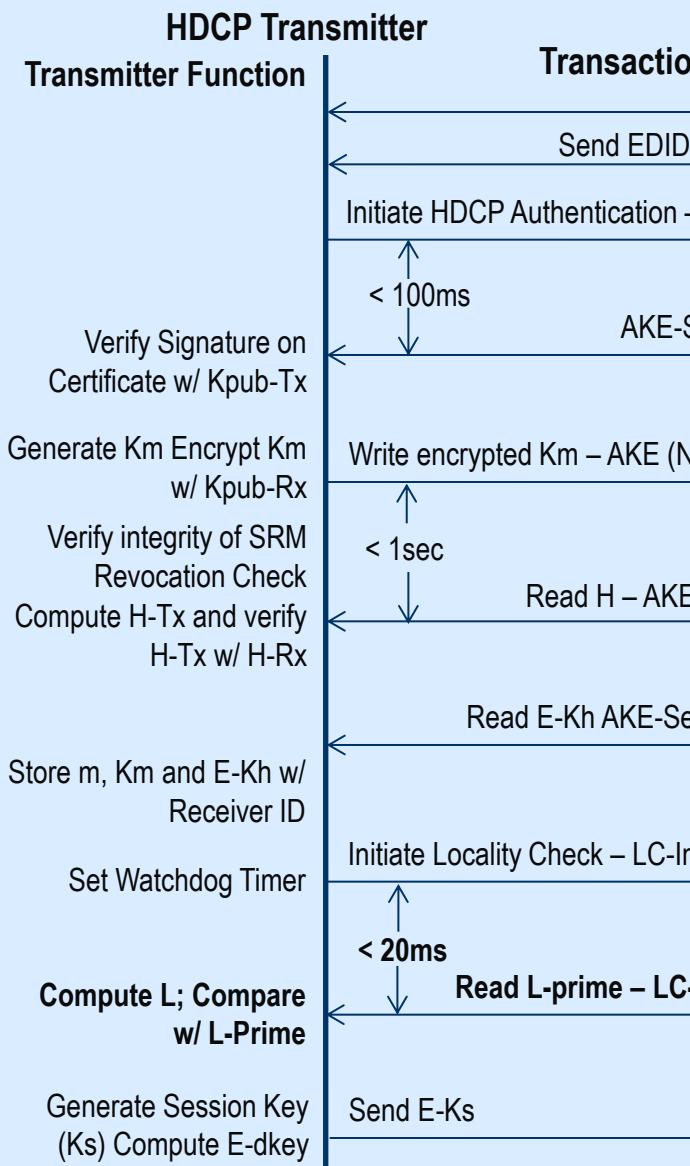
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# HDCP Authentication Locality Check

# HDCP 2.2 Sequence – Transmitter Initiates Locality Check



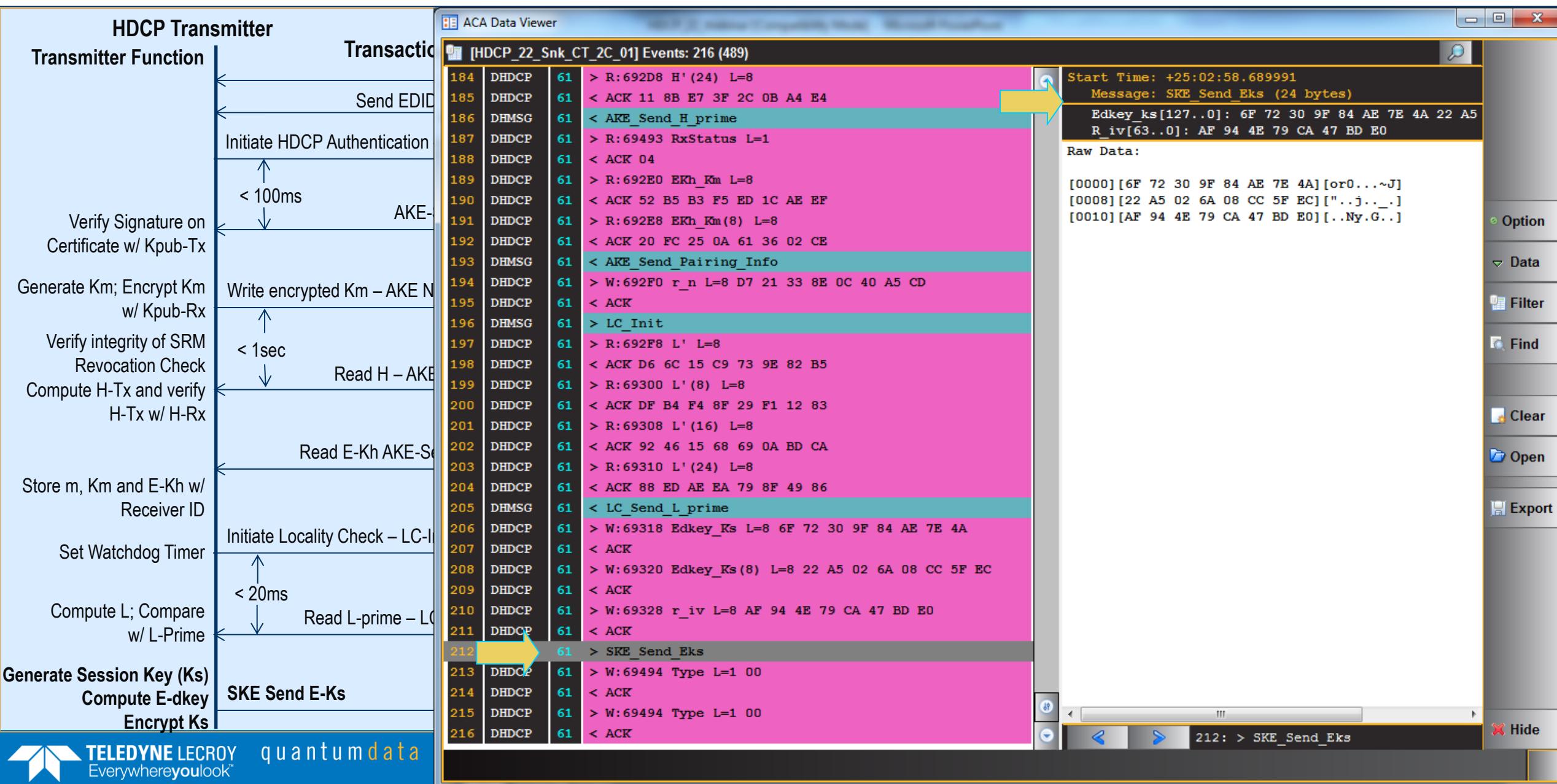
# HDCP 2.2 Sequence – Transmitter Verifies Locality



---

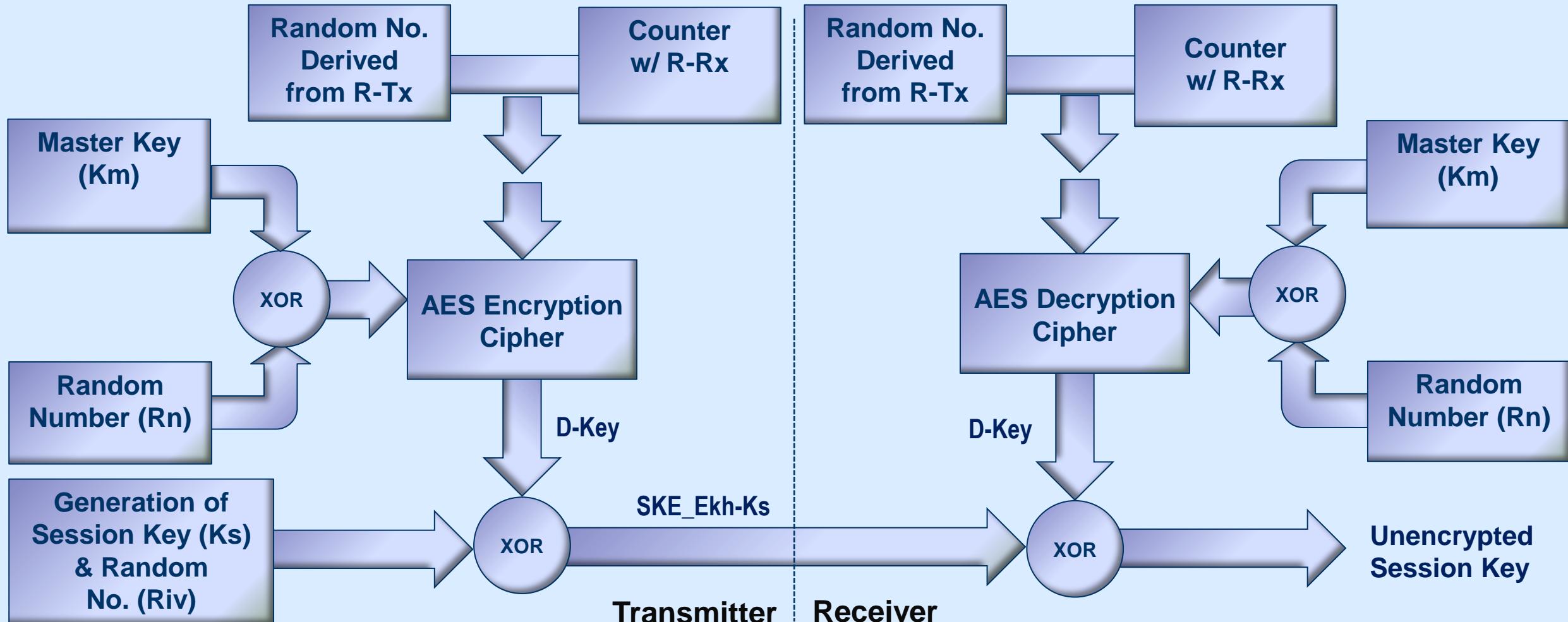
# HDCP Session Key Exchange

# HDCP 2.2 Sequence – Session Key Generation and Exchange



# HDCP 2.2 – Session Key Generation, Encryption and Exchange

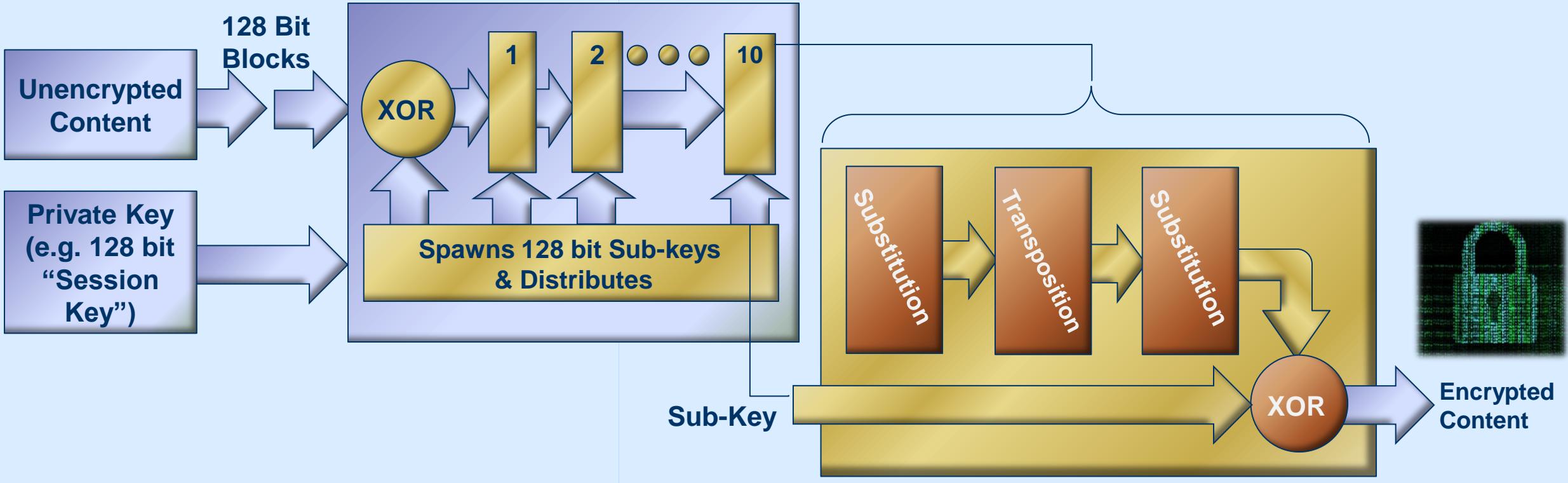
- Since you **now have a secret key** on both sides (i.e. Master Key exchanged via RSA) you can send a secure data (i.e. the Session Key) over the link **using AES** (symmetrical key encryption).



# AES Encryption – How Does it Work?

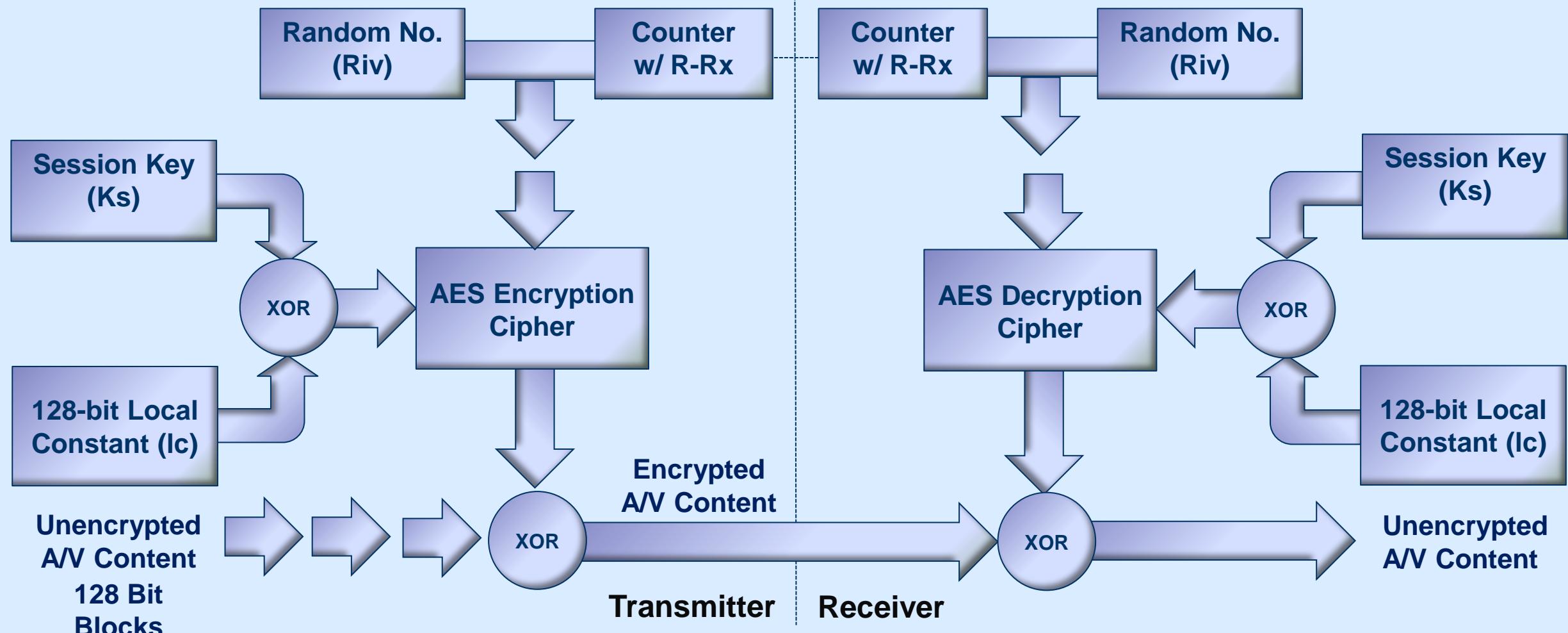
AES Encryption Cipher

- ◆ **Key expansion** – uses Rijndael Key Schedule.
- ◆ **Substitution** – Substituting one “character” of the message for different “character.” Uses lookup tables.
- ◆ **Transposition** – Swapping positions of small pieces of the message. Rows shifted cyclically. Mixing columns.



# HDCP 2.2 – A/V Content Encryption

- The key for the AES core is the Session Key (Ks) XORed with a Secret Global Constant (lc128) that both the Transmitter and Receiver have. We have just exchanged the Session Key.

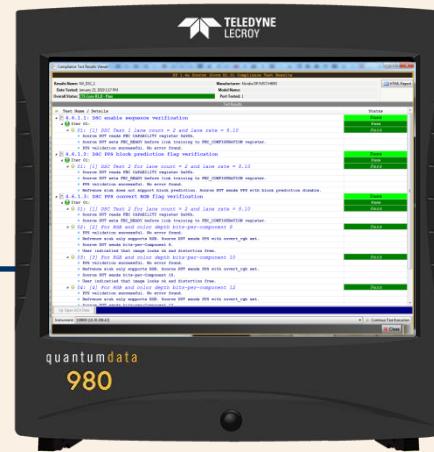


# DisplayPort HDCP Compliance Source Testing

# DisplayPort Source DUT



# DisplayPort Cable



## DP 1.4 Reference Sink

### Example: Teledyne LeCroy quantumdata 980 Test Platform with DP 1.4 Protocol Analyzer / Video Generator

# HDCP Source Compliance Testing – List of Tests

DP HDCP 2.2 TX CT 1.1

Instrument: SS980B [10.30.196.70] Connect Cards...

CDF Entry Test Selection Test Options / Preview

Test List

All ✓ X

Category / Test Name

TX with Receiver

- 1A-01: Regular Procedure: With previously connected Receiver (With stored Km) ✓
- 1A-02: Regular Procedure: With newly connected Receiver (Without stored Km) ✓
- 1A-03: Regular Procedure: Receiver disconnect after AKE Init ✓
- 1A-04: Regular Procedure: Receiver disconnect after Km ✓
- 1A-05: Regular Procedure: Receiver disconnect after locality check ✓
- 1A-06: Regular Procedure: Receiver disconnect after Ks ✓
- 1A-07: Regular Procedure: Receiver sends REAUTH REQ after Ks ✓
- 1A-08: Irregular Procedure: Verify Receiver Certificate ✓
- 1A-09: Irregular Procedure: SRM ✓
- 1A-10: Irregular Procedure: Invalid H' ✓
- 1A-11: Irregular Procedure: Pairing Failure ✓
- 1A-12: Irregular Procedure: Locality Failure ✓
- 1A-13: Regular Procedure - Encryption Disable Bootstrapping ✓

TX with Repeater

- 1B-01: Regular Procedure: With Repeater ✓
- 1B-02: Irregular Procedure: Timeout of Receiver ID list ✓
- 1B-03: Irregular Procedure: Verify V' ✓
- 1B-04: Irregular Procedure: MAX DEVS EXCEEDED ✓
- 1B-05: Irregular Procedure: MAX CASCADE EXCEEDED ✓
- 1B-06: Irregular Procedure: Incorrect seq num V ✓
- 1B-07: Regular Procedure: Re-authentication on HDCP HPD ✓
- 1B-08: Regular Procedure: Re-authentication on REAUTH REQ ✓
- 1B-09: Irregular Procedure: Rollover of seq num V ✓
- 1B-10: Irregular Procedure: Failure of Content Stream Management ✓

Execute Tests

Close

# HDCP 2.2 Source Compliance - Entering the CDF Information

DP HDCP 2.2 TX CT 1.1

Instrument: SS980B [10.30.196.70]

CDF Entry Test Selection Test Options / Preview Connect Cards...

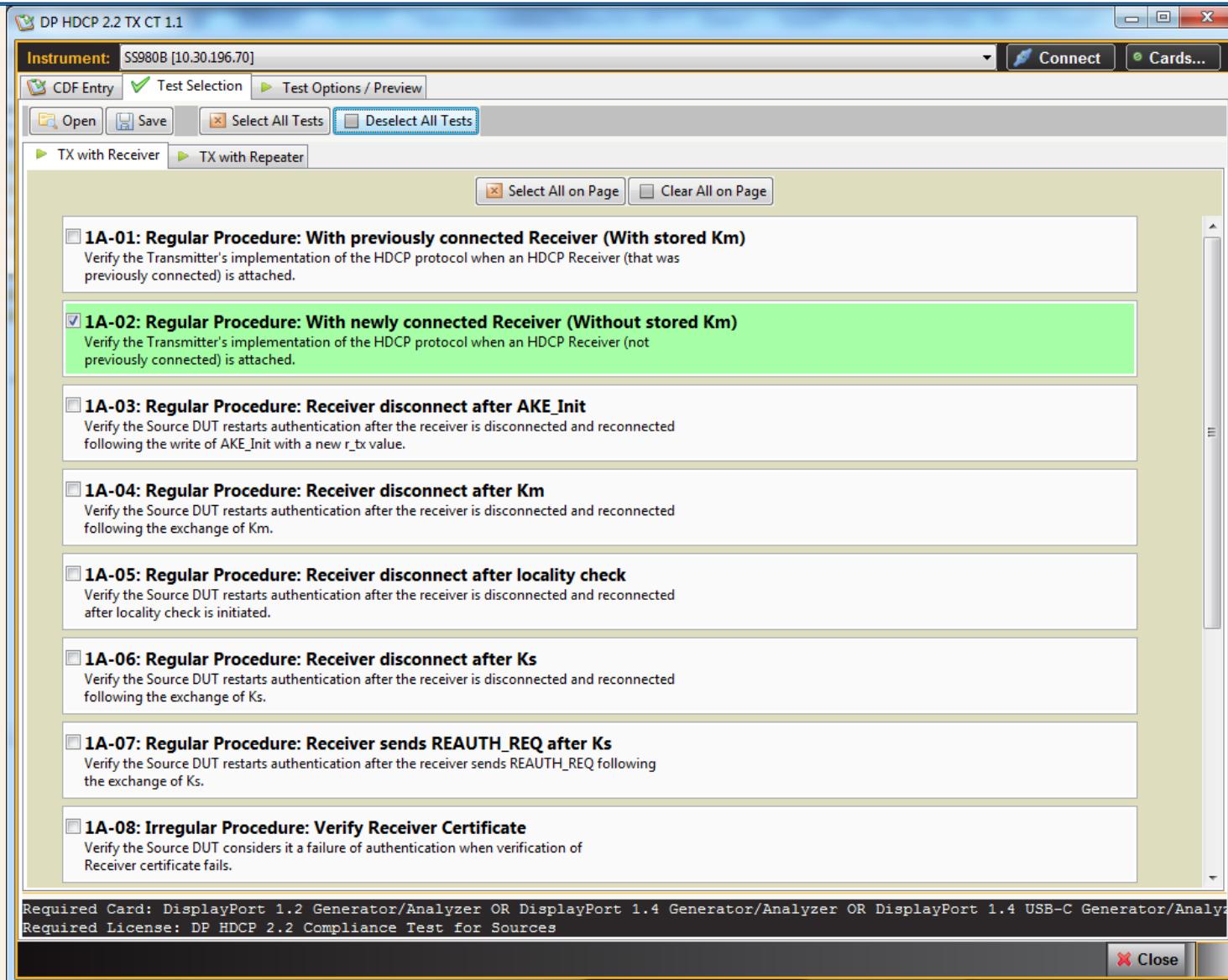
General

Manufacturer	What is the product manufacturer's name? ACME
Model	What is the model name/number of the product? XYZ
Port_Tested	What port is being tested? 1
Source_MultipleOutputs	Does the DUT support transmission of HDCP-protected content to more than one downstream device at the same time? <input checked="" type="radio"/> Yes <input type="radio"/> No
MST_Capable	Does the DUT support MST configuration? <input checked="" type="radio"/> Yes <input type="radio"/> No
SST	Does the DUT support SST configuration? <input checked="" type="radio"/> Yes <input type="radio"/> No
CP_IRQ	Does source support processing of CP_IRQ as per the HDCP2.2 spec? <input checked="" type="radio"/> Yes <input type="radio"/> No
Source_EncDisableBootstrapping	Does the DUT implement encryption disable bootstrapping when encryption is temporarily disabled? <input type="radio"/> Yes <input checked="" type="radio"/> No
Errata_Keys	Use facsimile keys for all tests. <input type="radio"/> Yes <input checked="" type="radio"/> No
DEVICE_COUNT	31 (1-31)
DEPTH	4 (1-4)

**X Close**

- ◆ Capabilities Declaration Form (CDF) must be filled out prior to the running the test.
- ◆ CDF is used by the reference sink to know which HDCP related source features to test.

# HDCP 2.2 Source Compliance Testing – Test Selection



- Select the desired test or tests.
- There are Regular Procedures and Irregular Procedures.

# HDCP 2.2 Source Compliance Testing – Test 1A-02

**Compliance Test Results Viewer**

DP HDCP 2.2

Results Name: DP\_HDCP\_22\_Source\_Comp\_1  
Date Tested: April 5, 2017 6:25 PM  
Overall Status: CTS 1.0 - Pass

Test Name / Details

- 1A-01: Regular Procedure: With previously connected Receiver (With stored Km)
- 1A-02: Regular Procedure: With newly connected Receiver (With stored Km)
- Iter 01:
  - TX AUTH:MSG:HPD\_DIS ts:92028001638.40 us
  - TX UNAUTH::ENTER
  - TX MSGR:Disable ENC\_EN ts:92028001832.96 us
  - TX MSGR:Disable ENC\_EN ts:92028003010.56 us
  - TX UNAUTH:MSG RD:HPD\_DIS ts:92028004055.04 us
  - TX UNAUTH:MSG RD:INVALID\_VER ts:92028002856.96 us
  - TX UNAUTH:MSG RD:INVALID\_VER ts:92028004034.56 us
  - RX UNAUTH::ENTER Rep: no DevCnt:0 Dep:0
  - RX UNAUTH:NO VIDEO Present
  - TX UNAUTH:MSG RD:VALID\_VER ts:92029994352.64 us
  - TX UNAUTH:MSG RD:HPD\_EN ts:92031994531.84 us
  - TX UNAUTH:AKE\_INIT ts:92031995064.32 us
  - TX UNAUTH:MSG RD:AKE\_Init ts:92031995064.32 us
  - RX UNAUTH:RCVD:AKE\_Init ts:92031994992.64 us
  - RX UNAUTH:\*\*Test Cond.\*\* NoStrdKm
  - RX AKE::enter
  - RX MSGR:WROTE to DPCD:AKE\_Send\_Cert:534 ts:92031995064.32 us
  - RX AKE:MSG SND:AKE\_Send\_Cert ts:92032061317.12 us
  - TX UNAUTH:MSG RCVDAKE\_Send\_Cert ts:92032046786.20 us
  - TX UNAUTH:RxCaps 2 0 2
  - TX AKE:Snd\_No\_Stored\_KM ts:92032064819.20 us
  - TX AKE:MSG RD:AKE\_No\_Stored\_km ts:92032064819.20 us
  - RX AKE:MSG RCVDAKE\_No\_Stored\_km ts:92032064757.20 us
  - RX AKE:\*\*Test Cond.\*\* NoStrdKm
  - RX AKE:No Stored KM Received
  - 1A-03: Regular Procedure: Receiver disconnected
  - 1A-04: Regular Procedure: Receiver disconnected
  - 1A-05: Regular Procedure: Receiver disconnected

Instrument: SS980B [10.30.196.155]

**ACA Data Viewer**

[ACA-1A\_02\_01] Events: 724 (1033)

Index	Event Type	Event ID	Timestamp	Message
686	DHDCP	DP-T61	+25:00:59.755899	< ACK
687	DHDCP	DP-T61	+25:00:59.755954	> W:69328 r_iv L=8 AF 94 4E 79 CA 47 BD E0
688	DHDCP	DP-T61	+25:00:59.756089	< ACK
689	DHMSG	DP-T61	+25:00:59.756090	> SKE_Send_Eks
690	DHDCP	DP-R62	+25:00:59.746330	> R:69493 RxStatus L=1
691	DHDCP	DP-R62	+25:00:59.746403	< ACK 02
692	DHDCP	DP-R62	+25:00:59.746482	> R:692C0 H' L=8
693	DHDCP	DP-R62	+25:00:59.746555	< ACK 80 49 64 FF D0 3D B7 15
694	DHDCP	DP-R62	+25:00:59.746681	> R:692C8 H'(8) L=8
695	DHDCP	DP-R62	+25:00:59.746754	< ACK F2 30 17 8B BE 46 4A F4
696	DHDCP	DP-R62	+25:00:59.746877	> R:692D0 H'(16) L=8
697	DHDCP	DP-R62	+25:00:59.746950	< ACK D2 E2 91 C1 36 7B CB OC
698	DHDCP	DP-R62	+25:00:59.747078	> R:692D8 H'(24) L=8
699	DHDCP	DP-R62	+25:00:59.747151	< ACK 45 C9 43 EA F7 C3 F5 19
700	DHMSG	DP-R62	+25:00:59.747152	< AKE_Send_H_prime
701	DHDCP	DP-R62	+25:00:59.747400	> W:692F0 r_n L=8 BA 63 B8 B7 09 DD 8D 6C
702	DHDCP	DP-R62	+25:00:59.747535	< ACK
703	DHMSG	DP-R62	+25:00:59.747536	> LC_Init
704	DHDCP	DP-R62	+25:00:59.754725	> R:692F8 L' L=8
705	DHDCP	DP-R62	+25:00:59.754798	< ACK 32 AD 2B 82 48 6C 78 92
706	DHDCP	DP-R62	+25:00:59.754921	> R:69300 L'(8) L=8
707	DHDCP	DP-R62	+25:00:59.754993	< ACK 29 02 BB AF 41 3B D6 C7
708	DHDCP	DP-R62	+25:00:59.755116	> R:69308 L'(16) L=8
709	DHDCP	DP-R62	+25:00:59.755188	< ACK B1 8C 17 13 7D B4 EB 82
710	DHDCP	DP-R62	+25:00:59.755310	> R:69310 L'(24) L=8
711	DHDCP	DP-R62	+25:00:59.755382	< ACK BE 02 49 10 EB 55 1B 50
712	DHMSG	DP-R62	+25:00:59.755383	< LC_Send_L_prime
713	DHDCP	DP-R62	+25:00:59.755572	> W:69318 Edkey_Ks L=8 A2 1C AB 2E 0E B6 AF 1E
714	DHDCP	DP-R62	+25:00:59.755708	< ACK
715	DHDCP	DP-R62	+25:00:59.755764	> W:69320 Edkey_Ks(8) L=8 C4 00 9F C5 FC 32 B4 D8
716	DHDCP	DP-R62	+25:00:59.755899	< ACK
717	DHDCP	DP-R62	+25:00:59.755954	> W:69328 r_iv L=8 AF 94 4E 79 CA 47 BD E0
718	DHDCP	DP-R62	+25:00:59.756089	< ACK
719	DHMSG	DP-R62	+25:00:59.756090	> SKE_Send_Eks
720	DHDCP	DP-T61	+25:00:59.765952	> W:69494 Type L=1 00
721	DHDCP	DP-T61	+25:00:59.766032	< ACK
722	DHDCP	DP-R62	+25:00:59.765952	> W:69494 Type L=1 00
723	DHDCP	DP-R62	+25:00:59.766032	< ACK

Start Time: +25:00:59.756090  
Message: SKE\_Send\_Eks (24 bytes)  
Edkey\_Ks[127..0]: A2 1C AB 2E 0E B6 AF 1E C4 00 9F C5 FC 32  
R\_iv[63..0]: AF 94 4E 79 CA 47 BD E0

Raw Data:

```
[0000][A2 1C AB 2E 0E B6 AF 1E][.....]
[0008][C4 00 9F C5 FC 32 B4 D8][.....2..]
[0010][AF 94 4E 79 CA 47 BD E0][..Ny.G..]
```

Option

Data

Filter

Find

Clear

Open

Export

Hide

# DisplayPort HDCP Compliance Sink Testing

DP 1.4 Reference Source  
Example: Teledyne LeCroy  
quantumdata 980 Test Platform  
with DP 1.4 Video Generator /  
Protocol Analyzer



DisplayPort Cable

DisplayPort Sink DUT (Monitor/TV)



# HDCP Sink Compliance – List of Tests

DP HDCP 2.2 Receiver CT 1.1

Instrument: SS980B [10.30.196.70] Connect Cards...

CDF Entry Test Selection Test Options / Preview

Test List

All Category / Test Name  Upstream with Transmitter

2C-01: Regular Procedure - With transmitter   
2C-02: Irregular Procedure - New Authentication after AKE Init   
2C-03: Irregular Procedure - New Authentication during Locality Check   
2C-04: Irregular Procedure - New Authentication after SKE Send Eks   
2C-05: Irregular Procedure - New Authentication during Link Synchronization   
2C-06: Regular Procedure - Encryption Disable Bootstrapping

Execute Tests

Close

Test Description	Status
2C-01: Regular Procedure - With transmitter	✓
2C-02: Irregular Procedure - New Authentication after AKE Init	✓
2C-03: Irregular Procedure - New Authentication during Locality Check	✓
2C-04: Irregular Procedure - New Authentication after SKE Send Eks	✓
2C-05: Irregular Procedure - New Authentication during Link Synchronization	✓
2C-06: Regular Procedure - Encryption Disable Bootstrapping	✓

# HDCP Sink Compliance - Entering the CDF Information

DP HDCP 2.2 Receiver CT 1.1

Instrument: SS980B [10.30.196.70] Connect Cards...

CDF Entry Test Selection Test Options / Preview

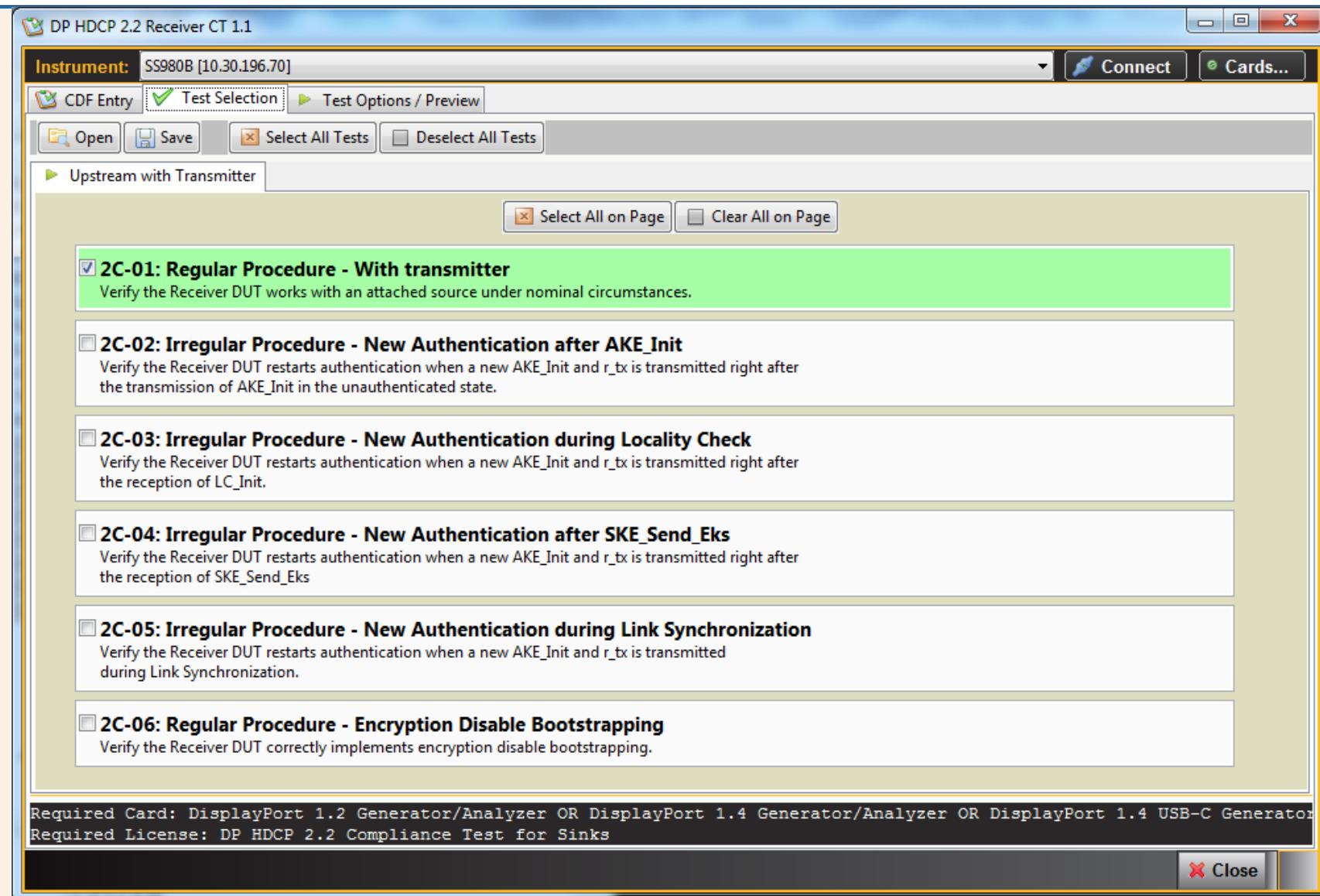
Open New Save Search CDF File: <not saved>

General

Manufacturer	What is the product manufacturer's name? ACME
Model	What is the model name/number of the product? XYZ
Port_Tested	What port is being tested? 1
Sink_EncDisableBootstrapping	Does the DUT implement encryption disable bootstrapping when encryption is temporarily disabled? <input checked="" type="radio"/> Yes <input type="radio"/> No
Errata_Keys	Use facsimile keys for all tests. <input type="radio"/> Yes <input checked="" type="radio"/> No

- ◆ Capabilities Declaration Form (CDF) must be filled out prior to the running the test.
- ◆ CDF is used by the reference sink to know which HDCP related sink features to test.

# DisplayPort Source Forward Error Compliance Testing – Test Selection



- ◆ Select the desired test or tests.
- ◆ There are Regular Procedures and Irregular Procedures.

# HDCP 2.2 Compliance Testing – Sink Regular Test

**Compliance Test Results Viewer**

DP HDCP 2.2 Receiver

Results Name: AA\_Comp\_Monitor\_1  
 Date Tested: March 15, 2017 7:57 PM  
 Overall Status: CTS 1.0 - Pass

Test Name / Details

2C-01: Regular Procedure - With transmitter

- Iter 01: With previously not connected receiver
  - TX:HPD::ENTER
  - TX HPD:\*\*Test Cond.\*\* auth
  - TX UNAUTH::ENTER
  - TX MSGR:Disable ENC\_EN ts:3930584248.32 us
  - TX UNAUTH:AKE\_INIT ts:3932086661.12 us
  - TX UNAUTH:MSG RD:AKE\_Init ts:3932086661.12 us
  - TX UNAUTH:MSG RCVD:AKE\_Send\_Cert ts:3932141537.26 us
  - TX UNAUTH:Rrx 1c,f5,7,94,e6,fa,4,fb
  - TX UNAUTH:RxCaps 2 0 2
  - TX AKE:Snd\_No\_Stored\_KM ts:3932171479.04 us
  - TX AKE:MSG:AKE\_No\_Stored\_km ts:3932171479.04 us
  - TX AKE:MSG RCVD:AKE\_Send\_H\_prime ts:3932203304.96 us
  - TX PAIR:MSG RCVD:AKE\_Send\_Pairing\_Info ts:39322040 us
  - TX LC:Snd LC\_Init ts:3932205240.32 us
  - TX LC:MSG:LC\_Init ts:3932205240.32 us
  - TX LC:MSG RCVD:LC\_Send\_L\_prime ts:3932214272.00 us
  - TX SKE:Snd SKE\_Send\_EKS ts:3932216145.92 us
  - TX:AUTH::ENTER
  - TX AUTH:Snd STRM\_TYPE ts:3932226385.92 us 0
  - TX MSGR:Enable ENC\_EN ts:3932466667.52 us
  - TX AUTH:MSG:SKE\_Send\_Eks ts:0.00 us
  - Transmitted test pattern was visible on the Sink
- Iter 02: With previously connected receiver
- 2C-02: Irregular Procedure - New Authentication
- 2C-03: Irregular Procedure - New Authentication
- 2C-04: Irregular Procedure - New Authentication
- 2C-05: Irregular Procedure - New Authentication
- 2C-06: Regular Procedure - Encryption Disab

Instrument: SS980B [10.30.196.70]

**ACA Data Viewer**

[ACA-2C\_01\_01] Events: 231

Event ID	Protocol	Port	Time	Message
111	DHDCP	DP-T11	+01:04:42.358024	< ACK 78 1B 8C 34 AA 70 F3 9D
112	DHDCP	DP-T11	+01:04:42.358153	> R:691AB cert_rx(416) L=8
113	DHDCP	DP-T11	+01:04:42.358275	< ACK DC B2 11 55 D1 48 43 CA
114	DHDCP	DP-T11	+01:04:42.358402	> R:691B3 cert_rx(424) L=8
115	DHDCP	DP-T11	+01:04:42.358523	< ACK E5 38 FE 4A D9 4E 3C 57
116	DHDCP	DP-T11	+01:04:42.358651	> R:691BB cert_rx(432) L=8
117	DHDCP	DP-T11	+01:04:42.358772	< ACK BD 27 8B 3E B9 9B 52 19
118	DHDCP	DP-T11	+01:04:42.358899	> R:691C3 cert_rx(440) L=8
119	DHDCP	DP-T11	+01:04:42.359021	< ACK DE A0 75 F5 17 25 D5 DA
120	DHDCP	DP-T11	+01:04:42.359148	> R:691CB cert_rx(448) L=8
121	DHDCP	DP-T11	+01:04:42.359269	< ACK A6 10 EC BE D8 41 17 6D
122	DHDCP	DP-T11	+01:04:42.359397	> R:691D3 cert_rx(456) L=8
123	DHDCP	DP-T11	+01:04:42.359519	< ACK DB 7E AC A1 69 00 9F 2C
124	DHDCP	DP-T11	+01:04:42.359646	> R:691DB cert_rx(464) L=8
125	DHDCP	DP-T11	+01:04:42.359767	< ACK 5B 15 EF 23 FF 48 70 FE
126	DHDCP	DP-T11	+01:04:42.359894	> R:691E3 cert_rx(472) L=8
127	DHDCP	DP-T11	+01:04:42.360016	< ACK 99 06 4E DC 25 3B 2C E5
128	DHDCP	DP-T11	+01:04:42.360144	> R:691EB cert_rx(480) L=8
129	DHDCP	DP-T11	+01:04:42.360265	< ACK BE 76 B3 70 FF 20 7E 2C
130	DHDCP	DP-T11	+01:04:42.360393	> R:691F3 cert_rx(488) L=8
131	DHDCP	DP-T11	+01:04:42.360513	< ACK 09 09 24 FF A6 CB 42 55
132	DHDCP	DP-T11	+01:04:42.360642	> R:691FB cert_rx(496) L=8
133	DHDCP	DP-T11	+01:04:42.360763	< ACK 29 F8 17 CE 0E 91 1F 53
134	DHDCP	DP-T11	+01:04:42.369238	> R:69203 cert_rx(504) L=8
135	DHDCP	DP-T11	+01:04:42.369358	< ACK 86 CA 67 CB D3 51 8F E6
136	DHDCP	DP-T11	+01:04:42.369486	> R:6920B cert_rx(512) L=8
137	DHDCP	DP-T11	+01:04:42.369607	< ACK 8C 6E 26 D3 C7 7F 26 0A
138	DHDCP	DP-T11	+01:04:42.369734	> R:69213 cert_rx(520) L=8
139	DHDCP	DP-T11	+01:04:42.369854	< ACK 01 DD 1C F5 07 94 E6 FA
140	DHDCP	DP-T11	+01:04:42.369984	> R:6921B r_rx(6) L=5
141	DHDCP	DP-T11	+01:04:42.370104	< ACK 04 FB 02 00 02
142	DHMSG	DP-T11	+01:04:42.370105	< AKE_Send_Cert
143	DHDCP	DP-T11	+01:04:42.370589	> W:69220 Ekpnb_Km L=8 8C D0 A2 CD 49 F6 73 61
144	DHDCP	DP-T11	+01:04:42.370772	< ACK
145	DHDCP	DP-T11	+01:04:42.370830	> W:69228 Ekpnb_Km(8) L=8 DB 25 82 15 59 C6 A3 26
146	DHDCP	DP-T11	+01:04:42.371013	< ACK
147	DHDCP	DP-T11	+01:04:42.371071	> W:69230 Ekpnb_Km(16) L=8 64 04 3B CD A7 17 9...
148	DHDCP	DP-T11	+01:04:42.371254	< ACK

Start Time: +01:04:42.370105  
 Message: AKE\_Send\_Cert (533 bytes)  
 cert\_rx:[4175..0]  
 Receiver ID: D2 35 F5 C0 9A  
 Receiver Public Key:  
 AC F5 CA 10 B4 E0 38 0A 3F A8 09 9B CF 0D 31 63  
 5E 1B 6F 93 AA 87 7D 36 4C 12 6E FE B1 02 EF 7D  
 D3 32 86 0C 93 8C 9F 6B 12 4B 58 3C E8 0F 42 E7  
 EE 8B 6B BD B6 B3 6D EE 55 68 30 A1 8F B9 0E 9E  
 69 13 C8 F6 DA B8 5C E0 53 A5 FD 0F 0D 0C D8 76  
 F3 E3 2B C2 EB 5D E5 A1 0B 16 05 A4 AE 67 F1 C9  
 8C E8 4B B2 96 26 CB 75 D8 AC 50 5D E7 2B 58 B8  
 30 DA 9C 73 E5 AE 6A F0 58 46 1D F1 A2 D3 BB AF  
 01 00 01  
 RESERVED: 00 00  
 DCP LLC Signature:  
 9B E4 8C C1 B4 5B 76 05 EB 21 35 CE 4A C5 13 12  
 70 B8 A1 4D 0E 6C 84 8B 29 F1 DA 8B CC 50 F4 3F  
 2B FF 92 31 E4 21 77 32 F7 E4 D5 D4 5B D2 5E F5  
 8E EF 4A BA D0 35 16 B4 FA 38 E0 D1 29 B2 58 C2  
 1B 38 7D D5 84 50 29 A0 DC 41 28 8D 69 61 FF 86  
 01 72 06 B6 25 22 42 FD 15 EA DE 85 89 65 97 A1  
 14 89 21 1C 85 1C 7D C0 EB F8 ED 64 D1 61 F6 D9  
 F5 13 18 74 9F 4A 49 9B C8 F0 6A CC CB 02 62 CF  
 FF F3 9F B8 6D CE 04 80 89 06 DB E5 C7 48 63 C2  
 8C AD 0A E4 F0 0D 66 98 82 81 35 0F 57 51 1B 76  
 F2 A1 D2 39 CB 95 D9 36 86 57 E2 54 28 1F EB AD  
 CC F7 D0 2B D3 0C 12 97 BB FA 83 6D 0E A4 47  
 89 55 9C 75 36 87 2B 31 CF 3F 20 48 2E 47 38 57  
 D1 C5 29 99 08 29 1D 7D 39 8E CB 57 65 F4 3F 9C  
 2C BE A9 56 AF 4B 39 A0 21 51 7C 7B 36 6E FF 37  
 58 9B 2F 00 50 CE 34 BC B1 8B F6 2C B2 E5 32 7C  
 C2 D3 94 76 49 81 A7 76 D8 CB BA FF 80 EB 78 1B  
 8C 34 AA 70 F3 9D DC B2 11 55 D1 48 43 CA E5 38  
 FE 4A D9 4E 3C 57 BD 27 8B 3E B9 9B 52 19 DE A0  
 75 F5 17 25 D5 DA 6A 10 EC BE D8 41 17 6D DB 7E  
 AC A1 69 00 9F 2C 5B 15 EF 23 FF 48 70 FE 99 06  
 4E DC 25 3B 2C E5 BE 76 B3 70 FF 20 7E 2C 09 09  
 24 FF A6 CB 42 55 29 F8 17 CE OE 91 1F 53 86 CA  
 67 CB D3 51 8F E6 8C 6E 26 D3 C7 7F 26 0A 01 DD  
 r\_rx[63..0]: 1C F5 07 94 E6 FA 04 FB  
 RxCaps: 02 00 02  
 REPEATER: false  
 CAP MASK: 0000h  
 HDCP\_CAPABLE: true (DisplayPort Only, not HDMI)  
 VERSION: 2

142: < AKE\_Send\_Cert

142 Hide



# Thank you for your Attention

Please contact me, Neal Kendall at:

[neal.kendall@teledyne.com](mailto:neal.kendall@teledyne.com)

If you have any questions.



**980B Test Platform**  
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- ◆ [Essentials of DisplayPort Display Stream \(DSC\) Protocols](#)
- ◆ [Essentials of DisplayPort Link Layer Compliance Testing](#)
- ◆ [Essentials of DisplayPort Forward Error Correction \(FEC\)](#)
- ◆ [Essentials of DisplayPort USB-C DP Alt Mode Protocols](#)

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