**Low Power ALU Design using Pass Transistor Logic.**

Dr.A.Balamanikandan Yatham.Srinivas Pathuri.Sreekanth

Associate Professor, Dept of ECE UG Student, Dept of ECE UG Student, Dept of ECE

Mohan Babu University (Erstwhile Mohan Babu University Mohan Babu University

SreeVidyanikethan Engineering Tirupati, India. Tirupati, India.

College), Tirupathi, India. [yathamsrinivas686@gmail.com](mailto:yathamsrinivas686@gmail.com) [pathurishree8688@gmail.com](mailto:pathurishree8688@gmail.com)

[balamanieee83@gmail.com](mailto:balamanieee83@gmail.com)

Nelluri.Harshitha Sk.Mohammad Sameer

UG Student, Dept of ECE UG Student, Dept of ECE

Mohan Babu University Mohan Babu University

Tirupati, India. Tirupati, India.

[nelluriharshitha112@gmail.com](mailto:nelluriharshitha112@gmail.com) [mohammedsameer@5726@gmail.com](mailto:mohammedsameer@5726@gmail.com)

**ABSTRACT**

The growing requirement for power-saving digital systems demands low-power Arithmetic Logic Units (ALUs). In this paper, a new ALU is designed based on Pass Transistor Logic (PTL) for lower power dissipation, less transistor utilization, and faster speed. Circuits based on PTL make use of the ability of MOS transistors to pass the signal directly without requiring any extra logic, and with fewer switching elements than regular CMOS logic. The ALU proposed here does basic arithmetic and logic operations like addition, subtraction, AND, OR, and XOR using optimized power efficiency. Important methods like transmission gates and clock gating are used to reduce voltage degradation and leakage currents. Simulation results show that the ALU based on PTL reduces dynamic as well as static power dissipation substantially without any compromise in functionality. This design philosophy is very apt for low-power applications such as embedded systems, IoT devices, and portable electronics.

**Keywords:**

Cadence Tool, Pass Transistor Logic, ALU, CMOS Logic, Clock Gating.