Basic Gates:-

Design of Basic gate using pass transistor logic where one of NMOS is replaced by PMOS

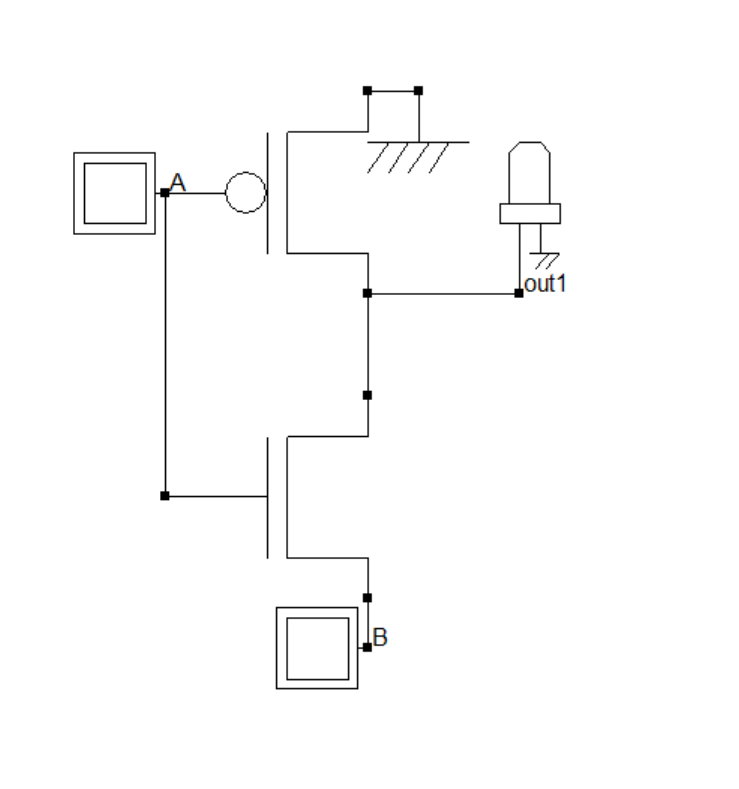
AND gate

It consist of One PMOS where source is connected to GND ,Drain to O/p and Gate to one of input A and One NMOS where source is connected to another input B ,Drain to O/p and Gate to one of input A

The circuit is designed based on truth table where one of input consider as the control input and other input pass to the output according to control input

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **A** | **B** | Y=A\*B | PMOS | NMOS | Output |
| 0 | 0 | 0 | ON | OFF | GND |
| 0 | 1 | 0 | ON | OFF | GND |
| 1 | 0 | 0 | OFF | ON | B=0 |
| 1 | 1 | 1 | OFF | ON | B=1 |

Circuit Diagram:-



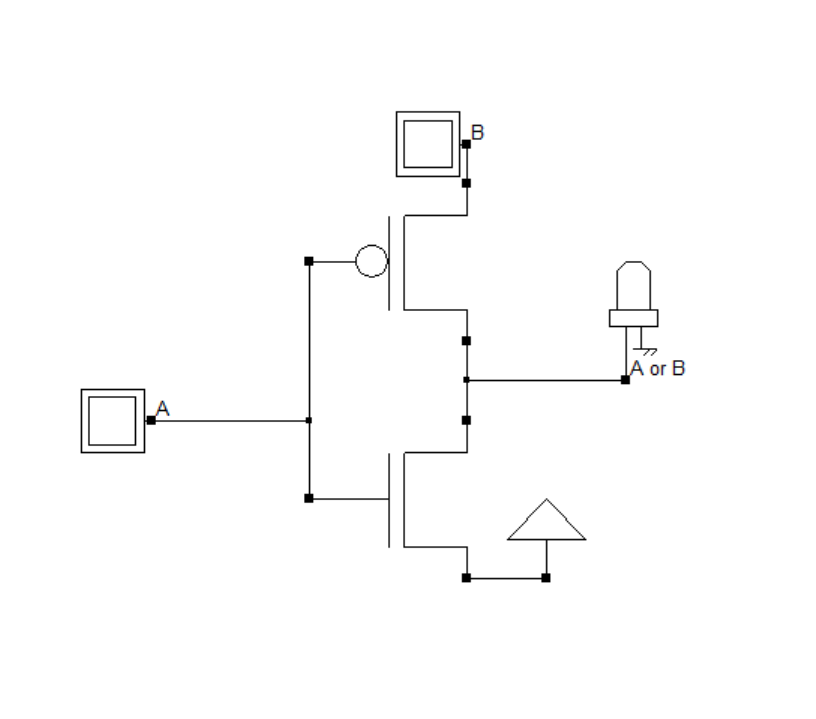
OR gate

It consist of One PMOS where source is connected to another Input B ,Drain to O/p and Gate to one of input A and One NMOS where source is connected to Vdd ,Drain to O/p and Gate to one of input A

The circuit is designed based on truth table where one of input consider as the control input and other input pass to the output according to control input

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **A** | **B** | Y=A OR B | PMOS | NMOS | Output |
| 0 | 0 | 0 | ON | OFF | B=0 |
| 0 | 1 | 1 | ON | OFF | B=1 |
| 1 | 0 | 1 | OFF | ON | Vdd |
| 1 | 1 | 1 | OFF | ON | Vdd |

Circuit Diagram:-



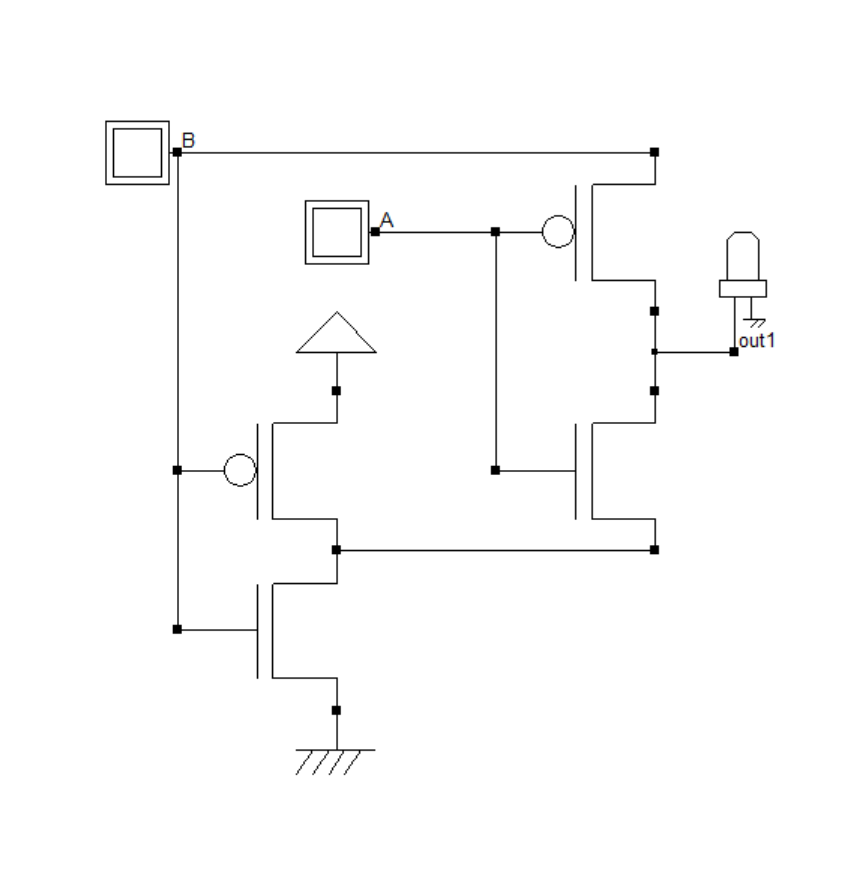
XOR gate

It consist of One PMOS where source is connected to another Input B ,Drain to O/p and Gate to one of input A and One NMOS where source is connected to input invert of B ,Drain to O/p and Gate to one of input A

The circuit is designed based on truth table where one of input consider as the control input and other input pass to the output according to control input

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **A** | **B** | Y=A XOR B | PMOS | NMOS | Output |
| 0 | 0 | 0 | ON | OFF | B=0 |
| 0 | 1 | 1 | ON | OFF | B=1 |
| 1 | 0 | 1 | OFF | ON | ~B=1 |
| 1 | 1 | 0 | OFF | ON | ~B=0 |

Circuit Diagram



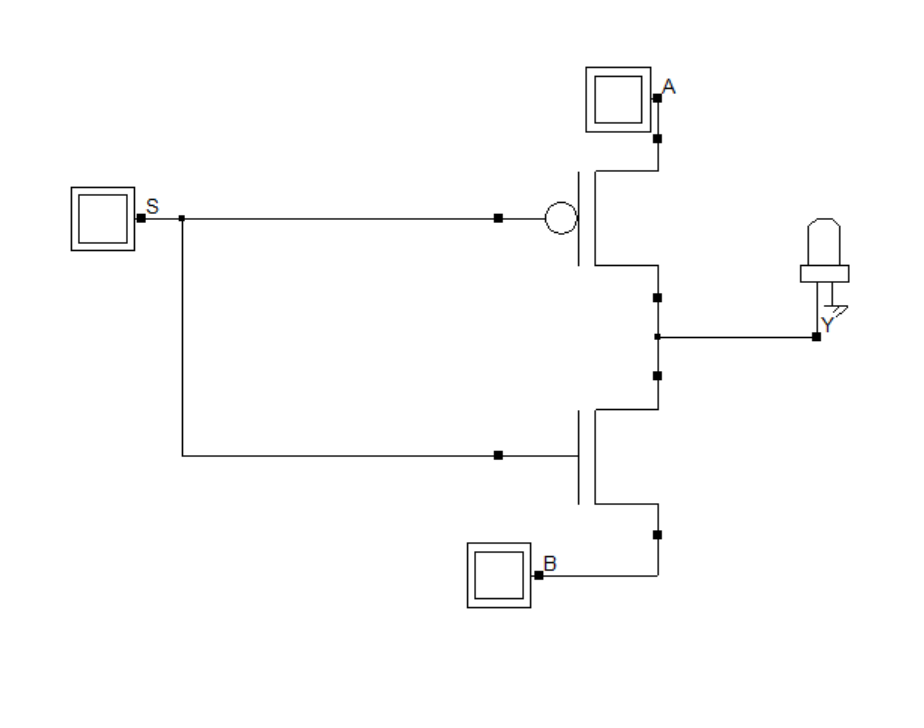
2:1 Multiplexer

It consist of One PMOS where source is connected to another Input A ,Drain to O/p and Gate to input SELECT and One NMOS where source is connected to Input B ,Drain to O/p and Gate to input SELECT

The circuit is designed based on truth table where one of input consider as the control input and other input pass to the output according to control input

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| DATA | SELECT | OUTPUT | PMOS | NMOS | OUTPUT |
| A | 0 | A | ON | OFF | A |
| B | 1 | B | OFF | ON | B |

Circuit Diagram



Using above basic gate and Mux’s Low power ALU is designed

ALU with two inputs A and B of each four bits ,opcode of 4 bit and A/B switch for single operand operations with output of 4 bit and Cout.

ALU For RISC Processor consist of mainly four types of operations :  
1.Arithmatic operations  
 1.1 Addition

1.2 Subtraction

2.Bitwise operations

2.1 Bitwise AND operation

2.2 Bitwise OR operation

2.3 Bitwise XOR operation

2.4 Bitwise NOT operation

3.Logical shift operations

3.1 Logical Right Shift

3.2 Logical Left Shift

4.Arithmatic Shift

4.1 Arithmatic Right Shift

4.2 Arithmatic Left Shift

ADDITION

Ripple adder based design

Half adder :-1 xor and 1 and gate

Full adder:- 2 half adder and 1 or gate

Ripple:-4 Full adder

Subtraction:-

Ripple adder with xor operation design

Ripple adder with XOR gates

Bitwise operations:

Basic gate based design

And Operation:

Four and gates

OR Operation:

Four OR gates

XOR Operation:

Four XORgates

NOT Operation:

Four NOT gates  
Logical shift operations:

MUXs based design

Logical right:-4:1 DeMux’s four

Logical Left:- 4:1 DeMux’s four

Arithmatic shift operations:-

MUXs based design

Arithmatic right:-4:1 DeMux’s four

Arithmatic Left:- 4:1 DeMux’s four

Opcode: Operation

3 Addition

F Subtraction

E Bitwise AND operation

A Bitwise Or Operation

6 Bitwise XOR Operation

2 A/B=0 NOT of A

2 A/B=1 NOT of B

1 A/B=0 Logical right shift of A

1 A/B=1 Logical right shift of B

D A/B=0 Logical Left shift of A

D A/B=1 Logical Left shift of B

0 A/B=0 Arithmetic right shift of A

0 A/B=1 Arithmetic right shift of B

C A/B=0 Arithmetic Left shift of A

C A/B=1 Arithmetic Left shift of B