PAVAN KUMAR M

(Design Verification Engineer)

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CAREER OBJECTIVE

An enthusiastic individual seeking a job role in a reputable organization, aiming to join a dynamic team of professionals as a VLSI Design & Verification Engineer where I can share my expertise and contribute to the success of the organization.

Work Experience

Working as Design Verification Engineer at Agasthya App Labs Pvt. Ltd from (Oct 2020 - Till date) currently working for client Wipro (AMD Project).

Technical Skills

HDL	: Verilog
HVL	: System Verilog, SVA
TB Methodology	: UVM
EDA Tool	: NCSim (Cadence), Synopsys Verdi, Model Sim, Quartus Prime,Questasim.
Operating System	: Windows, Linux
Text Editor	: VIM Editor
Version Control	: SVN
Core Skills	: RTL Coding using Synthesizable constructs of Verilog, FSM based design, Simulation, Synthesis, Coverages

SKILL DESCRIPTION

- Experience in building UVC's in UVM environment.
- working experience on AMBA (APB) Protocol verified using UVM Test Bench.
- Experience in writing Functional Coverage, Constraints and Assertions.
- Good Knowledge of assertion languages like System Verilog Assertions (SVA) for specifying design properties and constraints.
- Experience in creating randomized test scenarios to stress the design under various conditions.
- Proficiency in using simulation tools like Model Sim, Cadence NCSim, Questasim , Synopsys Verdi for running simulations and debugging designs.
- Strong analytical and problem-solving skills for identifying and resolving issues.
- Effective communication skills for collaborating with cross-functional teams, documenting test plans, and reporting verification results.

PROJECT DETAILS

Project (1): Canis - CDP Interrupts (APIC/AVIC/X2APIC)

Description:

APIC/AVIC/X2APIC serves the function of receiving interrupts, prioritizing them and dispatching them to CPU for service by an interrupt handler, interrupts are dispatched to cpu via writes to INTREDGE reg over a probe channel also Apic sends interrupt itself and other apics, DF includes one apic for local cpu core.

Roles and Responsibilities:

- Understanding the specification document of Interrupts.
- Understand the functionality and configs on CDP Interrupts.
- Implemented test cases as per the specification.
- Debugging the failure cases in regression (CRDB Portal) - identifying the root cause, back tracing to find source of bug and fixing failures on different error signatures.
- Jira management, p4 command usage, sqf submission, investigating p4v server.
- Maintained detailed records of the verification process, including test plans, test cases, test results and verification report.

Languages and tools used: System Verilog, UVM / Synopsys Verdi

Project (2): Register map validation in soc or subsystem using APB

Description:

The APB SoC Verification Project is dedicated to the thorough verification of the monitor register access functionality within a complex System-on-Chip (SoC) design. This project focuses on verifying that the monitor registers can be accessed and configured correctly through the Advanced Peripheral Bus (APB) interface, ensuring precise control and observation of SoC performance and debug features.

Roles and Responsibilities:

- Developed Test plan by going through the Register specification document.
- Understand the functionality and configuration options for each register.
- Implemented Register models for all registers as per the specification.
- Create test scenarios that exercise different register configurations and sequences.
- Developed test scenarios on negative scenarios for error testing.
- Debugged the failure test cases.
- Implemented a coverage monitor to make sure all the register bits are accessed

Languages and tools used: System Verilog, UVM / Cadence NCSI

Project (3): PCIE Physical layer Serdes Verification

Description:

PCIE SerDes Phy layer is composed of the TX and RX modules. Its inputs are the 4 8-bit signals and their respective validity (which first enter the TX module) and its outputs correspond to 4 8-bit signals and their validity, which come from the RX module and another 4 outputs that come from the recirculation. Its internal connections are from the output of the parallel to serial module of the TX to the serial to parallel of the RX (data flow), and from the output of the parallel to serial of the RX to the serial to parallel of the TX (idle signal), both signals They are 1 bit and have a frequency of 2.5 GHz

Roles and Responsibilities:

- Gone through relevant documents and specifications
- Testing of Muxes and De-Muxes in the intermediate layers.
- Dataflow testing on individual phy-rx and phy-tx modules.
- Data integrity of SerDes by connecting Serial-parallel and parallel-serial modules
- I have Debugged the failure cases
- Code coverage and functional coverage closure Implemented regression testing to ensure that design changes and updates do not introduce new issues or regressions.

Languages and tools used: System Verilog, UVM / **Cadence** NCSIM

Project (4): Router 1x3

Description:

The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1 and channel2.

Roles and Responsibilities:

- Architected the block level structure for the design.
- Implemented RTL using Verilog HDL.
- Architected the class-based verification environment using System Verilog
- Verified the RTL model using System Verilog.
- Generated functional and code coverage for the RTL verification sign-off
- Synthesized the design.

Languages and tools used: System Verilog, UVM / Synopsys Verdi

EDUCATIONAL DETAILS:

College / School	University / Syllabus	Branch / Class	Duration	Percentage / CGPA
Don Bosco Institute of Technology	Visvesvaraya Technological University	Electronics & Communication Engineering	2017 - 2020	7.23

DECLARATION

I hereby declare that above details are true and correct to the best of my knowledge and belief.

DATE:

PLACE: **Pavan kumar M**