Initial Project Report

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Project Scope

1. Registers containing Meta-data

- Method of encoding both data and metadata (e.g., bit-width, flags) within a 64-bit register, which is implemented as an array of structs with members as data and metadata.
- Specify conventions or simple ISA extensions for using registers in this "struct" mode.
- Implement the approach in simulation.
- Evaluate efficiency and flexibility as compared to the traditional registers usage.
- Example application: optimized arithmetic operations, e.g. performing 5-bit addition instead of 64-bit, for the addition of two 5-bit integers.
- Potential for adding more specific use cases as the project progresses.

2. Register Packing

- Explore dynamic partitioning of registers to pack multiple narrow-width operands per register, inspired by Ergin Register Packing.
- Extend a RISC-V simulator to support dynamic register partitioning and management.

Implementation Steps

- Design and code encoding of data and metadata in registers as arrays of structs.
- Extend the RISC-V simulator to incorporate register packing and management features.

- Simulate register width tracking, allocation logic, and packed instruction execution.
- Conduct experiments using micro-benchmarks to measure performance impact.
- Analyze improvements in register file utilization, resource efficiency, and limitations.
- Document benefits and potential drawbacks observed during testing.

Verification Plan

- Use simulation to test the encoding scheme and register packing mechanisms.
- Prepare test workloads with varying data widths to validate accuracy and efficiency.
- Compare performance and resource usage between the original and enhanced register systems.

Project Results

- ISA extensions for both approaches.
- Source code patches for the RISC-V simulator capturing the new features.
- Description of workloads for different test-cases.
- Comparative analysis of original versus enhanced designs.
- Benefits and trade-offs of each method.

Work Partitioning

- Sriraj: Responsible for designing the register encoding scheme, defining ISA extensions, and implementing the array-of-structs register simulation.
- Gagan: Focus on extending the RISC-V simulator to support register packing, implementing allocation logic, and conducting benchmark experiments.
- Both team members collaborate on testing, performance analysis, and documentation.