Two input NAND gate design using CMOS technology

Sriram G V

Sastra Deemed to be University, Thanjavur.

***Abstract*—** Complementary metal–oxide–semiconductor (CMOS) is a type of MOSFET fabrication process that uses complementary and symmetrical pairs of p-type and n-type MOSFETs for logic functions. CMOS technology is used for constructing IC chips, including microprocessors, microcontrollers, memory chips and other digital logic circuits. CMOS technology is also used for analog circuits such as image sensors (CMOS sensors), data converters, RF circuits (RF CMOS), and highly integrated transceivers for many types of communication.

Reference circuit details-

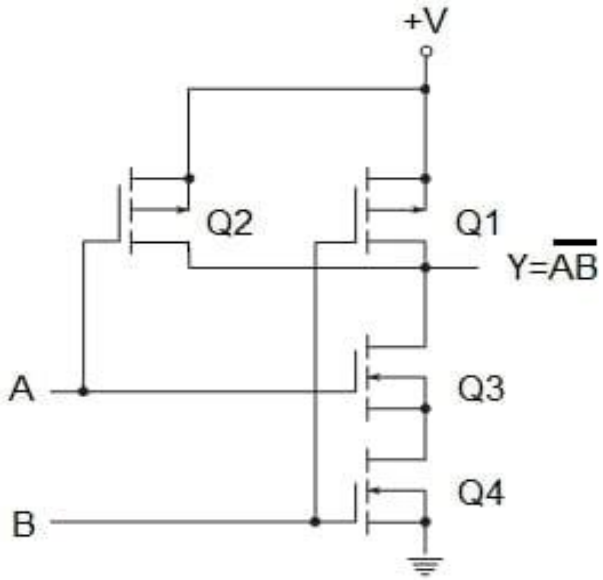
Figure 1 shows a CMOS two-input NAND gate. P-channel transistors Q1 and Q2 are connected in parallel between +V and the output terminal. N-channel transistors Q3 and Q4 are connected in series between the output terminal and ground. With Q3 and Q4 transistors “on” and Q1 and Q2 transistors “off”, the output is a logic 0. This condition happens when both inputs, A and B, are logic 1.

With logic 0 in inputs A and B, Q3 and Q4 transistors are “off”, and Q1 and Q2 transistors are “on”, producing a logic 1 output.

When one of the inputs is a logic “1” and the other one is a logic “0”, either Q3 is “off” and Q2 is “on” or Q4 is “off” and Q1 is “on.” The output in both cases is a logic “1”. The truth table for a NAND gate is as follows,

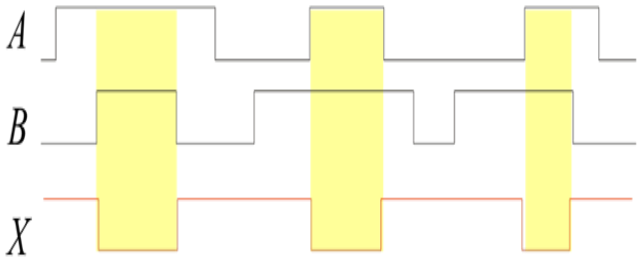
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Reference circuit design-



(Figure 1)

Reference circuit waveform



References-

- International Journal of Scientific & Engineering Research, Volume 7, Issue 1, January-2016 ISSN 2229-5518
- https://eepower.com/technical-articles/basic-cmos-logic-gates/#