Chapter-2
Electronic Devices & Circuits

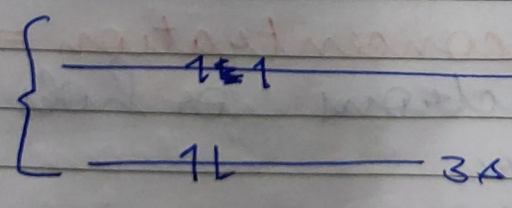
→ BASIC CONCEPTS

Insulators	Semi-conductors	conductors
	10^{-8} S/cm	10^{8} S/cm

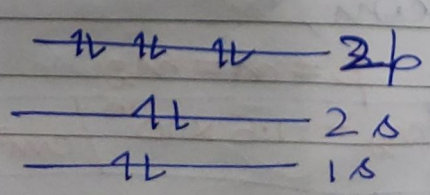
- conductivity of semi-conduc. can be changed using electric field or potential difference.
- Carbon can be used as semi-cond. if its atoms are arranged in diamond shape.

→ Silicon as semiconductor →

- Atomic no. = 14
- Silicon lattice has diamond all structure of unit cell (2 interpenetrating FCC lattices)
- In an isolated Si atom, we have energy states



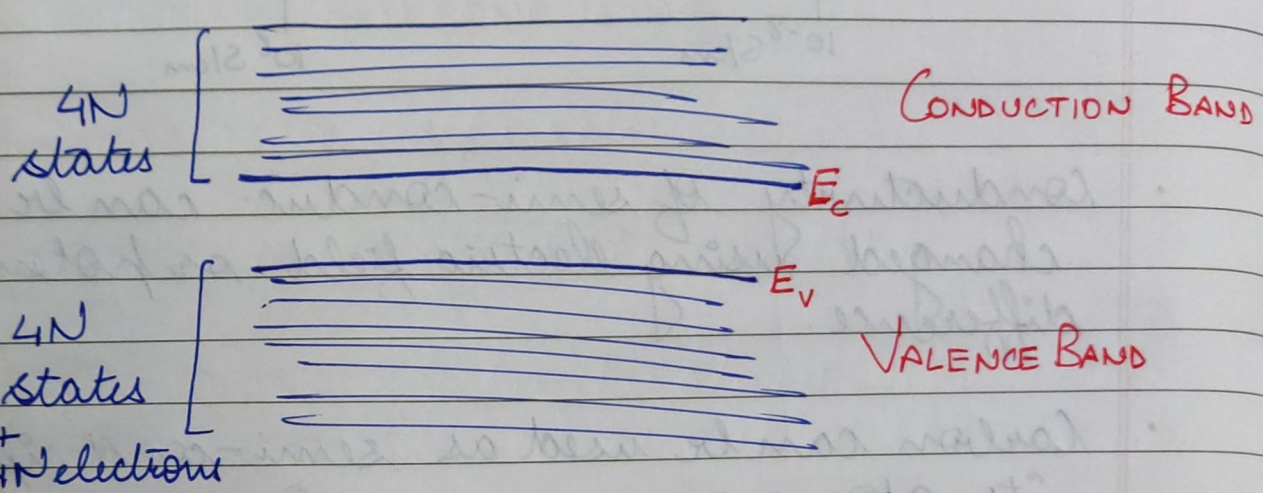
4 valence e
8 states.



- But in a system of N silicon atoms, the states don't exist in this way.

- In that system, we have 4N electrons and 8N states.

- The 8N states divide into 2 bands



E_v - highest E state in valence band
E_c - lowest E state in conduction band.

$$\boxed{E_c - E_v = E_g}$$ (band gap)

$= 1.12\ eV$ for silicon.

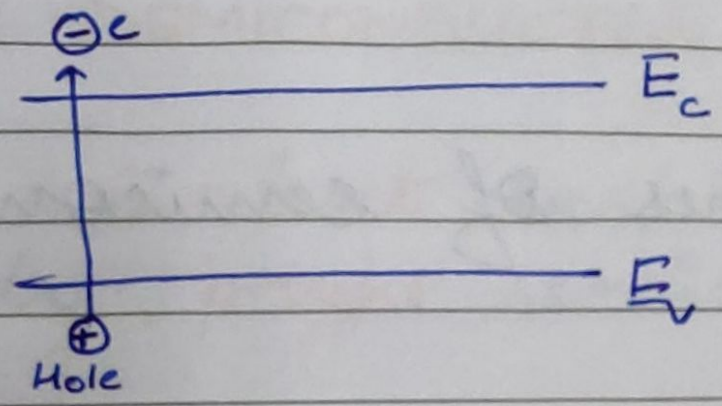
- At 0K all electrons reside in valence band.

- Intrinsic concentration $= n_i$ is no. of free electrons or holes at a given temperature.

For silicon,

$p = n = n_i$; p = holes ; n = electrons

$$\boxed{n_i = 1.5 \times 10^{10} / cm^3}$$ at room temp.



On transition.

- At room temperature, the atomic density of silicon is

5×10^{22} atoms/cm^3 are present

Out of this only 1.5×10^{10} electrons are released.

- Average energy of electrons at this room temperature is 0.026 eV. ∴ only elect. [illegible] conductor.

- At higher ~~t~~ temperatures, the electr
may free themselves out of the bond

- At any temperature,

$$n = p = n_i$$

we can calculate n_i from (at a given

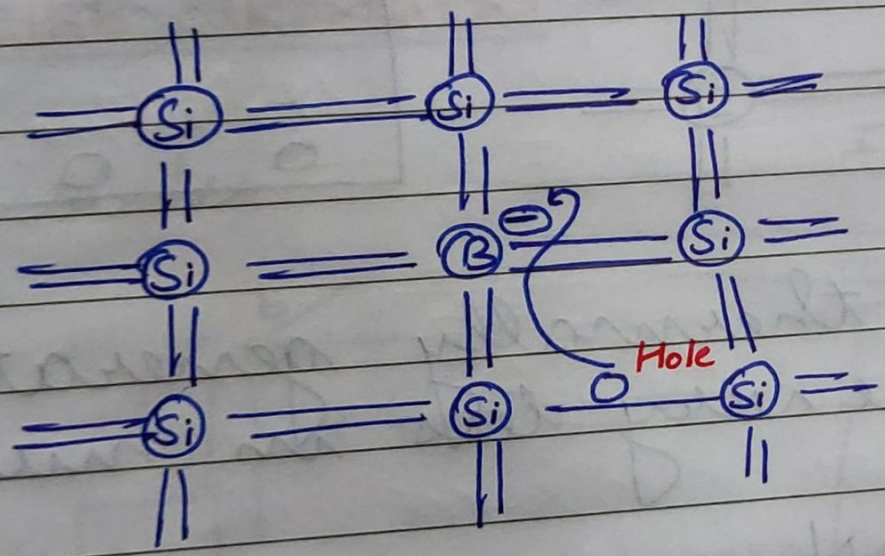
$$\boxed{n_i = BT^{3/2} e^{-E_g/2kT}}$$

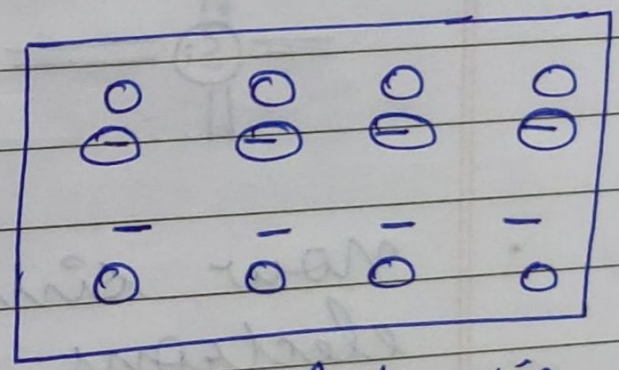
where

semiconductor is formed

- We need to choose an impurity whose lattice const. (dist b/w nearest atoms) is comparable.

a) → p-type





- — Intrinsic
⊖ — electrons on acceptor atoms

- If $N_a >> n_i$ then

$$p = N_a$$

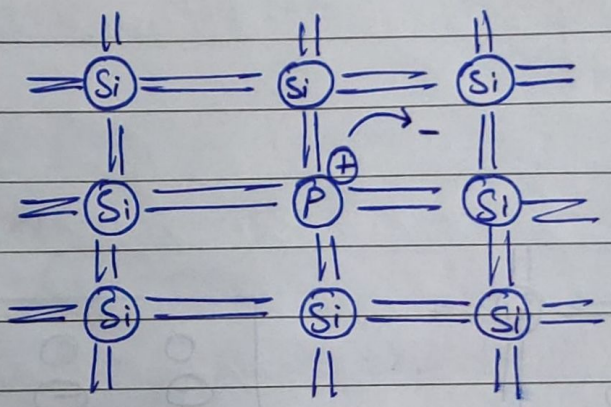
Action Law]

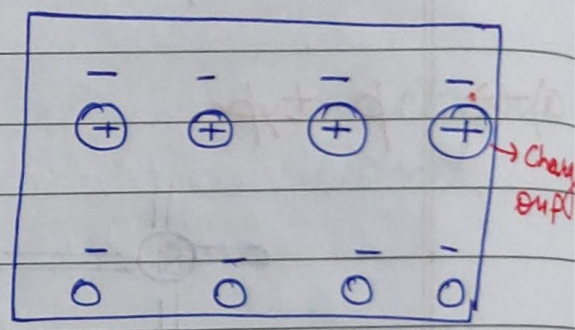
- In p-type $p \simeq N_a$

$$\therefore \Rightarrow \boxed{n = \frac{n_i^2}{N_a}}$$

b) → n-type

- The materials used as impurities for silicon are P, As, Sb

- 



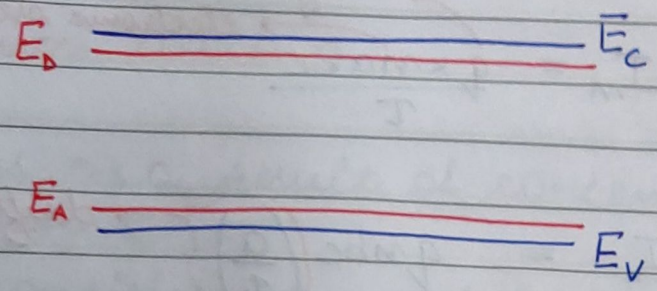
- Now since thermally generated electrons are very less in number,

$\therefore$

$$n = N_D$$

$\therefore$ Using mass action law

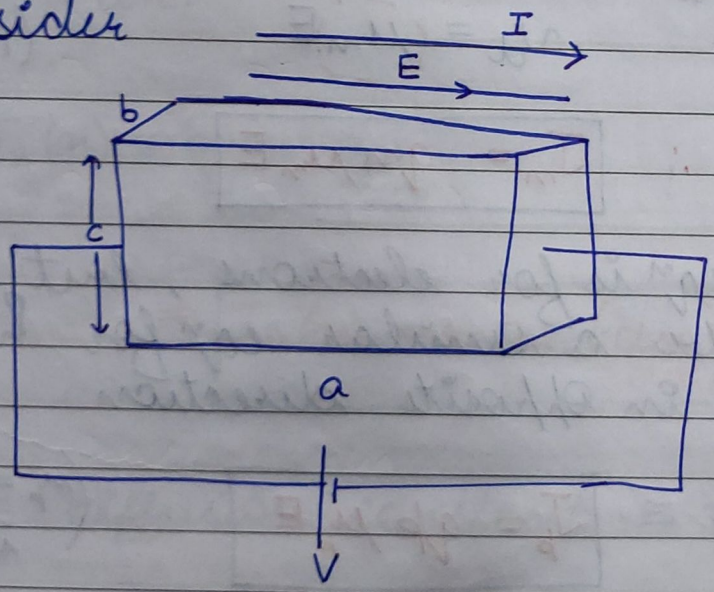
TE: When we add impurities, new energy level is introduced b/w the forbidden gap E_g



E_D is introduced when n-type is added and E_A is introduced when p-type is added.

→ CARRIER TRANSPORT →

- Consider



When p.d. is applied, e^- move in dir. opposite to $\vec{E}$ and thus equilibrium is broken

PTO

Now

$$I_n = \frac{Q}{\tau}$$

$$\Rightarrow \quad I_n = \frac{q \times nabc}{\tau}$$

charge on elect.

electronic density

$$\Rightarrow \quad I_n = qnbc\left(\frac{a}{\tau}\right)$$

drift velocit

$$\Rightarrow \quad I_n = qnbc\, v_d$$

$$\Rightarrow \quad \frac{I_n}{bc} = qn\, v_d$$

current density

Now

$$v_d \propto E$$

$$v_d = \mu_n E$$

electronic moli

(1350 cm²/v

for S

$$\therefore \quad \boxed{J_n = qn\mu_n E}$$

This eqⁿ is for electrons, but there will be a similar eqⁿ for holes w move in opposite direction

$$\boxed{J_p = qp\mu_p E}$$

(μ_p = hole

ie = 350

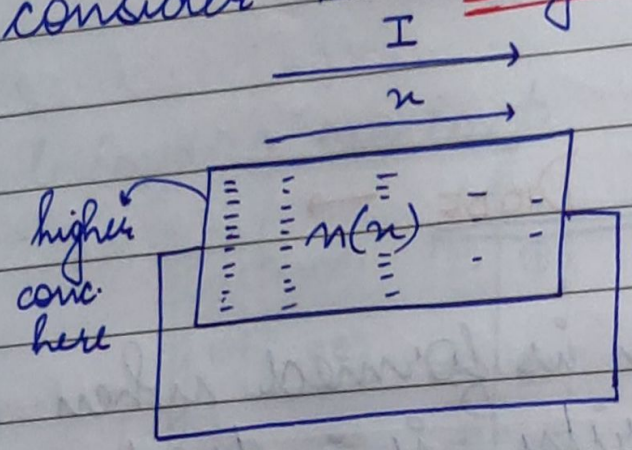
fo

∴ Total current will be addition of these 2

$$\boxed{J_{drift} = q(n\mu_n + p\mu_p)E}$$

- Occurs as a result of concen...

- we consider an n-type semiconductor (Si)



n(x) is concentration of e⁻ as a func. of x

Now

$$J_n(x) \propto \left(\frac{dn}{dx}\right)$$

$$\Rightarrow J_n(x) = q D_n \frac{dn}{dx}$$

$$\Rightarrow \boxed{J_n(x) = q D_n \left(\frac{dn}{dx}\right)}$$

D_n = Diffusion constant $\cong 35\ cm^2/sec$

NOTE D_n is related to electronic mobility as

$$\boxed{\frac{D_n}{\mu_n} = V_T}$$

V_T → Thermal voltage (average energy of ...

$$\boxed{V_T = \frac{KT}{q}}$$

$= 26\ mV$ at room T

$D_p = 12 cm^2/sec$

$$\boxed{\frac{D_N}{\mu_N} = \frac{D_P}{\mu_P} = V_T}$$

→ p-n JUNCTION DIODE →

- A p-n junction is formed when an n type impurity is introduced in a p-type impurity or vice-versa.

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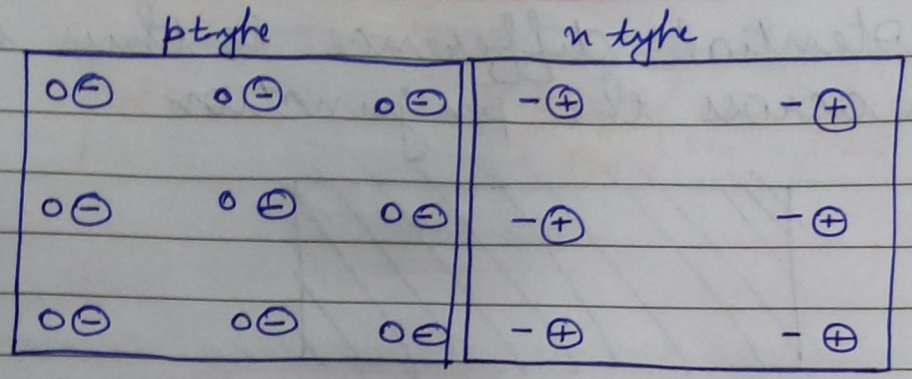
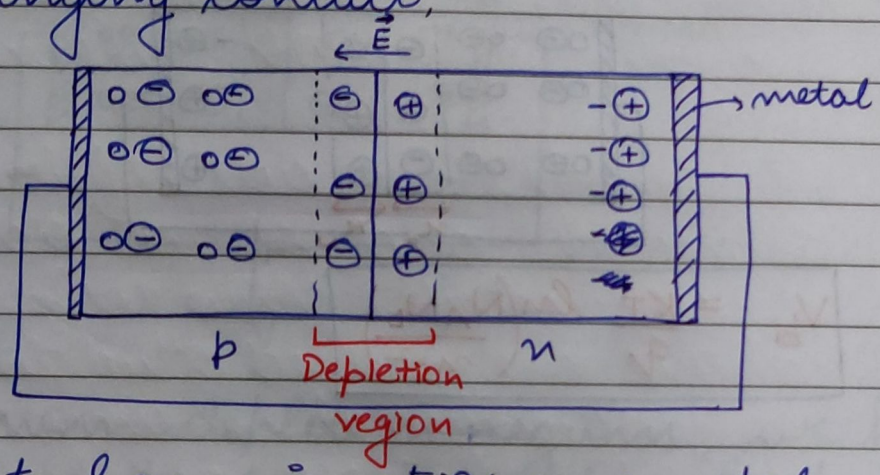


⊖ - acceptor atom with -ve charge

⊕ - donor atom with +ve charge

This is the situation on no contact

- On bringing contact,



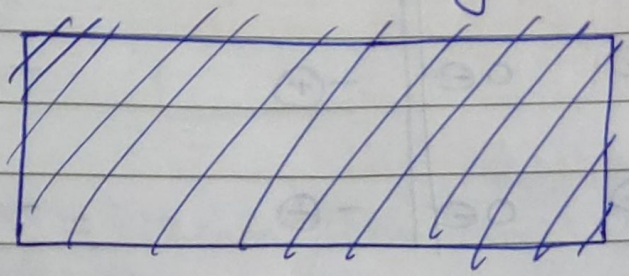
- now it has 3 junctions 2 metal - semicond junctions & p-n junction

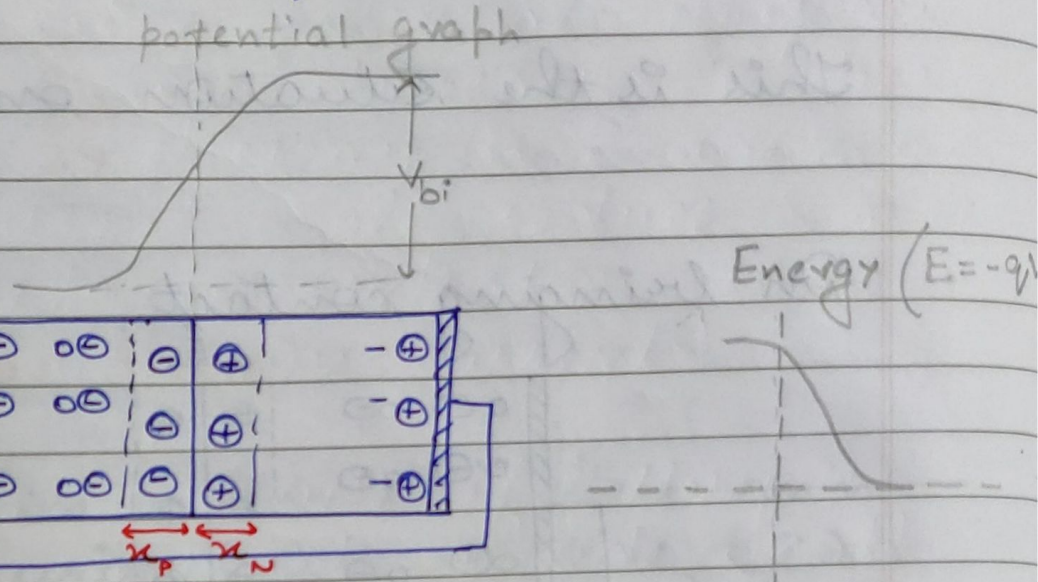
- Since p side has very high hole concentration $N_A = 10^{18}/cm^3$ but n type has very low hole concentration $= \frac{n_i^2}{N_D} = \frac{10^{20}}{10^{15}}$

$= 10^5/cm^3$

- ∴ gradient is set up and holes transfer from p to n type. But this does not occur for long since an electric field is set up as soon as transfer occurs. Thus an equilibrium is reached.

- A potential difference is thus set up across the pn junction





$$V_{bi} = \frac{KT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

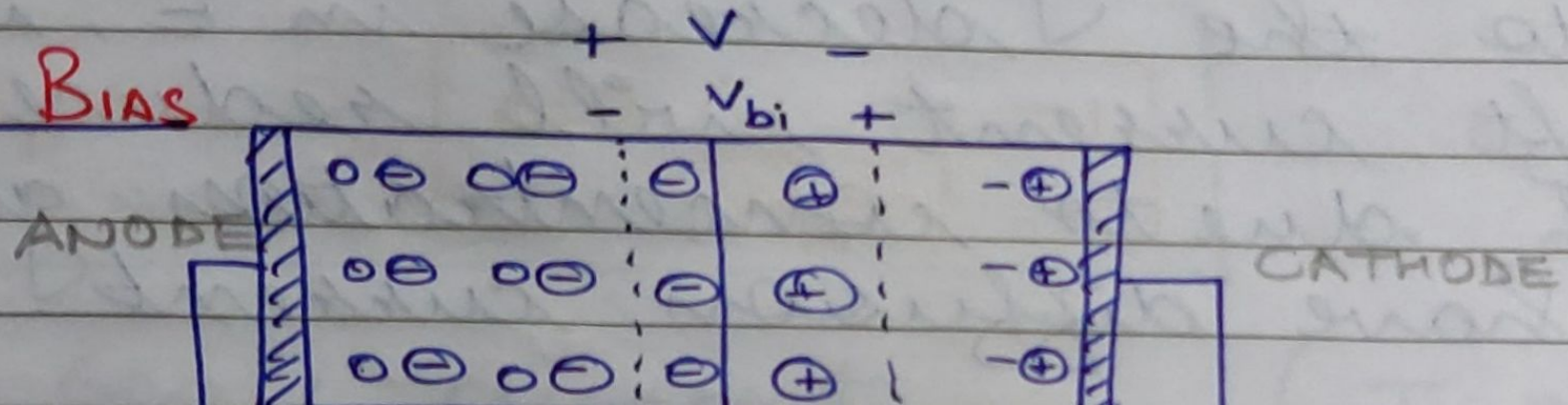
- The length of depletion region is smaller on p-side since concentration is higher there.

$$N_A + N_D$$

$$W = x_n + x_p = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right) \cdot V_{bi}}$$

For Si $\boxed{V_{bi} = 0.9V}$

Forward Bias



$$\cancel{I_D = I_0 \left[e^{\frac{V}{nV_T}} - 1 \right]}$$

~~scale current~~

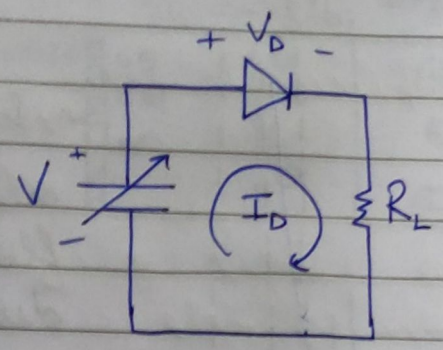
- However only diffusion current increases. Since potential drop across depletion region decreases, $\therefore \vec{E}$ decreases. Due to the decrease in $\vec{E}$, we know, drift current will reduce. & as such due to concentration gradient, we have diffusion current.

- At anode, +ve side of battery is connected and at -ve side cathode is connected. Now the holes in anode are pushed due to connection to +ve terminal & similarly for cathode electrons are pushed away. Basically, ~~anode~~ electrons are supplied to cathode & taken away from anode and further holes & electrons are pushed. Thus we can observe, THE DEPLETION REGION DECREASES in length.

$$\boxed{W = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_{bi} - V)}}$$

(valid when $V_{bi} > V$)

- Consider a circuit



$$\boxed{I_D = I_s\left[\exp\left(\frac{V_D}{\eta V_T}\right) - 1\right]}$$

I_s : Scale current $\left(I_s \propto \text{Area (of pn junc)}\right)$

$\left(I_s = 10^{-12}\text{ A to } 10^{-15}\right)$

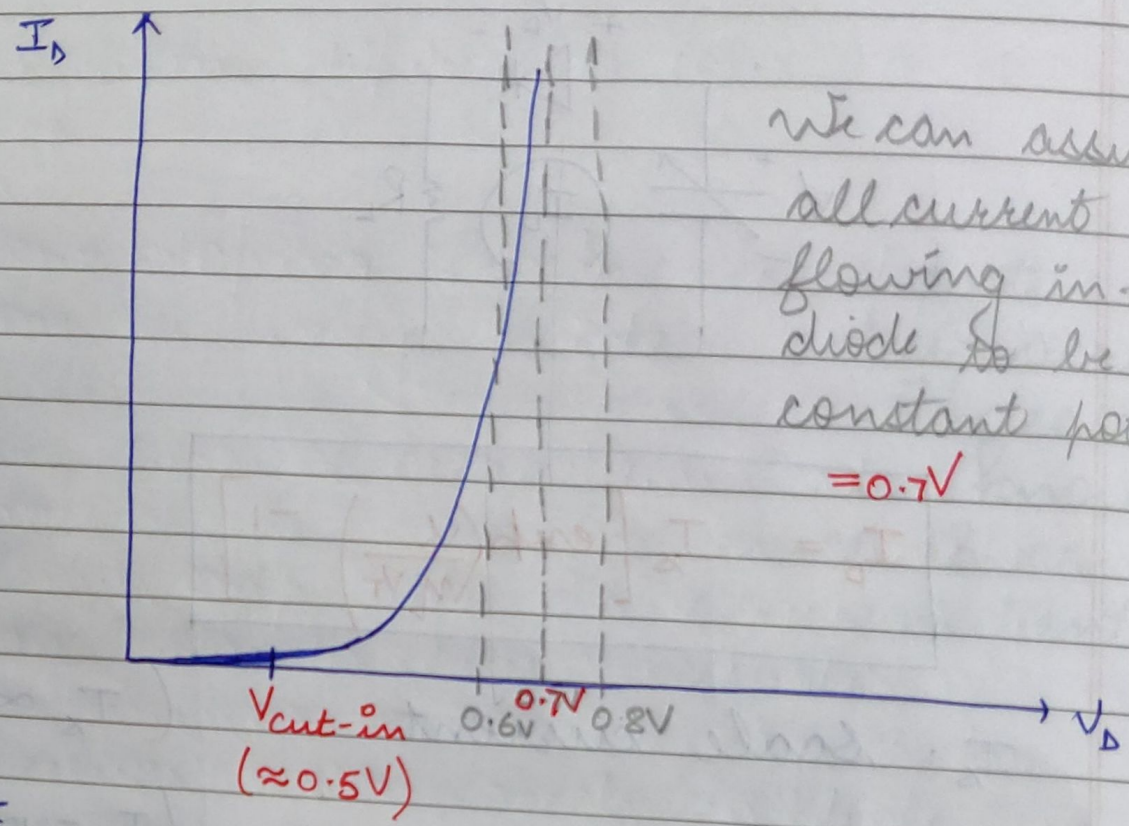
imp NOTE: I_s gets double for 5°C rise in temperature

- when under forward bias and when V_D is very large,

$$\boxed{I_D = I_s\left[\exp\left(\frac{V_D}{\eta V_T}\right)\right]}$$

PTO

- graph between I_D and V_D

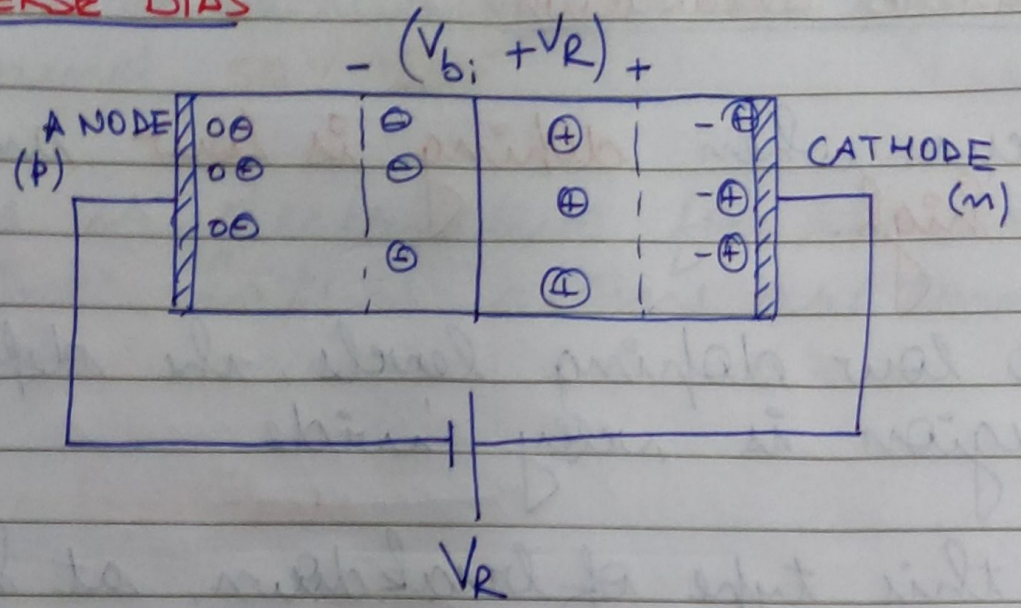


We can assume all current flowing in the diode to be at constant potential =0.7V

~~V_{cut}~~

- V_{cut-in} is 0.5V due to exponential nature of the curve. V_{cut-in} is the voltage from where we see exponential rise in current.
- Observe at 0.6V, current has risen and at 0.8V, we hardly find a plot in graph. ∴ we consider voltage 0.7V as a voltage where current has risen to lets ma

Reverse Bias



- V_R is applied and all V_R drops across the depletion region.
- ∴ voltage across depletion region $= V_{bi} + V_R$
- ∴ we can conclude that electric field increases and the depletion width increases (conclude in similar manner as in forward bias)
- $$W = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(V_{bi}+V_R)}$$

- Avalanche breakdown

- Occurs when doping is low and voltage is high.

- At low doping levels, the depletion region is very wide

- In this type of breakdown, at high voltages, the holes on n-side and electrons on p-side have very high energy. Due to this, inspite of being ~~in as~~ minor carriers, they enter depletion region and collide with lattice atoms there. Due to this collision, the atom converts to a hole electron pair and due to high electric field, they suddenly set up a current (a high current)

- I_D

E: when doping is low, carriers are reduced.
∴ to obtain a current of any value, a higher voltage must be applied. ∴ breakdown voltage in this is hig

his breakdown occurs at high voltages round 50V-80V

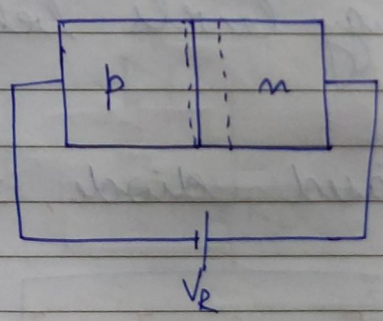
This is destructive for the diode since lattice atoms are tampered with.

Zener breakdown

Occurs at high doping and low voltag

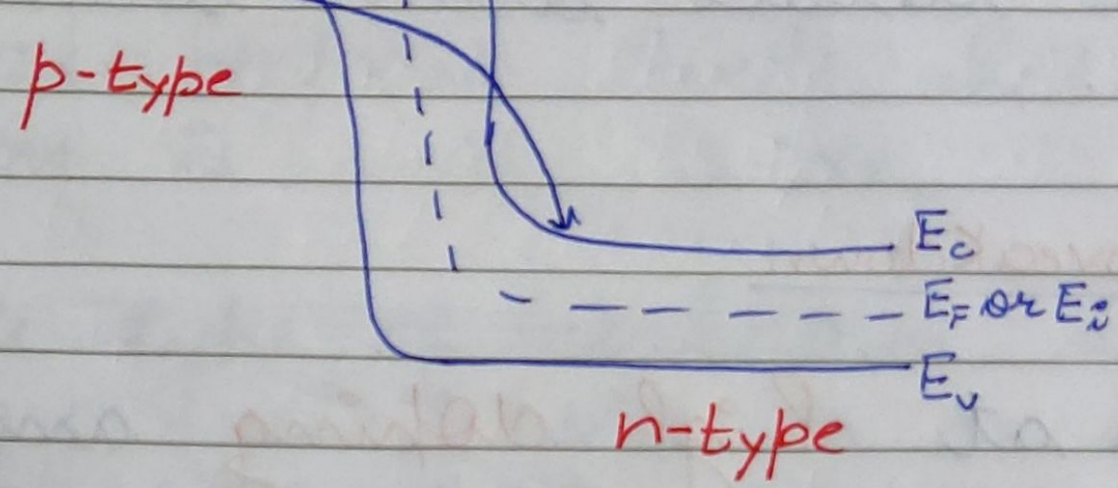
The depletion region is small. Due to this, the energy drops over a smaller region

When a potential is applied across p-n junction, the conduction band of n-type goes below the valence band of p-type



For some V_R, the E_c of n-side goes below E_v of p-side

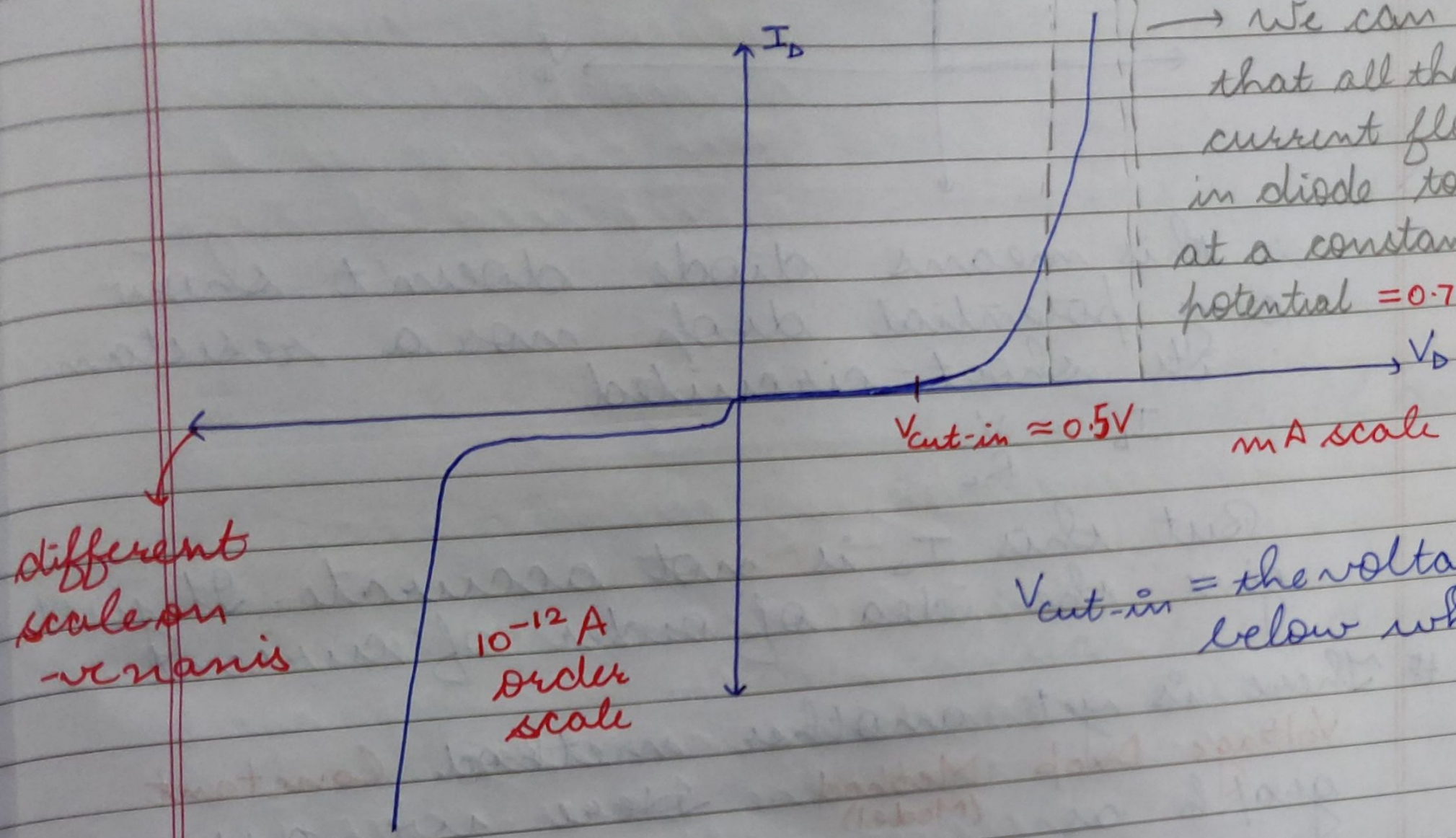
PTO



Due to such a formation and thin depletion, the electrons can tunnel through and go from valence band of p-type to conduction band of n-type.

NOTE: E_{Fermi} or $E_{intrinsic}$ is the energy level such that at 0K all electrons stay in all the energy levels below it

- I_D vs V_D characteristics

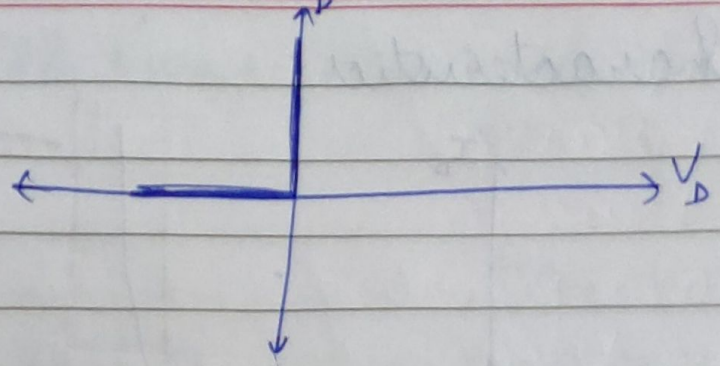


→ We can assume that all the current flowing in diode to be at a constant potential $= 0.7V$

$V_{cut\text{-}in}$ = the voltage below which

Q. ical solving

To solve it accurately

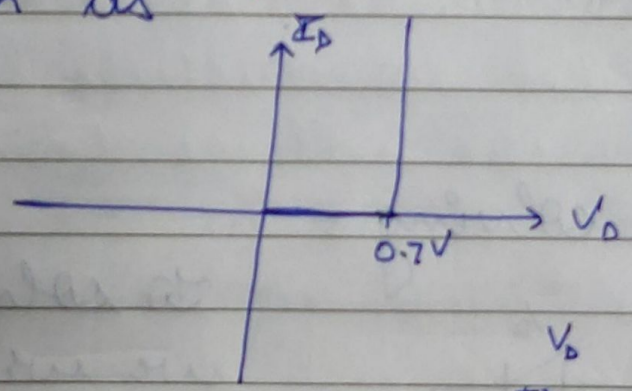


∴ this means diode doesn't show any potential drop nor a resistance
∴ its short-circuited

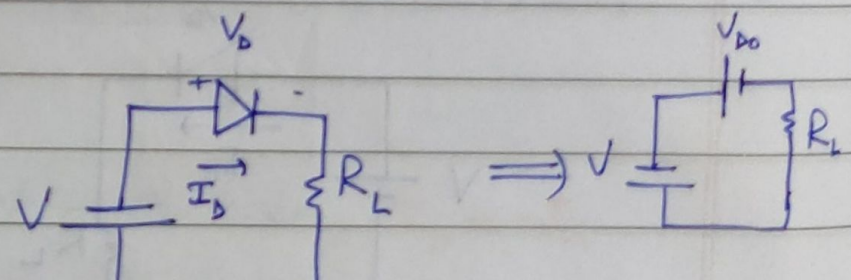
∴ $I_D = \frac{V}{R_L}$

But this I_D is not accurate. It just gives the idea of order of current.

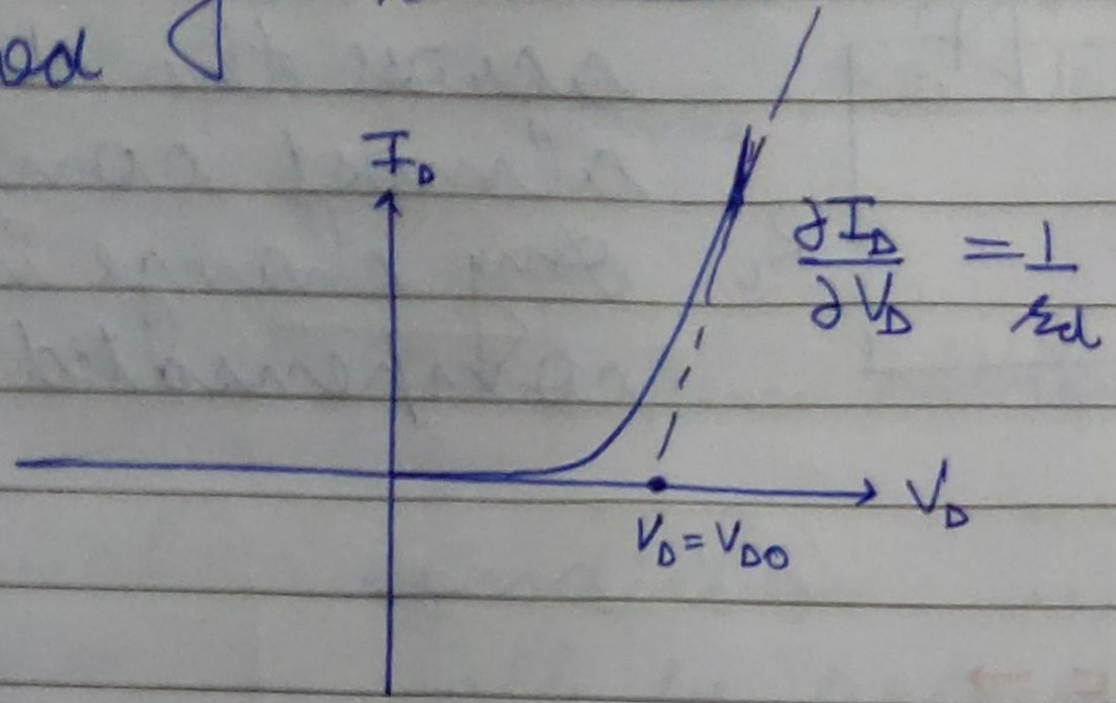
There is yet another method Constant Voltage Drop Method (Model). Here we assume graph as



∴ in circuit



There is yet another more accurate method

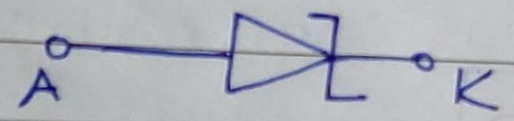


Here r_d = dynamic resistance of diode

For Si $\boxed{r_d \approx 10\,\Omega}$

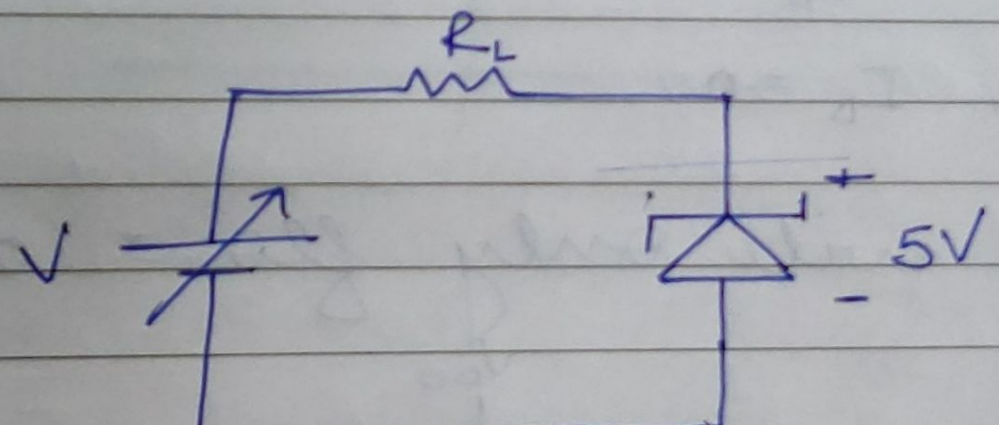
∴ Now we can replace the diode

ZENER DIODE →



Symbol for zener diode.

- When breakdown voltage $V = V_Z$ is reached, then the zener diode acts as a constant voltage source of $\boxed{V = V_Z}$

- 

i.e it remains $= 5V$

Now if $V < 5V$, then obviously $V_{across\ diode} < 5V$

In such a condition using graph, we know I_D will be around zero. ∴ drop across $R_L = 0$. ∴ All potential drops across the diode

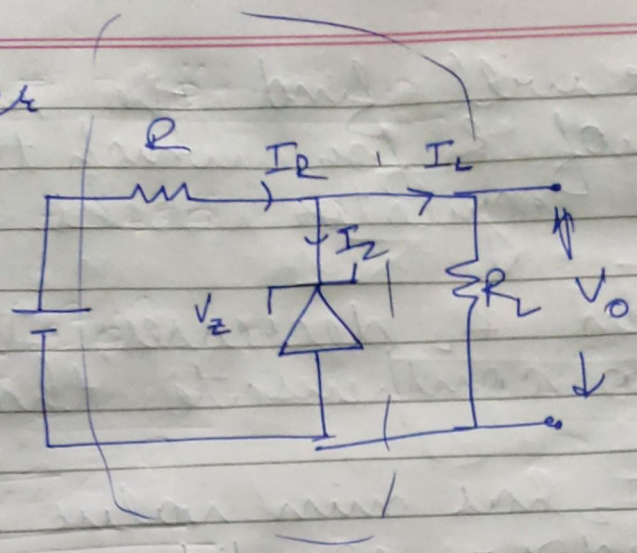
VOLTAGE REGULATOR →

- Whatever the value of input voltage or of R_L (load resistance), the value of voltage across the R_L must remain constant for our devices. This is done using voltage regulator

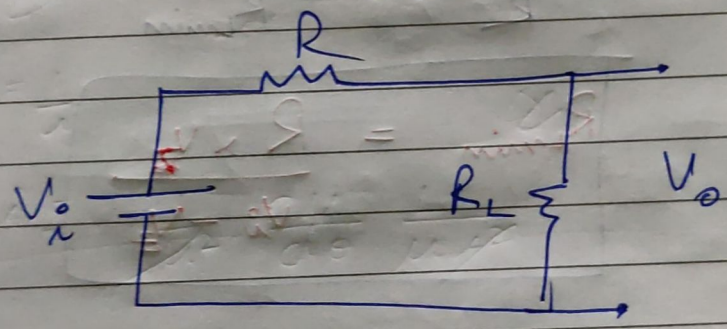
REGULATOR

Any change in ~~V_L~~ V_L is compensated across R.

- Consider



If $V_o < V_Z$ this means that no current flows through the diode ie we can remove the diode. ∴ we get a circuit



$$I_L = \frac{V_Z}{R_L}$$

$$I_R = I_Z + I_L$$

$$I_R = \frac{V_i - V_Z}{R}$$

∴ we can calculate V_o simply

NOTE: There is a safe limit of power dissipation for a zener diode. it is given by

$$P_Z = V_Z I_Z$$

Here I_Z is the max current that can flow without damaging the circuit.

- now we will find the range of values of R_L for which this voltage regulator works.

When R_L decreases, I_L increases & to compensate that, I_Z decreases

now I_Z has min value $=0$ in breakdown condition $\therefore$ I_L will be max at that point

$$\Rightarrow \quad I_R = I_{L\,max}$$

$$\Rightarrow \quad \frac{V_i - V_Z}{R} = \frac{V_Z}{R_{L\,min}}$$

$$\Rightarrow \quad \boxed{R_{L\,min} = \frac{R \times V_Z}{V_i - V_Z}}$$

now ~~to~~ to find $R_{L\,max}$, we will have a max allowed value of I_Z

$$\Rightarrow \quad I_R = I_{Z\,max} + I_{L\,min}$$

$$\Rightarrow \quad I_R = I_{Z\,max} + \frac{V_Z}{R_{L\,max}}$$

$$\Rightarrow \quad \boxed{\frac{V_i - V_Z}{R} = I_{Z\,max} + \frac{V_Z}{R_{L\,max}}}$$

For $V_{i\,max}$

$$I_R = I_Z + I_L$$

$$\Rightarrow \frac{V_{i\,max} - V_Z}{R} = I_{Z\,max} + \frac{V_Z}{R_L}$$

$\Rightarrow$ _____

Ans:

$$4.2 = i \times R$$

$$I_D = I_S \left(e^{0.7/V_T} \right)$$

$$I_D = I_S \left(e^{0.8/V_T} \right)$$

$$\frac{I_{D_2}}{I_{D_1}} = \frac{e^{0.8/V_T}}{e^{0.7/V_T}} = e^{0.1/V_T}$$

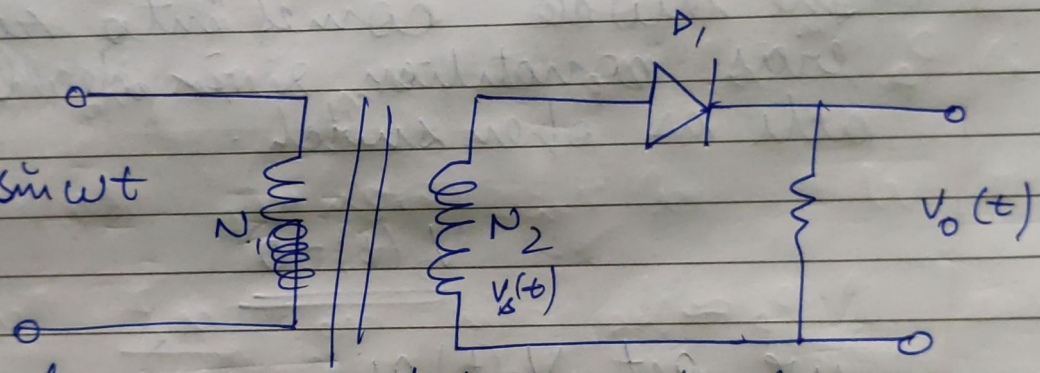
So

→ RECTIFIERS

a) Half wave

b) Full wave
- → Bridge
- → normal.

→ HALF WAVE RECTIFIER →

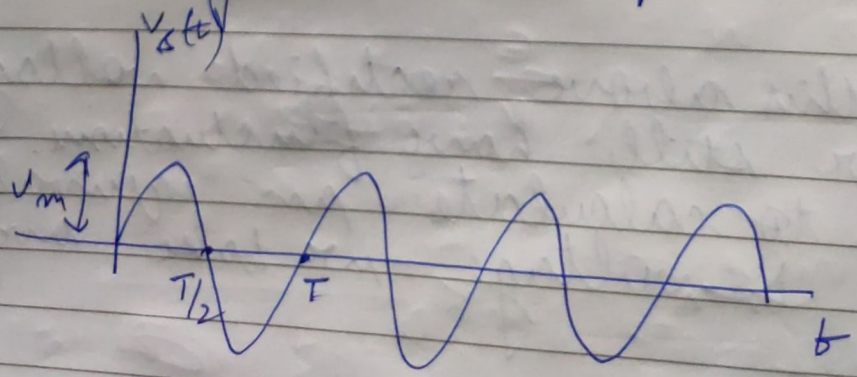


NOTE: Transformer is needed to step the voltage down acc. to the diode

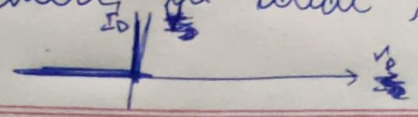
$$V_s(t) = \frac{N_2}{N_1} \times V_i \sin \omega t$$

$$\Rightarrow \boxed{V_s(t) = V_m \sin \omega t}$$

This signal is a bipolar signal



NOTE: Remember in ideal diode model we have →



∴ no potential drop across forw bias & no current in rev bias

In $0 < t < T/2$

the diode comes in forward bias condition & in ideal condition, we consider it as a perfect conductor here

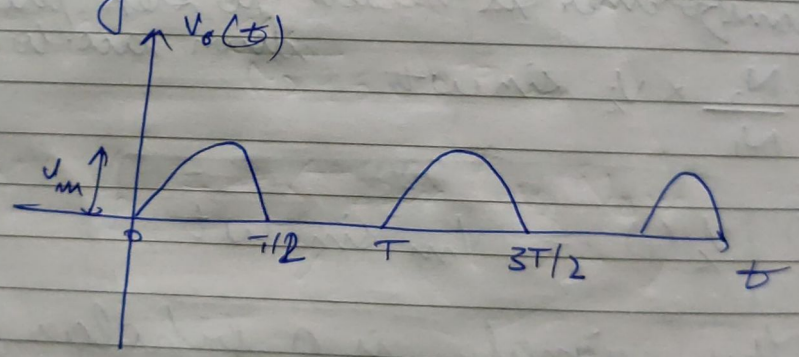
$$\therefore V_o(t) = V_s(t)$$

In $T/2 < t < T$

The diode comes into reverse bias condition & ideally, it acts as open switch.

$$\therefore \underline{\underline{V_o(t) = 0}}$$

∴ we get $V_o(t)$ as



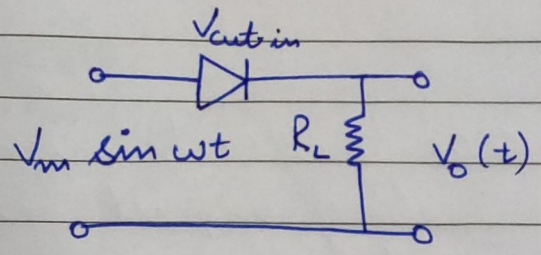
In this above rectified voltage, we still have fluctuations.
∴ to calculate an equivalent DC voltage, we take averaging

$$V_{avg} = \frac{1}{2\pi}\int_0^{2\pi} V_m \sin\theta \, d\theta$$

$$\Rightarrow V_{avg} = \frac{1}{2\pi}\int_0^{\pi} V_m \sin\theta \, d\theta$$

$$\Rightarrow V_{avg} = \frac{V_m}{\pi}$$

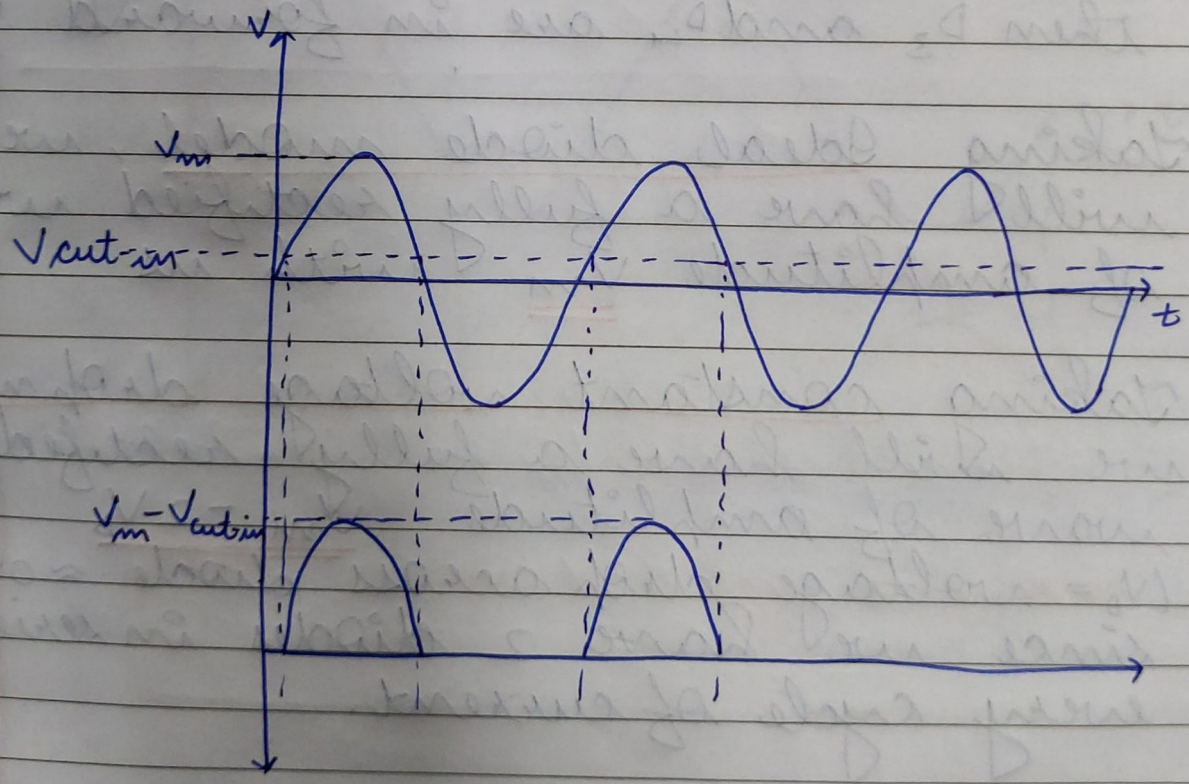
$$\therefore \boxed{V_{avg} = \frac{V_m}{\pi}}$$



In the above circuit if input voltage is < $V_{cut\text{-}in}$, then in that case the diode becomes conducting only if $V_{cut\text{-}in} < V_m \sin \omega t$

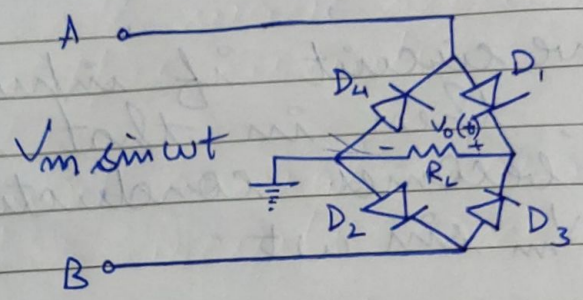
There is a drop of $V_{cut\text{-}in}$ (0.7V) across the diode

$$\therefore \quad V_o(t) = V_m \sin \omega t - V_{cut\text{-}in}$$



→ FULL WAVE RECTIFIER

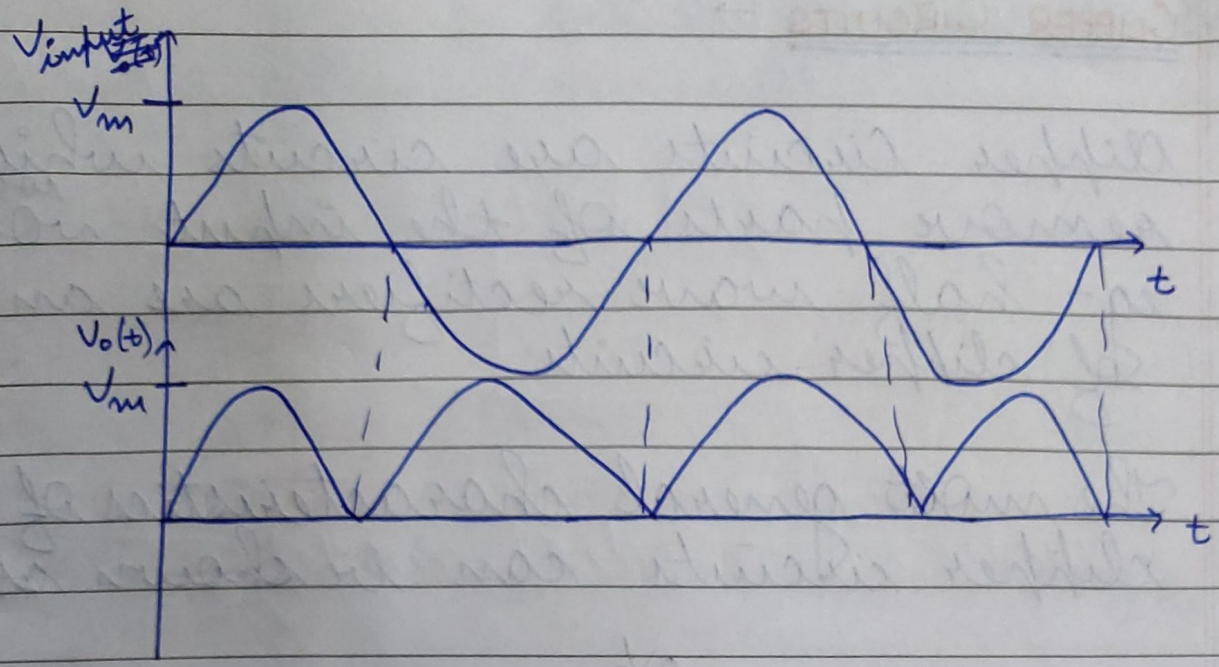
1. BRIDGE RECTIFIER



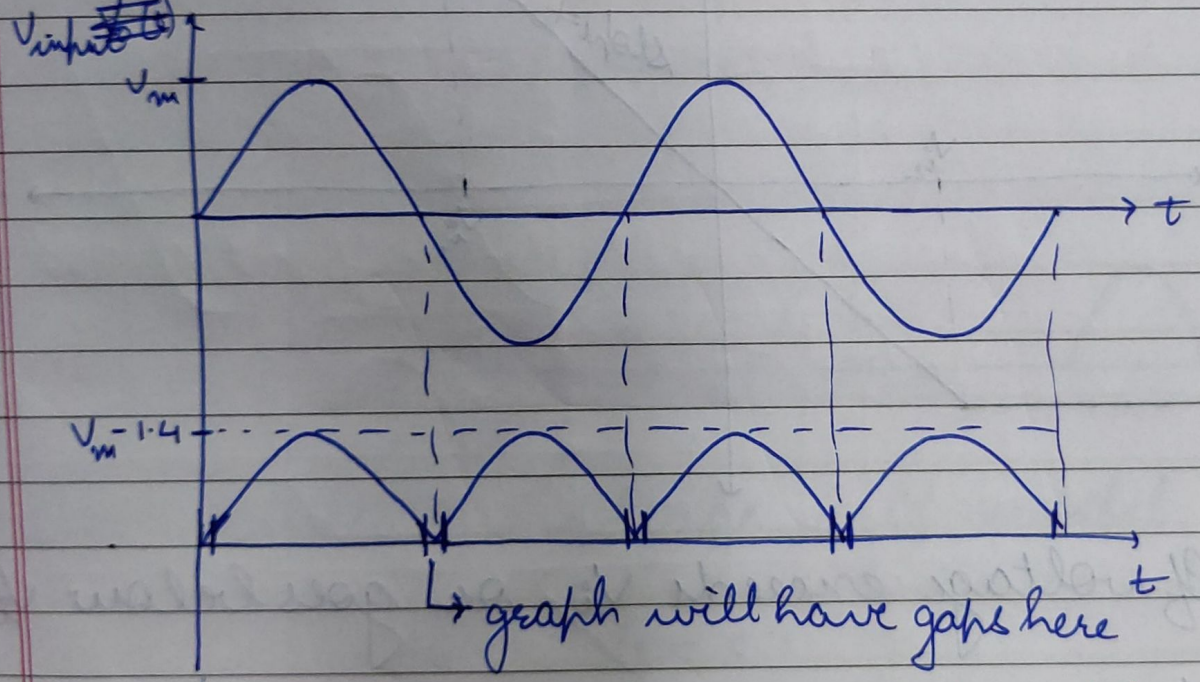
- When A is at higher potential than B, then D_1 and D_2 are in forward bias and when B is at higher po then D_3 and D_4 are in forward bia

- Taking Ideal diode model, we will have a fully rectified wav of amplitude V_m with us

- Taking constant voltage drop mo we still have a fully rectified wave of amplitude $V_m - 2V_D$ (V_D = voltage drop across diode ≈ 0.7 since we have 2 diodes in series every cycle of current.



Ideal diode model

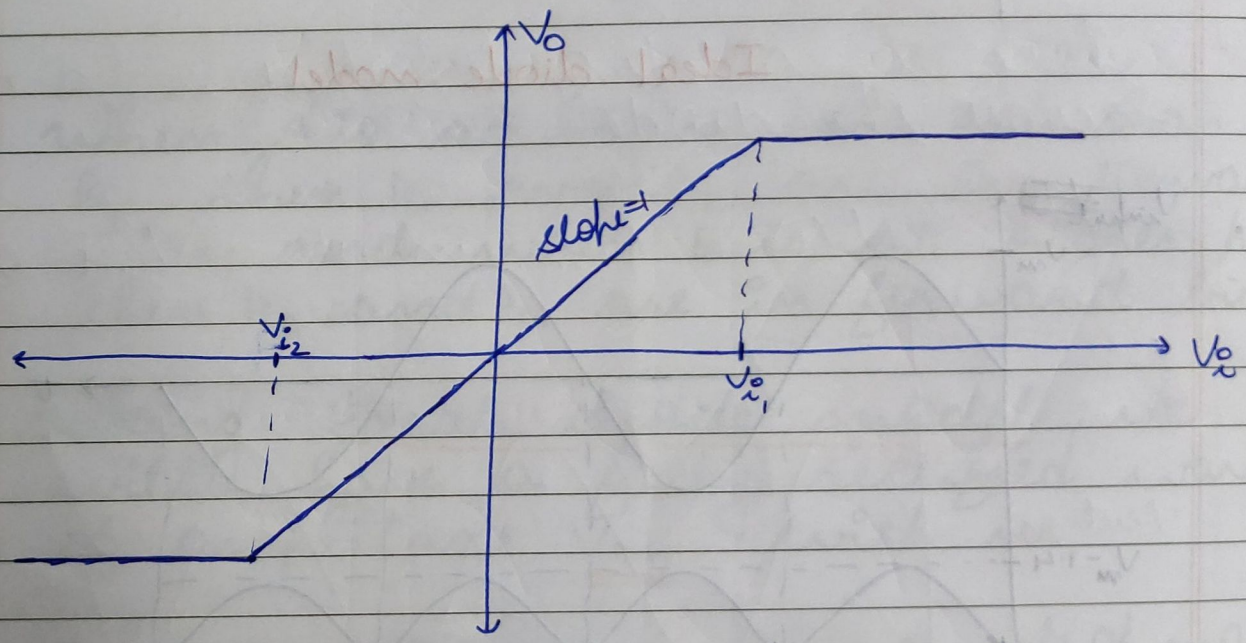


Constant voltage drop model

→ CLIPPER CIRCUITS →

- Clipper circuits are circuits which remove parts of the input voltage to get desired output. eg- half wave rectifiers are an eg. of clipper circuits.

- The most general characteristics of clipper circuits can be shown as

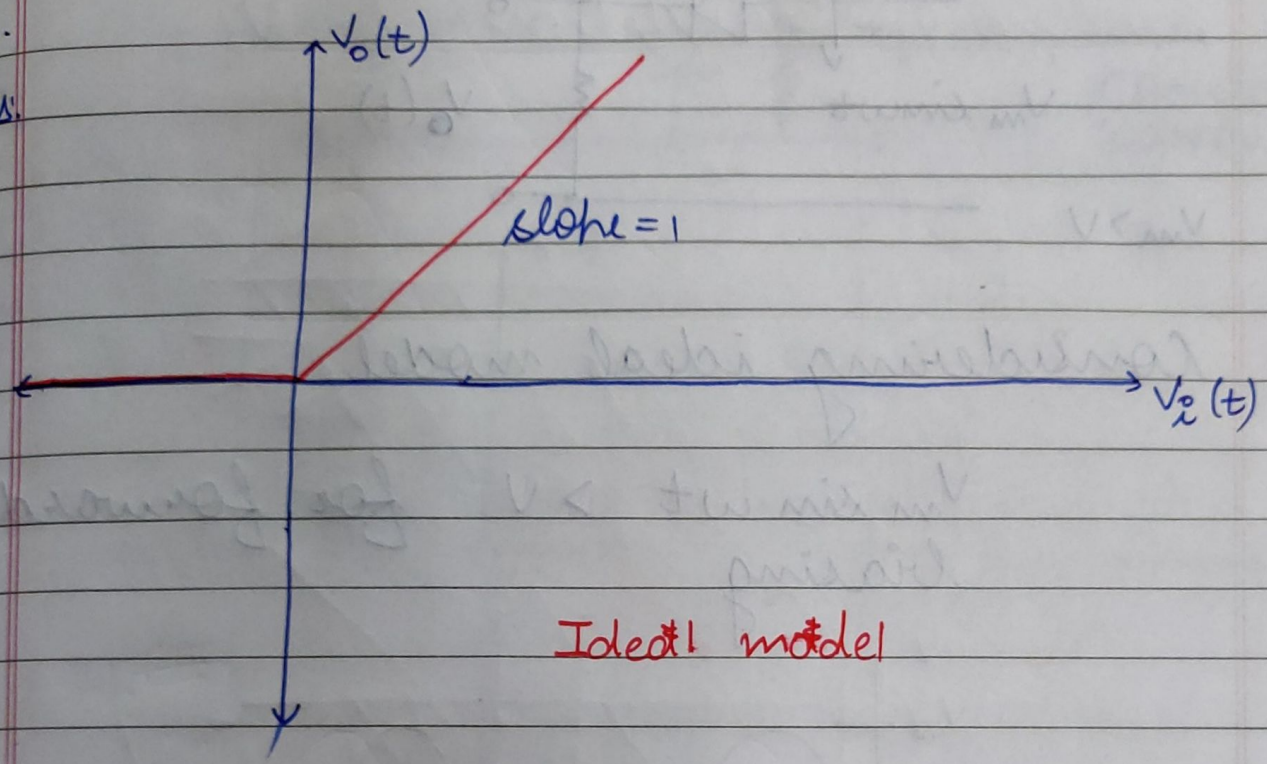


If voltage exceeds V_{i_1} or goes below V_{i_2}, V_o becomes constant.

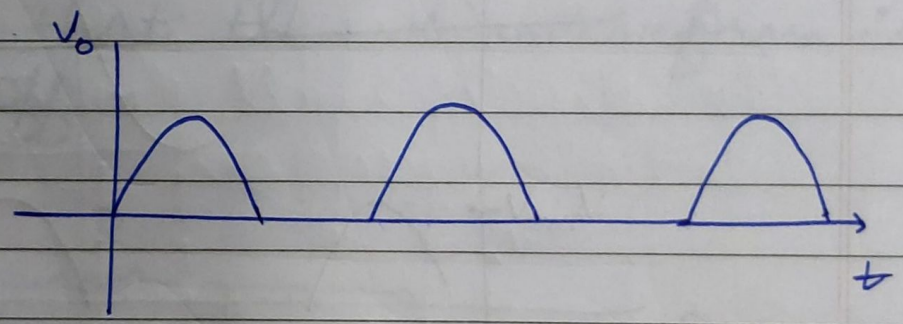
imp Q→ Draw V_o vs V_i characteristics for half wave rectifier circuits.

* voltage.

Ans:

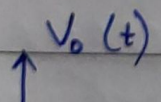


Ideal model

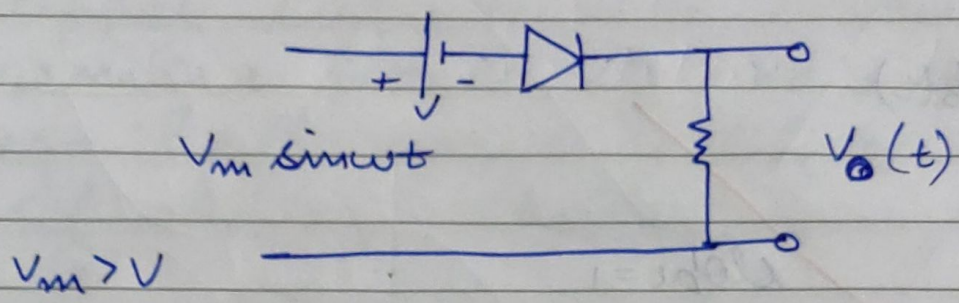


For constant voltage drop model

$$V_o = V_i - 0.7$$

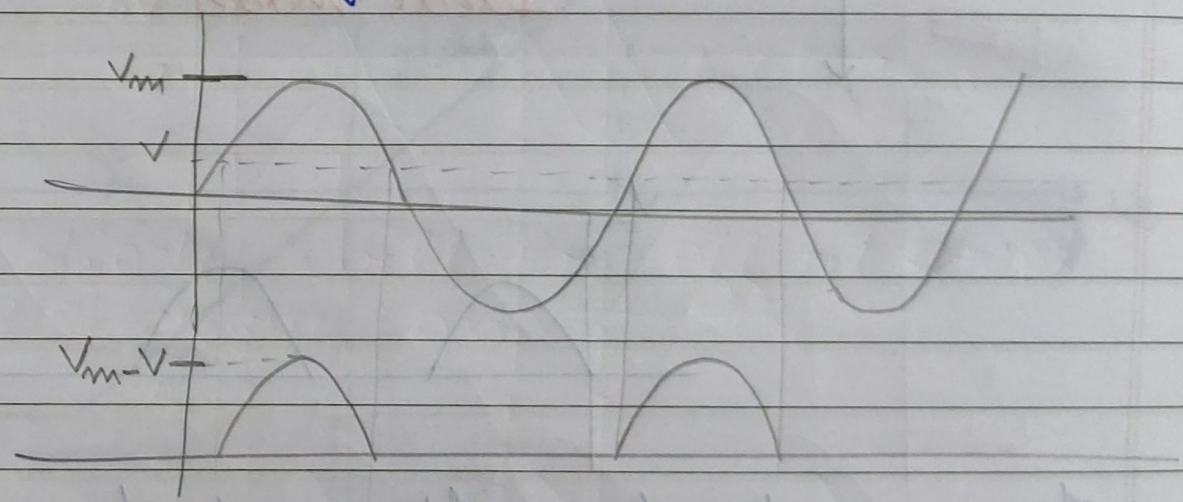


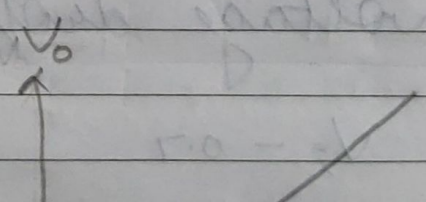
Q. Draw V_o vs V_i for



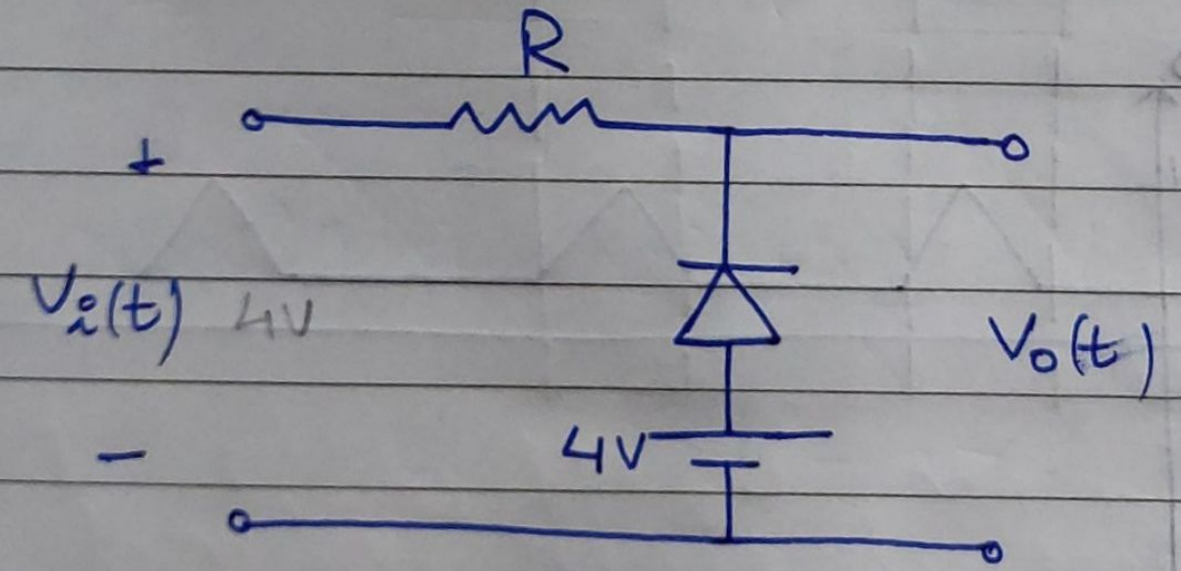
Ans: Considering ideal model

$V_m \sin \omega t > V$ for forward biasing

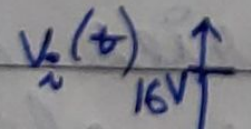




Here note that the +ve waveform is clipped off.

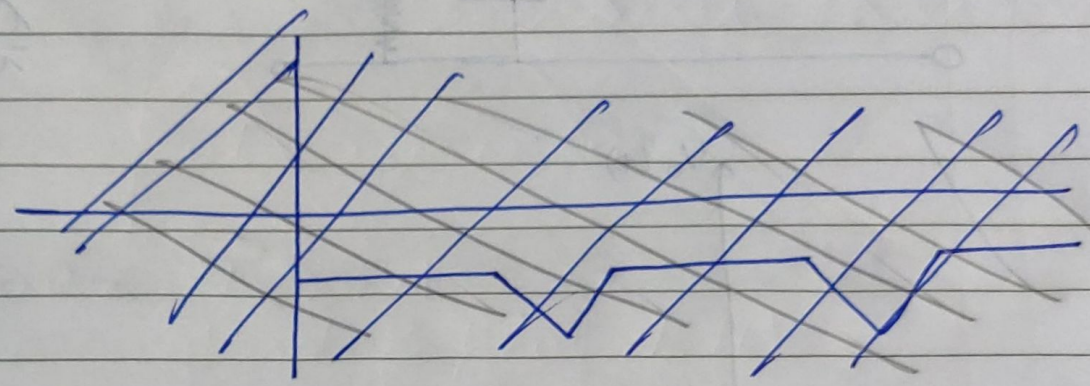


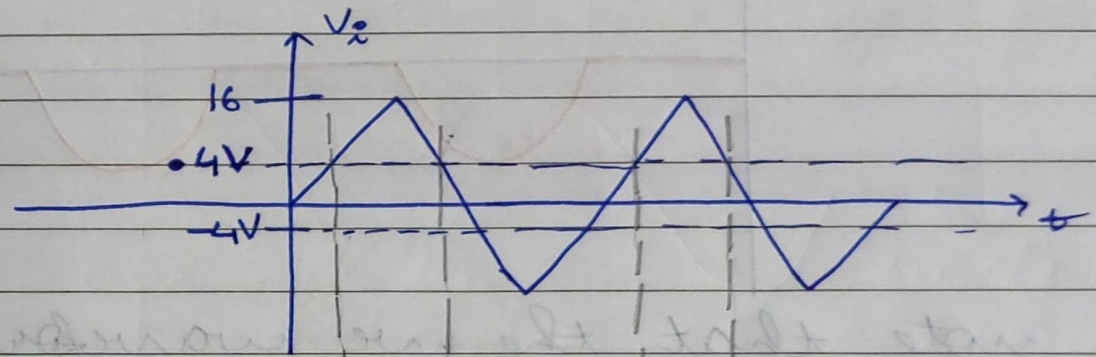
Draw output form



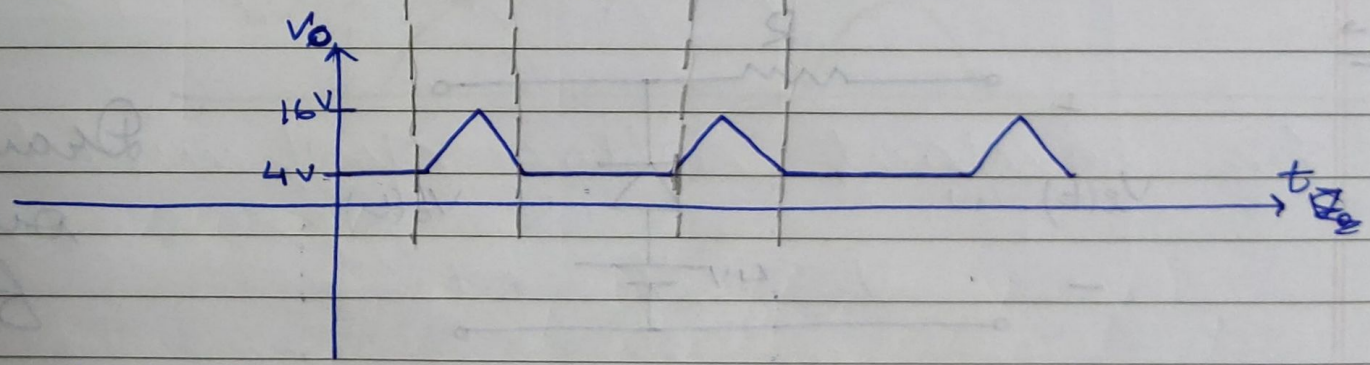
Ans. In ideal model,
in conducting (on) mode, $V_o = 4V$

and in off condition $V_o = V_i$

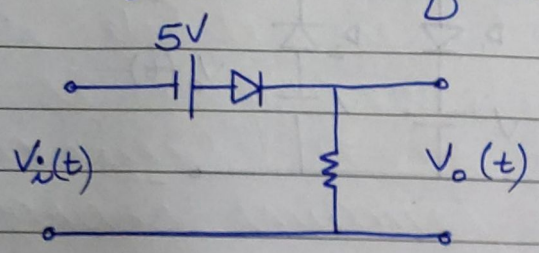


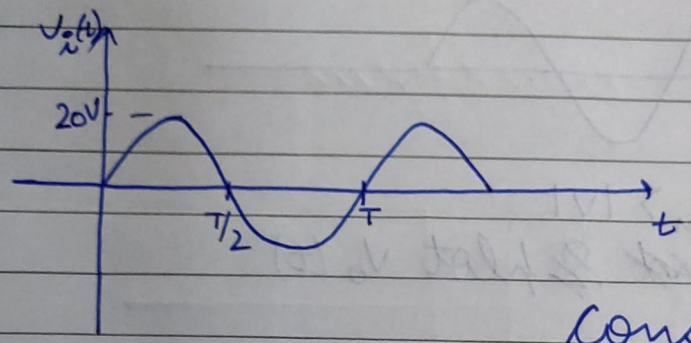


The diode will be off at $V_i > 4$
and otherwise on



Q. Draw $V_o(t)$ waveform





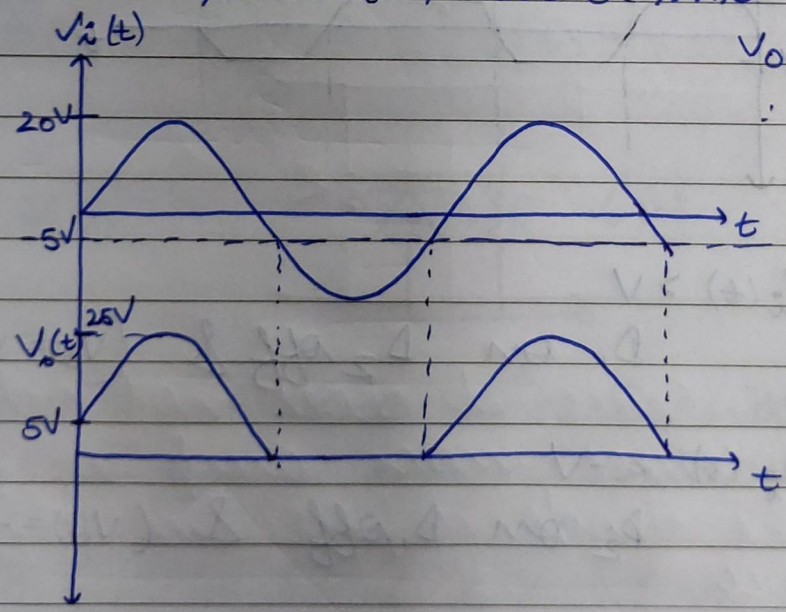
Consider ideal model.

Ans: At $V < -5V$ diode will be in off condition and $\therefore V_o(t) = 0V$

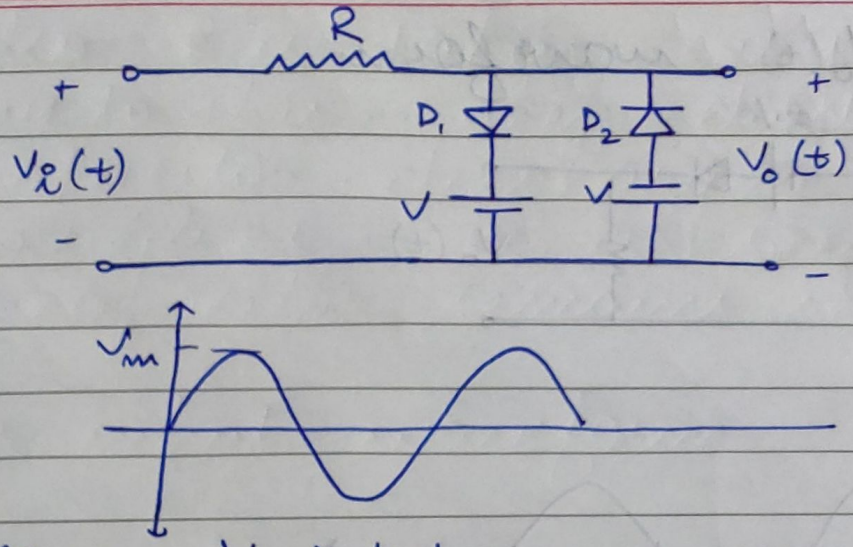
At $V > -5V$ diode will be in on condition

$V_o = V_i + 5$

$\therefore$ output signal is shifted by 5V



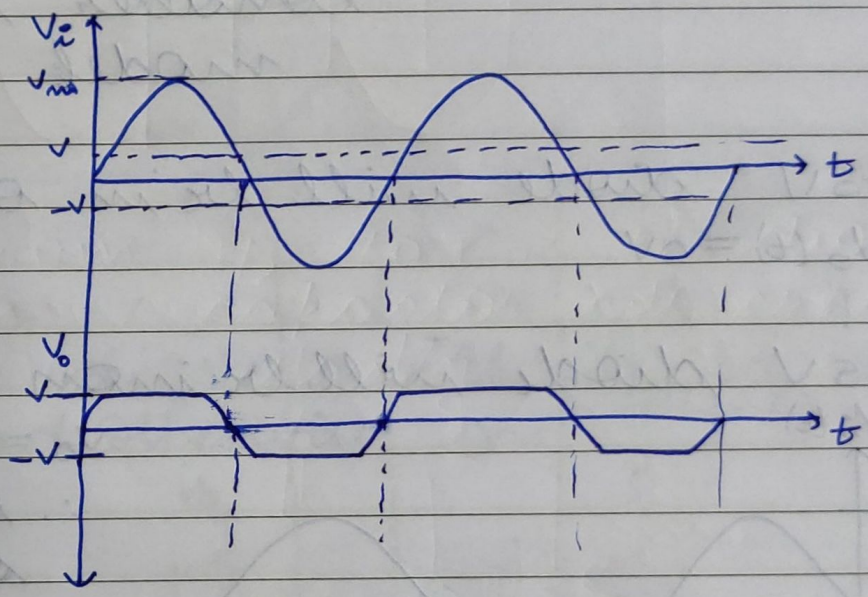
Q-



given $V_m > |V|$

~~find~~ & plot $V_o(t)$

Ans:



i) $V_i(t) > V$

D_1 on D_2 off & $(V_o(t) = V)$

ii) $V_i(t) < -V$

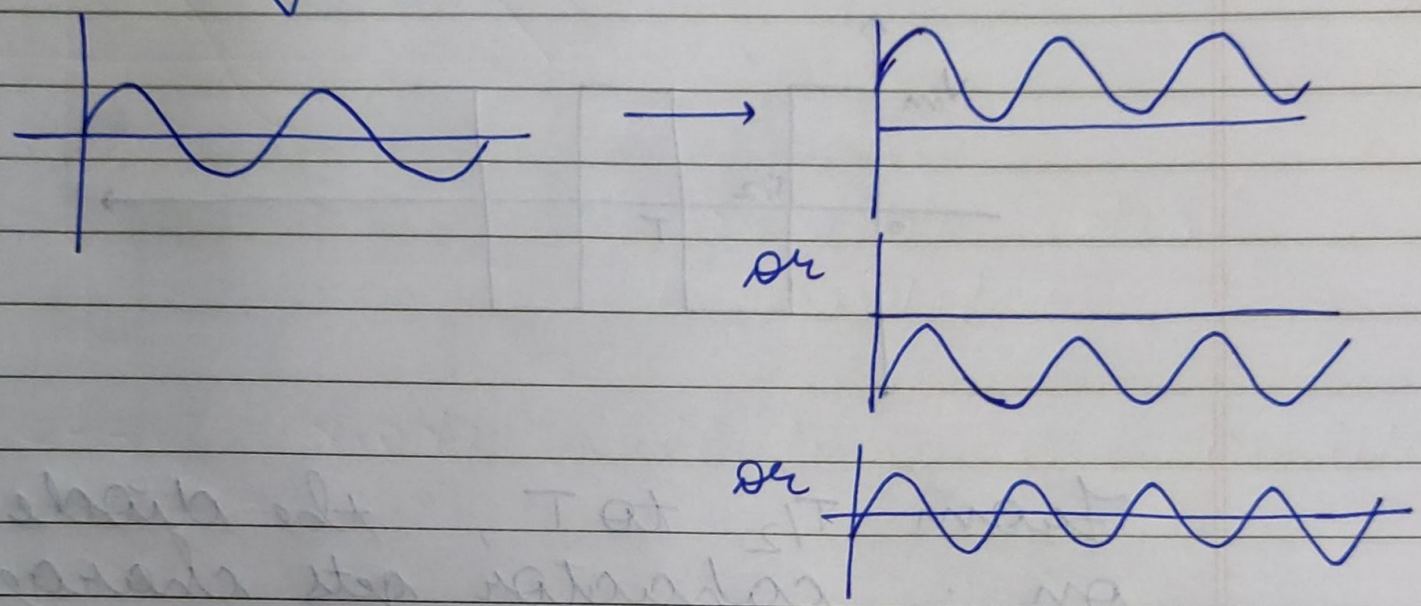
D_2 on D_1 off & $(V_o(t) = -V)$

iii) $-V < V_i(t) < V$

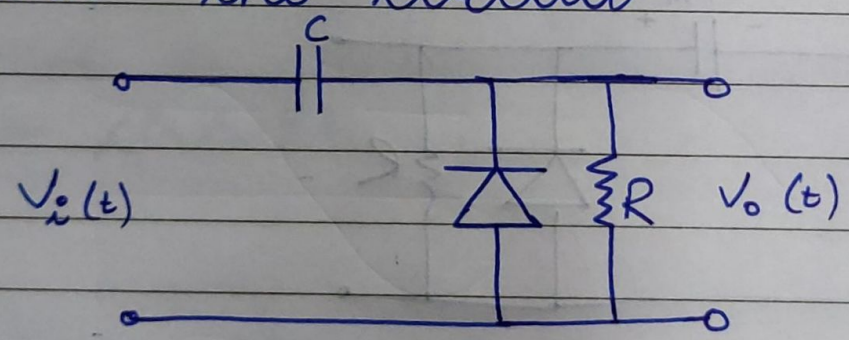
both off & $(V_o(t) = V_i(t))$

the waveform remains same ie no ≠ clipping.

- eg-



- consider the circuit

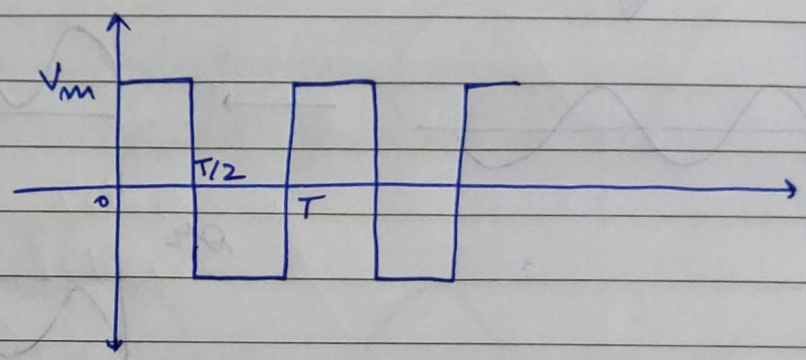


Before analysing the circuit, we make a few considerations

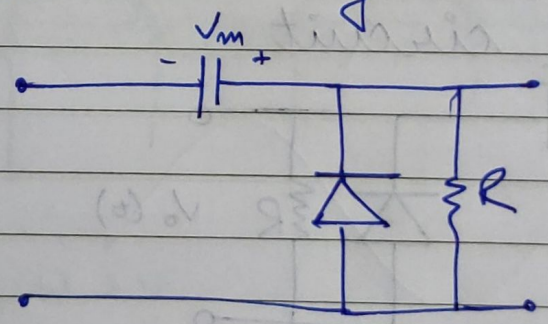
$T = RC$ ie time constant for calcuta

b) Also R is taken very large (say 200) due to this when diode is off, capacitor discharging is not possible as $\tau = RC$ is very very large. ∴ capacitor remains charged.

For input waveform



- From $T/2$ to T, the diode is on ∴ capacitor gets charged to $V = V_m$ instantly



- Now since it does not get discharged and since max amp. of waveform $= V_m$ ∴ the diode is put in off condition forever.

- In $T = T$ to $3T/2$

  no current flows ∴ $V_o = 0$

- In $T = 3T/2$ to $2T$

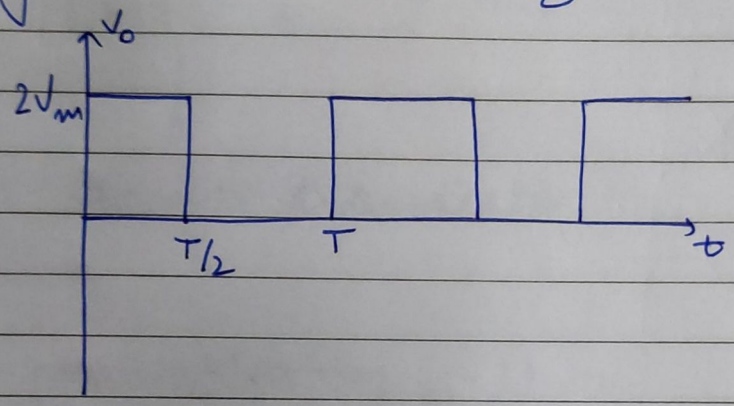
using KVL

$$-V_i(t) + V_o - V_m = 0$$

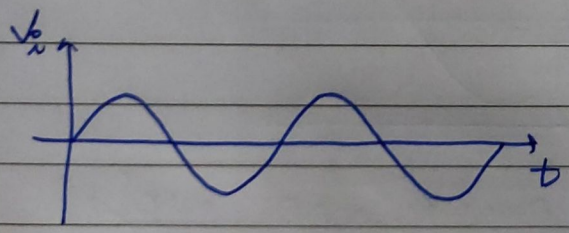
$$\Rightarrow V_o(t) = V_m + V_i(t)$$

$$\therefore V_o(t) = 2V_m$$

$\therefore$ we get output waveform

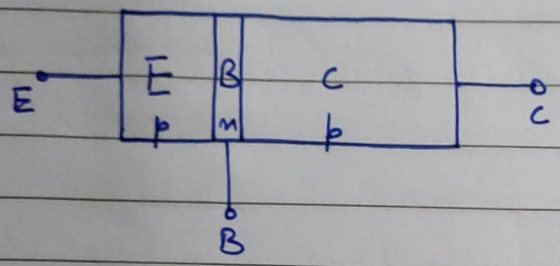


- Consider a sinusoidal waveform for above circuit

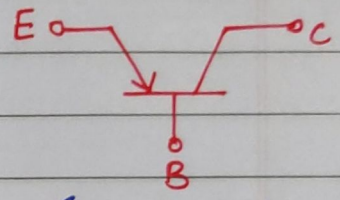


IPOLAR JUNCTION TRANSISTOR →

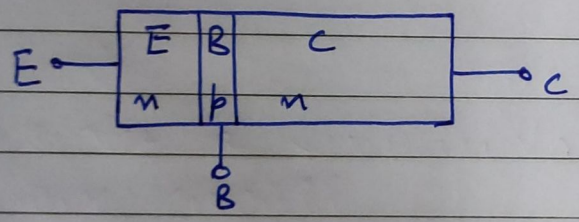
A bipolar junction transistor is a device with three layers of doped semiconductors forming 2 junctions. It may be p-n-p transistor or n-p-n transistor.



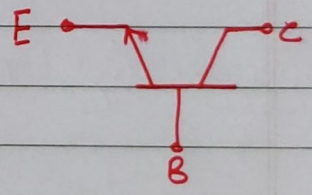
p-n-p transistor



Symbol for p-n-p transistor



n-p-n transistor



Symbol for n-p-n transistor

The doping concentration is as ~~as~~ follows

$$\boxed{N_E > N_C > N_B}$$

p	n	p
E	B	C

EBJ CBJ

$\Longrightarrow$ Two junctio

holes move from emitter to base
~~Since b~~ electrons move from base to emitter. However, since base is lightly doped, and emitter is heavily doped.
∴ the hole movement is very large as compared to electron movement from base i.e. c+a >> b

Now some holes ~~i~~ that reach the base combine with the electrons and thus a free electron is consumed. (c)
Due to this a current I_B is set up which provides the base with electrons to compensate for lost ones

The majority of holes transferred are logically redirected to the collector due

to lower potential there. Also Base and collector are in reverse bias condition. Due to this drift current dominates and holes transfer from base to collector region.

- $I_c = I_{c\,majority} + I_{c\,minority}$

$\Rightarrow$ $\boxed{I_c = \alpha I_E + I_{CBO}}$ (I_{CBO} means when emitter branch is op

However $I_{CBO} \approx 0$ at room temperature

& $\boxed{\alpha \approx 0.9, 0.98, 0.96}$

α is basically the ratio of current from emitter to collector and emi ~~to base~~ total current. ie $\frac{a}{a+c}$

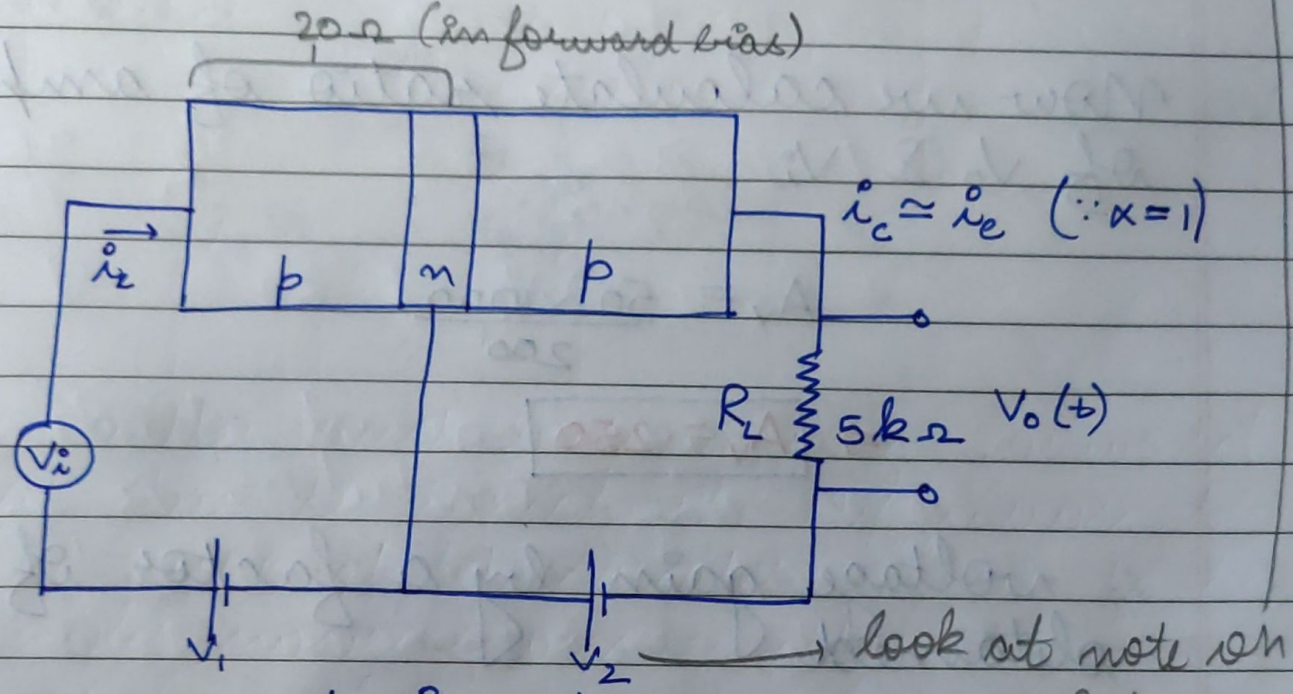
Since $I_{CBO} \approx 0$

$\therefore$ $\boxed{I_c \simeq \alpha I_E}$

V_1 & V_2 are insignificant for calculations and they are only used to keep EB in forward bias and BC in reverse bias.

TRANSISTOR AS AN AMPLIFIER →

Transistor can be used as an amplifier using the below given basic circuit



$V_i = 200\,mV \sin \omega t$

$\Rightarrow i_e = \dfrac{200\,mV}{20} \sin \omega t$

(The resistance of E-B combination in forward bias is 20 Ω, say)

$\Rightarrow i_e = 10\,mA \sin \omega t$

$\therefore i_c = 10\,mA \sin \omega t$ ($\because \alpha = 1$ is assumed)

$\therefore$ We can see the current in the collector will always remain the same. $\therefore$ if we connect a large load resistance, the current ...

$\Rightarrow \quad V_o(t) = 50\,V \sin \omega t$

Now we calculate ratio of amplitude of V_o & V_i

$$A_v = \frac{50 \times 1000}{200}$$

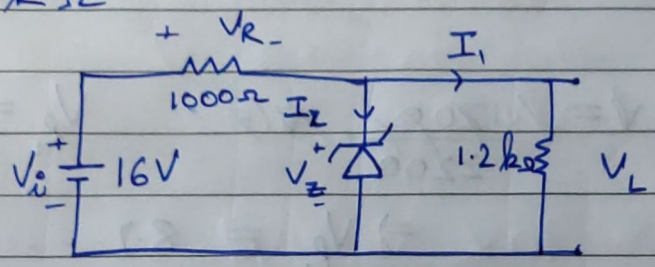
$$\Rightarrow \boxed{A_v = 250}$$

$\therefore$ voltage gain by a factor of 250 is obtained.

WHEN NOT GIVEN USE IDEAL MODEL

TUTORIAL

Q. Determine V_R I_Z and V_Z & repeat with $R_L = 3k\Omega$



$V_Z = 10V$

Ans: a) $V_Z = 10V$

$$I_Z = I_S\left[e^{10/V_T}\right]$$

$V_Z = 10$

$\therefore V_R = 6V$

$$I_R = \frac{6}{1000} = 6mA$$

$$I_1 = \frac{10}{1200}$$

$$\Rightarrow I_1 = \frac{1}{120} A$$

now $I_Z + I_1 = I_R$

$$\Rightarrow I_Z + \frac{1}{120} = \frac{6}{1000}$$

$$\Rightarrow I_Z = \frac{6}{1000} - \frac{1}{120}$$

$$\cancel{V_{R_L} = \frac{R_L}{1000+R_L} \times \frac{16}{2200}} \qquad V_{R_L} = \frac{16}{\frac{2200}{11}} \times \cancel{1200}\,6$$

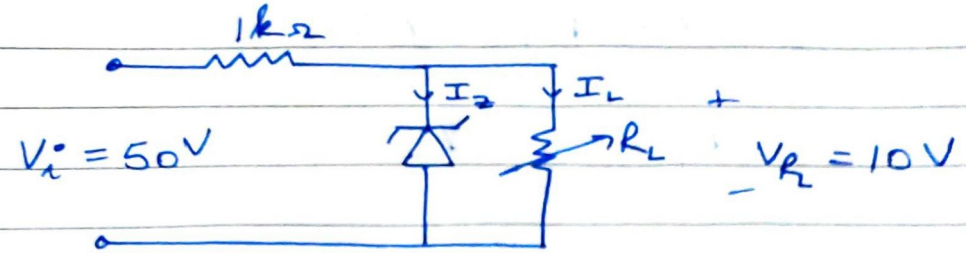
$$\cancel{\Rightarrow V_{R_L} = \frac{1200}{2200} \times 16} \qquad V_{R_L} = \frac{96}{11}$$

$$\Rightarrow V_{R_L} = 8.7\ldots\ V$$

$\therefore$ we were correct diode will be in off condition ie $I_Z = 0$

$$V_R = \frac{16}{2200} \times 1000$$

Q→



Determine range of I_L & R_L that will result in V_{R_L} maintained at 10V. Find $P_{z\,max}$. Given $I_{z\,max} = 32mA$; $I_{z\,min} = 0mA$

Ans:

a) For $I_z = 0\,mA$,

$$V_{R_L} = I_L \times R_L$$

$$I_L = \frac{V_i}{R_L + 1000}$$

$$\Rightarrow V_{R_L} = \frac{50}{R_L + 1000} \times R_L$$

$$\Rightarrow 10R_L + 10000 = 50R_L$$

$$\Rightarrow R_{L_{min}} = 250\,\Omega$$

b) For $I_z = 32\,mA$

Drop of 40 V across 1000 Ω

$$\therefore I = \frac{40}{1000}\,A$$

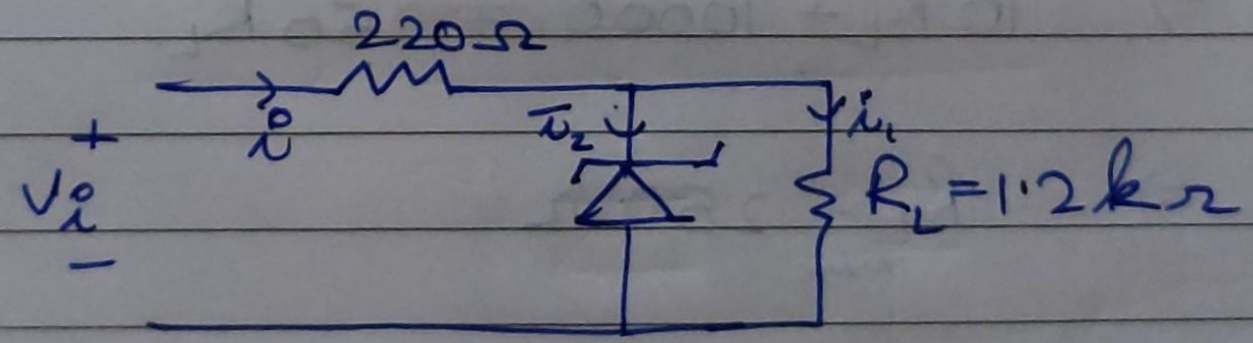
$$I = I_z + I_L \Rightarrow \frac{40}{1000} = \frac{32}{1000} + I_L$$

$$\Rightarrow I_L = \frac{8}{}$$

Q→ Determine range of values of V_i that will maintain zener diode in on state for figure.

$V_Z = 20V$ $\quad I_{Zmax} = 60mA$

$I_{Zmin} = 0mA$



Ans: at $i_Z = 0$

$\frac{\cancel{10}}{\cancel{600}\,3} \times 1420 \Rightarrow V = \frac{11}{3}\ V$

At $i_z = 60\,mA$

$R_L \times i_1 = 20V$

$\Rightarrow i_1 = \frac{10}{600}$

$i = \frac{100}{6000} + \frac{60}{1000}$

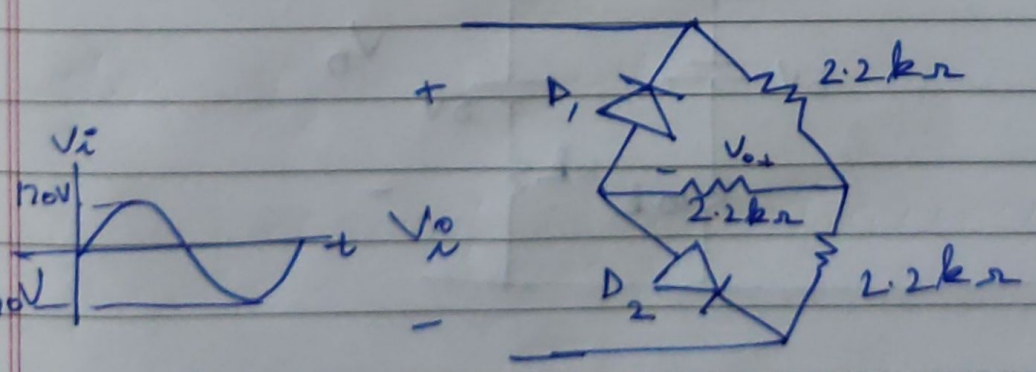
$i = \frac{460}{6000}$

now

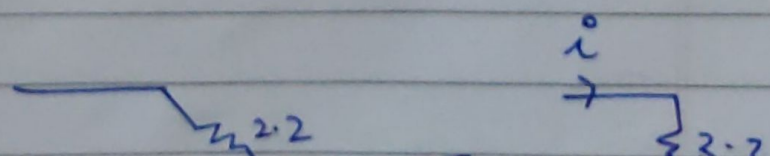
$V = +\frac{46\cancel{0}}{60\cancel{0}\cancel{0}} \times 22\cancel{0} + 20$

$V = 36.8\overline{66}\ V$

Sketch V_o for the figure shown



In +ve cycle



NOTE Transfer Char. = V_o vs V_i plot

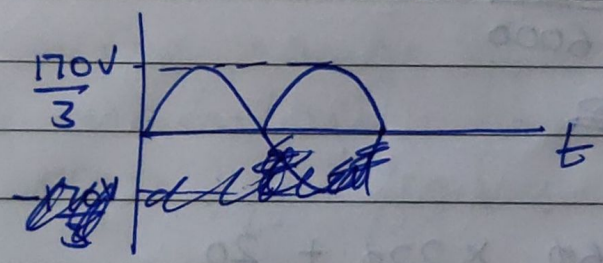
$$V_o = \frac{i}{2} \times 2200 \, V$$

$$\Rightarrow V_o = \frac{V_i}{3.3 \times 2} \times 2200$$

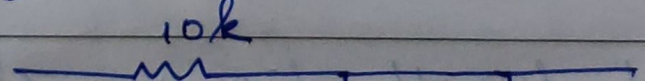
$$V_o = \frac{170}{3 \times 2} \times 2 \; V$$

$$\Rightarrow V_o = \frac{170}{3} V$$

Same for -ve cycle



Q→ Assuming diode to be ideal, plot transfer characteristics



D_1 & D_2 both are in reverse bias

$-5 \leq V_i \leq 5$

$\therefore$ For $-5 \leq V_i \leq 5$

$$V_o = V_i$$

For $V_i < -5$

D_1 turns on

$$\therefore \frac{V_i - 5}{20} \times 10 + 5 = V_o$$

$$\Rightarrow \frac{V_i}{2} + \frac{5}{2} = V_o$$

For $V_i > 5$

We have 3 currents involved

I_E, I_B and I_C

We know

$$I_E = I_B + I_C$$

$$\& \quad I_C = \alpha I_E + \underbrace{I_{CBO}}_{\approx 0}$$

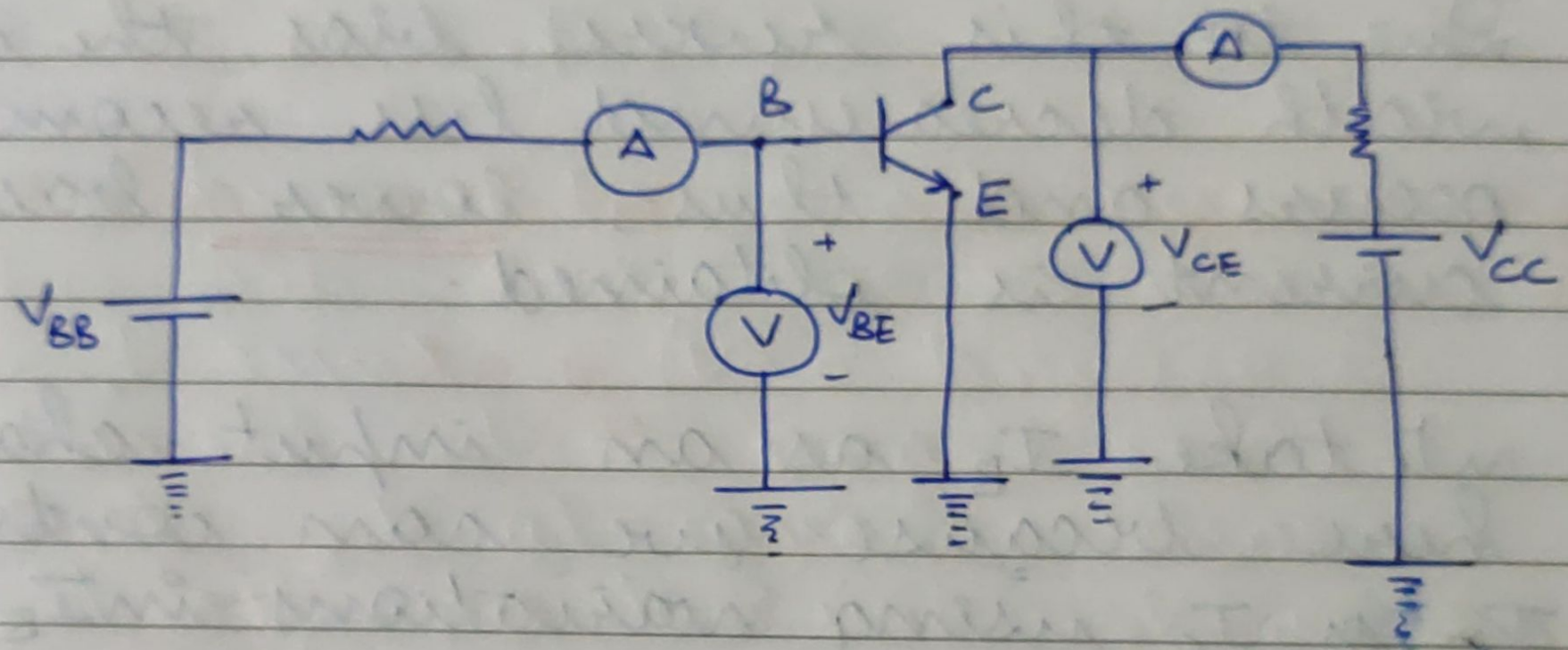
$$\Rightarrow I_C = \alpha I_E$$

$\boxed{\alpha = \text{common base short ckt current}}$

In different configurations, diffe
gains can be obtained ie

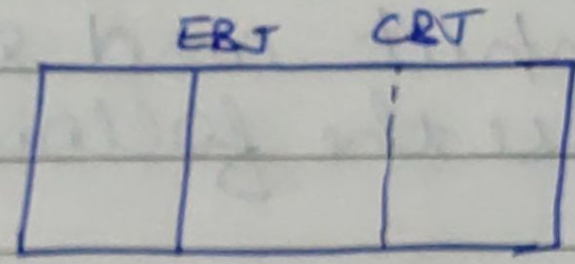
COMMON EMITTER CONFIGURATION →

To observe input and output characteristics, we use the following circuit.



Input characteristics

On increasing V_{CE}, observe carefully that the collector base junction goes into reverse bias



Due to this reverse bias, the depletion width decreases and less recombination occurs and thus, lower base current is obtained.

NOTE: We take I_B as an input character here because we can control I_C using variations in I_B using the relation $I_C = \beta I_B$

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$\Rightarrow (1-\alpha) I_C = \alpha I_B + I_{CBO}$$

$$\Rightarrow I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$

We here define a new quantity

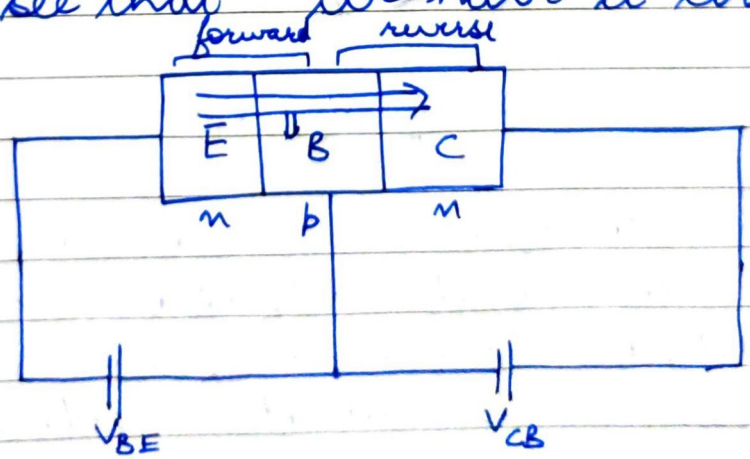
$$\beta = \frac{\alpha}{1-\alpha}$$

$$\therefore \Rightarrow I_C = \beta I_B + (1+\beta) I_{CBO}$$

output input

$$\Rightarrow \boxed{I_C = \beta I_B + I_{CEO}}$$

carefully see that we have a circuit like



We know

$$I_C = \alpha I_E + I_{CBO}$$

Here I_{CBO} is very very small and $\therefore$ I_C mainly depends on I_E which is

dependent on V_{BE} only. And I_{CBO} is dependent on V_{CB}. Due to this, we can say I_c has a major dependency only on V_{BE}.

Consider

$$V_{CE} = V_{BE} + V_{CB}$$

Say we fix V_{BE} at around 0.7V (since its in forward bias, drop expected is around 0.7V). Since V_{BE} is fixed ∴ any change to V_{CE} basically means change to V_{CB}. And we know V_{CB} does not significantly affect I_C. ∴ current becomes constant vs V_{CE} at least in cutoff region.

In saturation region

$$V_{CE} < 0.2\,V$$

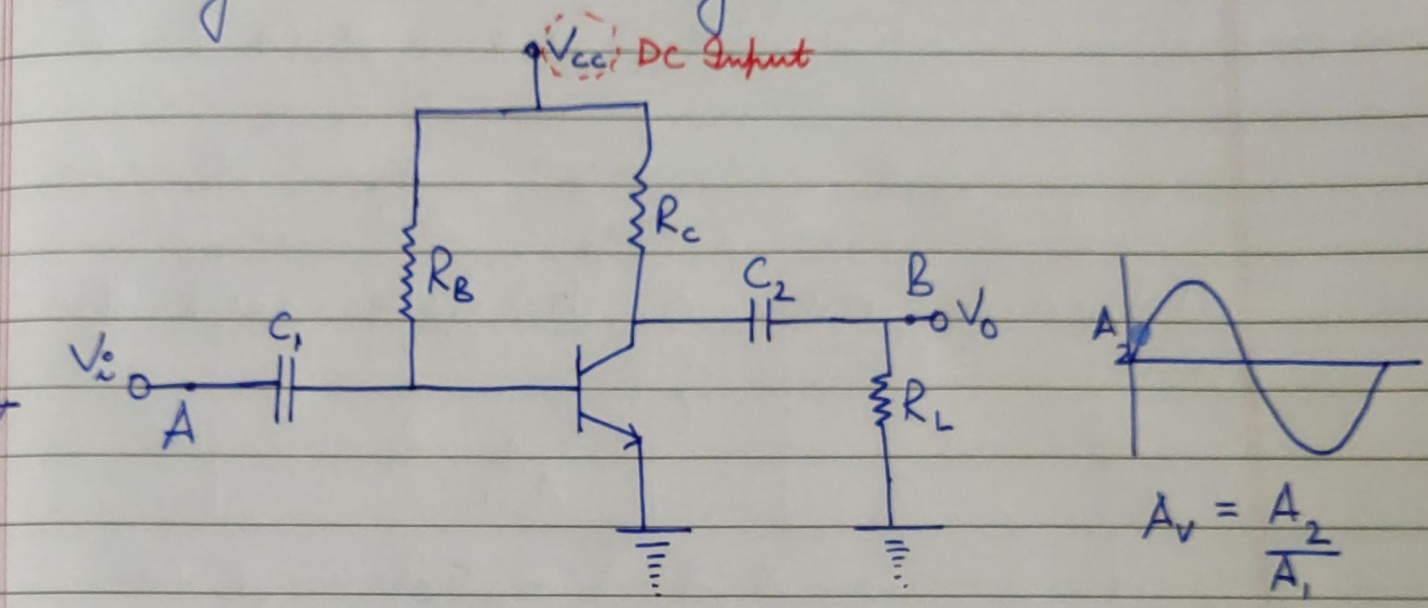
$$\Rightarrow \boxed{V_{CB} < 0}$$

Due to this, CBJ comes in forward bias and diffusion increases and opposes current from emitter. ∴ I_c is somewhat reduced.

∴ we see such a graph.

TRANSISTOR BIASING →

The transistor is used as an amplifier using the circuit given below



In the above circuit, we have both AC and DC inputs into the circuit. Now note that whenever a DC signal is applied across a capacitor, it charges and then acts as an open circuit for the DC signal. Now, note that in the circuit between C_1 and C_2, we have DC inputs for sure but at points A and B, we will have no effect of the DC signal due to the reasons mentioned above. ∴ capacitors prevent DC mixing with either the input or output signal and hence AC signals can be purely obtained. C_1 and C_2 are called coupling capacitors

When $V_i = 0$ there are certain

characteristics in [illegible] point is called Q point (It has a specific I_C, V_{CE} value.)

- The analysis of such a circuit is carried out in 2 steps:

a) DC Analysis
b) AC Analysis

- We will analyse in 3 configurations:

a) Fixed biasing
b) Potential Divider biasing
c) Collector ~~forward bias~~ feedback biasing

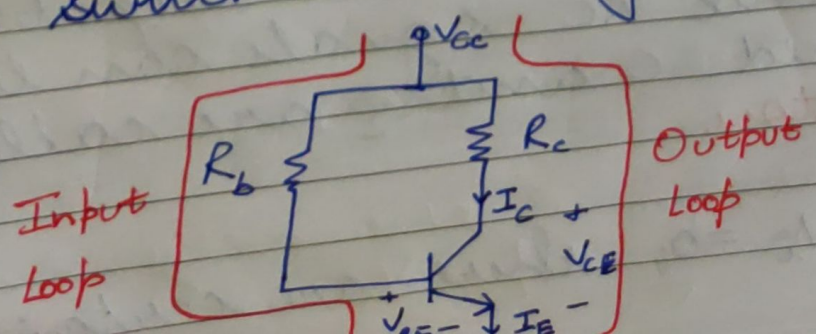
- DC Analysis

- We will carry out this analysis in 3 steps

i) Find I_B
ii) Find $I_C = \beta I_B$
iii) Find V_{CE}

A. Fixed biasing

- In the circuit, capacitors act as an open switch and we get



Here we make 2 considerations

$V_{BE} = 0.7V$ (Since EBJ is in forward bias)

and $I_C \approx I_E$

Clearly we can write

$$V_{CC} - I_B R_b = V_{BE}$$

$$\Rightarrow \boxed{I_B = \frac{V_{CC} - V_{BE}}{R_b}}$$

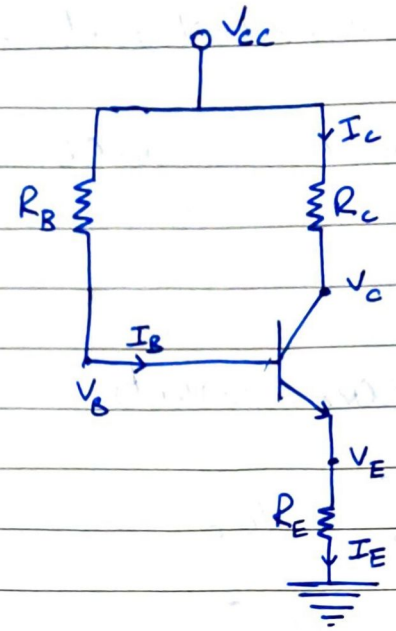
$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_b}} \quad \& \quad \boxed{V_{CE} = V_{CC} - I_C R_C}$$

$$\boxed{I_C = \beta I_B}$$

NOTE: a) 'β' is also called 'hfe' sometimes

b) V_{BE} and β are transistor parameters and may vary with temperature.

- In the above circuit, any changes in β or I_B (Due to V_{BE}) may cause changes in I_C and thus V_{CE} may not be as stable. ∴ we might get a fluctuating DC signal (with, say, changes in temp.) Due to this AC signal may be distort. To prevent this, we use the circuit



- Here, say, ~~xxx~~ ~~xxx~~ V_{BE} increases somehow. Then $I_C \uparrow$ and $I_E \uparrow$. ~~and~~ But ~~Q~~ due to R_E, ~~Q~~ V_E ~~Q~~ increases and in a manner V_{BE} is sort of reduced ie the circuit backfires on any change in V_{BE}.

- Carrying out proper DC analysis,

<u>KVL in input loop</u>

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

$$\& \; I_E = (\beta+1) I_B$$

$$V_{CC} = I_B R_B + V_{BE} + (\beta+1) I_B R_E$$

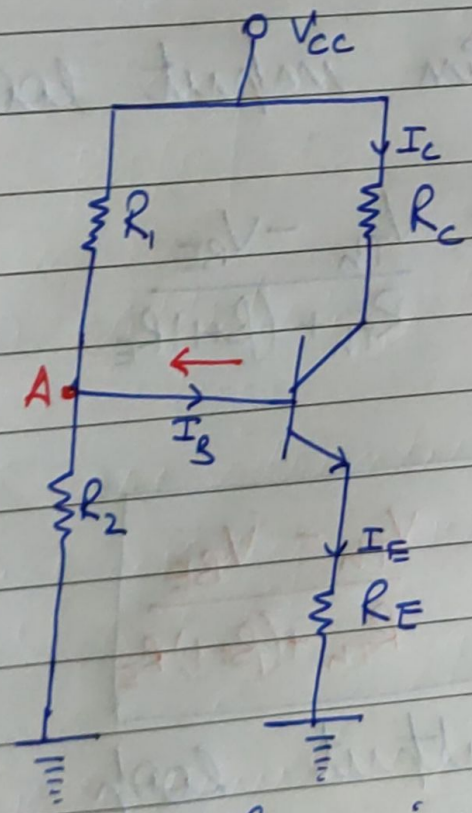
$$\Rightarrow \boxed{I_B = \frac{V_{CC} - V_{BE}}{(\beta+1) R_E + R_B}}$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

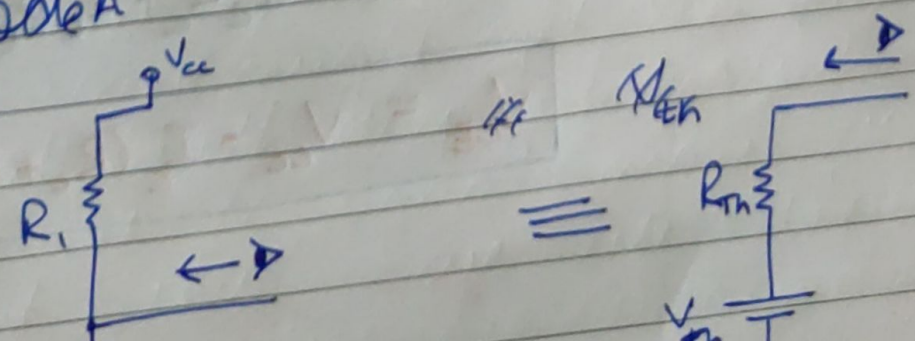
$$\therefore \boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)} \qquad \because \boxed{I_C \approx I_E}$$

On increasing R_C we obtain greater amplification but we need to take care that V_{CE} must not go below 0.2V i.e into saturation region.

Potential Divider biasing



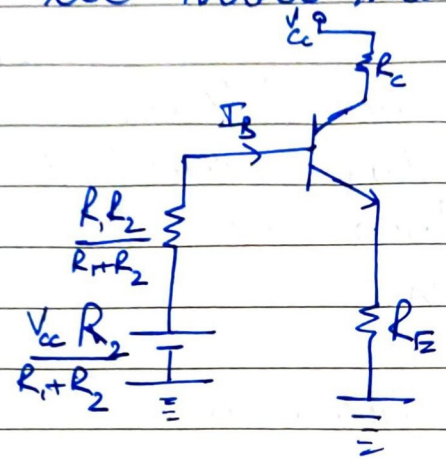
Now we use Thevenin Theorem looking at node A



$$\therefore \quad V_{Th} = \frac{V_{cc} R_2}{R_1 + R_2}$$

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2}$$

$\therefore$ we now have



By KVL in input loop,

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta+1) R_E}$$

$$\boxed{I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta+1) R_E}}$$ and $I_C = \beta I_B$

And in output loop

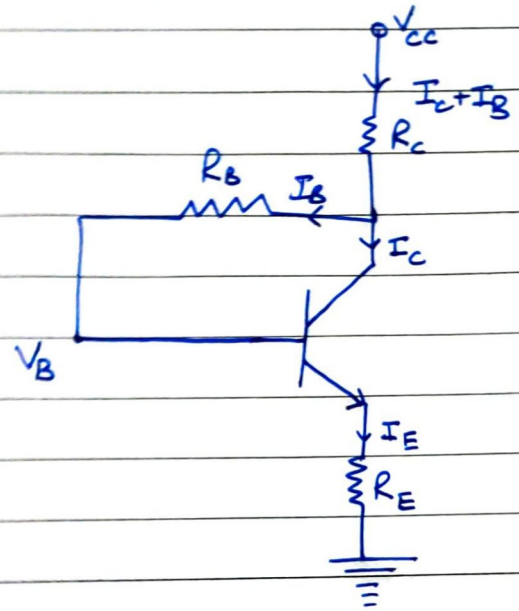
$$V_{CE} - V_{CC} = -I_C R_C - I_E R_E$$

$$\therefore \quad \boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)}$$

Also we can say.

$$\boxed{I_{C_{max}} = \frac{V_{CC} - 0.2}{R_C + R_E}}$$

c. Collector feedback biasing



KVL

$$V_{CC} = I_E R_E + V_{BE} + I_B R_B + R_C (I_C + I_B)$$

$$\Rightarrow V_{CC} = (1+\beta) I_B R_E + V_{BE} + I_B R_B + R_C (\beta I_B + I_B)$$

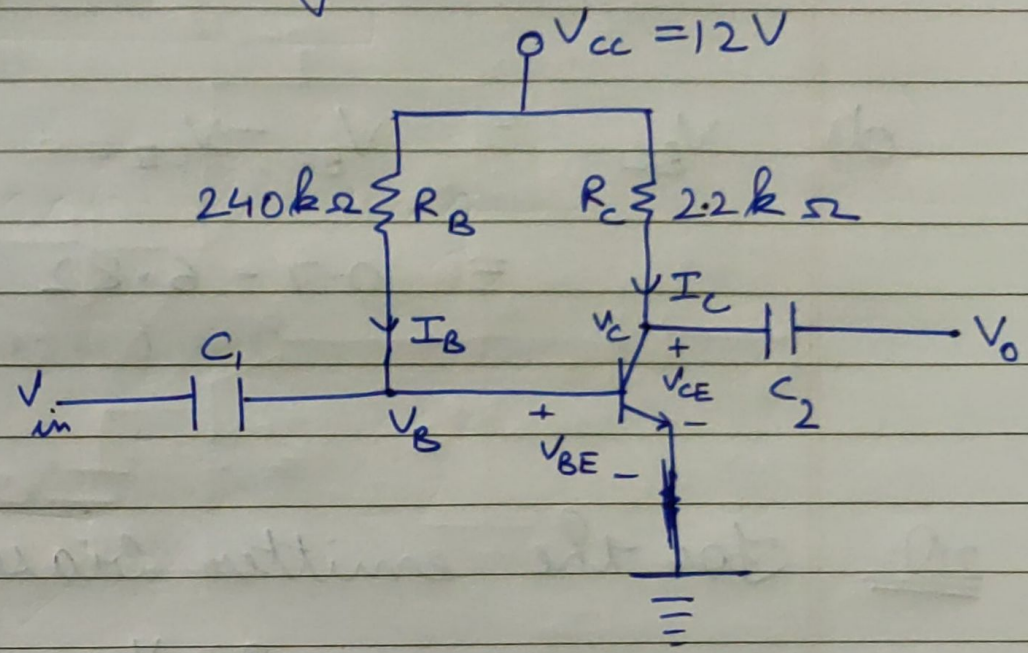
$$\Rightarrow V_{CC} - V_{BE} = \left[(\beta+1) R_C + (\beta+1) R_E + R_B \right] I_B$$

$$\Rightarrow \boxed{I_B = \frac{V_{CC} - V_{BE}}{(\beta+1) R_C + (1+\beta) R_E + R_B}}$$

TUTORIAL

Que: Determine the following for given circuit

a) I_B and I_C
b) V_{CE}
c) V_B and V_C
d) V_{BE}



$\beta = 50$
$V_{BE} = 0.7V$

Ans: a) $V_{BE} + I_B R_B = 12$

$$\Rightarrow I_B = \frac{12 - V_{BE}}{240} \text{ mA}$$

$$\Rightarrow I_B = \frac{11.3}{240} \text{ mA} = 47.08 \mu A$$

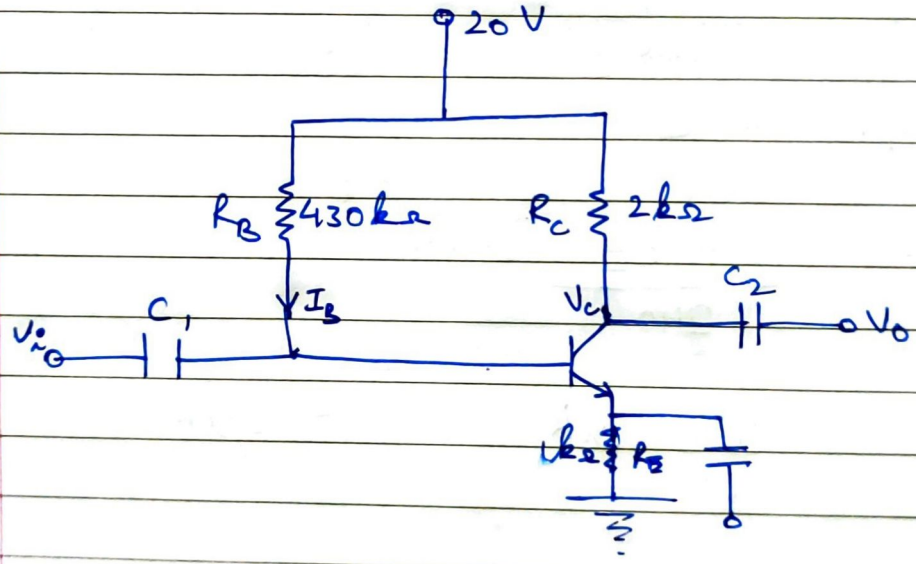
c) $V_B = V_{BE} = 0.7V$

$$V_C = V_{CE} = 12 - \frac{5 \times 11.3 \times 22}{24}$$

d) $V_{BC} = V_{BE} - V_{CE}$

$= 0.7 - 6.82 = 6.120V$

2Q: For the emitter biased network



Find i) I_B ii) I_C iii) V_{CE} iv) V_C

v) V_E vi) V_B vii) V_{BC}

Ans: i)

$$I_E R_E + V_{BE} + I_B R_B = 20$$

$$\Rightarrow (1+\beta) I_B R_E + V_{BE} + I_B R_B = 20$$

$$\Rightarrow I_B = \frac{20 - V_{BE}}{(1+\beta)R_E + R_B}$$

$$\Rightarrow I_B = \frac{20 - 0.7}{(1+50)1 + 430} \text{ mA} = 40.124 \ \mu A$$

ii) $I_C = \beta I_B$

$$\Rightarrow I_C = (50 \times 40.124) \ \mu A$$

$$\Rightarrow I_C = 2.006 \text{ mA}$$

iii) ~~V_{CE} 7 (I_B~~

$$I_E R_E + V_{CE} + I_C R_C = 20$$

$$\Rightarrow 51 I_B \times 1 + V_{CE} + 50 I_B 2 = 20$$

$$\Rightarrow V_{CE} = 20 - 51 (0.040124) - 100 (0.040124)$$

$$\Rightarrow V_{CE} = 13.941 \text{ V}$$

iv) $V_C = 1 \times I_E + V_{CE}$

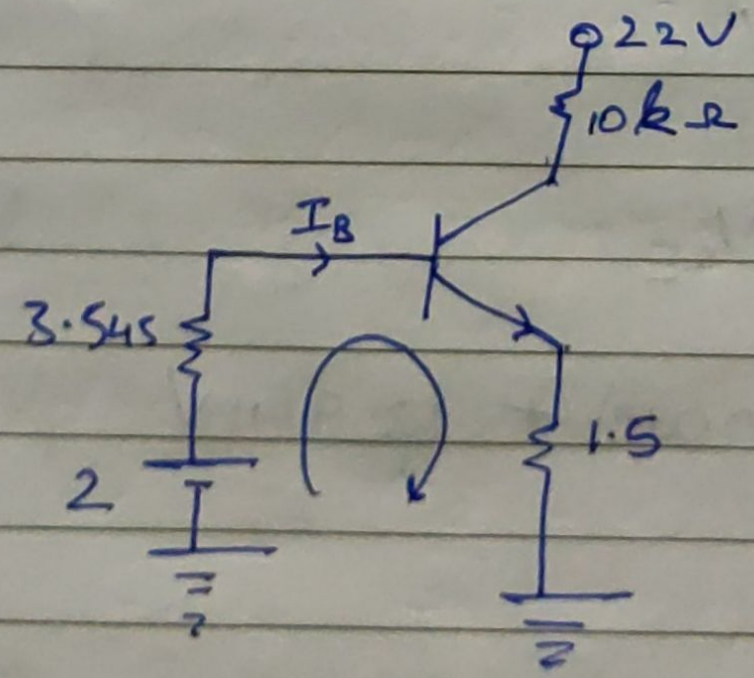
$$\Rightarrow V_C = 51 (0.040124) + 13.941 \text{ V}$$

$$\Rightarrow V_C = 15.987 \text{ V}$$

v) $V_E = I_E \times 1$

$$V_{Th} = \frac{22 \times R_2}{R_1 + R_2} = \frac{22 \times 3.9}{39 + 3.9} = 2V$$

$$R_{Th} = \frac{39 \times 3.9}{39 + 3.9} = 3.5454 k\Omega$$



$$\Rightarrow \frac{1.3}{3.5454 + 1.5\times 101} = I_B = 8.22\,\mu A$$

$$1.5 I_E + V_{CE} + 10 I_C = 22$$

$$\Rightarrow V_{CE} = 22 - 1.5(\beta+1) I_B - 10\beta I_B$$

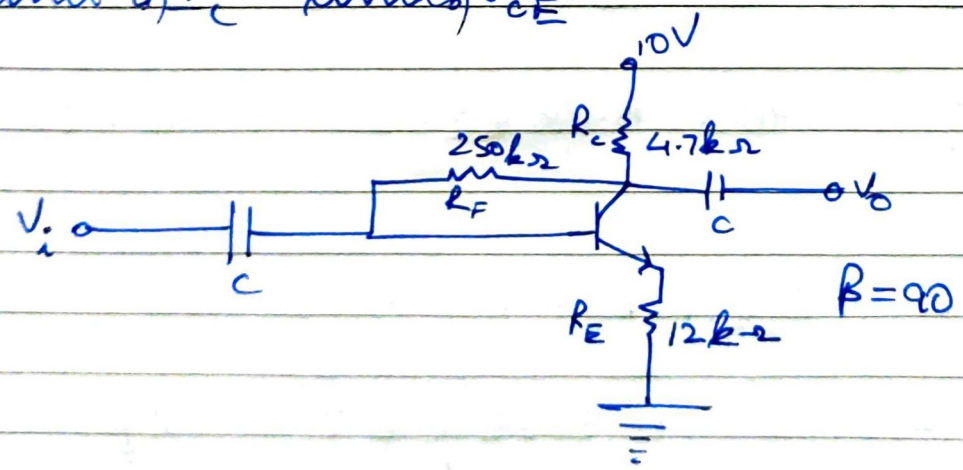
$$\Rightarrow V_{CE} = 22 - 1.5(101)\frac{1.3}{3.5454+1.5\times 101} - \frac{1000\times 1.3}{3.5454+1.5\times 101}$$

b) $I_C = \beta I_B$

$$= \frac{100 \times 1.3}{3.5454 + 1.5\times 103}\ mA$$

$$= 0.822\ mA$$

4Q→ Find a) I_C and b) V_{CE}



Ans: a) $10 - I_C R_C - 250 I_B - V_{BE} - I_E R_E = 0$

$\Rightarrow 10 - \beta I_B 4.7 - 250 I_B - 0.7 - (\beta+1) I_B \times 12 = 0$

$\Rightarrow 9.3 - 90\times 4.7 I_B - 250 I_B - 91\times 12 I_B = 0 \quad \Rightarrow I_B = 5.269\,\mu A$

$$\Rightarrow 10 - 91 \times 4.7 - 250 I_B - 0.7 - 12 \times 91 I_B = 0$$

$$\Rightarrow I_B = \frac{9.3}{1769.7} = 5.255 \mu A$$

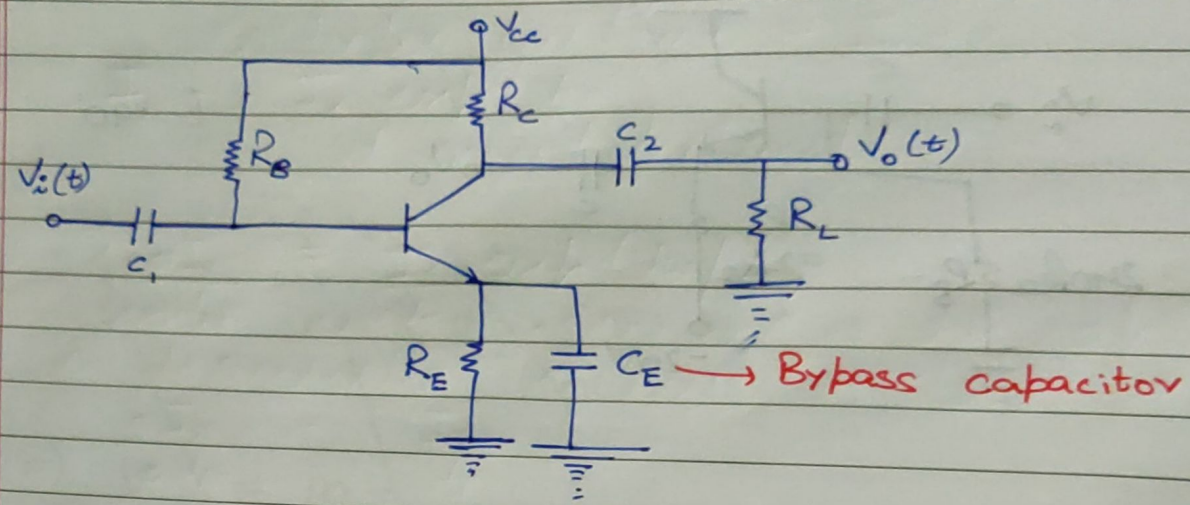
$$\Rightarrow I_C = 90 \times 0.005255 = 0.4729 \text{ mA}$$

b) $10 = (1+\beta) I_B (R_E + R_C) + V_{CE}$

$$\Rightarrow 10 = 91 \times 0.005255 (16.7) + V_{CE}$$

$$\Rightarrow V_{CE} = 2.01378 \text{ V}$$

b) AC or small signal Analysis



The above circuit is an amplifier circuit

Background study

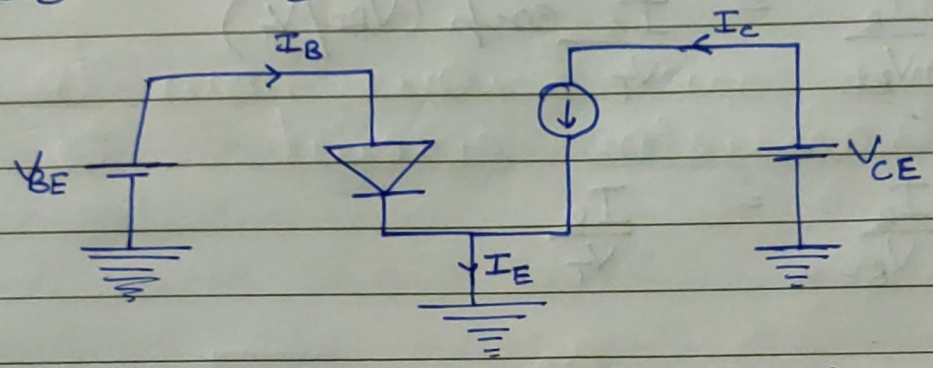
- In the above circuit, R_E (remember from before) is used to stabilize the DC components in the circuit. However, if AC is provided, then this resistor hinders amplification & to counter this, we use a 'bypass capacitor'. Due to high frequency, impedence of capacitor is low and thus AC signal prefer to get into capacitor branch.

NOTE: The I_s for calculating I_C is different from I_s for calculating I_B will be different $I_{s_1} > I_{s_2}$

It can be derived (derivation out of syllabus)

$$I_C = I_s \exp\left(\frac{V_{BE}}{V_T}\right)$$

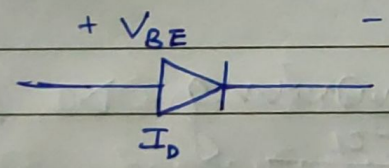
Now we will represent above transistor in a different form



We replace collector branch by a current source

$$I_C = I_s \exp\left(\frac{V_{BE}}{V_T}\right)$$

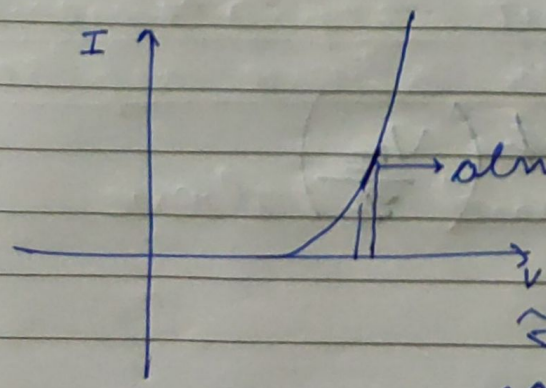
Now we consider the diode branch



$\therefore$

$$I_B = I_D = I_s \exp\left(\frac{V_{BE}}{V_T}\right)$$

This diode basically acts as a resistor for small changes in V_{BE}



→ almost linear graph for small ΔV_{BE}

for : $\Delta V_{BE} < 25\,mV$

For very small ΔV_{BE} we can consider linearity

NOTE: We are here actually removing V_{CC} ie DC source and then observing the changes made in circuit of V_{BE} is varied.

∴ we will replace diode by a resistor and to find resistance,

$$I_B = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$$

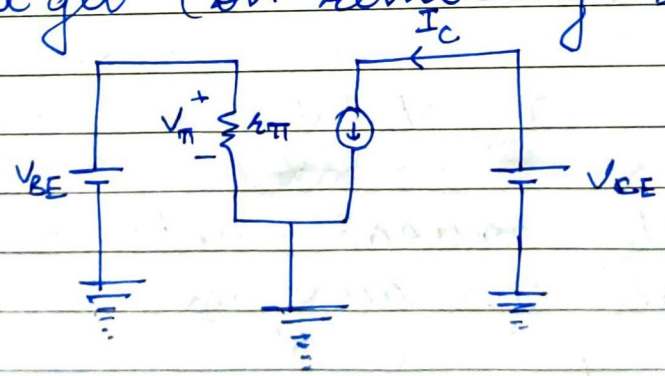
$$\Rightarrow \frac{\partial I_B}{\partial V_{BE}} = \frac{I_S}{V_T} \exp(V_{BE}/V_T)$$

$$\Rightarrow \frac{\partial I_B}{\partial V_{BE}} = \frac{I_B}{V_T}$$

$$\Rightarrow \frac{\partial V_{BE}}{\partial I_B} = \frac{V_T}{I_B} = r_\pi$$

$$\Rightarrow \boxed{r_\pi = \frac{V_T}{I_B}} \qquad \boxed{\Delta V_{BE} = V_\pi}$$

∴ we get (on removing DC source)



Now $I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$

$$\Rightarrow \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{V_T}$$

We define a quantity g_m ie transconductance

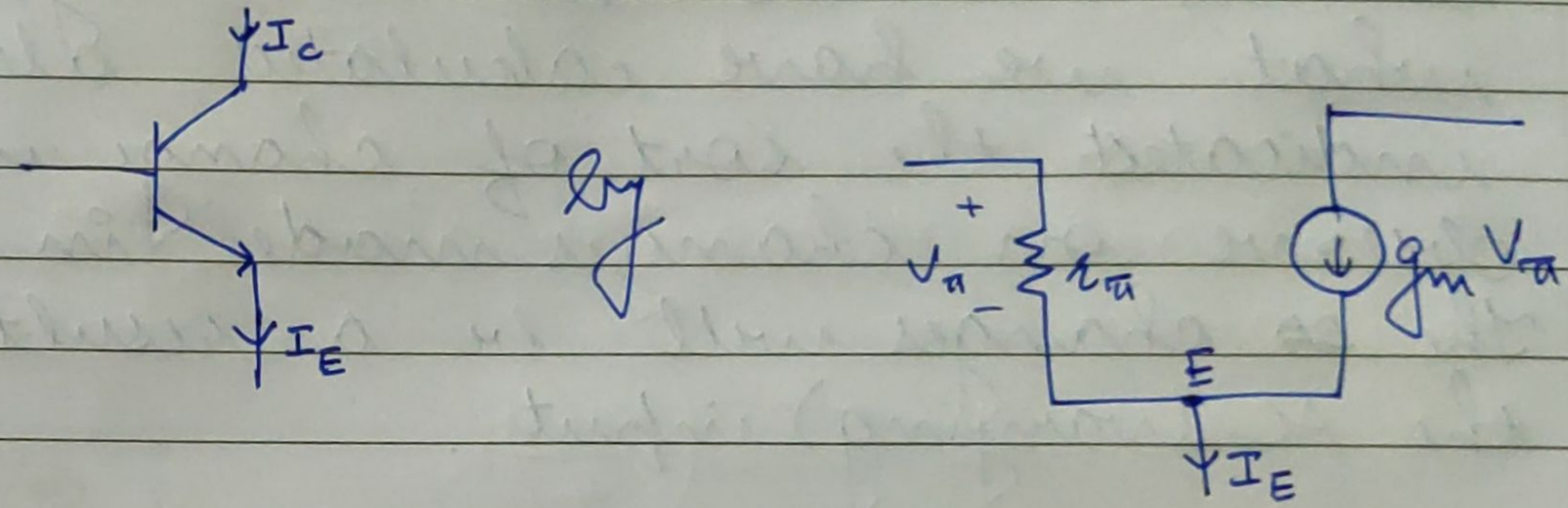
as

$$\boxed{g_m = \frac{I_C}{V_T}}$$

$$\therefore \quad \boxed{r_\pi = \frac{\beta}{g_m}}$$

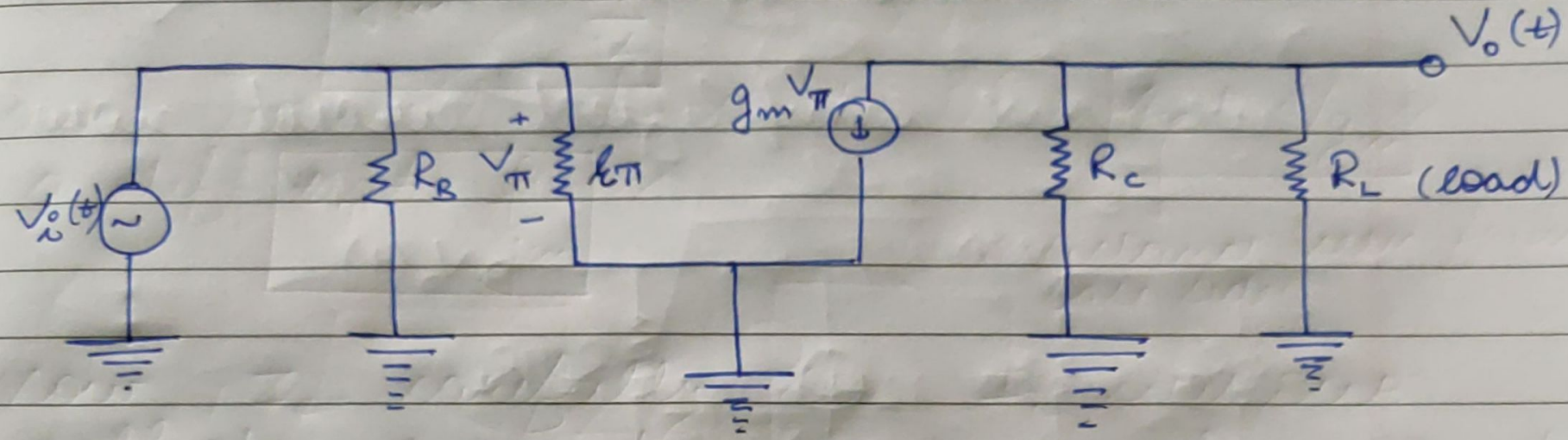
now ~~I_C~~ carefully see, I_C was our collector current in DC analysis, and what we have calculated above indicates the sort of change we will observe on changes made in V_{BE}. The ~~co~~ changes will be a result of the AC (varying) input.

$\therefore$ Using superposition, we can write any quantity $q = q_{DC} + q_{AC}$

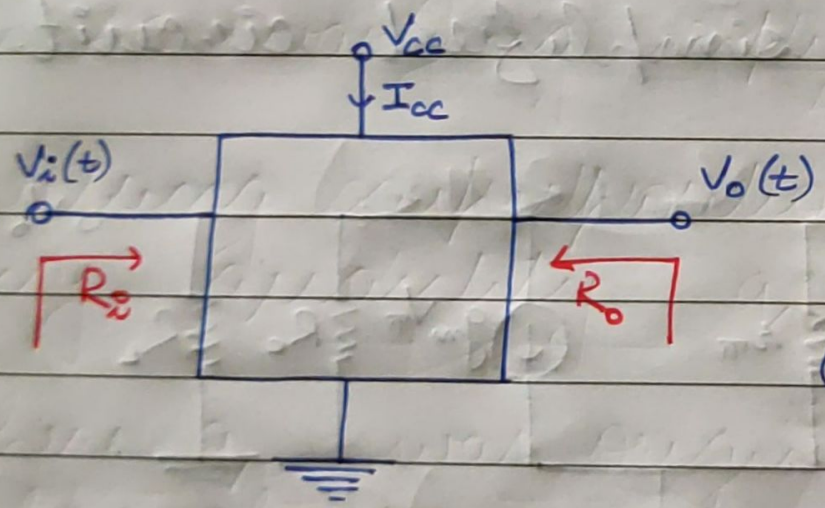


e.

- In original circuit now, when we consider AC component only, a) $V_{CC} = 0$ (since DC sources need to be remov and b) the capacitors behave mo or less like conductors due to low impedance (due to high ω). Also, we c) carry out replacement o transistor as per above replacem



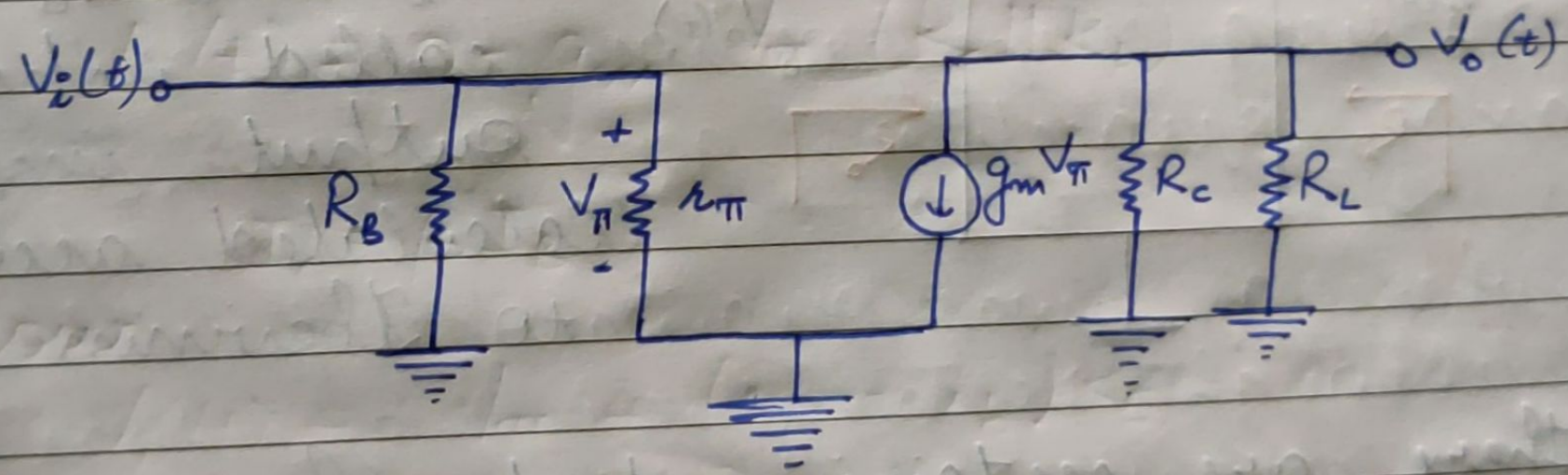
∴ we have this excessively simplified sort of circuit for analysing AC component



R_i and R_o are called input and output impedances (calculated according to Thevinin model)

There are certain output characteristics

- now, we had a simplified circuit as



will try to find A_v for

$$\Rightarrow \frac{V_o(t)}{V_i(t)} = -g_m (R_c \| R_L)$$

$$\Rightarrow A_v = \frac{V_o(t)}{V_i(t)} = -g_m (R_c \| R_L)$$

$$\therefore \boxed{A_v = -g_m (R_c \| R_L)}$$

If $R_L \longrightarrow \infty$

$$\boxed{A_v = -g_m R_c}$$

$\therefore$ we observe that there is a phase differen b/w input and output waveforms

- In above circuit,

$R_o = R_c \| R_L$ (Thevinin b/w $V_o(t)$ and groun

$R_i = R_B \| r_\pi$ (Thevinin b/w $V_i(t)$ & grou

NOTE: At higher values of R_i (say $\longrightarrow \infty$), we get better amplification. This is because $V_i(t)$ has internal resistanc and if R_i is large, internal 'r' does not affect input of voltage.

We will find $V_o(t)$ & R_i

$$V_o(t) = 0 - g_m V_\pi (R_C \| R_L)$$

$$I_C = \beta I_B$$

Now

$$V_i(t) = V_\pi + (i_c + i_b) R_E$$

Since i_b is small,

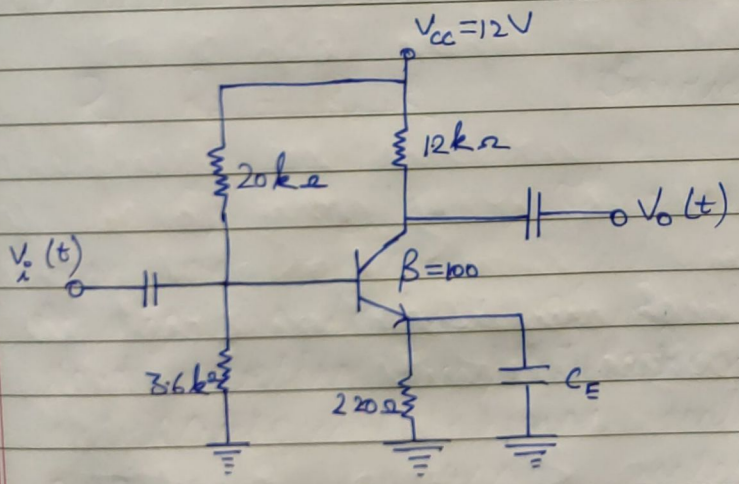
$$V_i(t) = V_\pi + (i_c) R_E$$

~~Since~~ ∴

$$A_v = \frac{-g_m (R_C \| R_L)}{1 + g_m R_E}$$

now, we will find R_i.

Q→



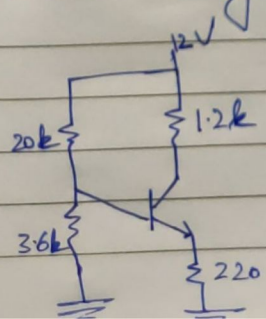
Find

a) A_v

b) R_i

c) R_o

Ans DC Analysis



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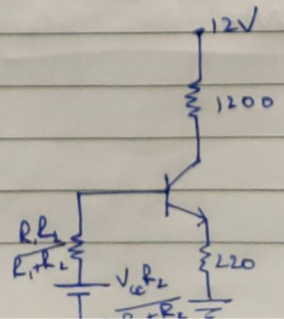


$$R_{Th} = \frac{20 \times 3.6}{20 + 3.6}$$

$$V_{Th} = \frac{12 \times 3.6}{20 + 3.6}$$

$$V_{Th} - I_B R_{Th} + \beta I_B 1.2 = 12$$

$$\Rightarrow I_B (\beta 1.2 - R_{Th}) = 12 - V_{Th}$$

$$\Rightarrow I_B = \frac{12 - V_{Th}}{1.2\beta - R_{Th}}$$

$$\Rightarrow I_B = \frac{12 - 1.839}{120 - 3.09}$$

NOTE: a) $A_v = -g_m (R_C \| R_L)$ – valid when load is connected

b) $A_v = -g_m R_C$ – valid when no load is connected

c) $A_v = \dfrac{-g_m R_C}{1 + g_m R_E}$ – valid when emitter resistance is not bypassed.

Also $g_m = \dfrac{1}{r_e}$

∴ in b) and c), we get

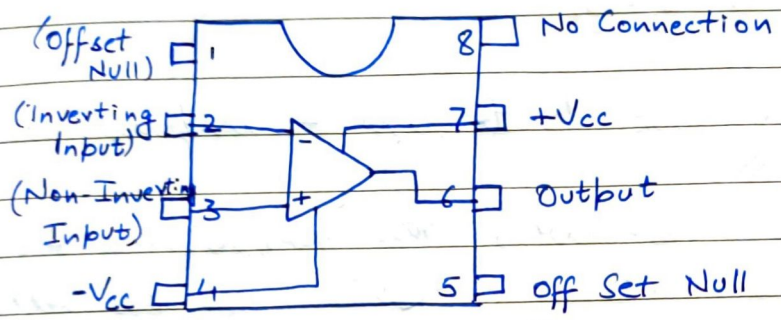
$$A_v = -\frac{R_C}{r_e}$$

$$A_v = \frac{-R_C}{R_E + r_e}$$

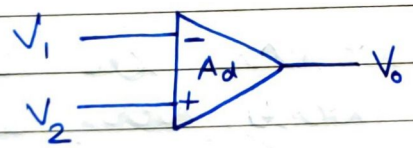
∴ we can observe that A_v ie voltage gain is total collector resistance / total emitter resistance.

OPERATIONAL AMPLIFIER (OP-AMP)

- It is an integrated circuit and is a combination of around 20 transistors.
- It has ~~20~~ 8 terminals (pins) conventionally. IC741 is a common OP-AMP used



- $+V_{cc}$ and $-V_{cc}$ pins are not used in general practice and we get



A_d : (Differential voltage gain) ~~Often Look~~

$$\boxed{V_o = A_d (V_2 - V_1)}$$

- $V_2 \uparrow$ then $V_o \uparrow$ $\therefore$ V_2 is non inverting input

  $V_1 \uparrow$ then $V_o \downarrow$ $\therefore$ V_1 is inverting input.

- For an ideal OP-AMP

a) $A_d = \infty$
b) $R_i = \infty$
c) $R_o = 0$
d) $BW = \infty$ (Bandwidth)

- ∴ we can conclude for open loop ideal OP-AMP

$$V_2 - V_1 = \frac{V_o}{A_d} = 0$$

$$\Rightarrow V_2 = V_1$$

$$\Rightarrow V_2 = V_1$$

∴ say we put an AC input at V_2, then we will get the same AC signal at V_1. This replication of signal is called virtual short.

- generally, for open loop OP-AMP,

$A_d \approx 10^6$ ∴ we can see amplification magnitude is very very large. Say $V_2 - V_1 = 1mV$, then $V_o \approx 10^3 V$. This sort of high amplification is not useful in electronic circuits

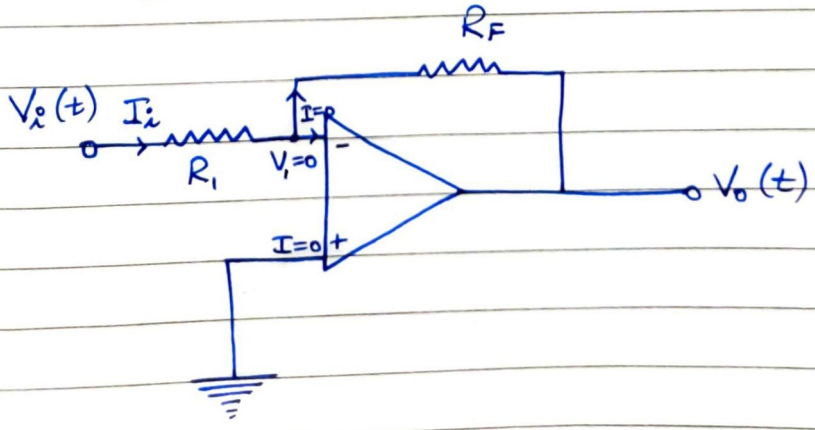
- $\boxed{R_i \approx 10^6 \Omega}$; $\boxed{R_o = 50 \Omega}$ and

$\boxed{BW = 6 MHz}$

Band Width

It is the range of frequencies of AC signal for which the transistor works as per calculations. In previous BJT discussion, we had taken a case of frequency e/w bandwidth. If frequency is very low, (in BJT case) then $\frac{1}{\omega C}$ would be high and AC amplification would not be facilitated by capacitors. In case of very very high freq., our circuit (transistor components) behave in a different manner (due to say damage) and we observe a decrease in ~~AC~~ ~~Eq~~ A_v (gain) because it becomes a function of frequency.

- We basically need to reduce the amplification for electronic circuits. For this purpose, we use the following sort of circuit.



Since OP-AMP is ideal, $A_d \to \infty$ and $R_i \to \infty$. Due to this, $V_2 = V_1 = 0V$

and also due to $R_i \to \infty$, I in both branches $= 0$

$$\therefore \quad I_i = \frac{V_i(t)}{R_1}$$

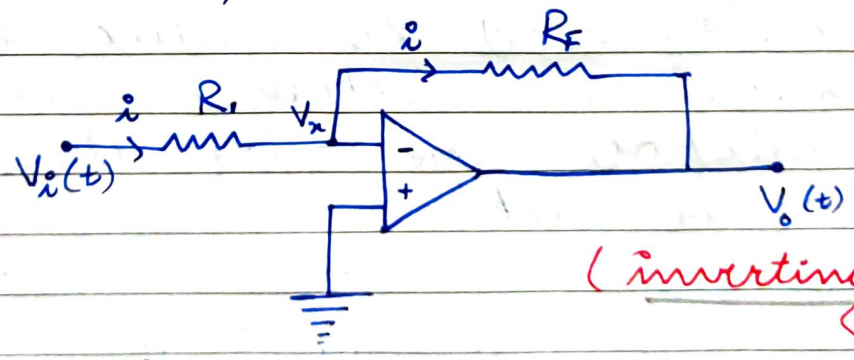
$$V_o(t) = -I_i R_F$$

$$\Rightarrow V_o = -\frac{V_i}{R_1} \times R_F$$

$$\Rightarrow \boxed{\frac{V_o(t)}{V_i(t)} = -\frac{R_F}{R_1} = A_v}$$ (IDEAL CASE)

(out of phase)

- If we consider case of non-ideal OP-AMP,



(inverting amplifier)

$A_d \neq \infty$

$$\Rightarrow V_2 - V_1 = \frac{V_o}{A_d}$$

$$\therefore V_o(t) = (0 - V_x) A_d$$

$$\Rightarrow V_x = \frac{-V_o(t)}{A_d}$$

now, we can also see that current entering input brach flows as such in R_F branch (ie it does not split) due to high resistance(R_i) of OP-AMP

Also: we can write

$$V_o(t) = V_x - iR_F$$

&

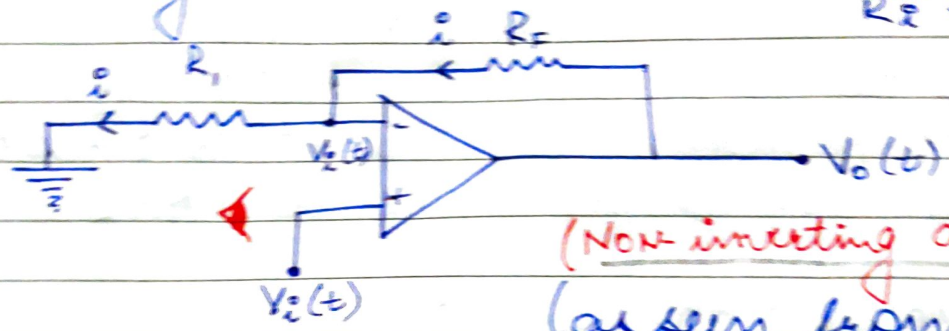
$$i = \frac{V_i - V_x}{R_1}$$

$$\Rightarrow V_o = V_x - (V_i - V_x)\frac{R_F}{R_1}$$

$$\Rightarrow \boxed{A_v = \frac{V_o(t)}{V_i(t)} = \frac{-R_F/R_1}{1 + \frac{1}{A_d}\left(1 + \frac{R_F}{R_1}\right)}}$$ (NON-IDEAL CASE)

We can see here that if $A_d \to \infty$ then we get $A_v = -R_F/R_1$!!

- We can have an even better circuit as considering ideal OP-AMP (ie $A_d \to \infty$, $R_i \to \infty$)



(Non-inverting amplifier)

(as seen from here $R_i = \infty$ since OP-AMP has ∞ R_i in ideal case)

$$i = \frac{V_i(t)}{R_1}$$

&

$$V_o(t) = V_i(t) + i R_F$$

$$\Rightarrow V_o(t) = V_i(t) + V_i(t)\frac{R_F}{R_1}$$

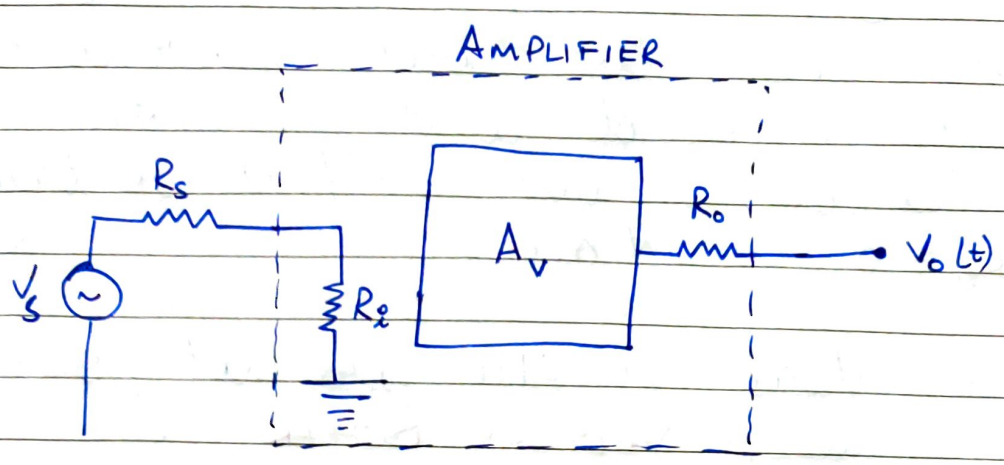
$$\Rightarrow \boxed{A_v = \frac{V_o(t)}{V_i(t)} = 1 + \frac{R_F}{R_1}}$$

(in phase)

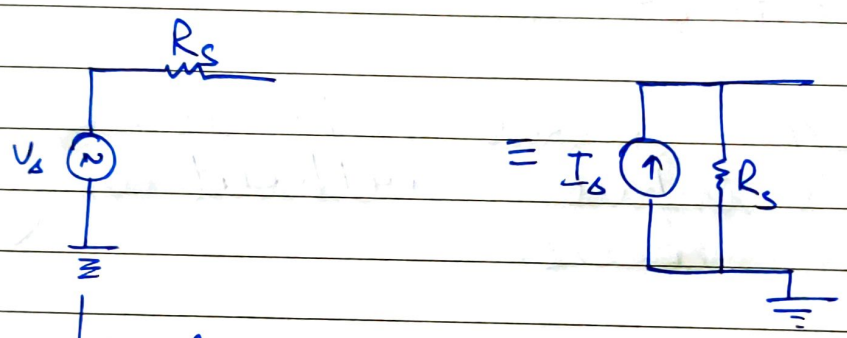
NOTE: For an ideal voltage amplifier, R_i (input impedance as seen from input terminal) must be very high and for ideal current amplifier R_i must be zero.

NOTE

Consider an amplifier basic structure



We have 2 sort of sources (interconvertable)



In this case

Consider if R_i is finite, ~~tho~~ then the input branch will obviously have some flow of current. And due to non-ideality of source, we also have a resistance R_s before the input terminal. ∴ Due to it we will have some potential drop if current flows in the circuit (of iR_s) Due to this we have a loss in input voltage. But if $R_i \longrightarrow \infty$, then $i = 0$ ∴ we have identical input voltage. ∴ $R_i \to \infty$ in ideal voltage amplifier.

Also, R_o must be zero. This is because, the

output branch will always have some current, say i_o. So, if $R_o \neq 0$, then we will have some drop across it and we will get a loss in our output voltage.
$\therefore R_o = 0$ for ideality.

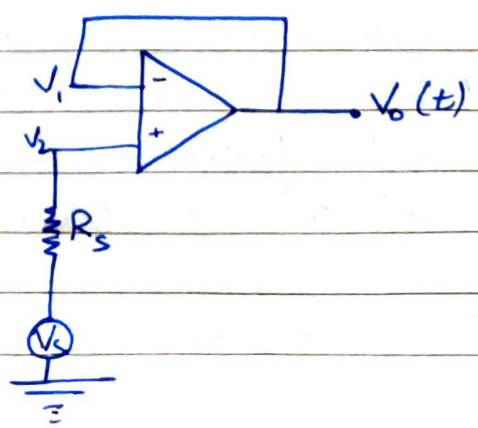
Since ideal OP-AMP are not possible, $\therefore$ we use a VOLTAGE BUFFER for input correction.

→ VOLTAGE BUFFER →

- A voltage buffer helps us in giving input without any voltage losses.
- A voltage buffer has the following characteristics

$R_i = \infty$
$R_o = 0$
$A_v = 1$

- Its circuit is as follows



$A_d = \infty$

Due to $R_i = \infty$ & $A_d = \infty$

$V_2 = V_i(t)$

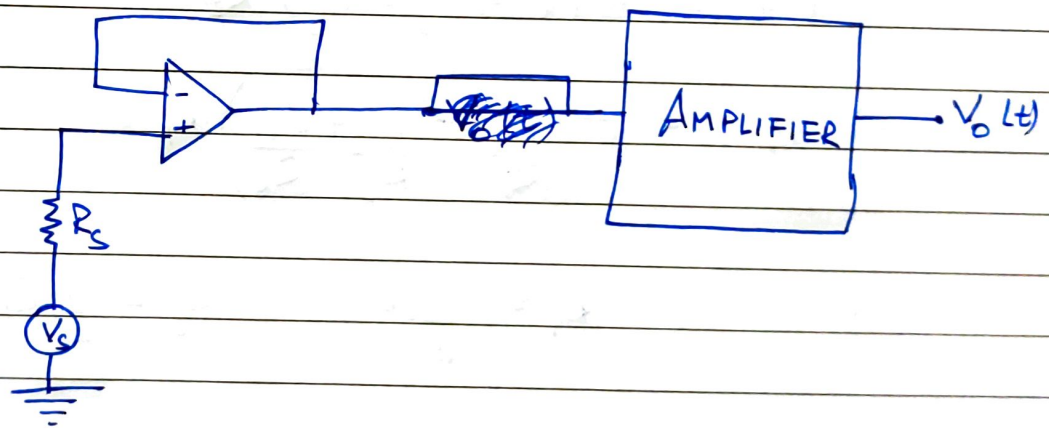
and $V_2 = V_1$

Since $V_1 = V_o(t)$

$\Rightarrow V_i(t) = V_o(t)$

$\therefore A_v = 1$

$\therefore$ we see we get an output V same as input voltage. $\therefore$ we can use this in a circuit as

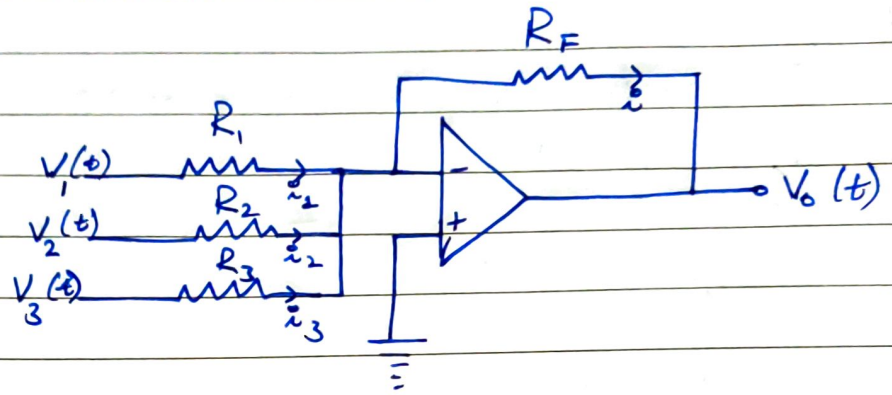


$\therefore$ we have removed the error in input using a voltage buffer as input provider.

PTO

→ WEIGHTED SUM →

- Say, how do we get a $V_o(t)$ of form $V_o(t) = 3V_1 + 4V_2 + 5V_3$
- Consider



We consider ideal OP-AMP

$\therefore\ i = i_1 + i_2 + i_3$ & $V_o(t) = -iR_F$

$\Rightarrow V_o(t) = -(i_1 + i_2 + i_3)R_F$

$\Rightarrow V_o(t) = -\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)R_F$

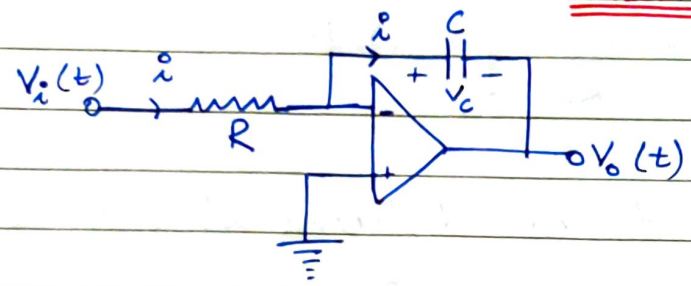
Now if $R_1 = \frac{1}{3}R_F$; $R_2 = \frac{1}{4}R_F$ & $R_3 = \frac{1}{5}R_F$

$\Rightarrow V_o(t) = -(3V_1 + 4V_2 + 5V_3)$

imp

Q→ Find $V_o(t)$ in given circuit

MILLER INTEGRATOR



Ans:

$$i = \frac{V_i(t)}{R}$$

$$V_c(t) = \frac{1}{C}\int_{-\infty}^{t} i\,dt$$

(We take limit from $-\infty$ since no initial $t=0$ condition is given ∴ we assume $V_c(-\infty)=0$)

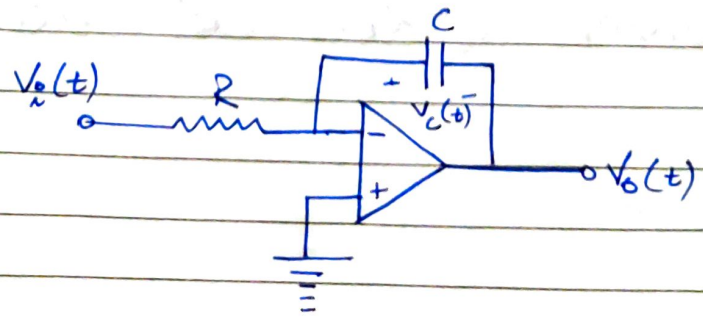
$$V_c(t) = \frac{1}{RC}\int_{-\infty}^{t} V_i(t)\,dt$$

Also

$$V_o(t) = -V_c(t)$$

$$\therefore \quad \boxed{V_o(t) = -\frac{1}{CR}\int_{-\infty}^{t} V_i(t)\,dt}$$

→ MORE INFO ON MILLER INTEGRATOR



- we write the output voltage equation

$$V_o(t) = \frac{-1}{RC} \int_{-\infty}^{t} V_1(t)\,dt$$

We can put conditions at $t=0$ and write

$$V_o(t) = -V_c - \frac{1}{RC} \int_{0}^{t} V_i(t)\,dt$$

If $V_c = 0$

$$V_o(t) = -\frac{1}{RC} \int_{0}^{t} V_i(t)\,dt$$

$$\Rightarrow V_o(t) = -\frac{1}{RC} Vt$$

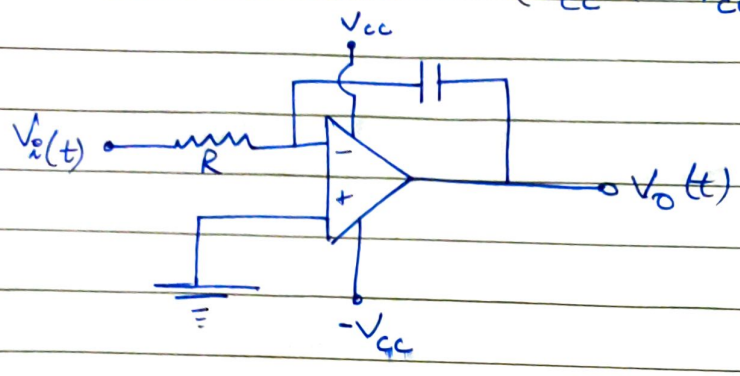
- Now say we have a DC input in that case, the capacitor is blocked and we can write

$$V_o = A_d (V_2 - V_1)$$

According to this eqn, V_o must be very large however we see practically that there is a maximum value ~~where~~ above which V_o does not rise.

PTO

- To understand this, remember that OP-AMP had 5 terminals (V_{cc} & $-V_{cc}$ were also there)

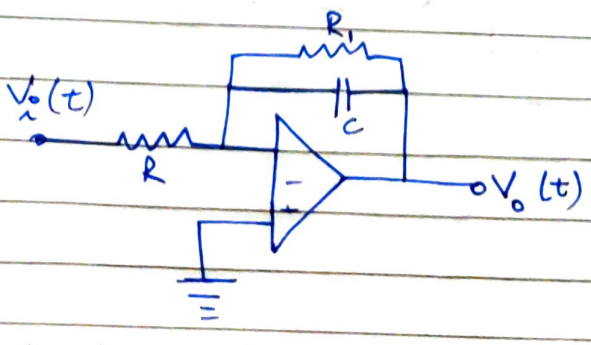


- It is a property of OP-AMP that potential at any node can only be in the range $[-V_{cc}, V_{cc}]$ (This is because if seen from V_{cc} & $-V_{cc}$ terminals we will see some resistance in OP-AMP)

- ∴ We will observe that voltage saturates at $+V_{cc}$ or $-V_{cc}$ as maximum and minimum.

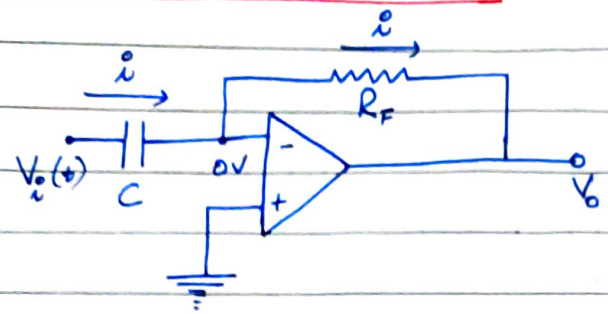
- We can use these maximum or minimum values to form logic circuits.

- To allow the passage of DC current, we can add a resistor in // to capacitor



AC input will also divide accordingly in the circuit.

→ DIFFERENTIATOR AMPLIFIER →



$$i = C\frac{dV_i(t)}{dt}$$

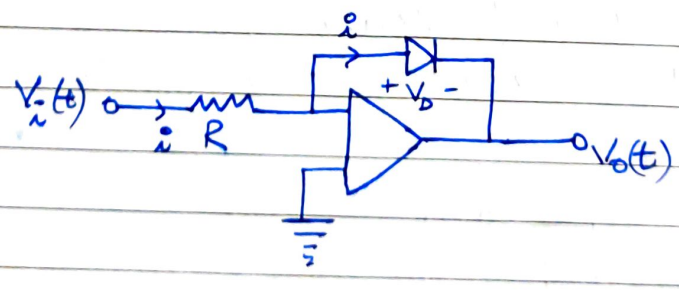
$$V_o = -iR_F$$

$$= -RC\frac{dV_i(t)}{dt}$$

$$\Rightarrow \boxed{V_o(t) = -RC\frac{dV_i(t)}{dt}}$$

- We must try to avoid the use of differentiation circuit and must use integrator circuit. This is because the circuit may catch some undesired signal of undesirable frequency, due to which the gain may suddenly increase. As a result, the circuit becom unstable.

→ LOG AMPLIFIER

- 

$$i = \frac{V_i(t)}{R}$$

We know

$$I_D = I_s \exp\left(\frac{V_D}{\eta V_T}\right)$$

$$\Rightarrow \frac{V_i(t)}{R} = I_s \exp\left(\frac{V_D}{\eta V_T}\right)$$

$$\Rightarrow \ln\left(\frac{V_i(t)}{R I_s}\right) = \frac{V_D}{\eta V_T}$$

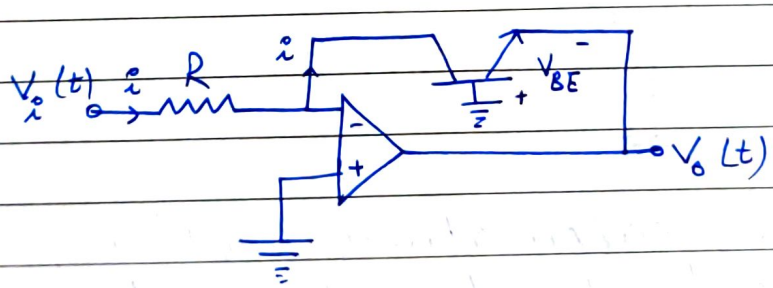
$$\Rightarrow V_D = \eta V_T \ln\left(\frac{V_i(t)}{R I_s}\right)$$

now

$$V_o = -V_D$$

$$\Rightarrow \boxed{V_o(t) = -\eta V_T \ln\left(\frac{V_i(t)}{R I_s}\right)}$$

- Instead of a diode, we can also use a BJT as



$$i = \frac{V_i(t)}{R}$$

whatever i is set up, it acts as collector current.

We know,

$$I_C = I_S \exp\left(\frac{V_{BE}}{\eta V_T}\right)$$

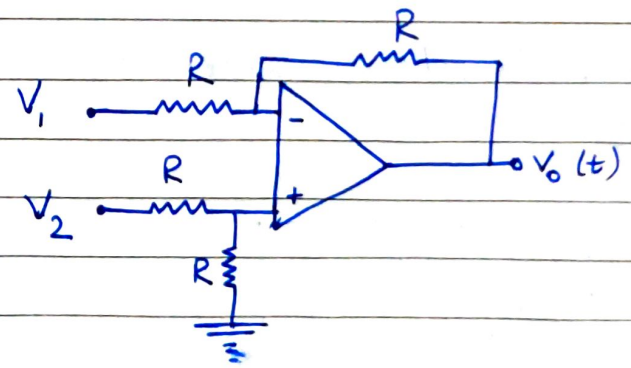
$$\therefore \frac{V_i(t)}{R} = I_S \exp\left(\frac{V_{BE}}{\eta V_T}\right)$$

$$\Rightarrow V_{BE} = \eta V_T \ln\left(\frac{V_i(t)}{R I_S}\right)$$

Now, we can see
$V_{BE} = -V_o$

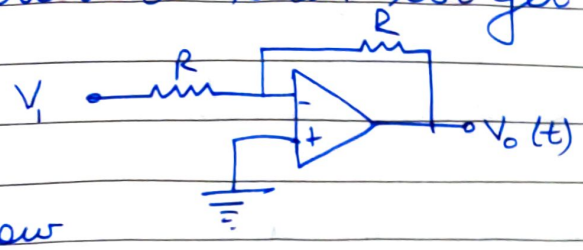
$$\Rightarrow \boxed{V_o(t) = -\eta V_T \ln\left(\frac{V_i(t)}{R I_S}\right)}$$

→ DIFFERENCE AMPLIFIER →



To make calculations for this, we use superposition ~~principle~~ principle on V_1 and V_2. First we ground V_2 and then find $V_o(t)$ & then do the same for V_1

V_2 grounded then we get



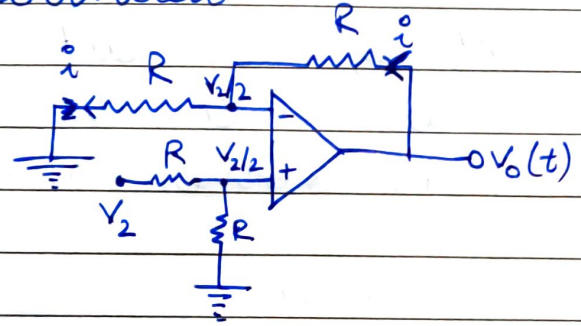
we know

This is inverting amplifier, ∴

$$V_o(t) = -\frac{R_F}{R_1} \times V_i(t)$$

$$\Rightarrow \boxed{V_o(t) = -V_1}$$

now V_1 grounded



$$i = \frac{V_2}{2R}$$

$$\therefore V_o(t) = \frac{V_2}{2R} \times R + \frac{V_2}{2R} \times R = V_2$$

$$\therefore \boxed{V_o(t) = V_2}$$

now applying superposition,

$$\boxed{V_o(t) = V_2 - V_1}$$

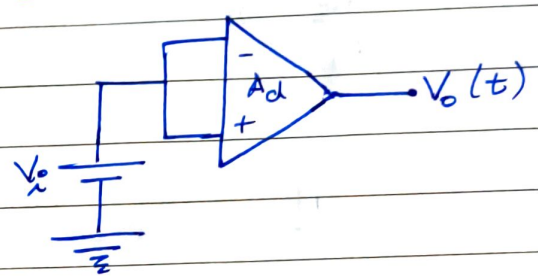
∴ we have a difference amplifier.

→ COMMON MODE REJECTION RATIO (CMRR) →

- Ideally, we can write

$$V_o = (V_2 - V_1) A_d$$

Hence, if we consider the circuit,



we expect $V_o = 0$. But in practical practice, we observe $V_o(t) \neq 0$. It always has some value.

- ∴ to express this non ideality, we write

$$\boxed{V_o = A_d (V_2 - V_1) + A_c \left(\frac{V_1 + V_2}{2}\right)}$$

$V_{id} = V_2 - V_1$

$V_{cm} = \frac{V_1 + V_2}{2}$

$$\Rightarrow \boxed{V_o = A_{ad} V_{id} + A_{cm} V_{cm}}$$

where A_c is called common mode gain also written as A_{cm}

- A_c is basically a measure of non-ideal of our OP-AMP and is fixed for a given OP-AMP

- We define CMRR as

$$\boxed{CMRR = 20 \log\left(\frac{A_d}{A_c}\right)}$$

The units for this CMRR is deciBel (dB) and this definition is most commonly used.

- We can also define CMRR in absolute terms

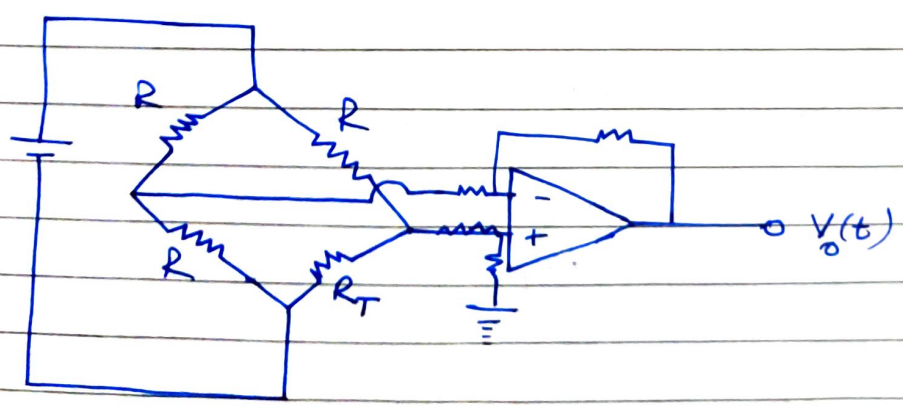
$$\boxed{CMRR = \frac{A_d}{A_c}}$$

- In ideal case, CMRR $= \infty$

- For OP-AMP IC741, CMRR = 70dB (approx.)

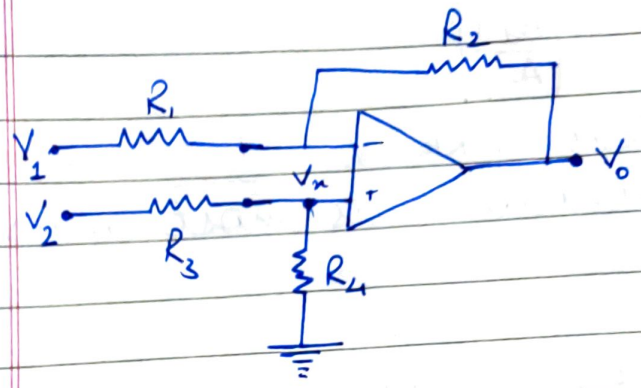
NOTE: APPLICATION OF DIFFERENCE AMPLIFIER

Consider circuit



R_T is variable with temp. ∴ the $V_o(t)$ obtained (ie difference in voltage) can be used to measure temperature.

→ MORE INSIGHT INTO DIFFERENCE AMPLIFIER →

- 

- **Calculating A_d**

We can write

$$V_o = V_x\left(1+\frac{R_2}{R_1}\right) - \frac{R_2}{R_1}V_1$$

$$V_x = \frac{V_2 R_4}{R_3+R_4}$$

Calculating V_{od}

$$V_o = \frac{R_4}{R_4+R_3}\left[1+\frac{R_2}{R_1}\right]V_2 - \frac{R_2}{R_1}V_1$$

Now if we <u>assume</u>

$$\frac{R_1}{R_2} = \frac{R_3}{R_4}$$

$$\therefore\ V_o = \frac{R_2}{R_1}(V_2 - V_1)$$

$$\therefore\ \boxed{A_d = \frac{R_2}{R_1}}$$

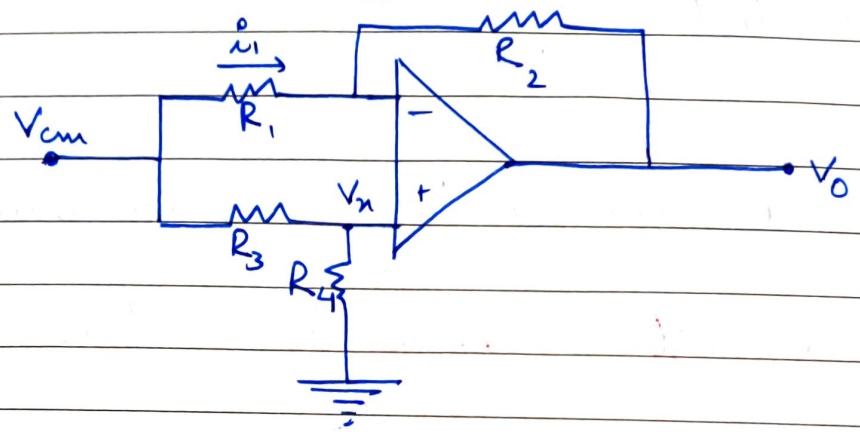
Calculating A_{cm}

we know

$$V_o = A_d (V_2 - V_1) + A_{cm}\left(\frac{V_2 + V_1}{2}\right)$$

$\therefore$ If $V_2 = V_1$ we can find A_{cm}

$\therefore$



Now $V_x = V_{cm} \times \frac{R_4}{R_4 + R_3}$

$$i_1 = \frac{V_{cm} - V_x}{R_1} = \frac{1}{R_1}\left[V_{cm} - \frac{R_4}{R_4 + R_3} V_{cm}\right]$$

$$= \frac{V_{cm}}{R_1}\left[\frac{R_3}{R_3 + R_4}\right]$$

Also now

$$V_o = V_x - i_1 R_2$$

$$= \frac{V_{cm} R_4}{R_4 + R_3} - \frac{1}{R_1}\left[\frac{R_3}{R_3 + R_4}\right] R_2 V_{cm}$$

$$A_{cm} = \frac{V_o}{V_{cm}} = \left[\frac{R_4}{R_4 + R_3} - \frac{R_2}{R_1} \times \frac{R_3}{R_3 + R_4}\right]$$

$$\Rightarrow \boxed{A_{cm} = \frac{R_4}{R_4+R_3}\left[1-\frac{R_2}{R_1}\frac{R_3}{R_4}\right]}$$

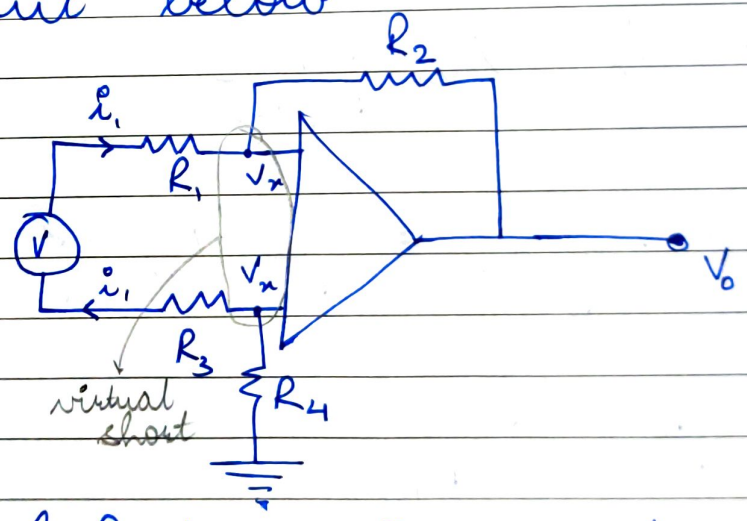
Considering $\frac{R_1}{R_2} = \frac{R_3}{R_4}$ like initially we did.

$$A_{cm} = 0$$

$\therefore$ theoretically A_{cm} can be made zero.

- Improving difference amplifier

In circuit below



If branch R_1 draws i_1 current, obviously i_1 will return from R_3.

$\therefore$ If we try & see input resistance due to virtual short & same curre we will kind of observe R_1 & R_3 in series.

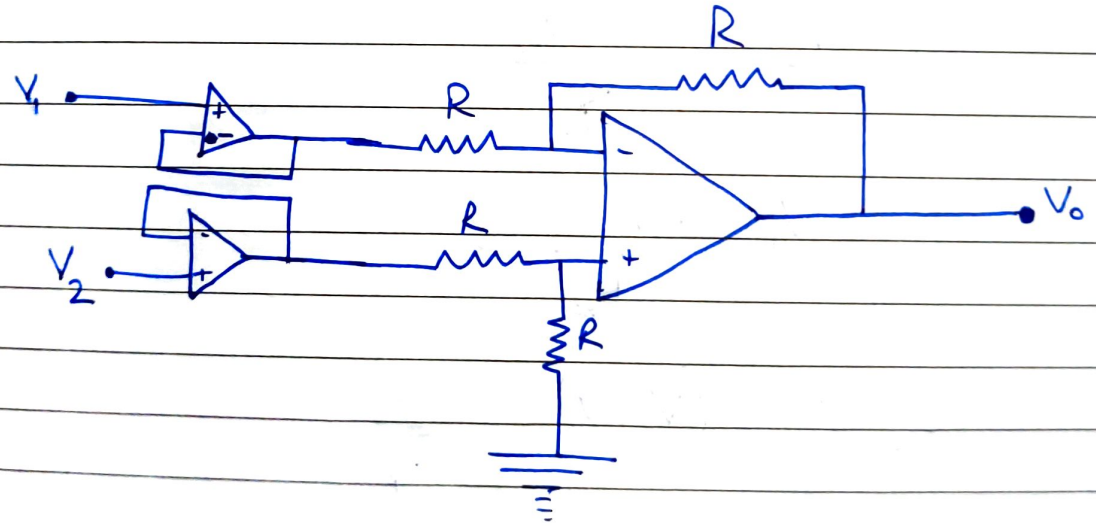
$\therefore$ Input resistance $= R_1 + R_3$

∴ to increase input impedance, we will form a new sort of amplifier called instrumentation amplifier.

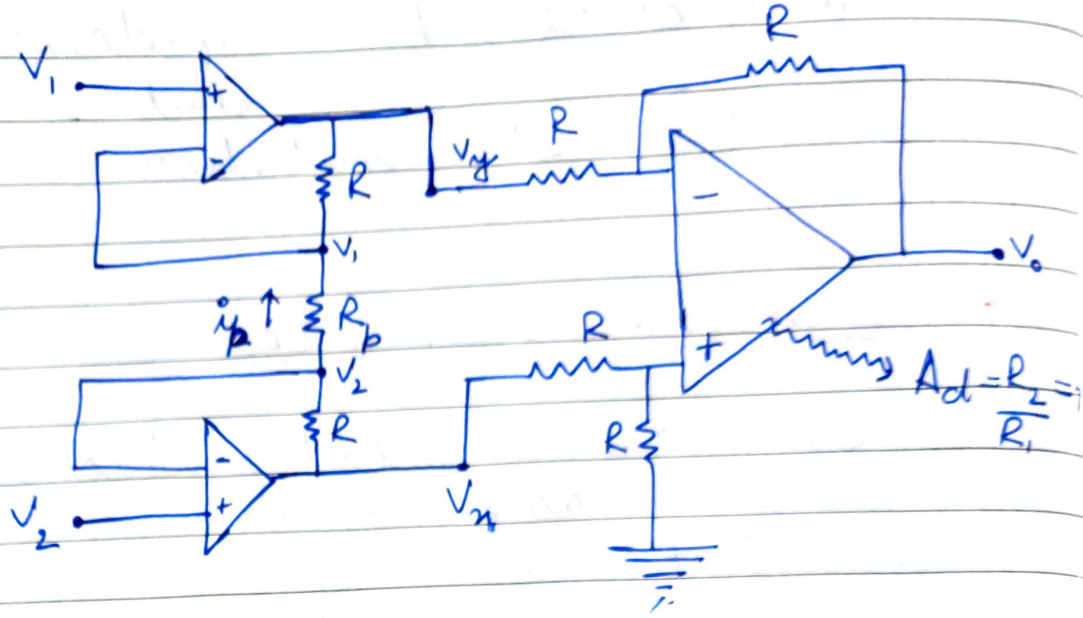
→ INSTRUMENTATION AMPLIFIER →

- To increase input impedance, we add voltage buffers to each ~~to~~ of 2 input branches, since input impedance for voltage buffers is ∞ & output is same as input.

∴ we get a circuit like



- ∴ we have increased input impedance now we will try to increase voltage gain in above circuit. To do this we use following circuit.



we can write

$$V_x = V_2 + R\frac{(V_2 - V_1)}{R_p}$$

$$V_y = V_1 - R\frac{(V_2 - V_1)}{R_p}$$

$$\therefore V_x - V_y = (V_2 - V_1)\left(1 + \frac{2R}{R_p}\right)$$

$$\frac{V_o}{V_2 - V_1} = A_d$$

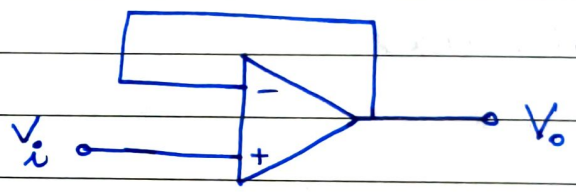
$$\therefore \Rightarrow \boxed{A_d = 1 + \frac{2R}{R_p}}$$

NOTE: Difference amplifier (instrumentation version) is very widely used because we can bring A_{cm} to zero nearly, thus removing non-ideality. Also we can increase voltage gain & increase input resistance to ∞ using instrumentation version.

* → NON-IDEALITY IN OPERATIONAL AMPLIFIERS →

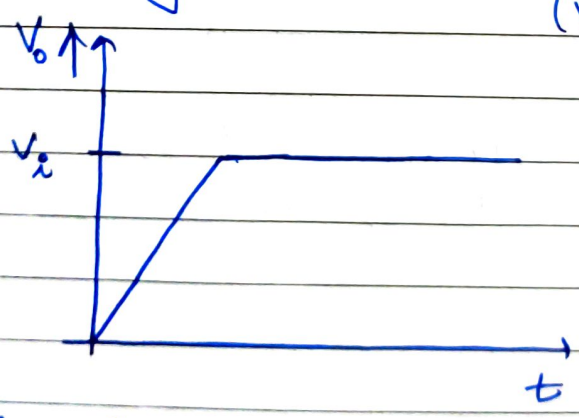
1. SLEW RATE →

- Consider



Here $V_o = V_i$ ideally at all times, but we get a graph like

(V_i is DC constant signal)



∴ V_o slowly increases to reach the saturation value

imp

And the maximum rate of increase in V_o w.r.t time is called slew rate

ie $\boxed{\text{Slew Rate} = \left.\frac{dV_o}{dt}\right|_{max}}$

- eg- Consider $V_i = V\sin\omega t$

$\therefore V_o = V\sin\omega t$

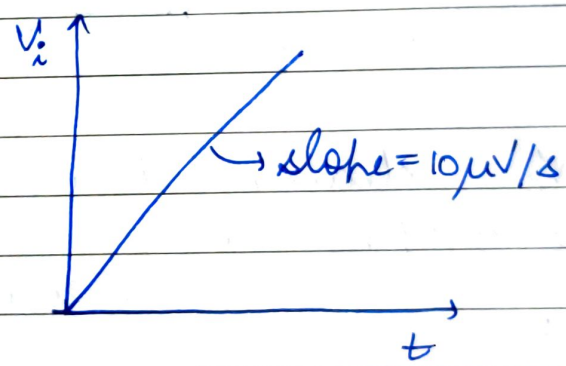
$\therefore \frac{dV_o}{dt} = V\omega\cos\omega t$

$\left.\frac{dV_o}{dt}\right|_{max} = V\omega$

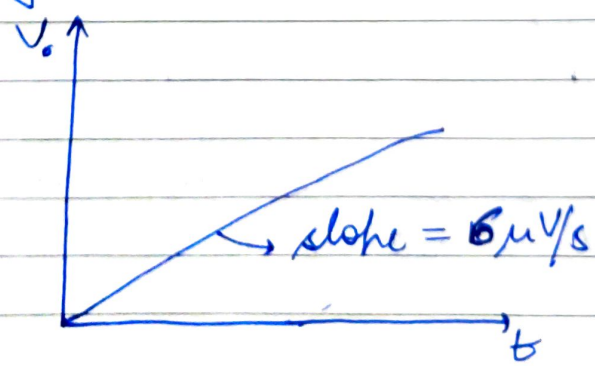
$\therefore$ Slew Rate $= V\omega$ in this case

- Consider in above circuit we have

V_i graph like



but if SR = 6μV/s then we will get a graph of V_o like



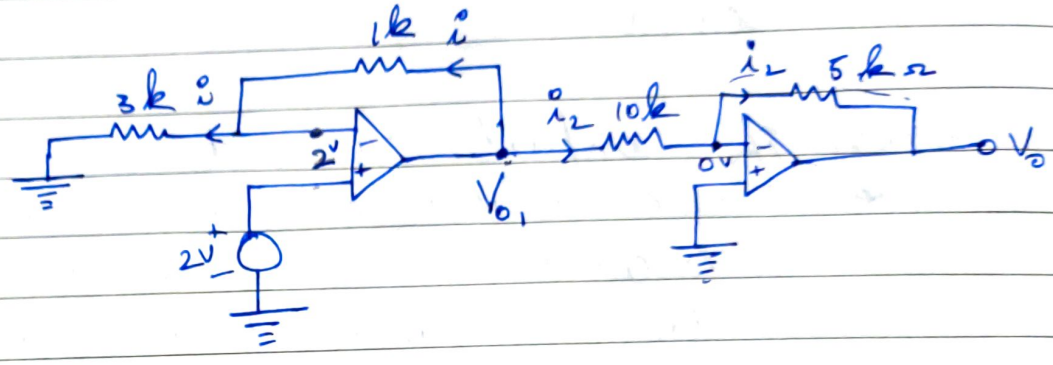
$\therefore \frac{dV_o}{dt}$ can never be greater than SR

2. We assume that current in input branches is zero. But ideally the current is not zero. There remains low levels of current in the branches.

3. Even if input is not given, there we observe some output on V_o branch. Due to this, we need to remove this error in OP-AMP. For this we use terminal 1 and 5 of OP AMP (ie offset null terminals). We connect a voltage b/w them and this removes the error in V_o. Thus error removal is possible.

TUTORIAL

1. Find V_o if OP-AMP is considered ideal



Ans

$$\frac{2}{3k} = I$$

$$i = \frac{2}{3} mA$$

$$\cancel{V_{o_1} = \left[1 + \frac{R_2}{R_1}\right] V_{in}}$$

$$\cancel{= \left[1 + \frac{1}{3}\right] \times 2}$$

$$\cancel{\frac{2}{3} mA \times 8k\Omega}$$

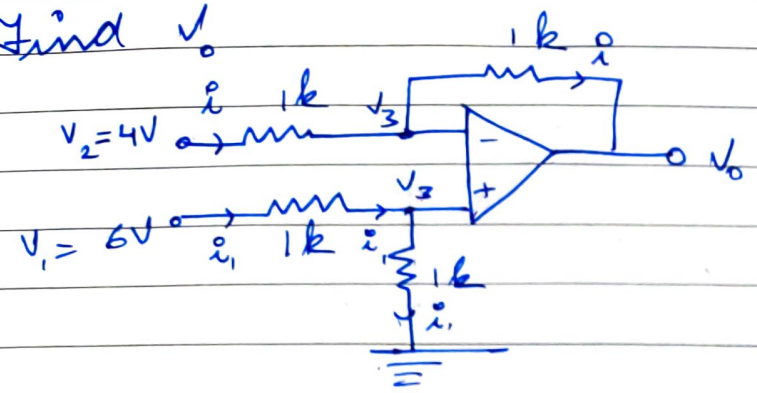
$$2 + \frac{2}{3} mA \times 1 = V_{o_1}$$

$$\Rightarrow 2 + \frac{2}{3} V = V_{o_1} \quad \Rightarrow \frac{8}{3} = V_{o_1}$$

$$i_2 = \frac{8}{30} mA$$

$$V_o = -\frac{8}{\cancel{30}\,6} \times \cancel{5} = \frac{-4}{3} V$$

2. Find V_o



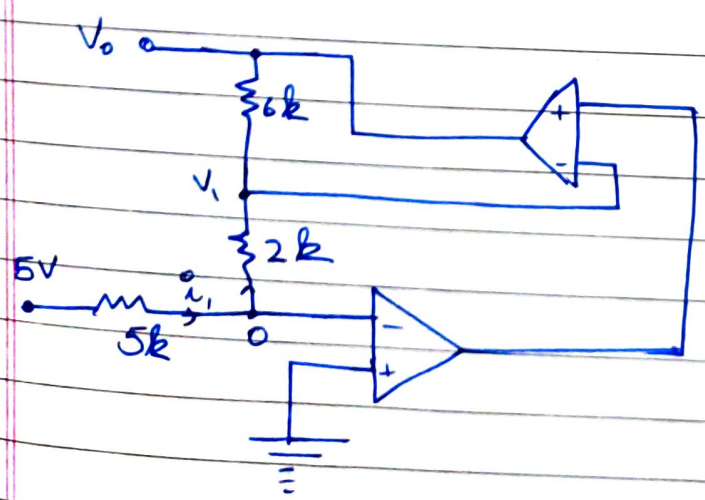
Ans: $i_1 = \frac{6}{2}$ mA

$\Rightarrow V_3 = 1 \times \frac{6}{2} V = 3V$

$\therefore i = \frac{4-3}{1}$ mA $= 1$ mA

$\therefore V_o = 3V - (1 \times 1)V = 2V$

3. Find V_o

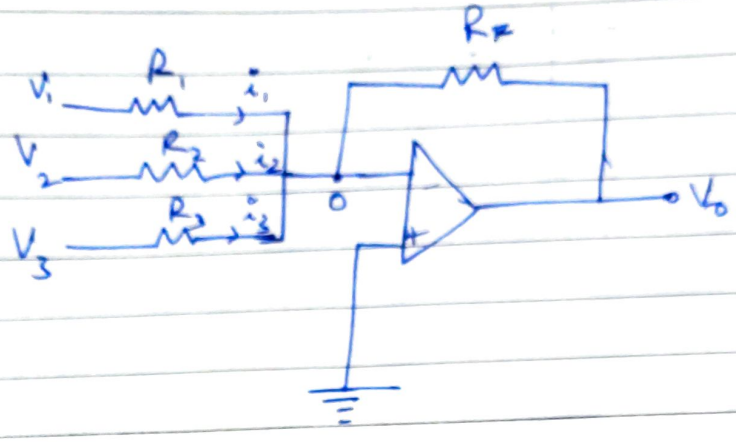


Ans.

$i_1 = 1$ mA $\quad \therefore V_1 = (0 - 2)V$

$\therefore V_o = (-2 - 6)V = -8V$

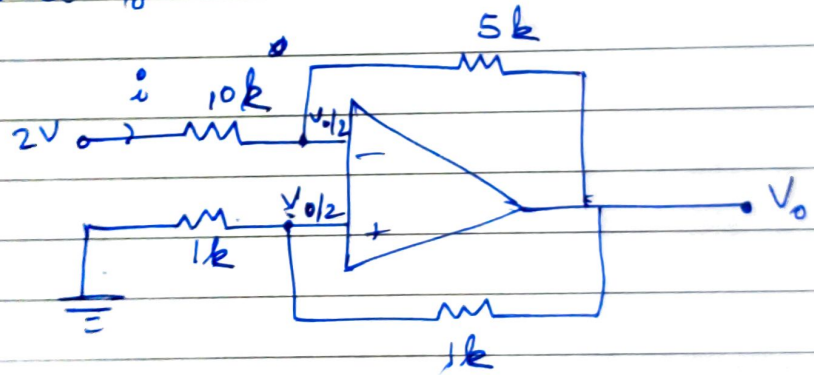
4Q → Find V_o



Ans:

$$-\left(\frac{V_1}{R_1}+\frac{V_2}{R_2}+\frac{V_3}{R_3}\right)R_F = V_o$$

5Q → Find V_o



$$V_1 = \frac{V_o}{2k} \times 1k = \frac{V_o}{2}$$

$$2 - \left(\frac{2-V_o}{\cancel{10}\,3}\right)\cancel{10}^{2} = \frac{V_o}{2} \Rightarrow 4 - \left(\frac{8-4V_o}{3}\right) = V_o$$

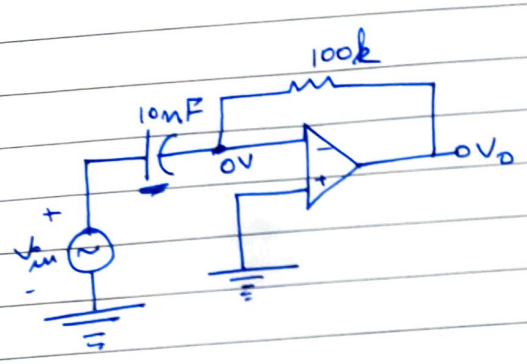
$$\Rightarrow 12 - 8 + 4V_o = 3V_o$$

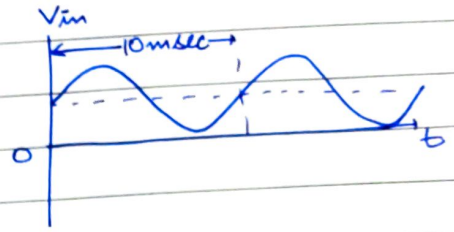
$$\cancel{\Rightarrow 4-(8-4V_o) = 3V_o} \quad \cancel{\Rightarrow 4-8+4V_o = 3V_o}$$

$$\cancel{\Rightarrow V_o = 8V} \quad \cancel{\Rightarrow V_o = 4V}$$

$\Rightarrow V_o = -4V$

6 Que:





$\cancel{V_{in} = 1 + \sin(200\pi t)}$

Ans:

$I = \dfrac{V_{in}\,\omega C}{}$

$\cancel{i = C\dfrac{dv}{dt}}$

$\cancel{\dfrac{2\pi f}{10}}$

$\cancel{\dfrac{2\pi}{10}}$

$0 - V_{in}\,\omega C\,100 = V_o$

$\cancel{j\omega C}$

$\Rightarrow V_o = -V_{in}\,\omega C\,100$

$\Rightarrow V_o = -V_{in}\,\dfrac{2\pi}{10} \times 10^3 \times 10 \times 10^{-9} \times 100 \times 10^3$

$\Rightarrow V_o = -\dfrac{V_{in}\,2\pi}{10}$

$\Rightarrow V_o = \dfrac{-\pi V_{in}}{5}$

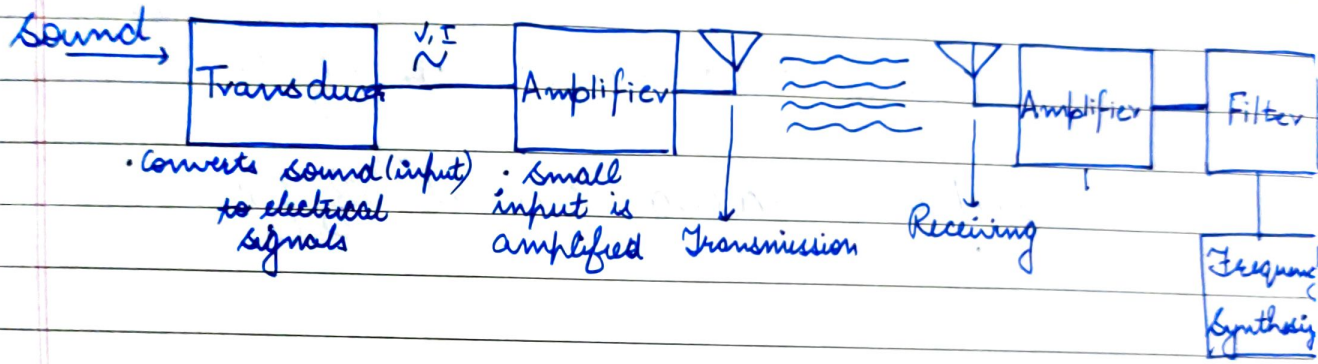
$\Rightarrow V_o = -\dfrac{\pi}{5} - \dfrac{\pi}{5}\sin(200\pi t)$

Chapter - 3
Digital Signals and Systems

- Signals are broadly divided into 2 categories

a) Analog
b) Digital

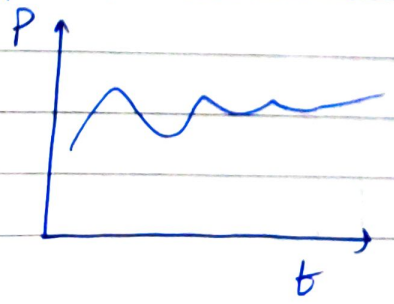
- Sound transmission (through mic system)



→ ANALOG SIGNAL AND DIGITAL SIGNAL

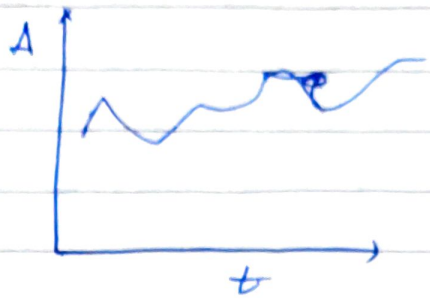
- ANALOG SIGNAL - It is a continuous signal and it is defined at every point of time.

eg- Consider we have pressure varying with time as . . .



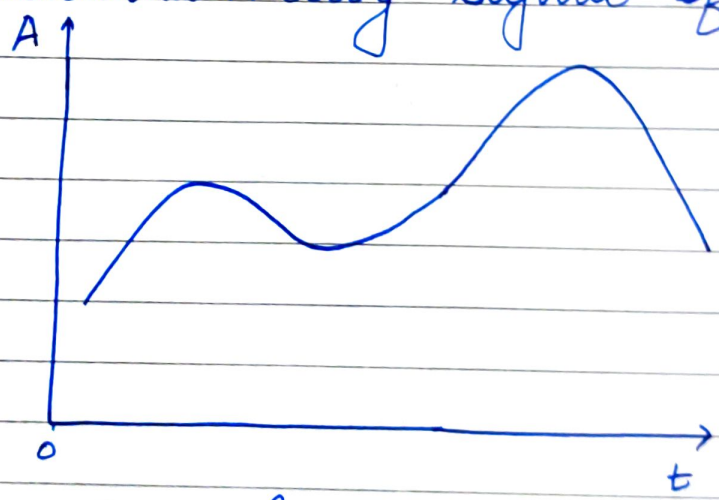
then, If we use an instrument to record it, then the transducer will convert it to signals analogously to give us

a continuous signal of form, say,

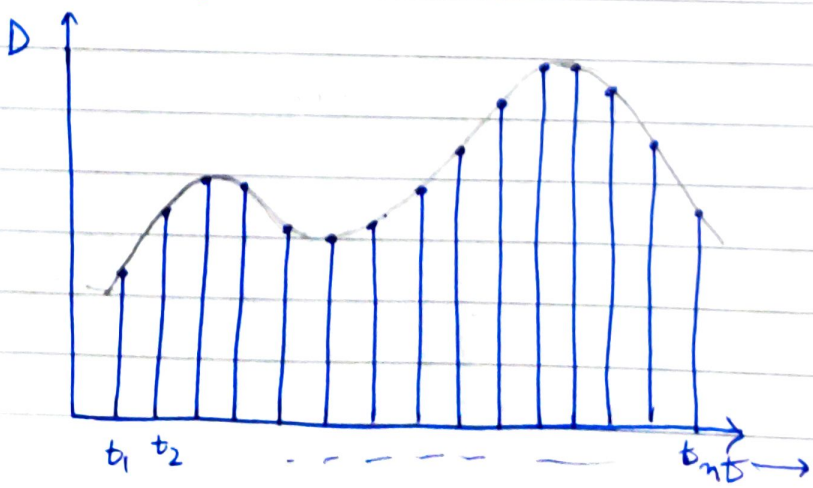


- Discrete Signal
- An analog signal can be converted to another form of signal called discrete signal by discretising the time ie ~~it~~ the signal is defined at only specific points ~~to~~ of time

Consider an Analog signal of form



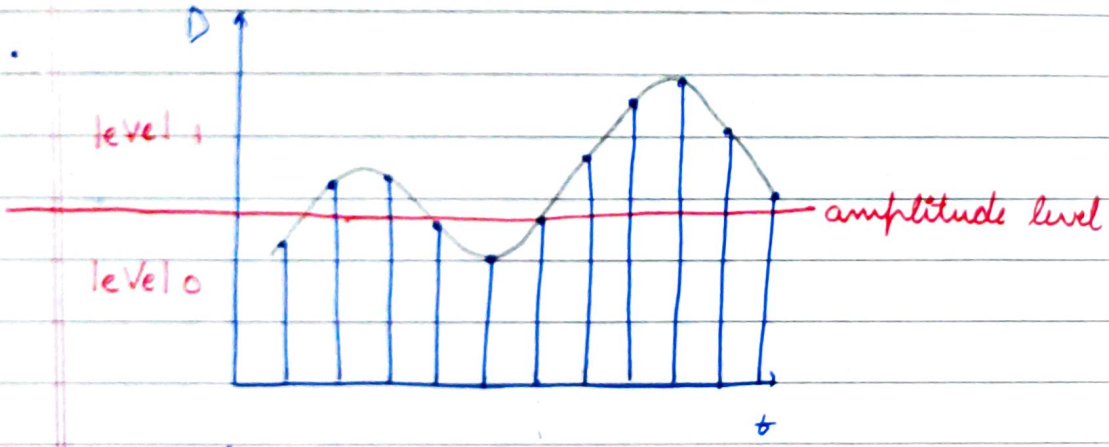
Converting this to discrete form will give us

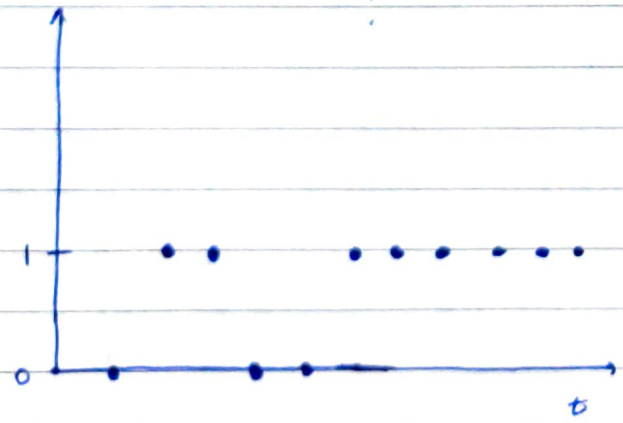


This process of conversion is called sampling & interval b/w 2 discrete levels times would be called sample length.

- DIGITAL SIGNAL

- Digital signal is further formed when we discretize the amplitude as well. This is done by first deciding a level of amplitude. The discrete levels above it are mapped to '1' and below it to zero.





ie we have a digital signal of form:

0 1 1 0 0 1 1 1 1 1 1

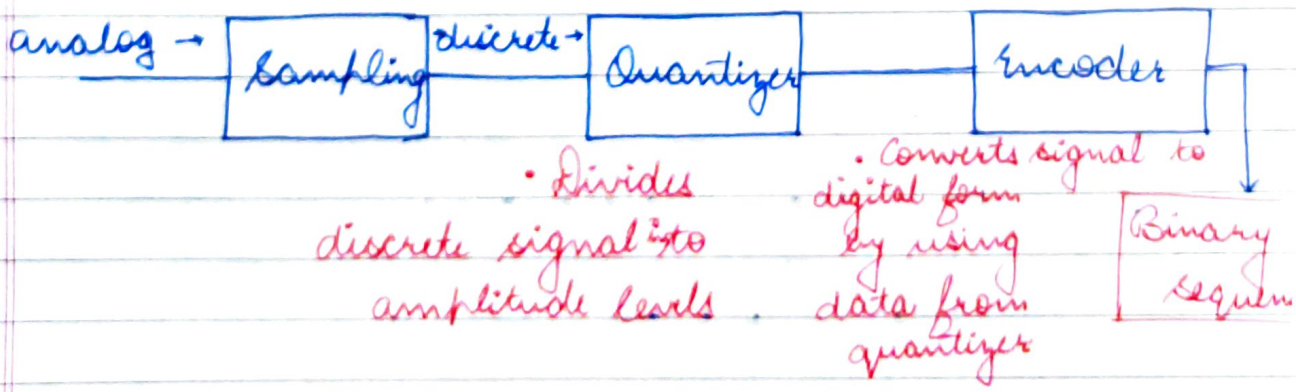
- We can even have more than 1 amplitude level divisions. But number of levels created can only be of form 2^n ie we can have no. of levels as: 2, 4, 8, 16 .....
This is because we have digital signal output in form 0 & 1 only and we can only use them to express levels.

For:

2 levels	4 levels	8 levels
level 0 → 0	level 0 → 00	level 0 → 000
1 → 1	1 → 01	1 → 001
	2 → 10	2 → 010
	3 → 11	3 → 011
		4 → 100
		5 → 101
		6 → 110
		7 → 111

∴ we can observe why we have 2^n form of levels
eg- if we need minimum 17 levels, we have to create 32 levels only.

- The conversion from analog to digital is done in following manner.



→ BINARY SYSTEM OF NUMBERS →

- In decimal system, we have radix = 10. This means digits range from 0 to 9

ie if radix ie $r = 10$ then digits range from 0 to $r-1$.

For a number

$$\begin{array}{cccccc} 10^3 & 10^2 & 10^1 & 10^0 & & 10^{-1} & 10^{-2} \\ 7 & 5 & 6 & 3 & . & 3 & 1 \end{array}$$

Its decimal conversion ie conversion to decimal system (Its already in decimal system but the following method is used for any system)

$$7 \times 10^3 + 5 \times 10^2 + 6 \times 10^1 + 3 \times 10^0 + 3 \times 10^{-1} + 1 \times 10^{-2}$$

- ∴ In binary system $r = 2$

∴ digits range from 0 to 1.

Consider number

$(1011.101)_2$ → (represents radix)

∴ decimal conversion $= 2^3 \times 1 + 2^2 \times 0 + 2^1 \times 1 + 2^0 \times 1 + 2^{-1} \times 1 + 2^{-2} \times 0 + 2^{-3} \times 1$

$= 8 + 0 + 2 + 1 + 0.5 + 0.125$

$= (11.625)_{10}$

- In binary system, the 2 digits 0 and 1 are called 'bits'.

Consider we write a number

MSB ← 1 0 0 1 → LEAST SIGNIFICANT BIT (LSB)

- Now say we have to write the values of digits from 0 to 9 in binary and consider we use 4 digits for this (you could take more), then we get:

0 - 0000
1 - 0001
2 - 0010
3 - 0011
4 - 0100
5 - 0101
6 - 0110
7 - 0111
8 - 1000
9 - 1001

imp

- In decimal system we had

kilo → 10^3, mega → 10^6, giga → 10^9

tera → 10^{12}

In binary, we have

kilo $\rightarrow 2^{10}$
mega $\rightarrow 2^{20}$
giga $\rightarrow 2^{30}$
tera $\rightarrow 2^{40}$

NOTE: A byte = 8 bits
ie eg- 10011001 this piece of data is called 1 byte.

$\therefore$ 1 kilobyte = 8×2^{10} bits

1 megabyte = 8×2^{20} bits.

→ OTHER SYSTEMS →

- OCTAL SYSTEM

In this system $r = 8$. $\therefore$ digits range from 0 to 7

eg- $(123)_8 = 1 \times 8^2 + 2 \times 8^1 + 3 \times 8^0$

PTO

- ## HEXADECIMAL SYSTEM

- Here $r = 16$ & digits are

  0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F

* → BINARY OPERATIONS

→ ADDITION AND SUBTRACTION

- Performed like simple addition and subtraction. However all numbers must be represented and perceived in binary method.

- eg-

a)

```
  1 1 1 1 1
  1 0 1 1 0 1
+ 1 1 0 0 1 1
1 1 0 0 0 0 0   Ans:
```

(Since $1+1 = 10$ → 2
and $1+1+1 = 10+1 = 11$ → 3)

b)

```
  1 0 0 0 1
+ 1 1 0 0 1
1 0 1 0 1 0   Ans
```

NOTE: These methods of operations that we use are based on decimal system. However, the computer does not use these methods to process them.

- **Subtraction →**

```
  1 1 0 0 1 0 1
- 1 0 1 0 1 1 0
-------------
  0 0 0 1 1 1 1
```

Ans:

NOTE: If confused, try and remember what method of borrowing we used in normal subtraction. Apply that analogy carefully.

→ **MULTIPLICATION**

eg-

```
        1 0 1 1
      × 1 1 1 0
      ---------
        0 0 0 0
      1 0 1 1 ×
    1 0 1 1 × ×
  1 0 1 1 × × ×
  -------------
  1 0 0 1 1 0 1 0
```

PTO

→ CONVERSION FROM ONE SYSTEM TO ANOTHER

- Conversion from decimal system
- Consider a number

$$(41)_{10}$$

To convert it to binary (ie $r=2$), divide it continuously with r until quotient is less than radix. (write remainders on the side)

2	41	1
2	20	0
2	10	0
2	5	1
2	2	0
	1	1

NUMBER

$\therefore$ binary number $= 101001$

NOTE: you can think about its reason from the statement

$$(41)_{10} = 2\times10^5 + 0\times10^4 + 1\times10^3 + 0\times10^2 + 0\times10^1 + 1\times10^0$$

$$= 32 + 8 + 1$$

NOTE: we can apply this method to convert into any system.

- Consider we have a decimal point number

0.6875

To convert this to binary, multiply by radix

Collect the integer

$0.6175 \times 2 = 1.3750$ 1

Take decimal part

$0.3750 \times 2 = 0.7500$	0		Decimal form in binary
$0.75 \times 2 = 1.500$	1		
$0.5 \times 2 = 1$	1		

$\therefore (0.6875)_{10} = (0.1011)_2$

- When the decimal never reaches zero after repeated steps, then after a certain number of steps, leave the calculation as is

eg- $(0.513)_{10} \longrightarrow (?)_8$

$0.513 \times 8 = 4.104$	4
$0.104 \times 8 = 0.832$	0
$0.832 \times 8 = 6.656$	6
$0.656 \times 8 = 5.248$	5
$0.248 \times 8 = 1.984$	1

Ans: $(0.40651\ldots)_8$

• BINARY TO OCTAL AND VICE VERSA

- Octal system has digits from 0 to 7 & to ~~to~~ represent it in binary, we need 3 binary digits.
  ∴ if we take group of 3 binary digits in a binary number, we get octal number

eg- $\underbrace{10}_{2}\ \underbrace{101}_{5}\ \underbrace{100}_{4}\ \underbrace{101}_{5} \cdot \underbrace{101}_{5}\ \underbrace{001}_{1}\ \underbrace{00}_{0}$

∴ Octal no. = 2545.510

- For conversion from octal to binary, represent each octal digit by 3 binary digits.

eg- $(75\ 321)_8$
$= (111\ 101\ 011\ 010\ 001)_2$

• BINARY TO HEXADECIMAL AND VICE-VERSA

- It is similar to binary to octal conversion & vice-versa, except here, we represent each hexadecimal digit by 4 ~~d~~ binary digits

eg- $(F12A)_{16}$
$= (1111\ 0001\ 0010\ 1010)_2$

→ COMPLEMENTS →

- Consider a number $= N$
  with radix $= r$
  and no of digits $= n$

- We define

$$\boxed{(r-1)\text{'s complement} = (r^n - 1) - N}$$

and

$$\boxed{r\text{'s complement} = r^n - N}$$

- eg Consider number $(2371)_{10}$
  It has 4 digits & $r = 10$

$$\therefore 9\text{'s complement} = (10^4 - 1) - 2371$$
$$= 9999 - 2371$$
$$= 7628$$

$$10\text{'s complement} = 9\text{'s complement} + 1$$
$$= 7629$$

- eg Consider you have to calculate 10's complement of a number ending with zeroes then write zeroes as it is, and next subtract first non-zero digit from 10 and rest from 9. You will get the same result as obtained from formula

$$(23710)_{10}$$

$$10^s \text{ complement} = 76290$$

NOTE: 10's complement & 9's complement are valid only for decimal system. Similarly 2's complement & 1's complement are valid for binary

- Finding 1's complement

$$1^s \text{ complement} = (2^n - 1) - N$$

all of this should be converted to binary first

eg- 10101

$$= (2^5 - 1) - 10101$$

$$= 011111 - 10101$$

$$= 01010$$

$\therefore$ 1's complement of 10101 $\longrightarrow$ 01010

- We can observe that we obtained the 1's complement by flipping the digits. $\therefore$ we can use this as a short cut

- 2's complement = 1's complement + 1

$\therefore$ 2's complement of 10101 = 01011

- For writing 2's complement in shortcut, from the end, keep the digits until first non-zero digit intact & flip the rest of the digits

eg- 100 0 11100

2's complement = 011100100

NOTE: complements are basically used when we need to subtract in computer systems since computers can't perform borrowing ~~opp~~ operations like us.

→ SUBTRACTION METHOD (COMPUTERS) →

- consider we have 2 numbers M and N and we need to calculate

$$M - N$$

- For operating this, follow these steps

i) First ensure ~~na~~ M and N have same no. of digits. If not, then add zeroes required before ~~tt~~ ~~on~~ the smaller number.

ii) compute r's complement of N

$$r^n - N$$

iii) Add M to ~~r~~ r's complement of N

$$r^n - N + M$$

iv) Case I : $M \geq N$

remove end carry

Case II : $M < N$

$$= r^n - (N - M)$$

$(N-M)$ → r's complement of $r^n - (N-M)$

put ve sign $-(N-M) = (M-N)$

eg- a) $M > N$

$M = (1110)_2$

$N = (1011)_2$

2's complement of N = 0101

$\therefore (2^n - N + M)$

$$\begin{array}{r} 0101 \\ 1110 \\ \hline 10011 \end{array}$$

remove end carry

$\therefore M - N = 0011$

b) $M < N$

$M = (1011)_2$ $N = (1110)_2$

2's comp = 0010

$$\begin{array}{r} 0010 \\ +1011 \\ \hline 1001 \end{array}$$

$\xrightarrow{\text{Taking its 2's complement}}$ 0001 $\xrightarrow{\text{putting -ve sign}}$ -0011

$\therefore M - N = -0011$

- you can also calculate it using $(r-1)$'s complement (by adding 1 when $M>N$ and then removing carry and following procedure similar to r's complement when $N>M$)

→ -ve number representation in Binary System

1. Signed magnitude representation

- The most significant bit determines the sign. 0 is +ve and 1 is -ve. note that an extra bit has to be added for this

- eg - To represent 7, we write 111 ie 3 digits are needed. We add another digit like

$+7 \longrightarrow 0111$

$-7 \longrightarrow 1111$

2. 1's complement representation

- The 1's complement representation is basically when we write 1's complem of signed mag. representation

$+7 \longrightarrow 1000$

3.- 2's complement representation.

- We write 2's comp. of signed mag. rep.

$$+7 \longrightarrow 1001$$

→ COMPLEMENTS FOR DECIMAL NOS: →

- Suppose we have to write 2's complement of :

$$1011001.001$$

- For 2's complement

$$= 2^{n} - N$$

number of integral digits

$$= 2^{7} - N$$

$$\begin{array}{r} 100000000.000 \\ -\ 1011001.001 \\ \hline 0100110.111 \end{array}$$

$\therefore$ 2's complement $= 100110.111$

NOTE: Keep last decimal intact and ~~remove the first~~ flip the rest of the digits to get 2's complement.

classmate

Date
Page

imp

For 1's complement

when we had integral number, we wrote

$$(r-1)\text{'s complement} = (r^n - 1 - N)$$

but in reality $(r-1)$'s complement is written as

$$\boxed{(r-1)\text{'s complement} = (r^n - r^{-m} - N)}$$

where m = no. of digits after decimal

∴ say we calculate 1's complement of 1011001.001, we will get it by flipping

ie 1's comp. = 0100110.110

∴ we need to simply flip. (we would not have had the correct ans if we used $r^n - 1 - N$)

PTO

ENCODING →

1. → BINARY CODED DECIMAL NUMBER →

- each decimal digit (ranging from 0 to 9) is represented by 4 binary digits.
  ∴ using this we can encode any decimal no. eg – 2 digit nos will have 8 binary digits.

0 →	0000	6 →	0110
1 →	0001	7 →	0111
2 →	0010	8 →	1000
3 →	0011	9 →	1001
4 →	0100		
5 →	0101		

eg – we write 10 as 00010000

Imp

NOTE: This is just a method of encoding. Binary representation of 10 and BCD of 10 will be different.

2. → GRAY CODE →

- In binary coded decimal system, say if we need to change a value from 7 to 8, we perform an operation like

0111 → 1000

we notice that all the bits cha here. Due to this, the computer tak

in large amounts of power and energy is wasted as 4 ON or OFF operations are performed.

- In gray coding, our motive is that only one bit must change when we shift from one digit to next one.

- consider digits from 0 to 3

0 → 00	gray encoding →	0 → 00	only one change per step
1 → 01		1 → 01	
2 → 10		2 → 11	
3 → 11		3 → 10	

we basically changed encoding order of 2 and 3

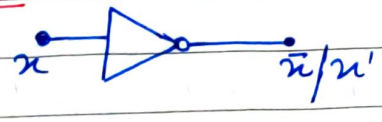
- To extend this further take the mirror image of codes

00	add 0 in front	000	→ 0
01		001	→ 1
11		011	→ 2
10		010	→ 3
10	image →	110	→ 4
11	add 1 in front	111	→ 5
01		101	→ 6
00		100	→ 7

- we can use the above algorithm to extend to any number of digits.

* → BASIC LOGIC GATE →

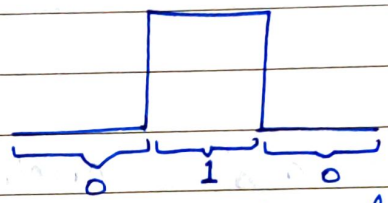
1. → NOT GATE :

- 

(also called inverter)

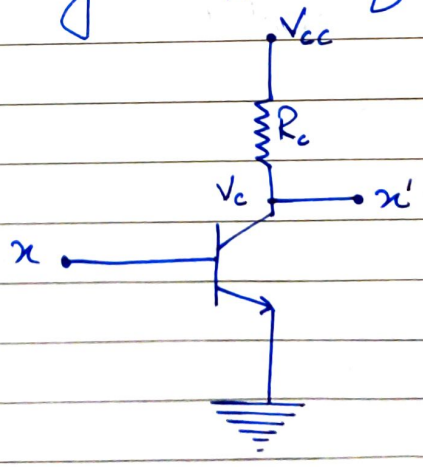
- We take input in logic gates as 0 and 1.

- 0 and 1 may represent different schemes. eg the most commonly used is a pulse



There are several other schemes as well

- NOT Logic gates is formed using BJT



- ∴ we can see that this circuit acts as a logic gate.
- An inverter is also called a ~~not~~ NOT gate.
- Truth Table for NOT gate

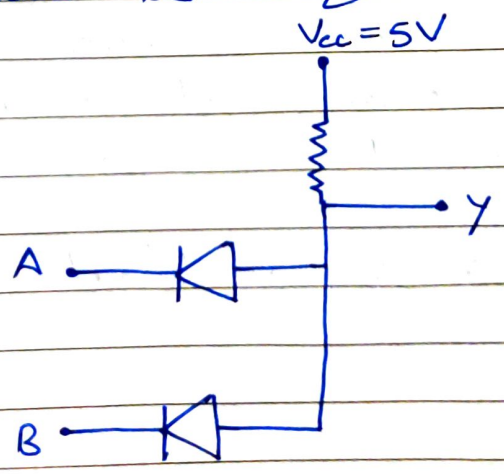
x	y
0	1
1	0

Its boolean expression is $Y = \bar{x}$

2 → **AND GATE:**

- An 'and' gate returns 1 if both inputs are 1 else zero
-

- Its circuit is as following



NOTE: We can have AND gate with as many input terminals.

- On low input in any of A or B (ie 0 as input), the diode is in forward bias. Since it is in forward bias, the potential drop across it is low. ∴ output is low.

- On high input at both, the diodes are in reverse bias and due to this p.d across diode is higher than in previous case. ∴ due to this output is high.

- We can also look at it as:

When A or B is low, we have forward bias. Then the current b/w V_{cc} and A or B will be of order mA (forward bias) and there will be a potential drop across R.

When A & B both are high, then we have current b/w V_{cc} & A and B in order μA (reverse bias). And there is again some potential drop across R. But this drop is lower than that in previous case.

∴ We get a higher output in second case.

- Truth table

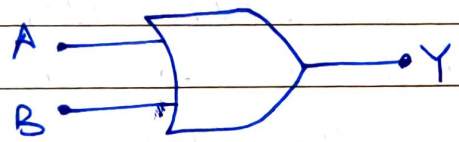
A	B	Y
1	1	1
1	0	0
0	1	0
0	0	0

Its boolean expression is

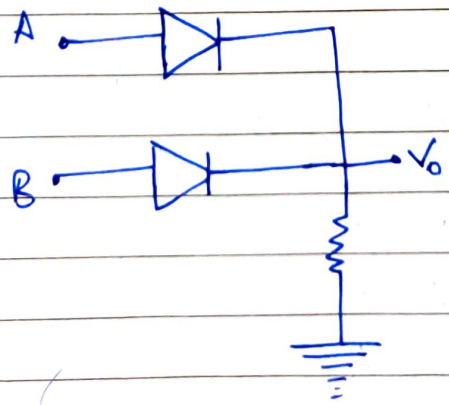
$Y = A.B$

3. → OR GATE

- OR gate returns 1 when either of ~~them~~ inputs is 1.

- 

- Its circuital form is



circuit analysis from explanation like that on previous page.

- ~~Clearly~~ We can observe that when A or B either of them are high, then we get higher V_o as compared to when A and B are zero.

- Truth Table

A	B	Y
0	1	1
0	0	0
1	0	1
1	1	1

Its boolean expression

$Y = A + B$

NOTE: We don't use these standard circuits actually for logic gates as they ~~ex~~ consume high power. We now use MOSFET circuits.

BOOLEAN ALGEBRA →

- THEOREMS / POSTULATES (where A, B and C may be 0 or 1)

Name	AND form	OR form
Identity	$1 \cdot A = A$	$0 + A = A$
Null	$0 \cdot A = 0$	$1 + A = 1$
Indempotent	$A \cdot A = A$	$A + A = A$
Inverse	$A \cdot \bar{A} = 0$	$A + \bar{A} = 1$
Commutative	$A \cdot B = B \cdot A$	$A + B = B + A$
Associative	$(A \cdot B) \cdot C = A \cdot (B \cdot C)$	$(A + B) + C = A + (B + C)$
Distributive	$A + B \cdot C = (A + B)(A + C)$	$A \cdot (B + C) = AB + AC$

name	AND form	OR form
Absorption	$A \cdot (A+B) = A$	$A + AB = A$
De morgan's Law	$\overline{A \cdot B} = \bar{A} + \bar{B}$	$\overline{A+B} = \bar{A} \cdot \bar{B}$

Q.i) $x(x'+y)$

$= xx' + x.y$

$= x.y$

ii) $x + x'y$

$= x + y$

iii) $(x+y)(x+y')$

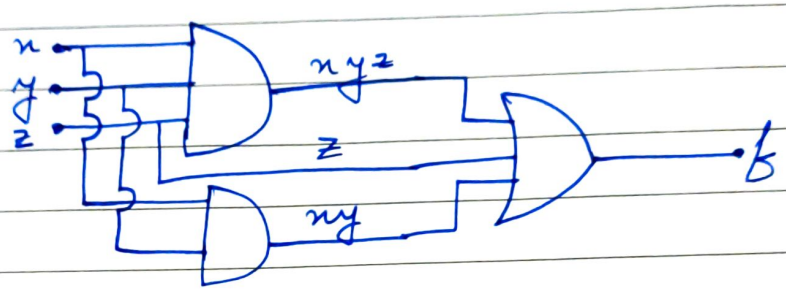
iv) $xy + x'z + yz$

v) $(x+y)(x'+z)(y+z)$

Designing hardware from boolean f^n

- consider $f = xyz + xy + z$

  $\therefore$ we need a circuit like



Minterms and Maxterms

- consider we have 2 variables

  x and y.

- Its minterms are defined like

$x'y'$	m_0
$x'y$	m_1
xy'	m_2
xy	m_3

For minterms, we take $x=1$ and $x'=0$ & $y=1$ and $y'=0$

- Minterms for 3 variables would be

  variables x, y, z

$x'y'z'$	m_0
$x'y'z$	m_1
$\vdots$	$\vdots$
xyz	m_7

- maxterms are complements of minterms
  - maxterms for x, y, z

$$\overline{x'y'z'} = x+y+z \qquad M_0$$
$$\overline{x'y'z} = x+y+z' \qquad M_1$$
$$\vdots$$
$$\overline{xyz} = x'+y'+z' \qquad M_7$$

- minterms and maxterms prove very useful in digital electronics.

Consider $Y = A+BC$

To write this using minterms

A	B	C	Y	
0	0	0	0	m_0
0	0	1	0	m_1
0	1	0	0	m_2
0	1	1	1	m_3
1	0	0	1	m_4
1	0	1	1	m_5
1	1	0	1	m_6
1	1	1	1	m_7

To write Y in terms of minterms, we take minterms with truth value and add them.

$\therefore Y = m_3 + m_4 + m_5 + m_6 + m_7$

$\Rightarrow \boxed{Y = A'BC + AB'C' + \ldots\ldots + ABC}$

imp SOP (Sum of product)

$\Rightarrow Y = \sum(3,4,5,6,7)$

now to write this in form of manterms,

$Y' = m_0 + m_1 + m_2$

$= A'B'C' + A'B'C + A'BC'$

Taking complement

$\therefore Y = (Y')' = \overline{A'B'C'} \cdot \overline{A'B'C} \cdot \overline{A'BC'}$

$\Rightarrow \boxed{Y = (A+B+C)(A+B+C')(A+B'+C)}$

imp POS (Product of sums)

$\Rightarrow Y = M_0 M_1 M_2$

$\Rightarrow Y = \Pi(0,1,2)$

imp

Q→ If we have n-variables, then how many functions can be formed out of it?

Ans: every f^n will be a summation of some minterms

we will have 2^n minterms and either the minterm will be included or it wont be included in function.

$\therefore$ total number of $f^n = 2^{2^n}$

• SOME MORE LOGIC GATES

a) NAND $\longrightarrow$ $Y = \overline{A \cdot B} = \bar{A} + \bar{B}$

b) NOR $\longrightarrow$ $Y = \overline{A+B} = \bar{A} \cdot \bar{B}$

c) EXOR $\longrightarrow$ $Y = AB' + A'B$

d) EXNOR $\longrightarrow$ $Y = AB + A'B'$

• Some examples to write functions in terms of minterms or maxterm.

• Consider AND gate

Truth Table

A	B	Y		
0	0	0	$A'B'$	$\rightarrow m_0$
0	1	0	$A'B$	$\rightarrow m_1$
1	0	0	AB'	$\rightarrow m_2$
1	1	1	AB	$\rightarrow m_3$

$\therefore Y = m_3$

$\Rightarrow \boxed{Y = AB}$

$Y' = m_0 + m_1 + m_2$

$\Rightarrow Y' = A'B' + A'B + AB'$

$\Rightarrow Y = \overline{A'B' + A'B + AB'}$

$\Rightarrow Y = (A+B)(A+B')(A'+B)$

$\Rightarrow \boxed{Y = M_0 M_1 M_2}$

- consider OR gate

Truth table

A	B		
0	0	0	$A'B'$
0	1	1	$A'B$
1	0	1	AB'
1	1	1	AB

$\therefore Y = m_1 + m_2 + m_3$

$\Rightarrow Y = A'B + AB' + AB$

& $Y' = A'B'$

$\Rightarrow Y = (A+B)$

$\therefore Y = M_0$

Q→ TT

x	y	z	$f_1(x,y,z)$	$f_2(x,y,z)$	
0	0	0	0	0	m_0
0	0	1	1	0	m_1
0	1	0	0	0	m_2
0	1	1	0	1	m_3
1	0	0	1	0	m_4
1	0	1	0	1	m_5
1	1	0	0	1	m_6
1	1	1	1	1	m_7

Ans: $f_1 = m_1 + m_4 + m_7$

$\Rightarrow f_1 = x'y'z' + xy'z' + xyz$

$f_1' = x'y'z' + x'yz' + x'yz + xy'z + xyz'$

$$f_1 = (x+y+z)(x+y'+z)(x+y'+z')(x'+y+z')(x'+y'+z)$$

$$= M_0 M_2 M_3 M_5 M_6$$

Now

$$f_2 = m_3 + m_5 + m_6 + m_7$$

$$= xy'z' + xy'z + xyz' + xyz$$

$$f_2' = m_0 + m_1 + m_2 + m_4$$

$$= x'y'z' + x'y'z + x'yz' + xy'z'$$

$$\Rightarrow f_2 = (x+y+z)(x+y+z')(x+y'+z)(x'+y+z)$$

$$= M_0 M_1 M_2 M_4$$

NOTE: you need not write in form of x, y and z every time. you can write in form of Σ and Π.

NOTE:
- SOP and POS are also known as canonical form of functions.
- minterms are called standard product
- max terms are called standard sum

→ WRITING CANONICAL FORM WITHOUT GENERATING TRUTH TABLE :

- consider function

$$F = A + B'C$$

- We know

$$A+A'=1 \; ; \; B+B'=1 \; ; \; C+C'=1$$

- In next step, we multiply every term in F by the expressions above ~~with~~ excluding the same variable

multiply by $(B+B')(C+C')$

$$F = A + B'C$$

multiply by $(A+A')$

$$\Rightarrow F = A(B+B')(C+C') + B'C(A+A')$$

$$\Rightarrow F = (AB+AB')(C+C') + AB'C + A'B'C$$

$$\Rightarrow F = ABC + ABC' + AB'C + AB'C' + AB'C + A'B'C$$

repetition ∴ remove one

$$\therefore F = ABC + ABC' + AB'C + AB'C' + A'B'C$$

$$\Rightarrow F = \sum(1,4,5,6,7)$$

- To express in form of man terms, we see

$$AA' = 0 \; ; \; BB' = 0 \; ; \; CC' = 0$$

now

$$F = A + B'C$$

Using distributive law

$$F = (A+B')(A+C)$$

B term missing

C term missing

$$\Rightarrow F = (A+B'+CC')(A+BB'+C)$$

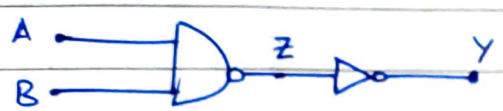
Using distributive law

$$\Rightarrow F = (A+B'+C)(A+B'+C')(A+B+C)$$

$$\Rightarrow F = \Pi(0,2,3)$$

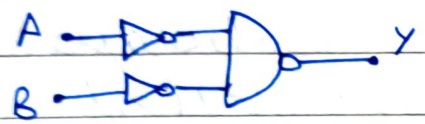
USING NAND GATE FOR IMPLEMENTATION

- AND gate



$$Z = \overline{A.B}$$
$$Y = Z'$$
$$\Rightarrow Y = \overline{\overline{A.B}}$$
$$\Rightarrow Y = A.B$$

- OR gate



$$Y = \overline{A'.B'}$$
$$\Rightarrow Y = A+B$$

KARNAUGH MAP (K-MAP) →

- When we write a function in terms of min-terms or max-terms and if we directly design a circuit from it, it might prove to be very costly. ∴ to optimise our circuit, we use K-maps.

- 2-variable K-MAP (4 min terms)

$x'y'$	m_0
$x'y$	m_1
xy'	m_2
xy	m_3

$x \backslash y$	0	1
0	$x'y'$ m_0	$x'y$ m_1
1	xy' m_2	xy m_3

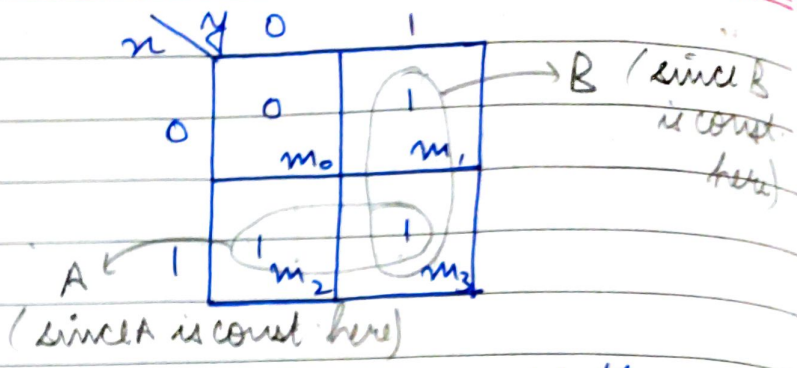
y remains constant

x remains constant

- We write the outputs in boxes and if we have 1 in 2 adjacent (vert. or hori.) boxes, we make their group & take something common

eg- Q→

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



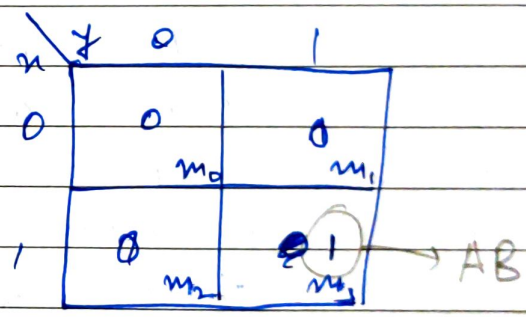
Ans:

- Now we make a group of 1. Note that we can't make a group of 2 diagonal boxes.
- We make groups of subsequent boxes. Because this ensures that only one variable is changing

Hence $Y = A + B$

Q→

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



Ans: No pairing possible ∴ directly we write $Y = A.B$

3-variable K-map

- Say we have 3-variables x, y, z
- We form a K-map of 8 columns like

$x \backslash yz$	00	01	11	10
0	m_0	m_1	m_3	m_2
1	m_4	m_5	m_7	m_6

we follow gray code sequence since we need to make sure that only one bit changes in adjacent box

- Consider

$x \backslash yz$	00	01	11	10
0	m_0	1 m_1	1 m_3	m_2
1	m_4	m_5	m_7	m_6

On combining

$$x'y'z + x'yz = x'z(y+y') = x'z$$

- consider again

yz	00	01	11	10
0	m_0	1 m_1	1 m_3	m_2
1	m_4	1 m_5	1 m_7	m_6

on combining

$$xy'z + xyz + x'y'z + x'yz = xz + x'z = z$$

NOTE: we can combine adjacent boxes only. Here we can also have a combination like

$x \backslash yz$	00	01	11	10
0	1			1
1	1			1

This combination is also possible.

Q→ Minimize

$$F(x,y,z) = \sum(3,4,6,7)$$

Ans:

$x \backslash yz$	00	01	11	10
0	0	1	1 3	2
1	1 4	5	1 7	1 6

yz remains constant

xz' remains constant

$$\therefore F(x,y,z) = (xyz + x'yz) + (xyz' + xy'z')$$

$$= yz + xz'$$

- **Don't Care**

- For some function $F(x,y,z)$, sometimes we define a 'don't care' term like

$$d(x,y,z) = \sum(5) \qquad \text{(for eg)}$$

If such an expression is given, we can take the minterms of 'don't care' for granted in a K-map. We can use them to

our advantage irrespective of whatever they might contain.

- eg- Consider previous question

$$F(x,y,z) = \Sigma(3,4,6,7)$$

& given $d(x,y,z) = \Sigma(5)$

then we write K-map as

x \ yz	00	01	11	10
0	0	1	1 (3)	2
1	1 (4)	X (5)	1 (7)	1 (6)

yz remains const in the group

x remains const in the group

Since 5 is not cared for, we can take it in the group.

∴ we can write

$$F(x,y,z) = x + yz$$

- we can also use the 3-variable K-map to write a function in POS form (in maxterms)

- Consider F from previous que

$$F(x,y,z) = \Sigma(3,4,6,7)$$

x \ yz	00	01	11	10
0	0 (0)	0 (1)	1 (3)	0 (2)
1	1 (4)	0 (5)	1 (7)	1 (6)

y'z const.

x'z' const

Here, what we do is, that we write F' from K-map. For that, we group the zeroes and then follow the procedure

$$F'(x,y,z) = \sum(0,1,2,5)$$

$$= x'z' + y'z$$

$$\Rightarrow \overline{F'} = F = \overline{x'z' + y'z}$$

$$\Rightarrow F = (x+z)(y+z')$$

Q. Simplify

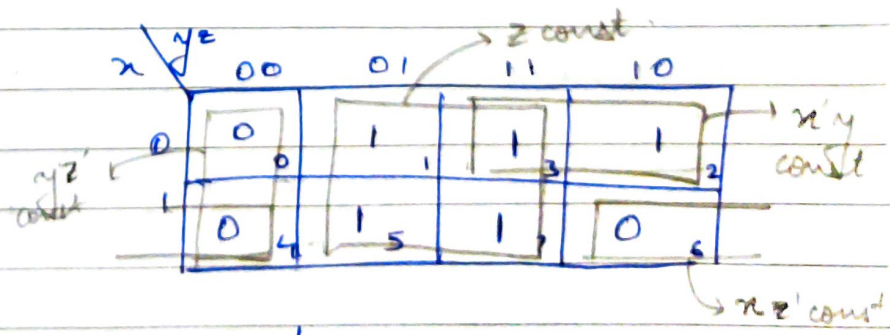
$$F = A'C + A'B + AB'C + BC$$

Ans:

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

$$\therefore F = \prod(0,4,6)$$

$$= \sum(1,2,3,5,7)$$



$$F = y'z + yz + x'yz'$$

$$\Rightarrow F = z + x'yz'$$

$$\Rightarrow F = C + A'BC' = C + A'B$$ (absorption theorem)

Or directly

$$F = (x'y + z)$$

$$\Rightarrow F = A'B + C$$

$F' = xz' + yz'$

$\therefore F = (x'+z)(y'+z)$

METHOD 2:

$$F = A'C + A'B + AB'C + BC$$

$$= A'C(B+B') + A'B(C+C') + AB'C + (A+A')BC$$

$$= A'BC + A'B'C + A'BC + A'BC' + AB'C + ABC + A'BC$$

$$= A'BC + A'B'C + A'BC' + AB'C + ABC$$

$$= A'C + A'BC' + AC$$

$$= C + A'BC'$$

$$= C + A'B$$

- 4-variable K-map:-
- Consider we have 4 variables (A, B, C, D)
- Then we form K-map like

AB \ CD	00	01	11	10
00	m_0	m_1	m_3	m_2
01	m_4	m_5	m_7	m_6
11	m_{12}	m_{13}	m_{15}	m_{14}
10	m_8	m_9	m_{11}	m_{10}

- eg-

AB \ CD	00	01	11	10
00	1			1
01				
11				
10	1			1

$F = B'D'$

eg-

AB \ CD	00	01	11	10
00	1	1		
01	1	1		
11				
10				

$F = AC$