EE 2310 Homework #8 – MIPS Architecture Question Solutions

Below are a set of questions that come primarily from Lectures 17 through 22 (although a few may be from other lectures). Answers will not be posted. However, five of these questions will be the bonus questions on the final exam (worth 3 points each for a total of 15 points). Find the answers to these questions and make sure they are on your "cheat sheet" – they will be worth 15 points on the final.

1. **The instruction pair used to call and return from procedures are:**

   jal and jr

2. **Where is the stack? In what direction does it grow?**

In the top of memory. It grows down.

3. **Is the stack "LIFO" or FIFO?"**

   LIFO

4. **The stack pointer is what register number and what is its symbol?**

   $29, $sp

5. **A reserved section on the stack for a procedure or some other function is called a _____?**

   A frame

6. **Is the following true or false? The s-registers must be protected by the calling program and the t-registers by the called program.**

   False

7. **True or false: Windows is an application program that runs under Unix.**

False

8. **In a multiprogramming environment, what does "simultaneous" mean?**

It means that many programs can be resident in computer memory at once, although only one is active at a time (and many may be active in a short time such as a second).

9. **What is the difference in a program and a process?**

A program is an executable file, such as a SPIM NotePad file. A process is an instance of a program in execution, such as a NotePad file assembled and loaded into PCSPIM and ready to execute.

10. **What is a process switch?**

A process switch is an act of the operating system suspending a process and starting up the highest-priority process not currently running.

11. **What is an exception?**

In general an exception is an event that causes the CPU of a computer to suspend operation and attend to that event. It may be a benign event (such as a request for I/O) or a more serious one such as an I/O, memory, or CPU error.

12. **Define the computer ALU.**

The ALU (arithmetic-logic unit) is the part of the CPU that actually processes the information.

13. **Define the computer control unit.**

The control unit decodes the instructions and tells the ALU what information to process and what process to use.

14. What is the 32-bit ALU made up of?

It is actually constructed of 32 1-bit processors.

15. What do we really mean by references to "instruction memory" and "data memory," since all memory is the same?

The references "data memory" and "instruction memory" refer to the paths into the same memory unit, since there are different paths for retrieving instructions and data.

16. How many registers are there in the MIPS register block?

32

17. What does the sign extender do?

It adds the upper 16 bits to the 16-bit immediate in many instructions by matching those upper bits to bit 15 (the sign bit of the lower 16 bits).

18. Why and how is the ALU used in data memory access instructions?

It is used to calculate the memory address for memory data accesses.

19. Name any two places in the single-cycle ALU where multiplexers are used.

On the input to the write register address, on one of the ALU inputs, on the MEM/ALU output, and on the PC input.

20. Explain how the multicycle implementation speeds up the MIPS CPU.

The multicycle design splits up the MIPS CPU into five sections, each of which executes on a different (speeded up) clock cycle. Since not all instructions need to use all five sections of the multicycle CPU, many instructions finish faster.

21. How is the MIPS pipeline different from the multicycle design?

The MIPS pipeline splits the single-cycle CPU into the same five sections, but in the case of the pipeline, each section can be doing its part of an instruction concurrently. Thus instructions "march" down the pipeline, with a new instruction being started each clock cycle.

22. Name the five parts of the multicycle implementation (which have the same names as the five sections of the MIPS R-2000 pipeline).

The sections are INSTRUCTION FETCH, INSTRUCTION DECODE/REGISTER FETCH, ALU EXECUTION (EX/ALU), MEMORY ACCESS, and REGISTER WRITEBACK.

23. Why are intermediate results registers required in the MIPS pipeline implementation?

Because each section of the pipeline is a separate "processor," and when its results are complete, they must be "handed off' to the next section of the CPU.

24. What are the acronyms for the interfaces between the pipeline sections?

IF/ID, ID/EX, EX/MEM, and MEM/WB

25. When is the ALU bypass bus used?

When the ALU output is not a memory address but the result of a register-register calculation (math, logic, shift, etc.) that must be written back to a destination register.

26. What is a data hazard in the MIPS pipeline?

A data hazard occurs when an instruction in the pipeline needs data from a register which is a destination register of an instruction still in the pipeline. In that case, the desired register data is not available yet, so that the "upstream" (newer) instruction will get incorrect data if it reads the source register at that point.

27. What is a control hazard in the MIPS pipeline?

A control hazard is similar to a data hazard except that the instruction needing data is a branch instruction, so that if it reads the (incorrect) register at the wrong time, the branch instruction may not execute correctly.

28. How can a forwarding unit prevent both data and control hazards?

The forwarding unit extracts write register data from one of the intermediate pipeline registers that is destined for writeback to a destination register and forwards it to the correct ALU input instead of the incorrect data that still resides in the source register called out in the instruction requiring the data.

29. Why does the forwarding unit not always work?

If a memory access is required, the data may simply not be available when the newer instruction requires it.

30. How is this problem overcome by stalling?

In a CPU stall, the instruction about to get the wrong register information and all instructions upstream from it are halted in the pipeline. The instructions "further down the pipeline" are allowed to complete, making the desired register available to the stalled instruction. The pipeline is then restarted and instructions resume their travel down it.

31. What is the latency in a hard disk drive?

Latency is a delay that occurs when the disk drive gets a read or write command, but the head must be moved over the correct track, and the correct point in the track must spin around under the head. This can amount to several milliseconds.

32. True or false: Cache memory, or static RAM, is composed of flip-flops. Dynamic random access memory (or DRAM) is a much simpler electronic memory with only one transistor per cell.

True

33. True or false: Hierarchical memory management and cache memories result in an environment where each application appears to have the full range of memory.

True

34. Arrange the following memory devices in order, from <u>fastest</u> to <u>slowest</u>:

Hard disk, L1 cache, DRAM, L2 cache, CPU registers

CPU registers, L1 cache, L2 cache, DRAM, hard disk

35. True or false: Modern DRAM memories are much faster than state-of-the-art CPU chips such as the AMD or Intel processors.

False