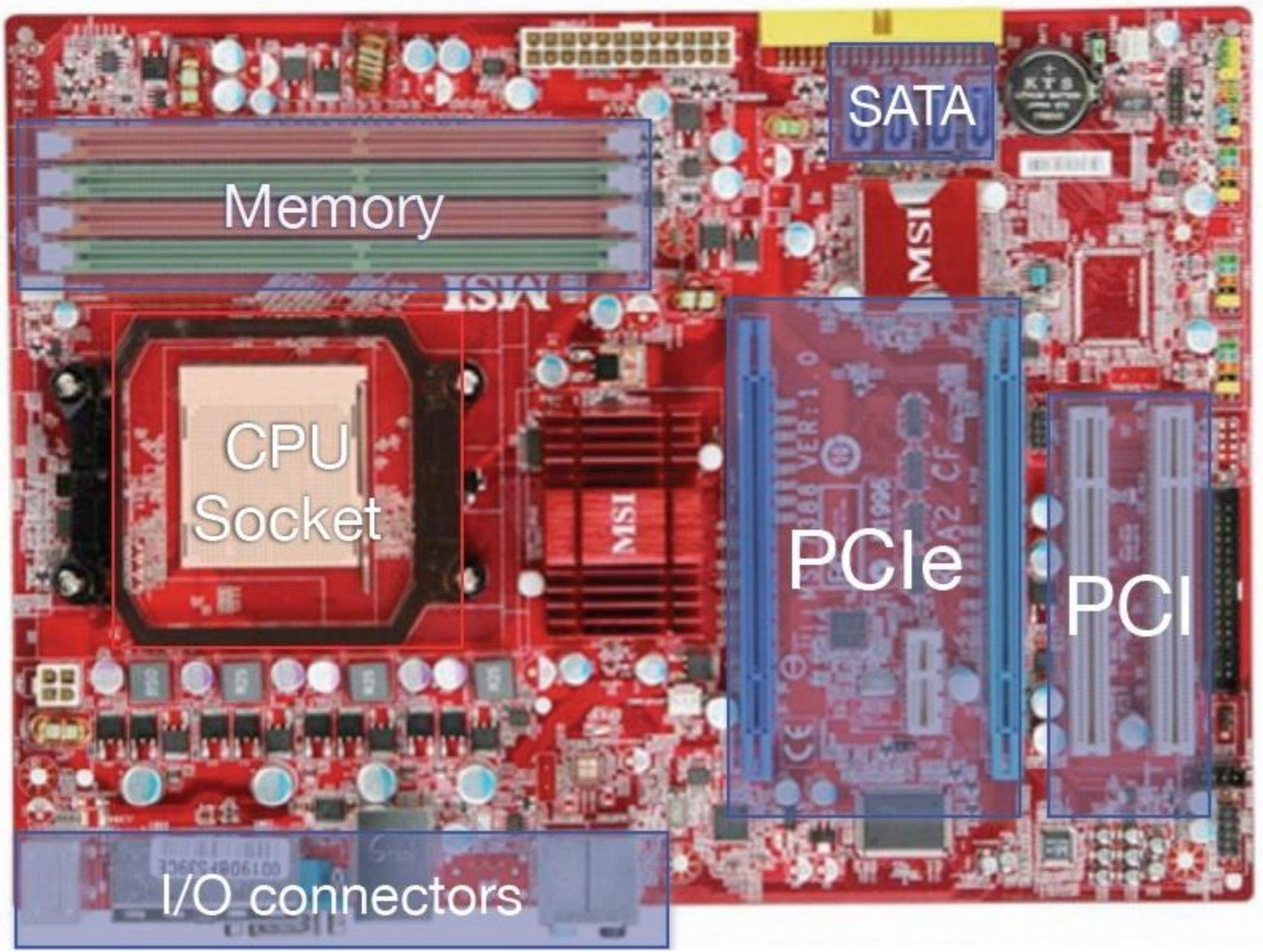
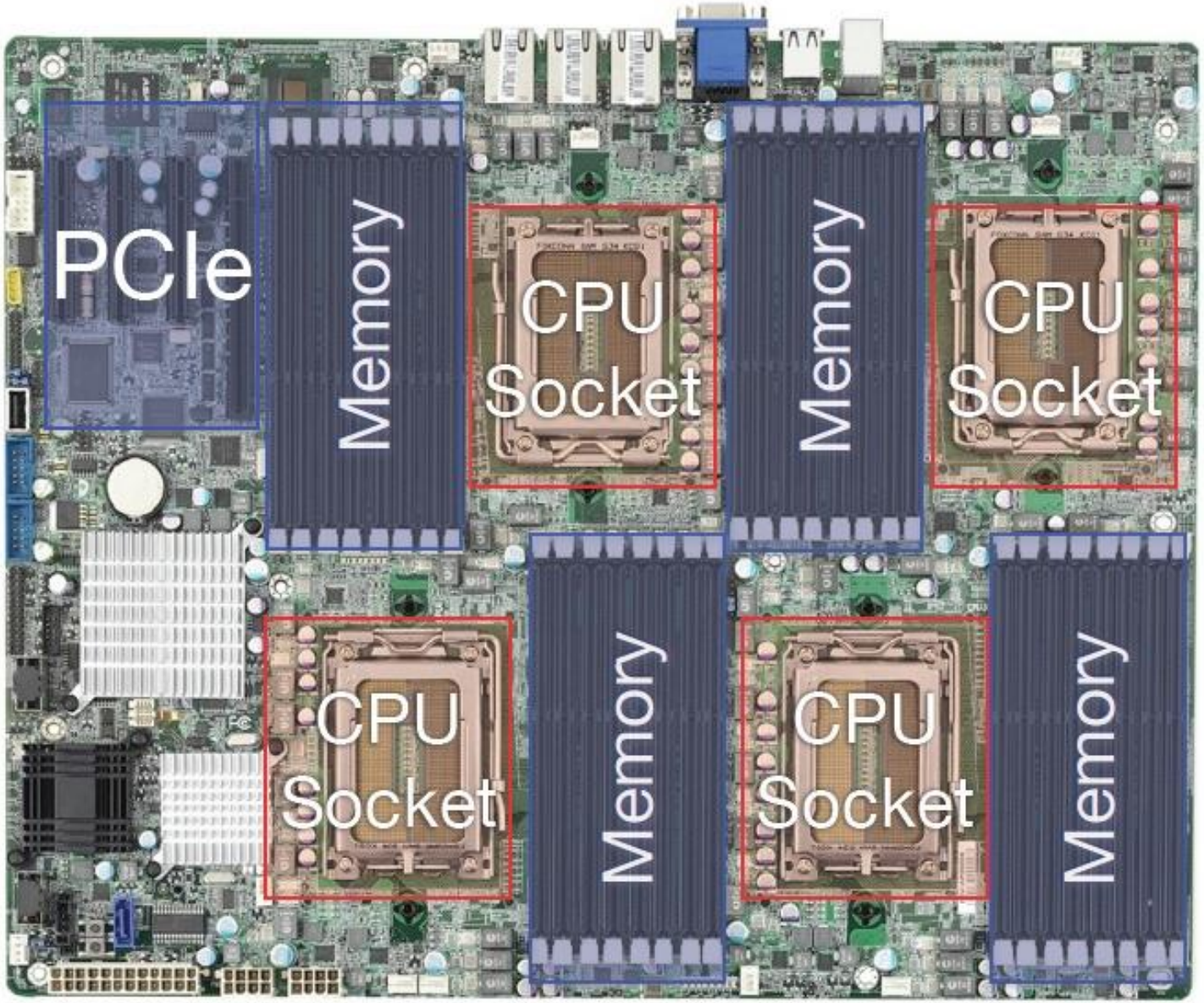
Memory


DRAM
CPU
CPU
5:30
9:00
72°
DRAM
CPU
DRAM
CPU
CPU
DRAM
CPU
DRAM
DRAM
CPU
DRAM
DRAM

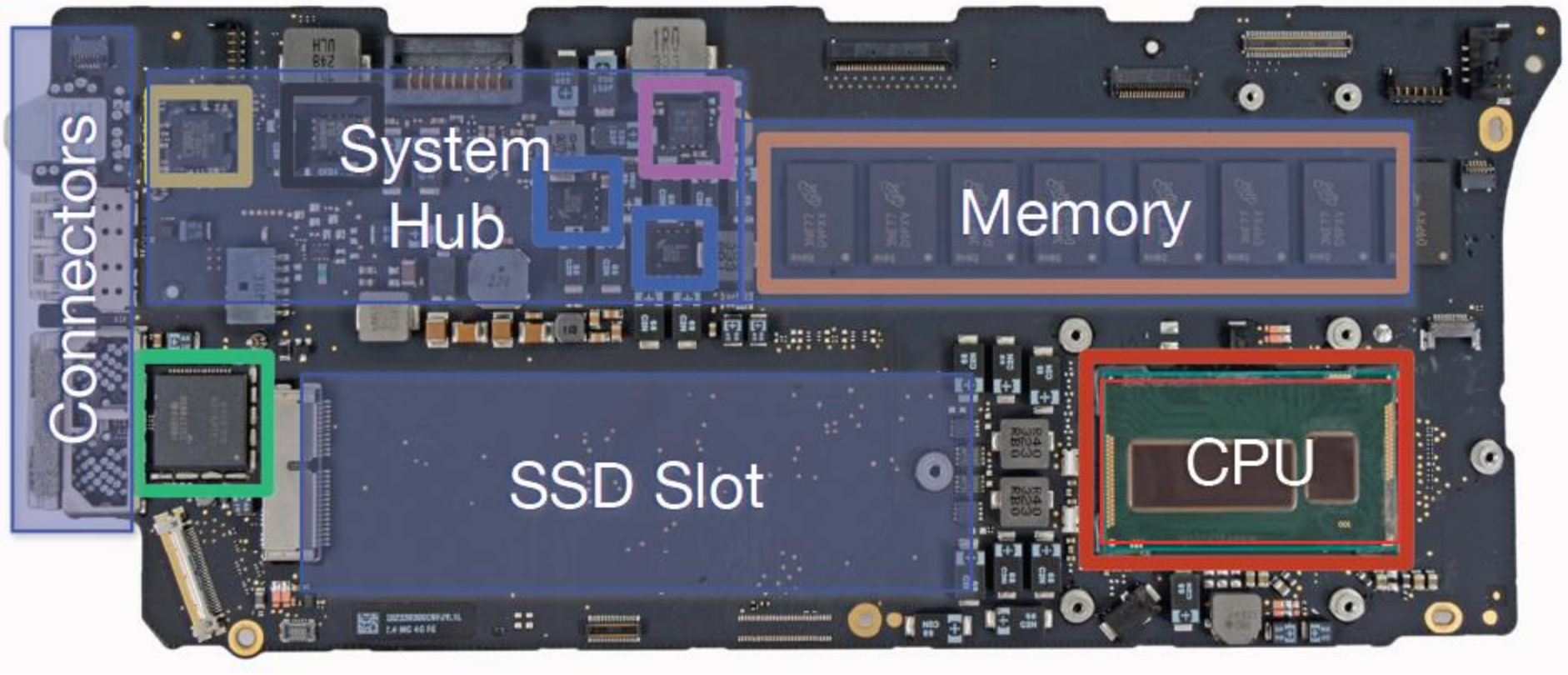
Desktop PC



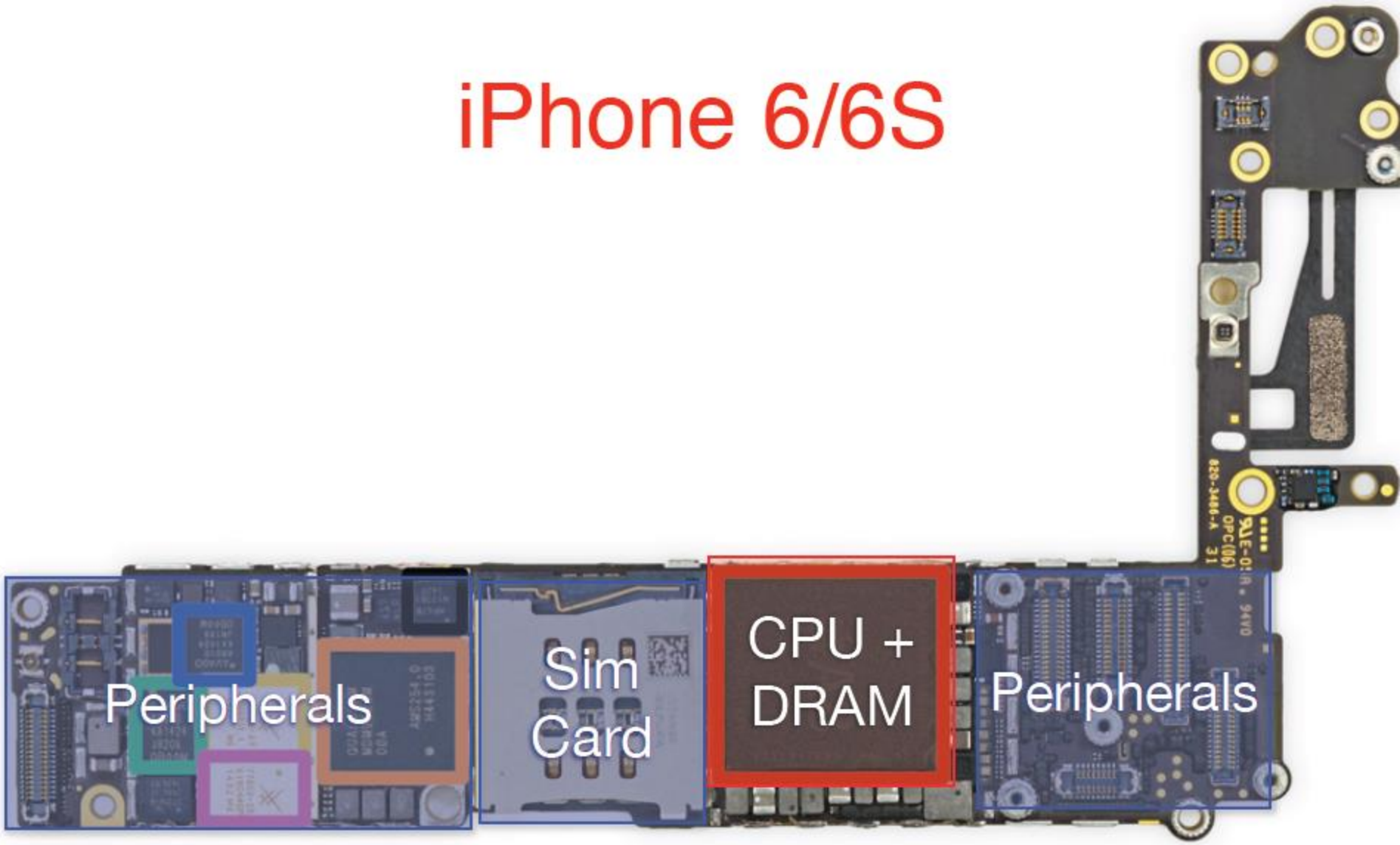
Server


PCIe
Memory
CPU Socket
Memory
CPU Socket
CPU Socket
Memory
CPU Socket
Memory

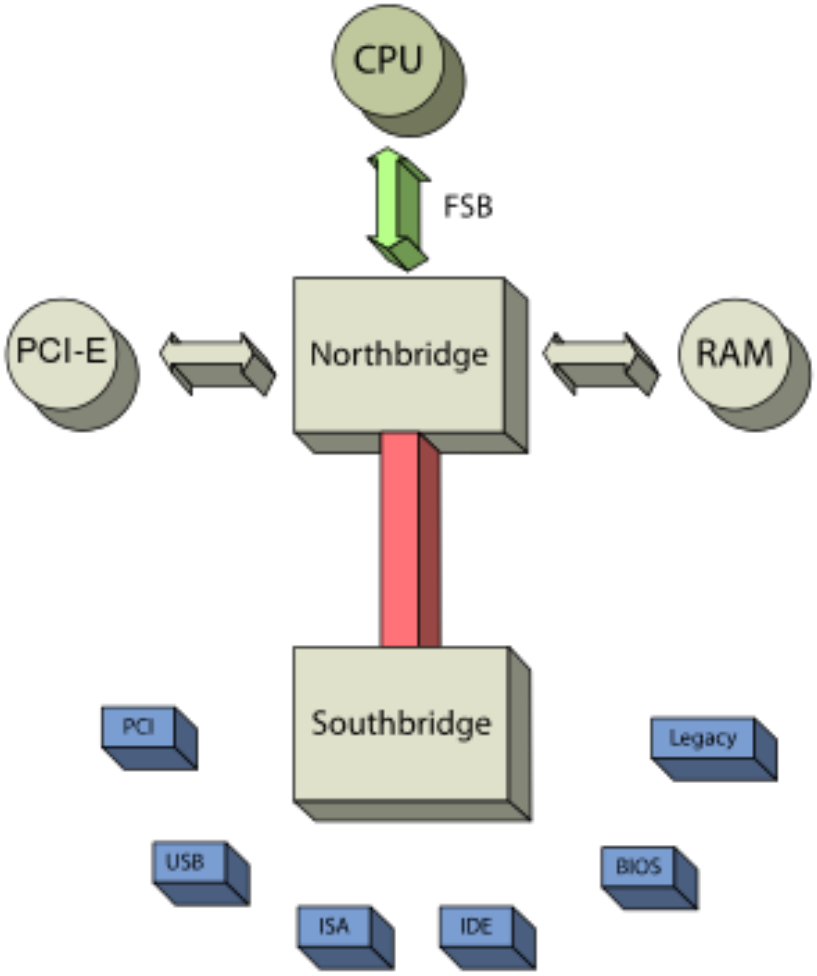
Macbook Pro w/ Retina



iPhone 6/6S



Typical PC Architecture: **northbridge** or **host bridge**

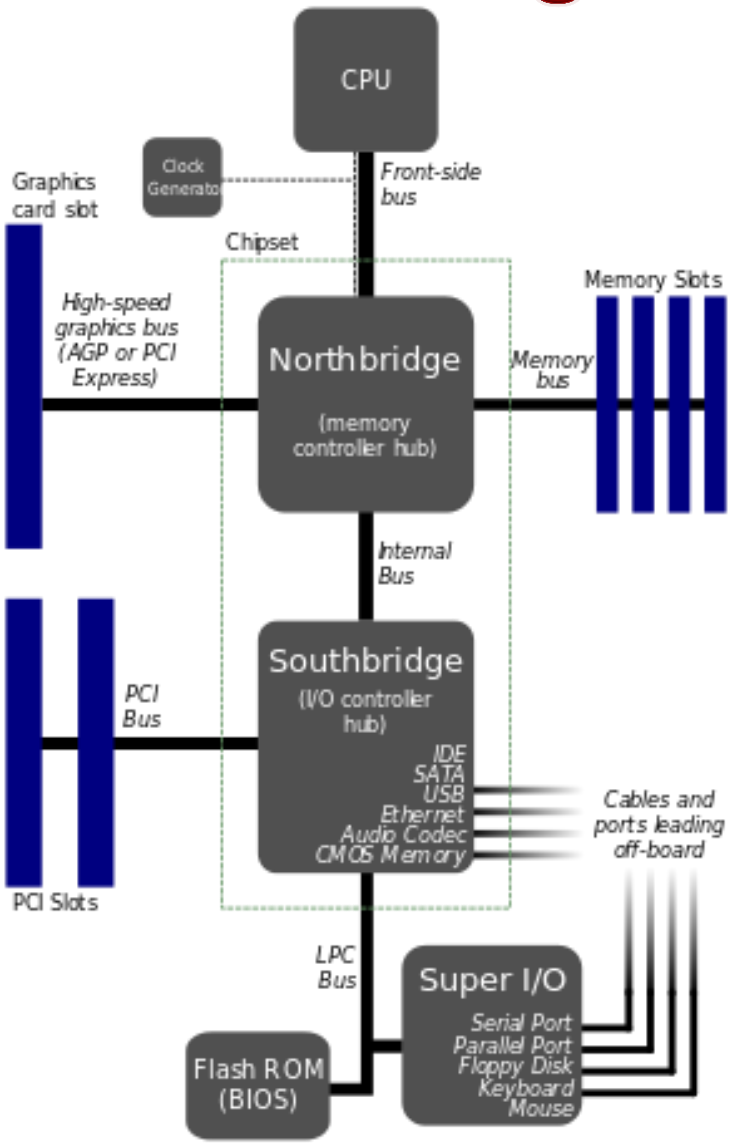


front-side bus (FSB)

I/O controller hub

(Typical PC Architecture)

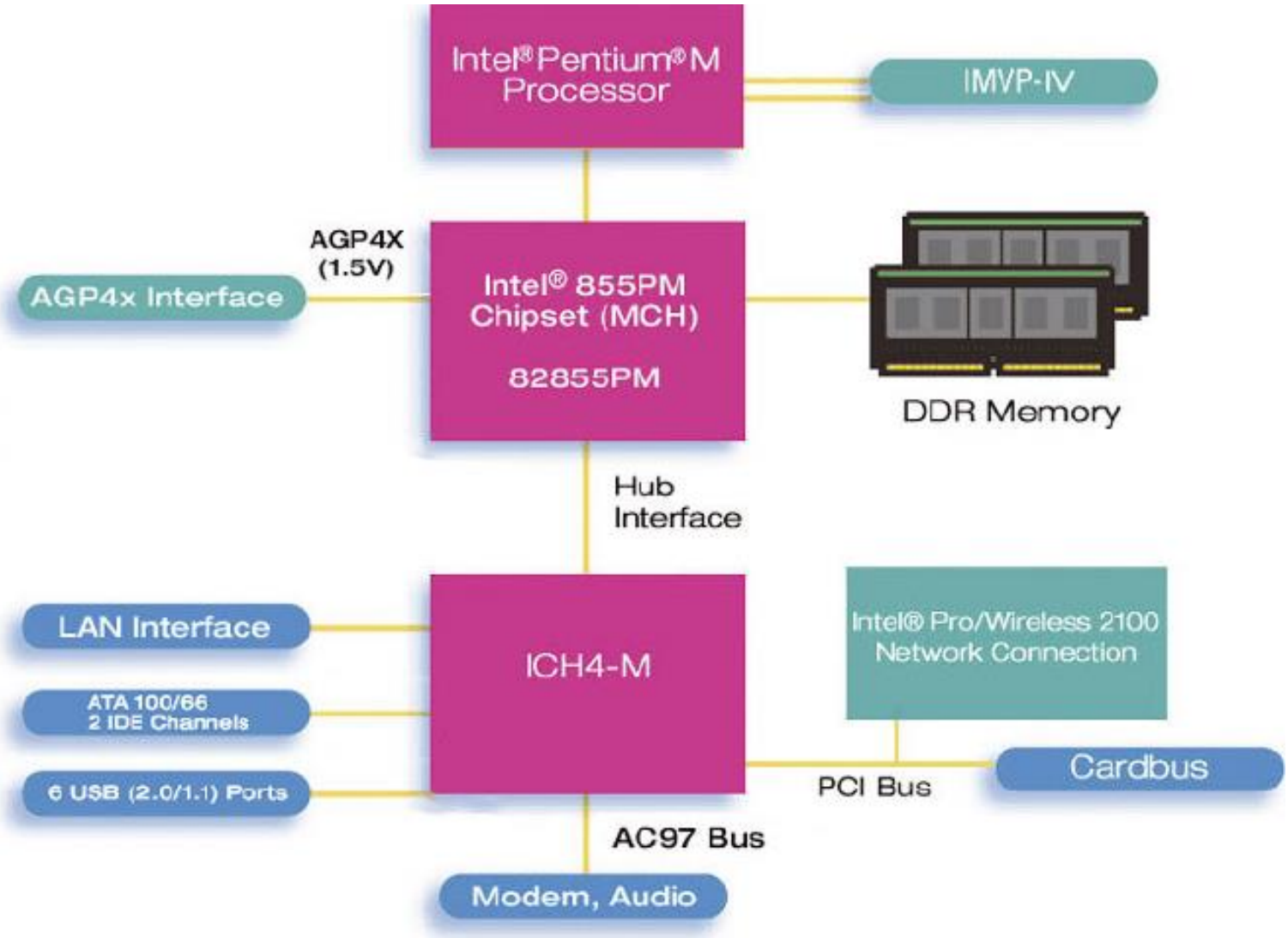
northbridge or host bridge



Graphics and Memory Contro
(GMCH)

I/O Controller Hub (ICH)

What is A Computer?



Courtesy, Intel

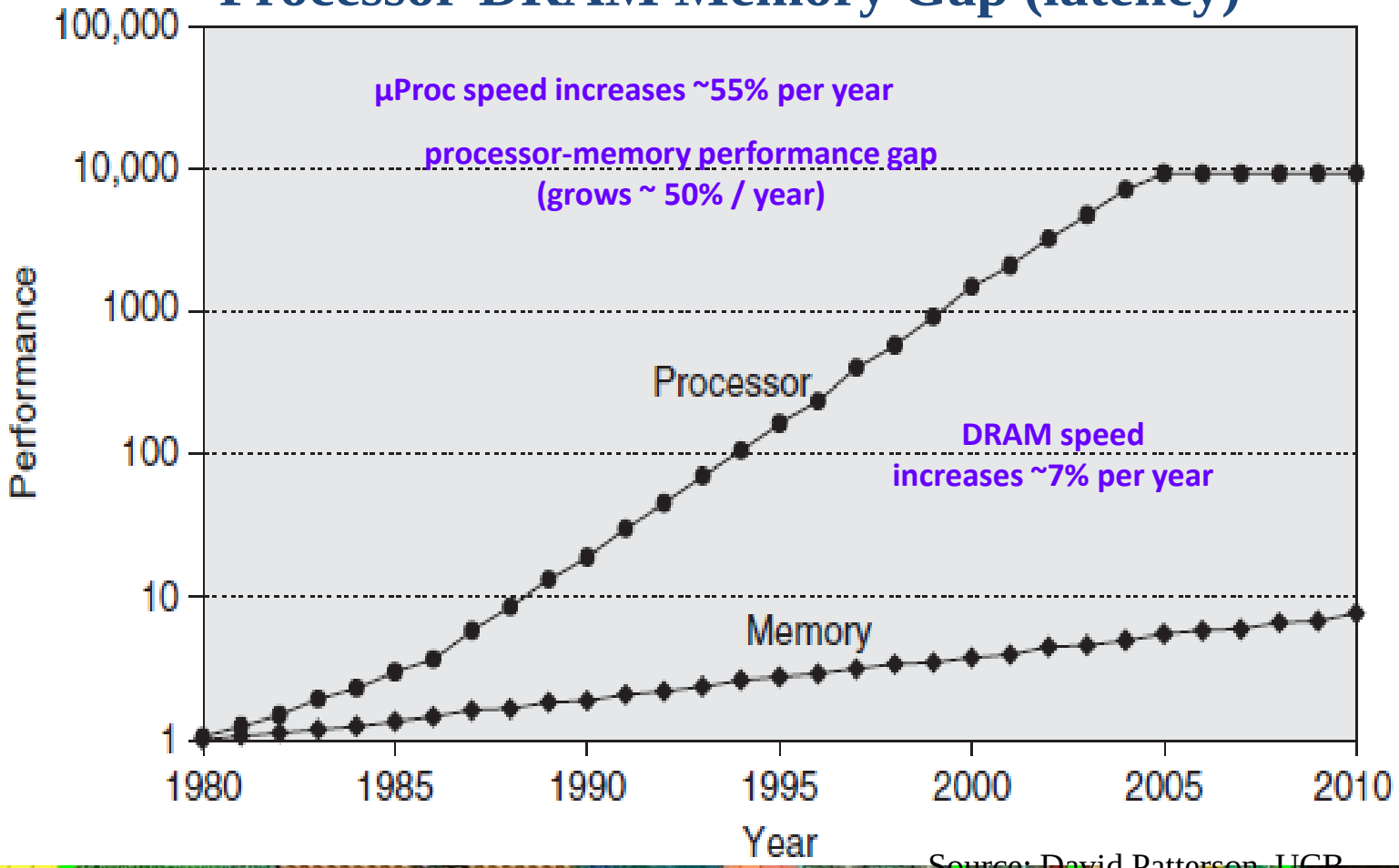
Memory in a Modern System

Overview

- **Review of Memory Technologies**
- **Overview of Memory Hierarchy**

- Learning Objectives
  - Why is that some memories slow ?
  - What is memory hierarchy?
  - Why do we need memory hierarchy?

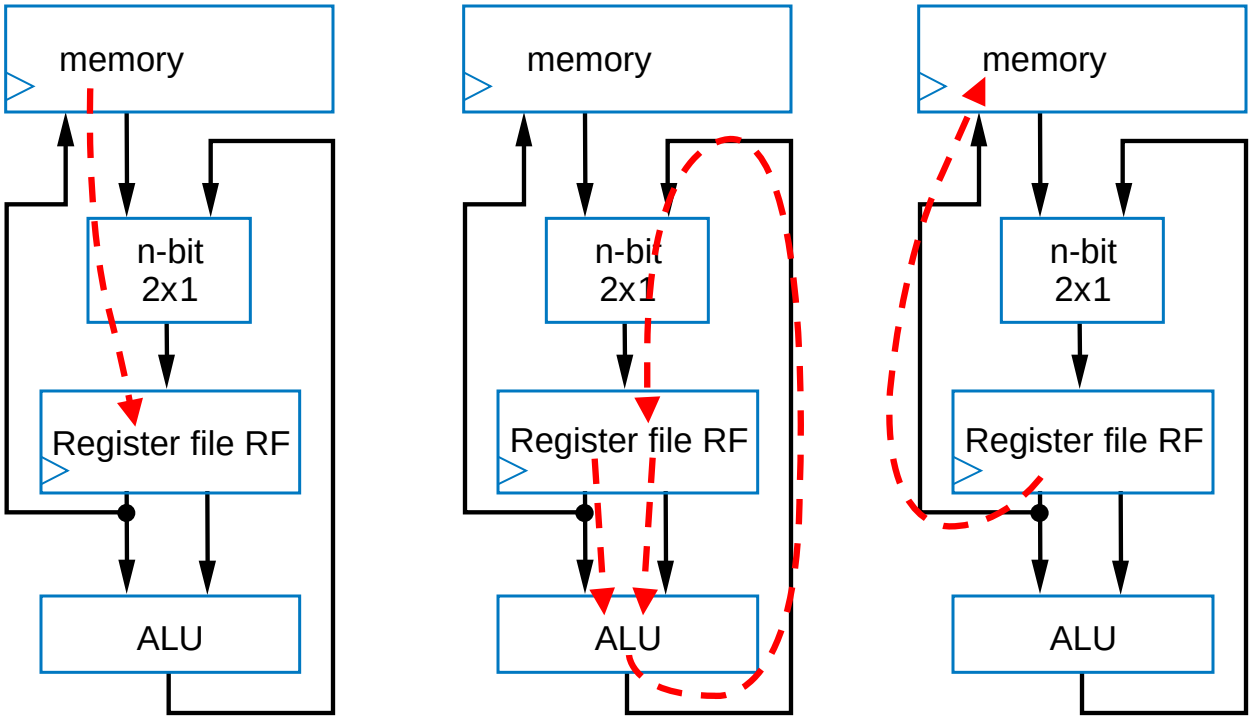
Processor-DRAM Memory Gap (latency)



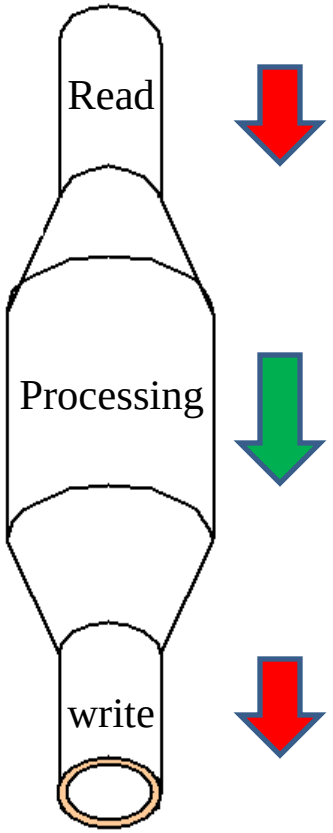
Source: David Patterson, UCB

Review: Datapath Operations

- Load operation: Load data from data memory to RF
- ALU operation: Transforms data by passing one or two RF register values through ALU, performing operation (ADD, SUB, AND, OR, etc.), and writing back into RF.
- Store operation: Stores RF register value back into data memory
- Each operation can be done in one clock cycle

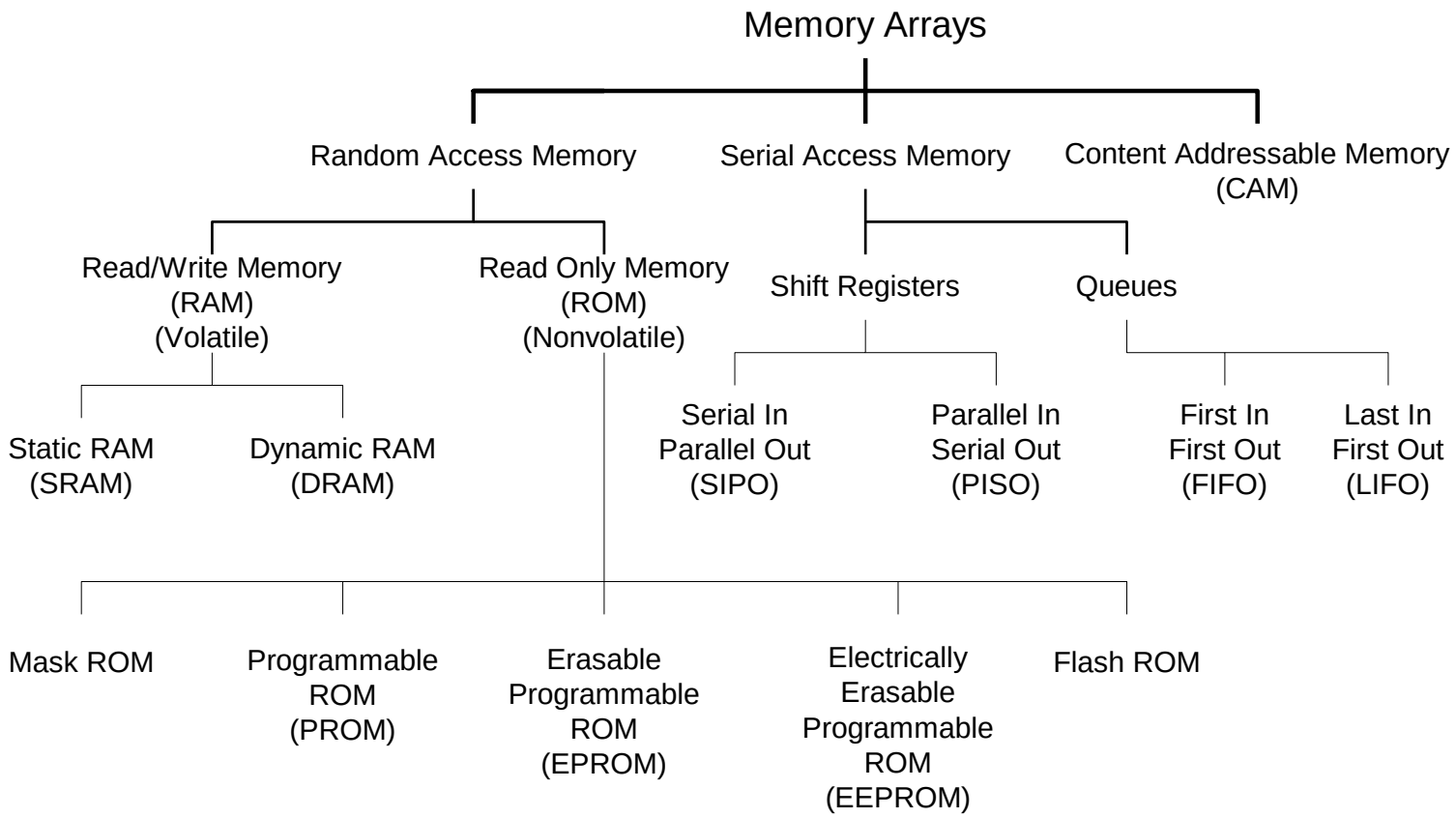


Load operation ALU operation Store operation

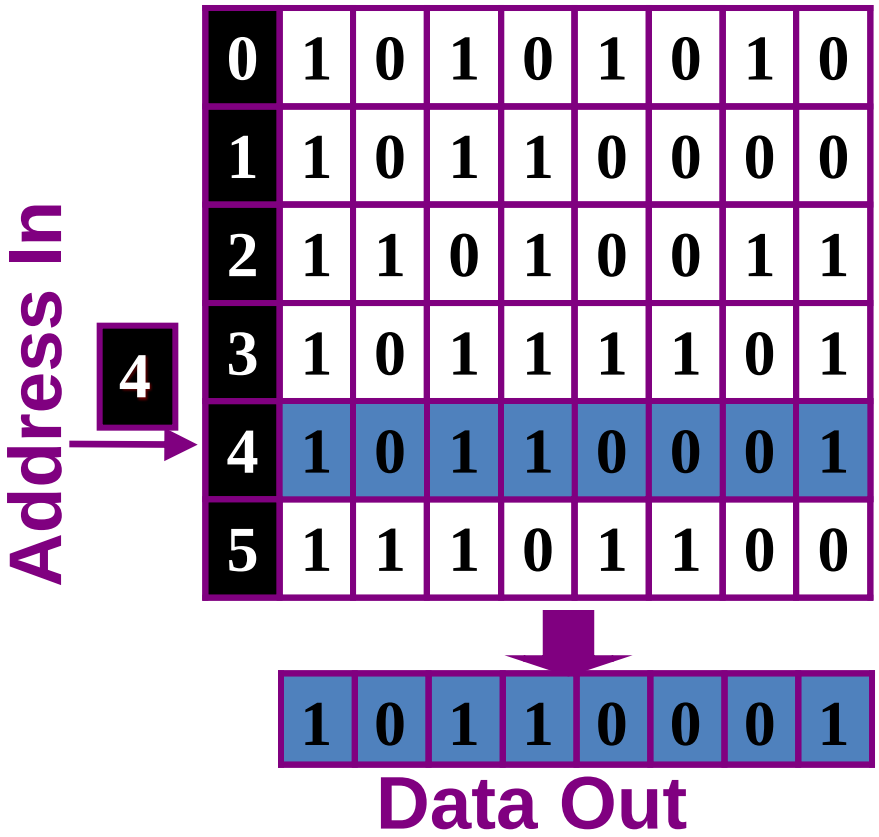


What are the Common Memory Technologies?

Memory

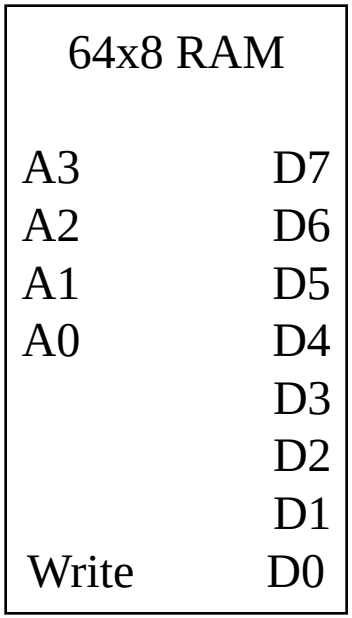

Memory Arrays
Random Access Memory
Serial Access Memory
Content Addressable Memory (CAM)
Read/Write Memory (RAM) (Volatile)
Read Only Memory (ROM) (Nonvolatile)
Shift Registers
Queues
Static RAM (SRAM)
Dynamic RAM (DRAM)
Serial In Parallel Out (SIPO)
Parallel In Serial Out (PISO)
First In First Out (FIFO)
Last In First Out (LIFO)
Mask ROM
Programmable ROM (PROM)
Erasable Programmable ROM (EPROM)
Electrically Erasable Programmable ROM (EEPROM)
Flash ROM

RAM

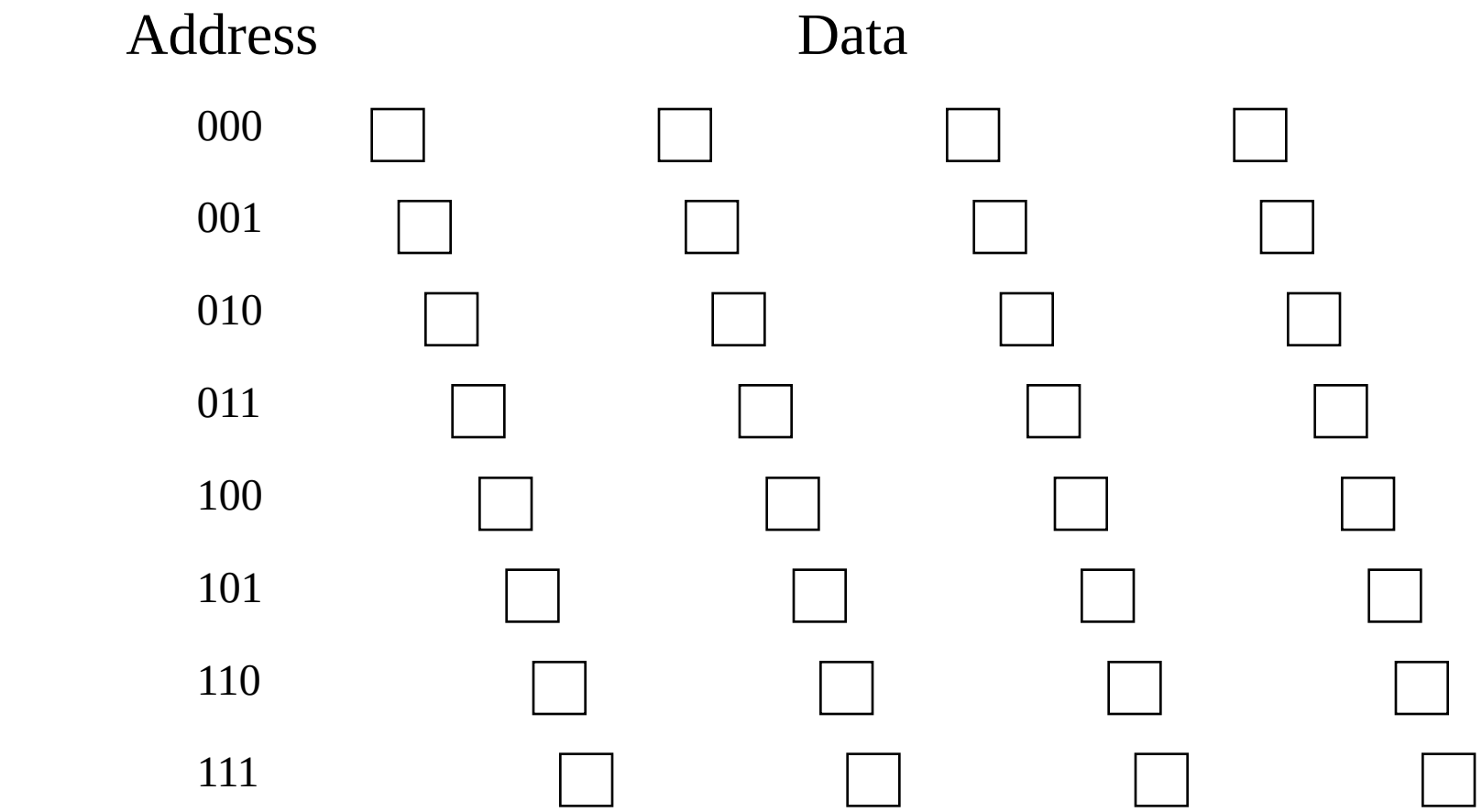

Address In
4
0 1 0 1 0 1 0 1 0
1 1 0 1 1 0 0 0 0
2 1 1 0 1 0 0 1 1
3 1 0 1 1 1 1 0 1
4 1 0 1 1 0 0 0 1
5 1 1 1 0 1 1 0 0
1 0 1 1 0 0 0 1
Data Out

Memory

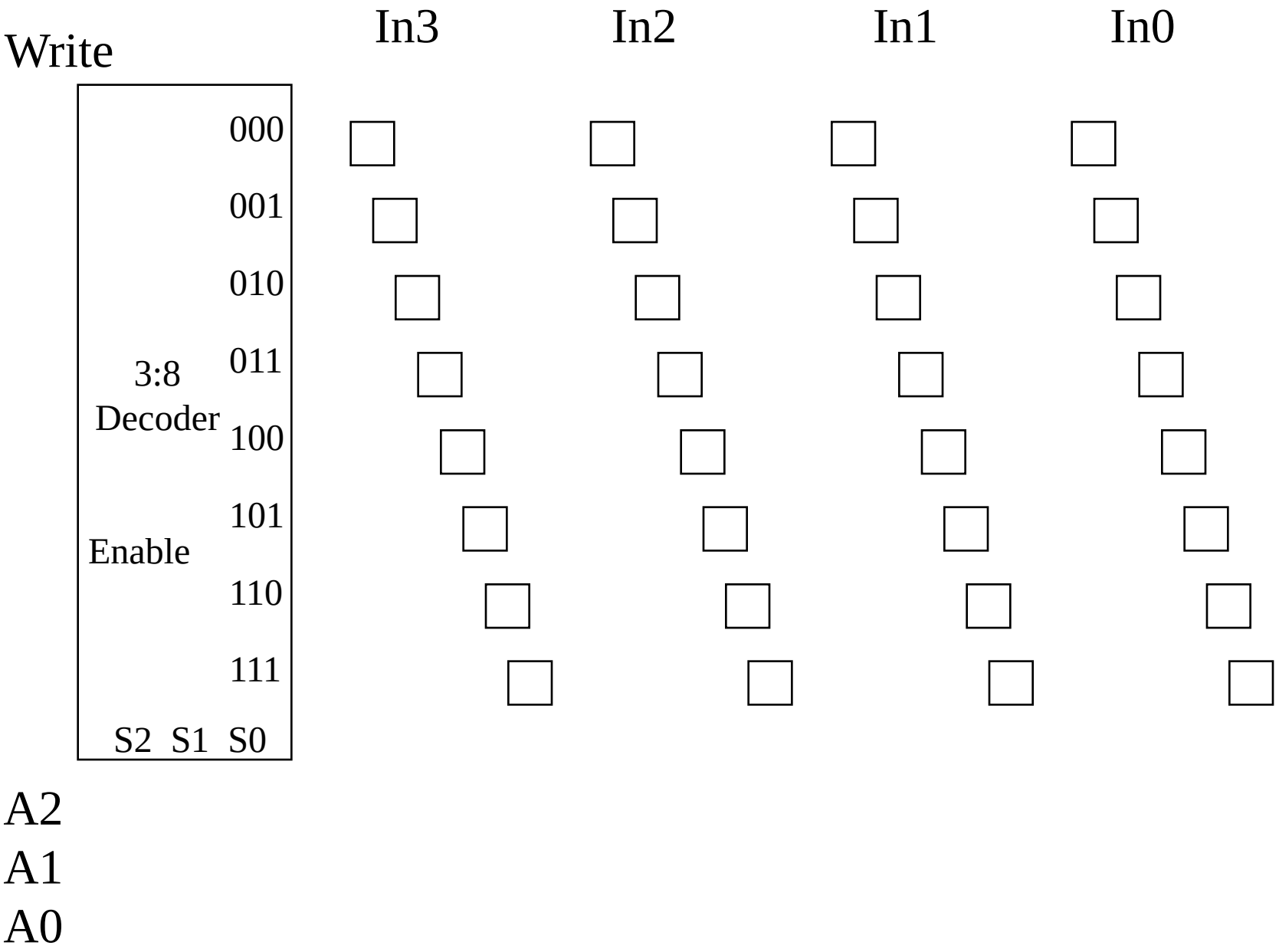
Address	Data
000000	00111110
000001	01101011
000010	01011101
000011	01100011
000100	00111110
000101	00000000
000110	11111111
000111	01010101
001000	10101010
001001	00100001
001010	11011010



8x4 RAM



8x4 RAM


In3
In2
In1
In0
Write
000
001
010
011
100
101
110
111
3:8
Decoder
Enable
S2 S1 S0
A2
A1
A0

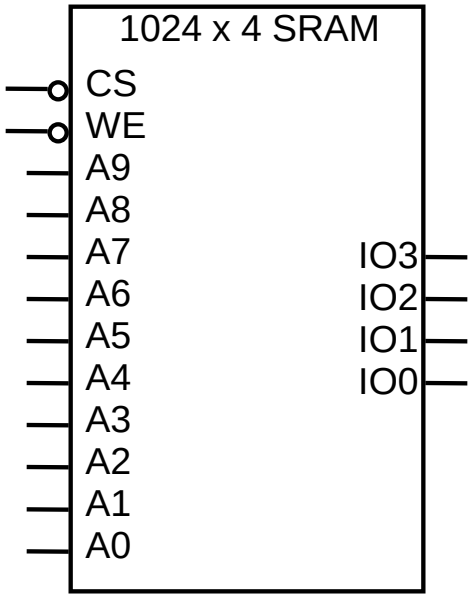
Static RAM Organization

Chip Select Line (active lo)

Write Enable Line (active lo)

10 Address Lines

4 Bidirectional Data Lines



RAM Organization

Long thin layouts are not the best organization for a RAM