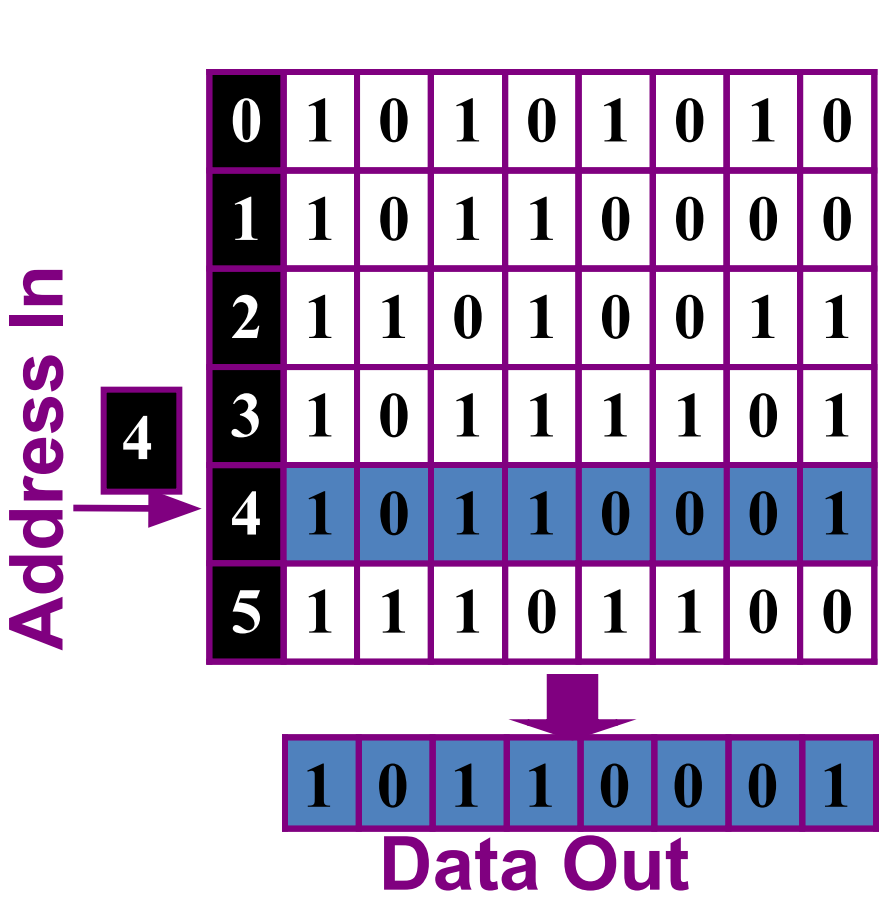
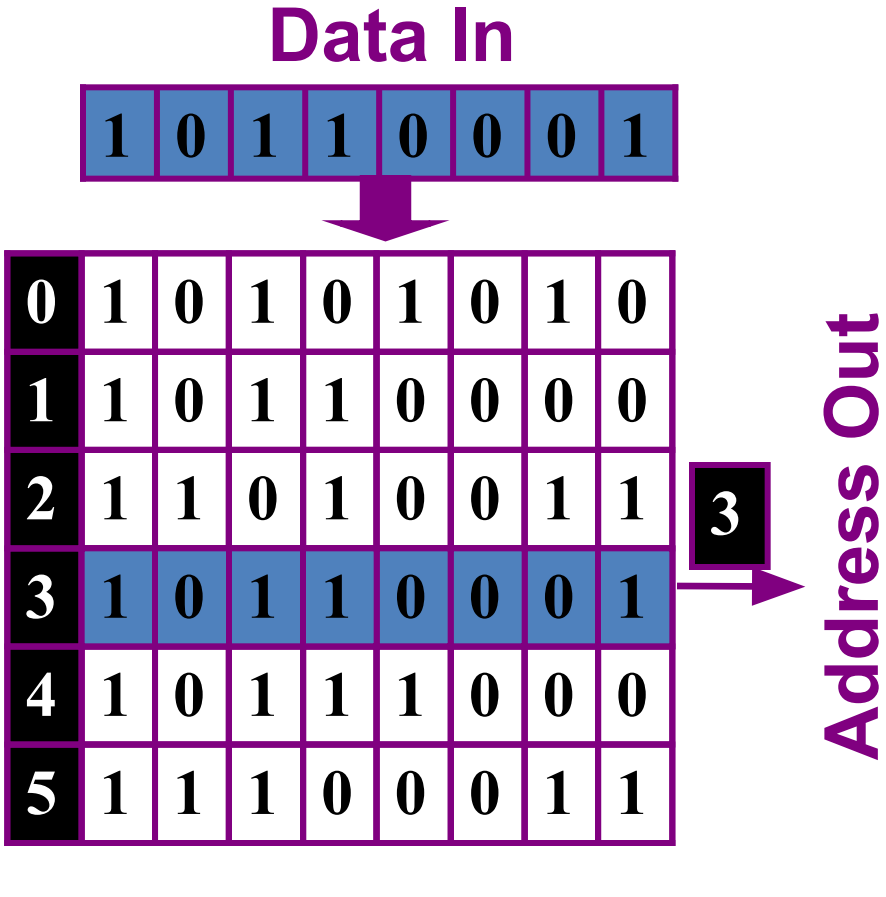
CAM

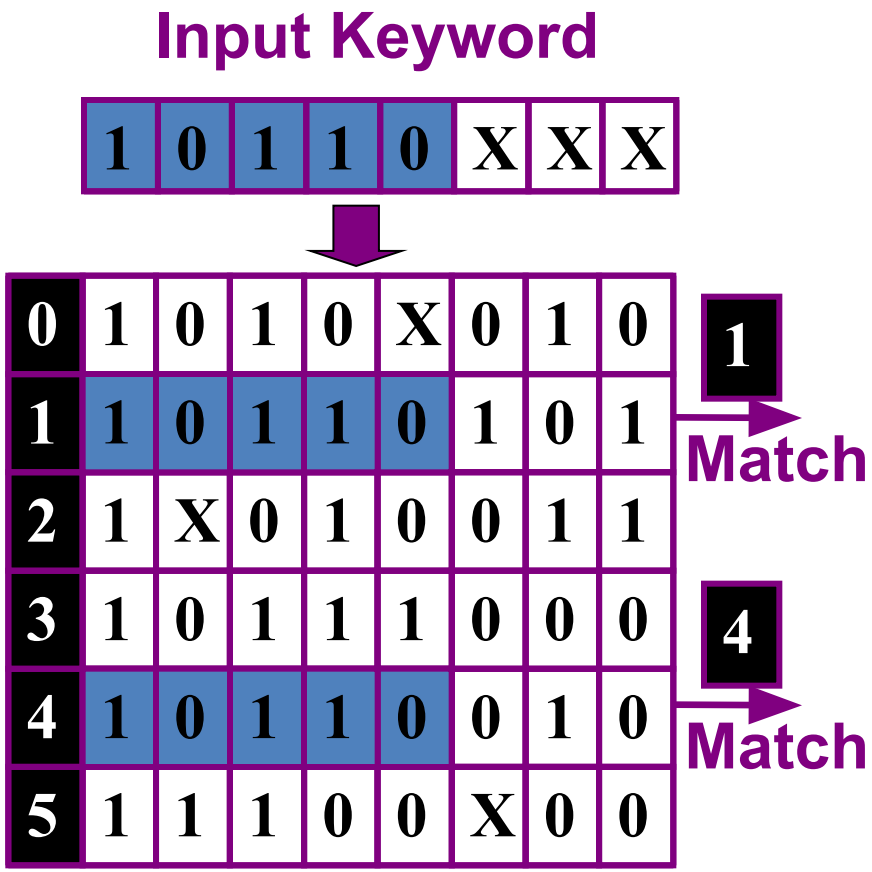
- CAM vs. RAM

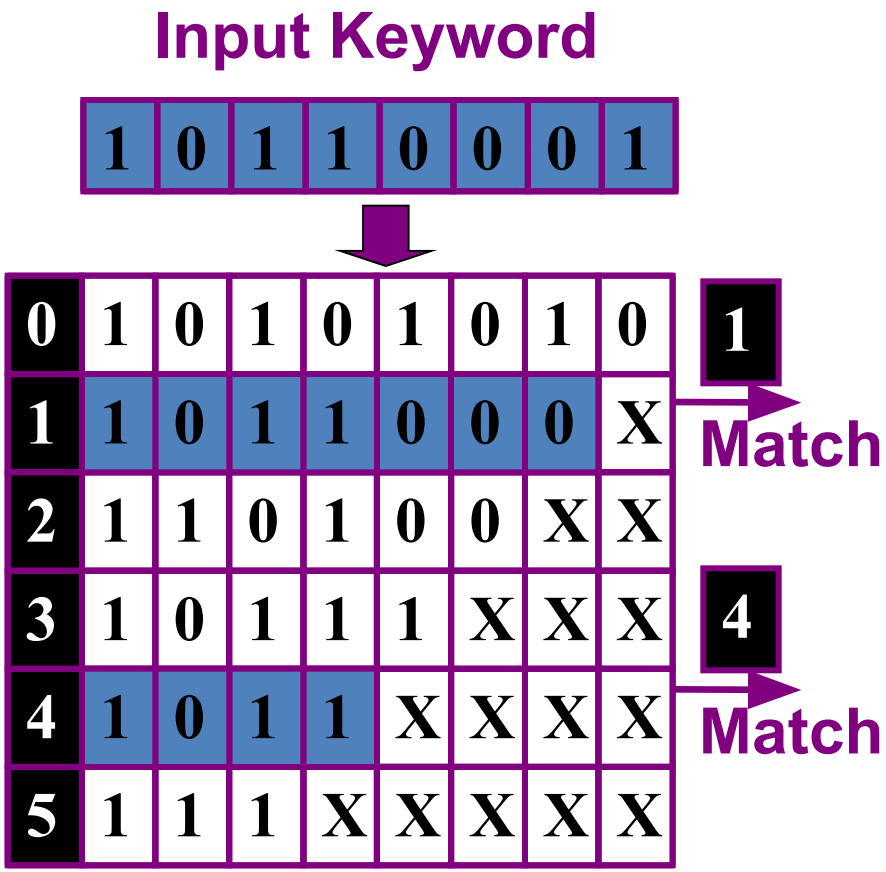




CAM

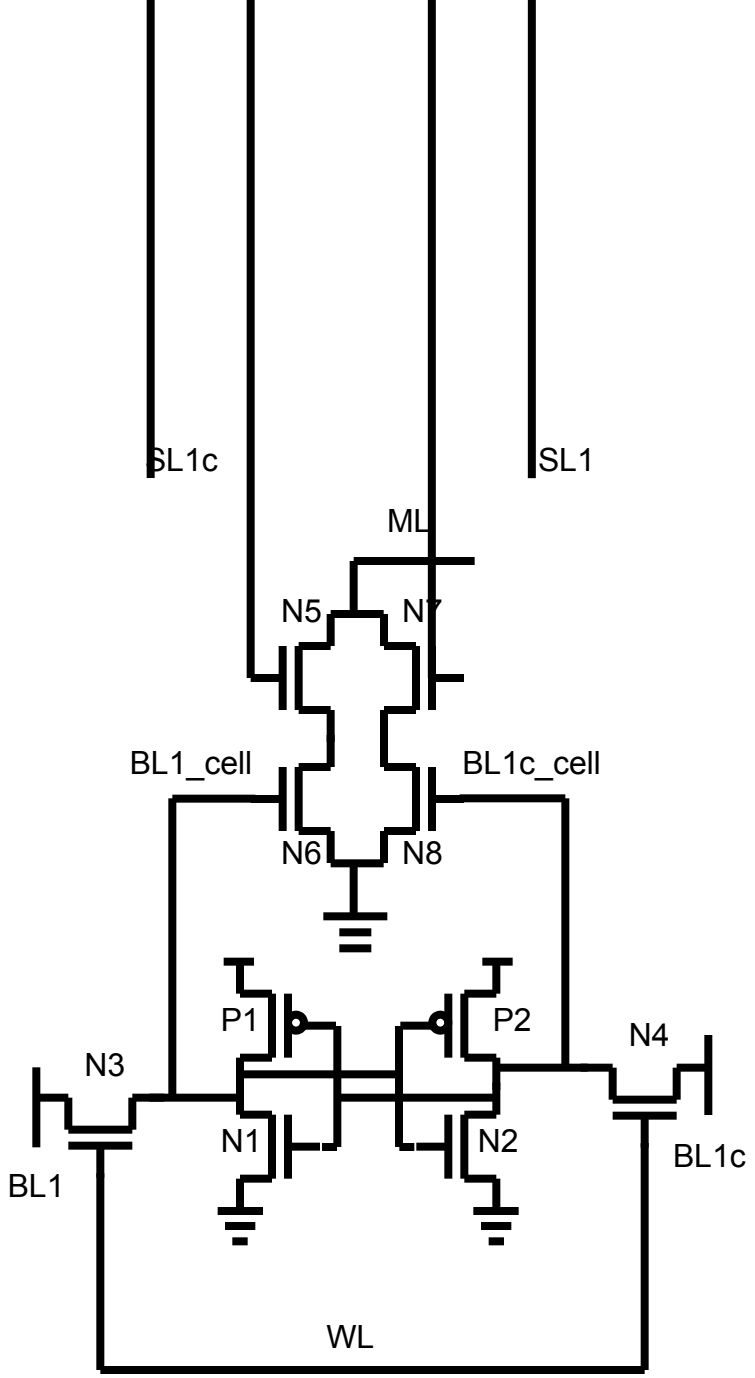
- Ternary CAM (TCAM)





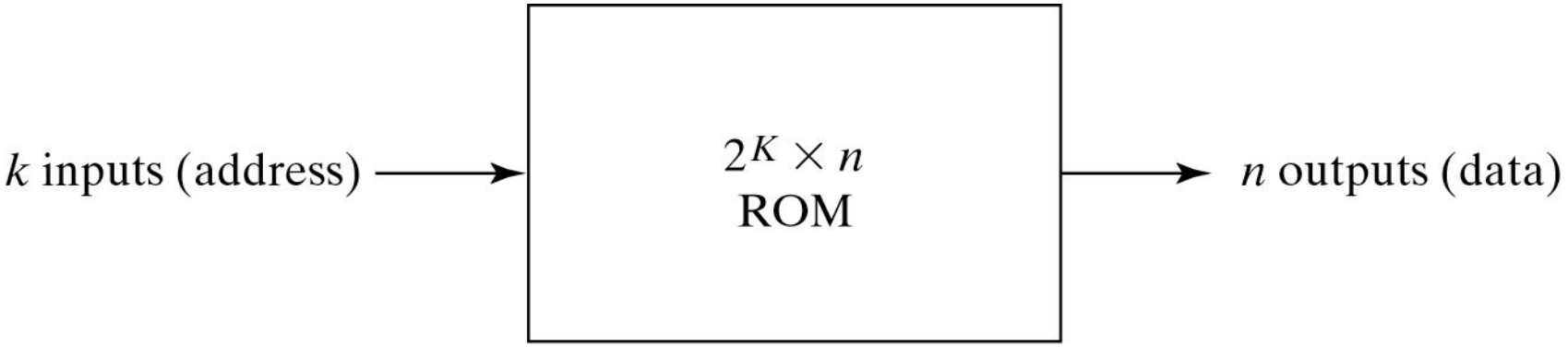
CAM

- Binary CAM Cell
  - ML pre-charged to V_{DD}
  - Match: ML remains at V_{DD}
  - Mismatch: ML discharges



Read-Only Memory

- A block diagram of a ROM is shown below. It consists of k address inputs and n data outputs.
- The number of words in a ROM is determined from the fact that k address input lines are needed to specify 2^k words.



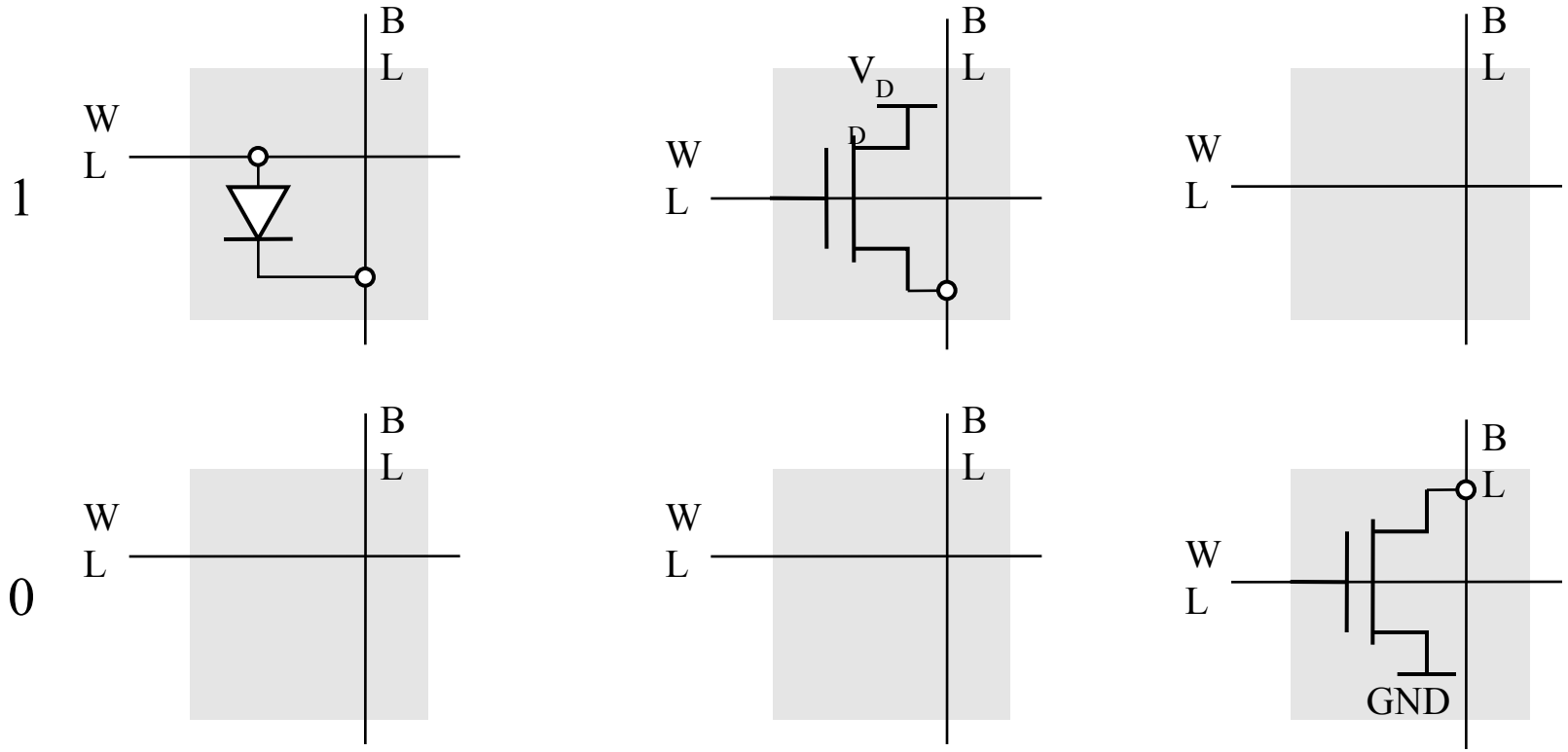
ROM Block diagram 2^k xn Module

Read-Only Memory Cells

Bit line (BL) is resistively clamped to the ground, so its default value is 0

Diode disadvantage – no electrical isolation between bit and word lines

BL is resistively clamped to VDD, so its default value is 1



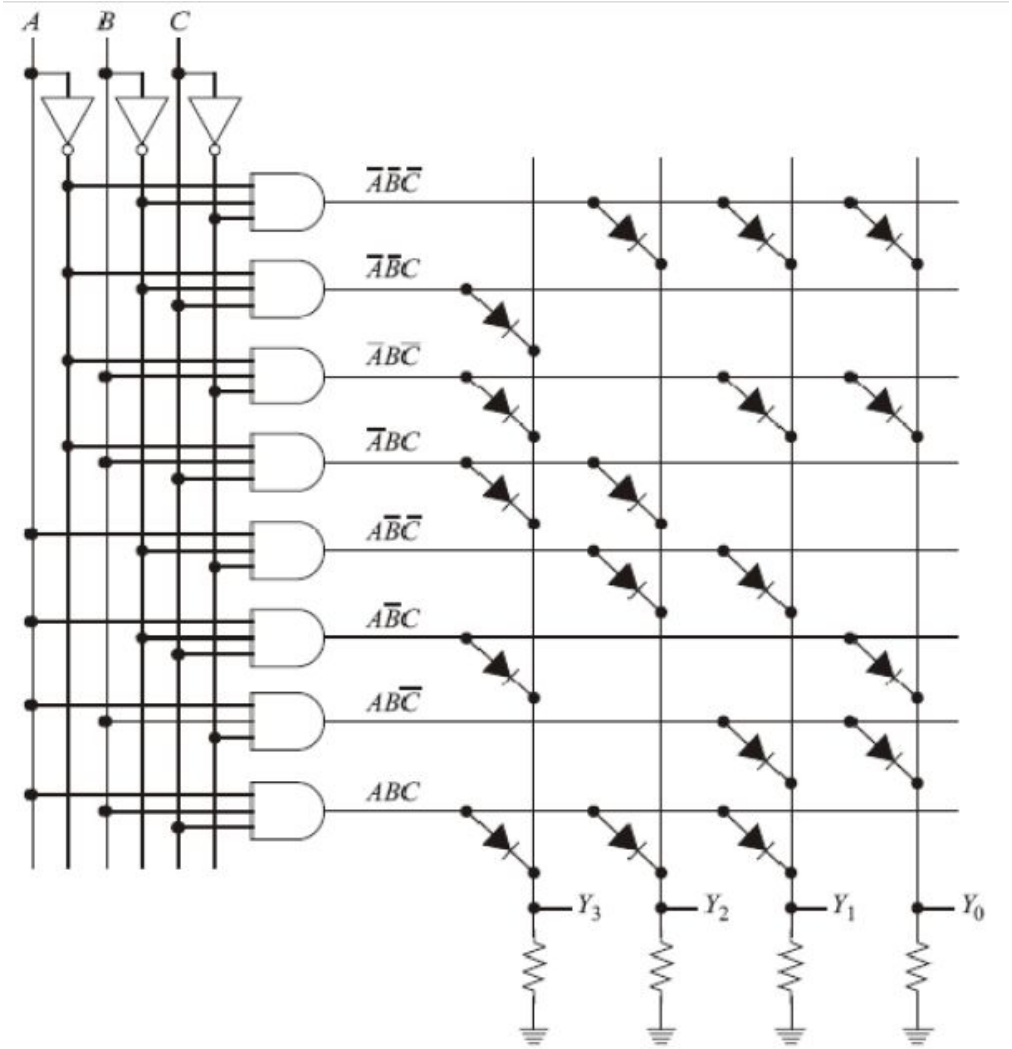
Diode ROM

MOS ROM 1

MOS ROM 2

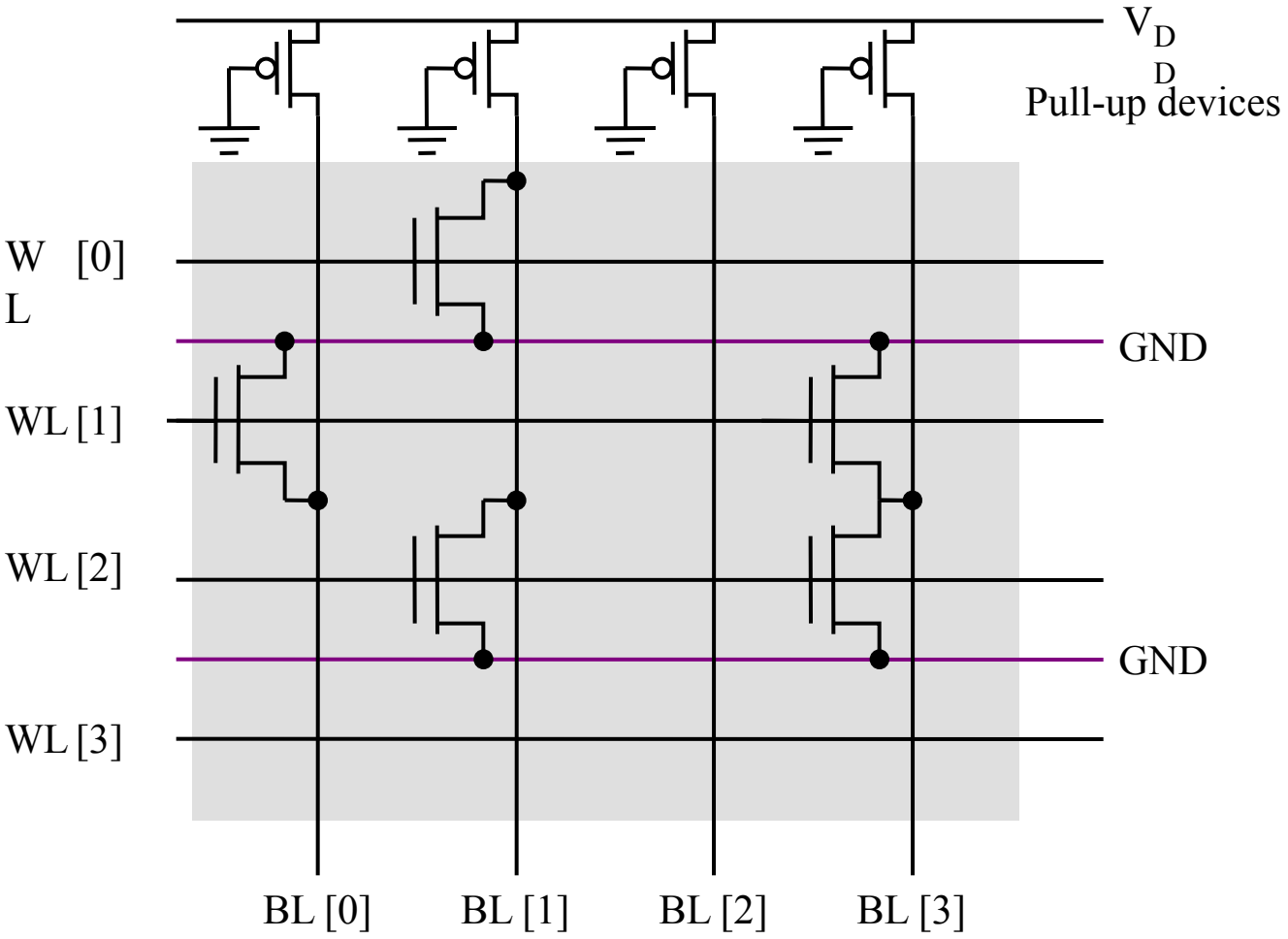
Nonvolatile Memory

ROM
PROM
EPROM

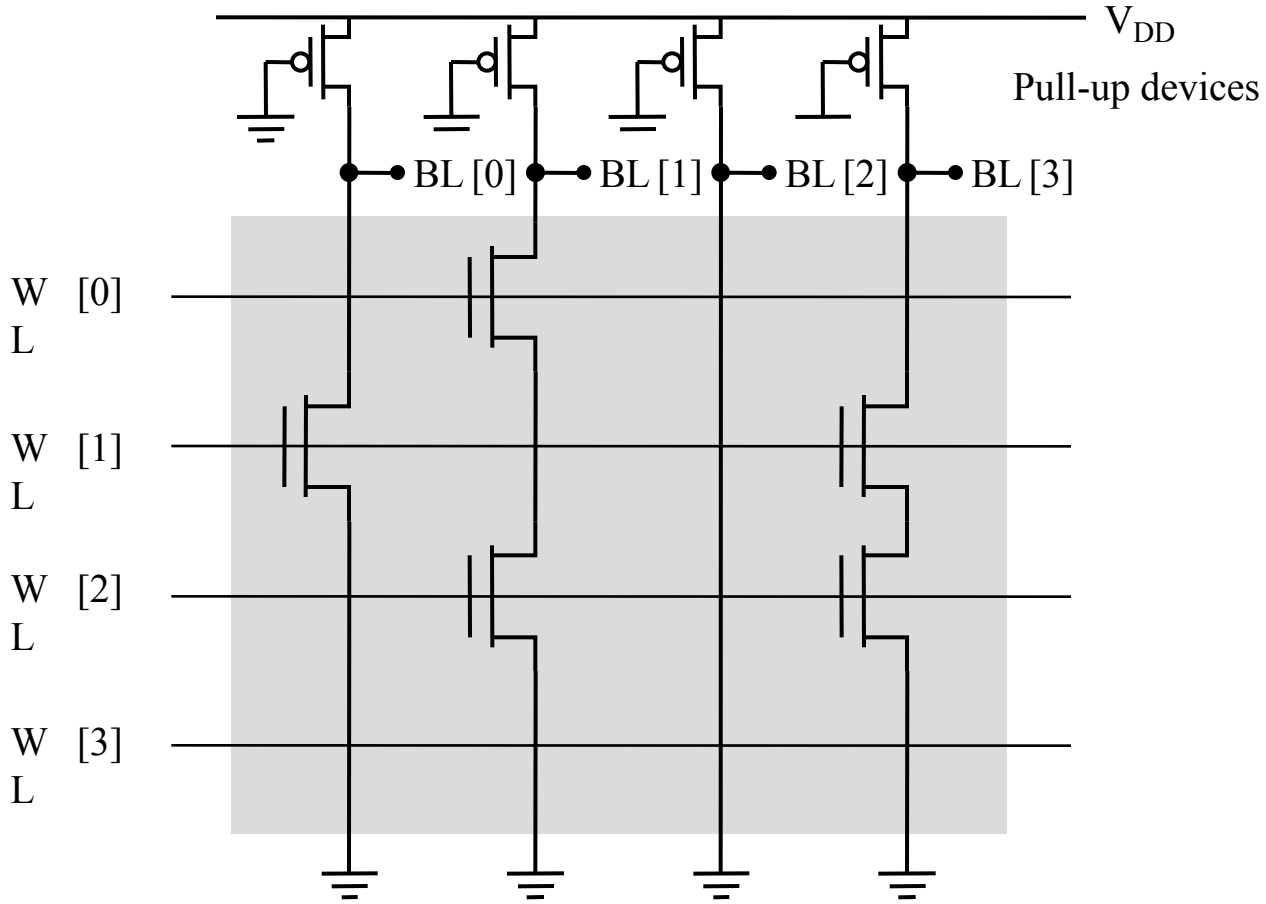


Read-only memory organization, with the fixed contents shown on the right.

MOS NOR ROM

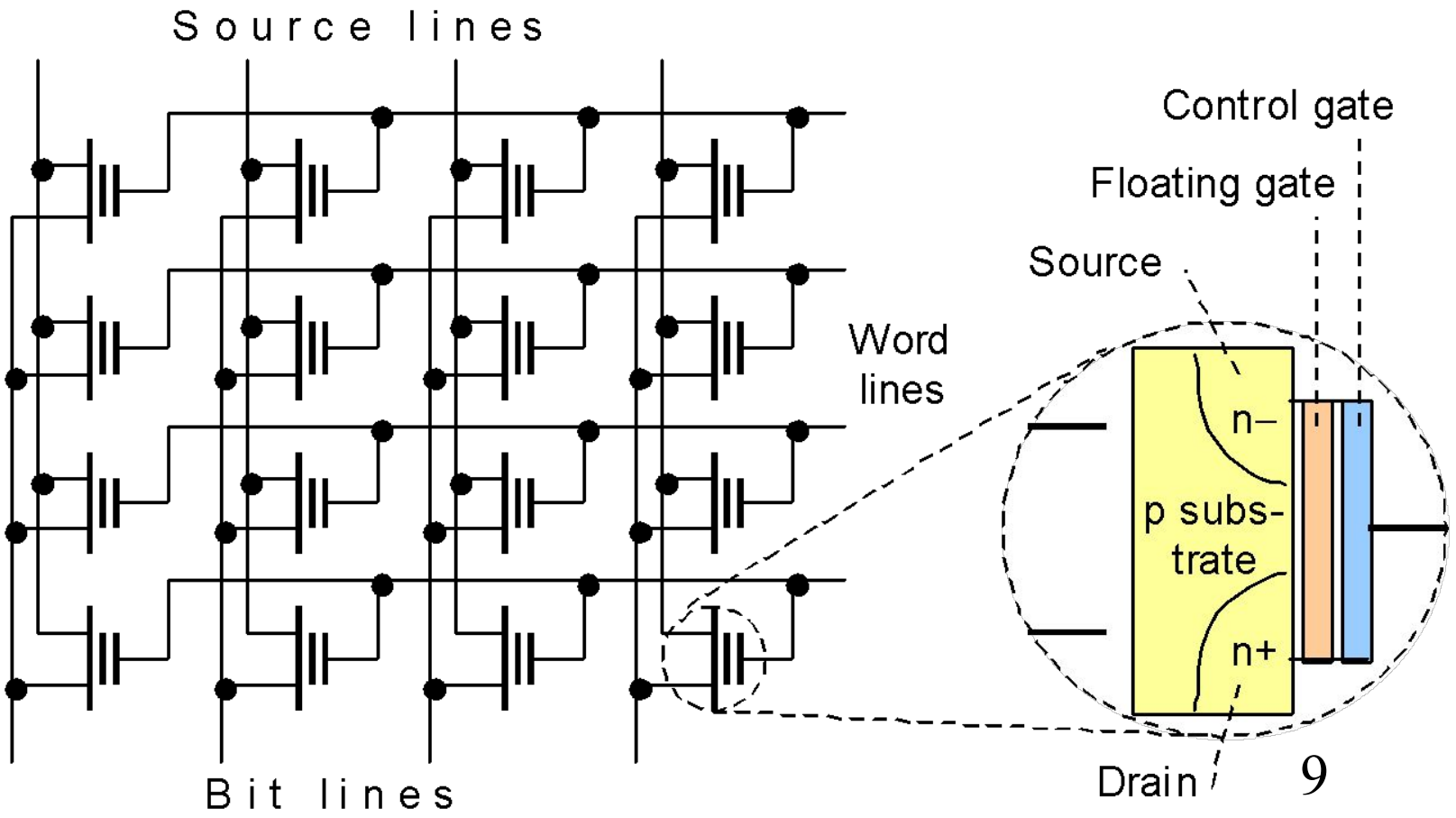


MOS NAND ROM



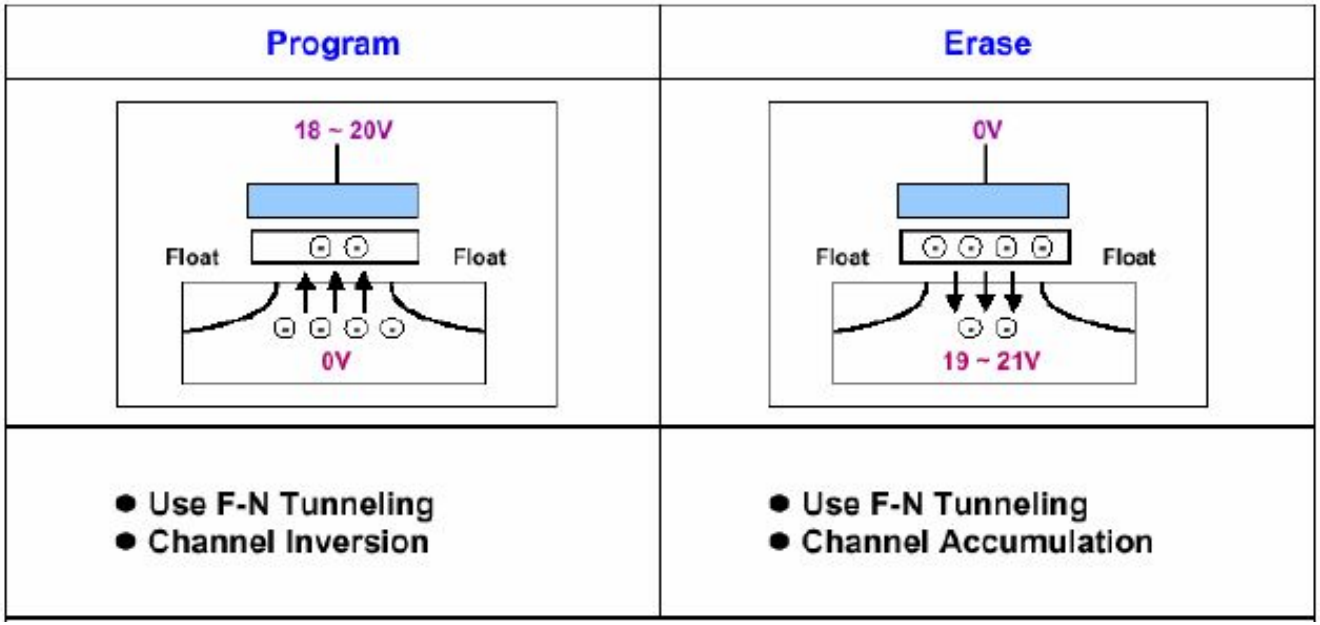
All word lines high by default with exception of selected row

Flash Memory

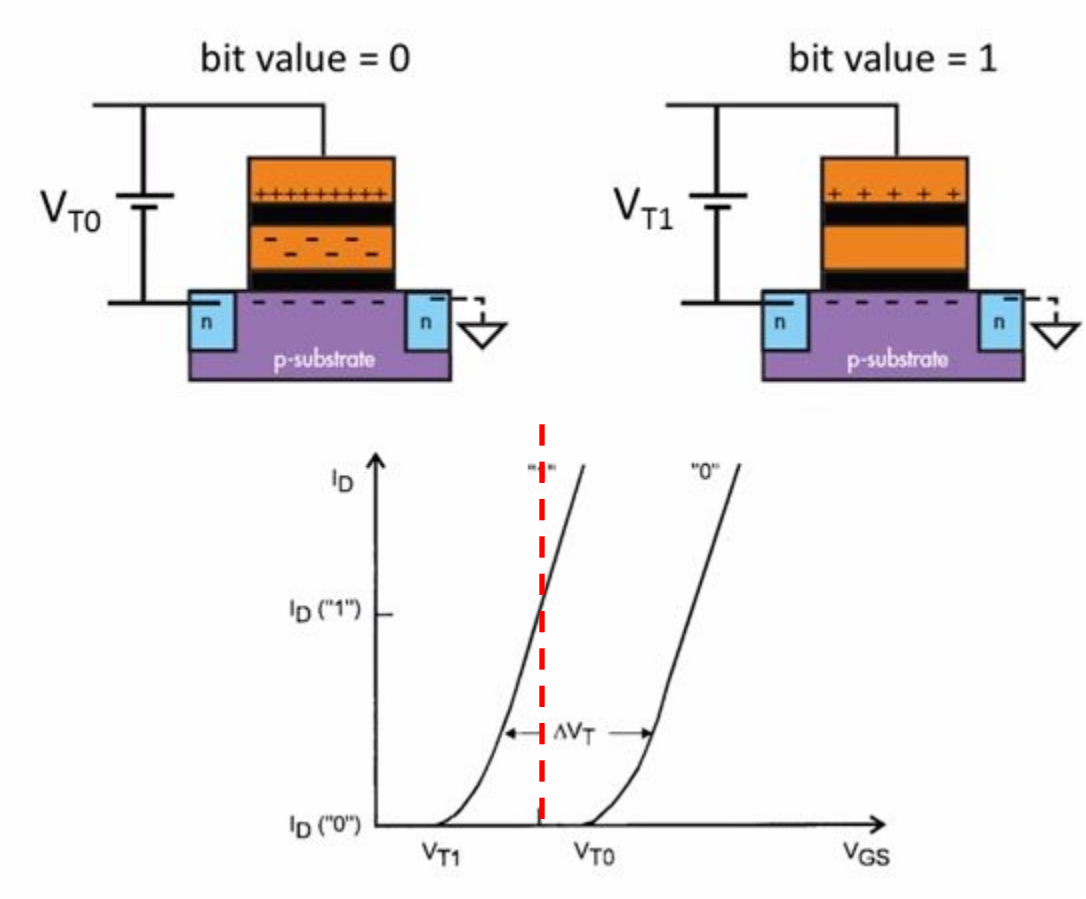


Flash memory

- Flash memory
  - Non volatile read only memory (ROM)
  - Erase Electrically or UV (EPROM)
  - Uses F-N tunneling for program & erase
  - Reads like DRAM (~ns)
  - Writes like DISK (~ms).

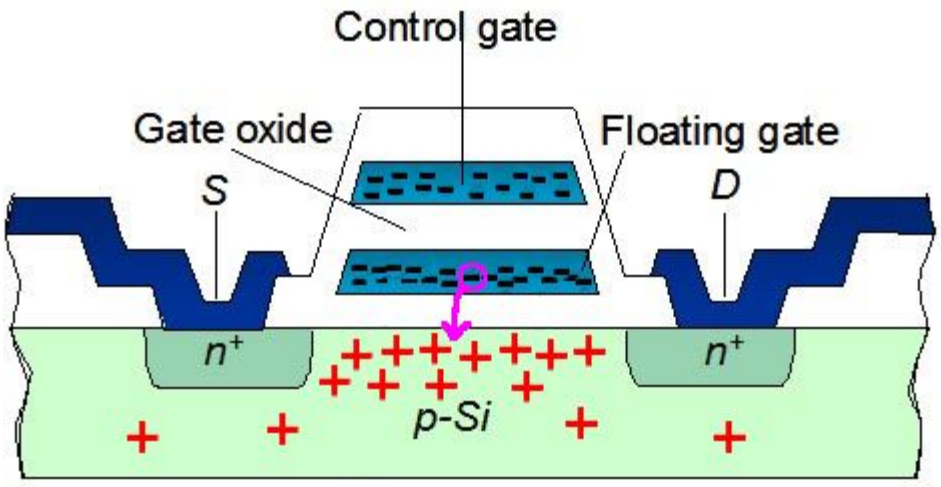


Reading Memory State



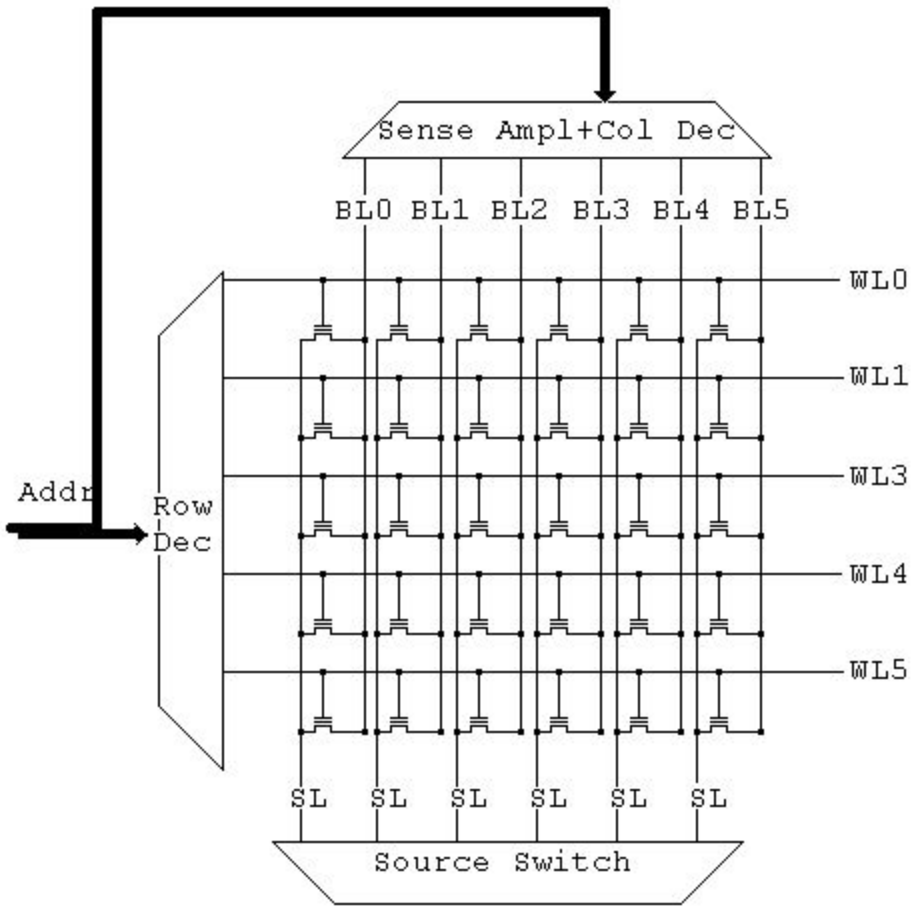
Change in Threshold Voltage due to **Screening Effect** of Floating Gate
Read mode: Apply intermediate voltage, check whether current is flowing or not

Writing Memory State



Control gate voltage determines whether electrons are injected to, or push/pulled out of floating gate.

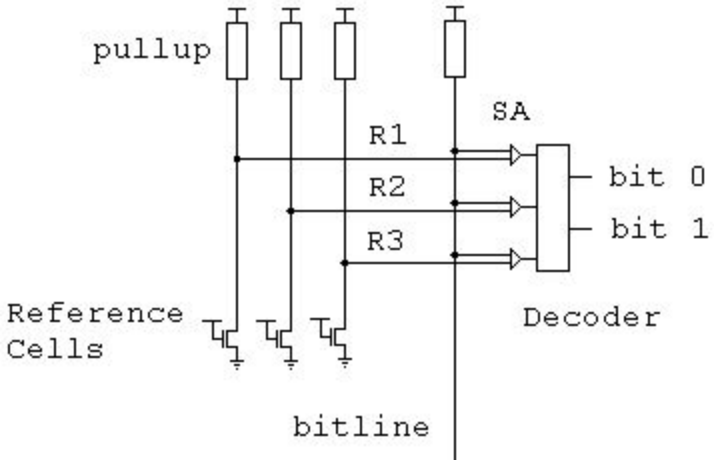
NOR Array



Reading:

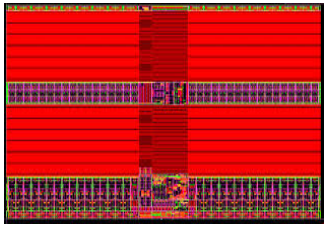
Assert a single word line. The source lines are asserted and the read of the bitline gives the contents of the cell.

Multi-Levels



- By using reference cells set at given levels and comparing them to the value from the bitline, we can determine the value stored.

Review of memory technologies



Memory type	SRAM	DRAM	Flash
Speed	Very fast	Slow	Slow
Density	Low	High	Very high
Power	High	Low	Very low
Refresh	No	Yes	No
Mechanism	Bi-stable latch	Capacitor	FN tunneling