INDIAN INSTITUTE OF TECHNOLOGY PATNA

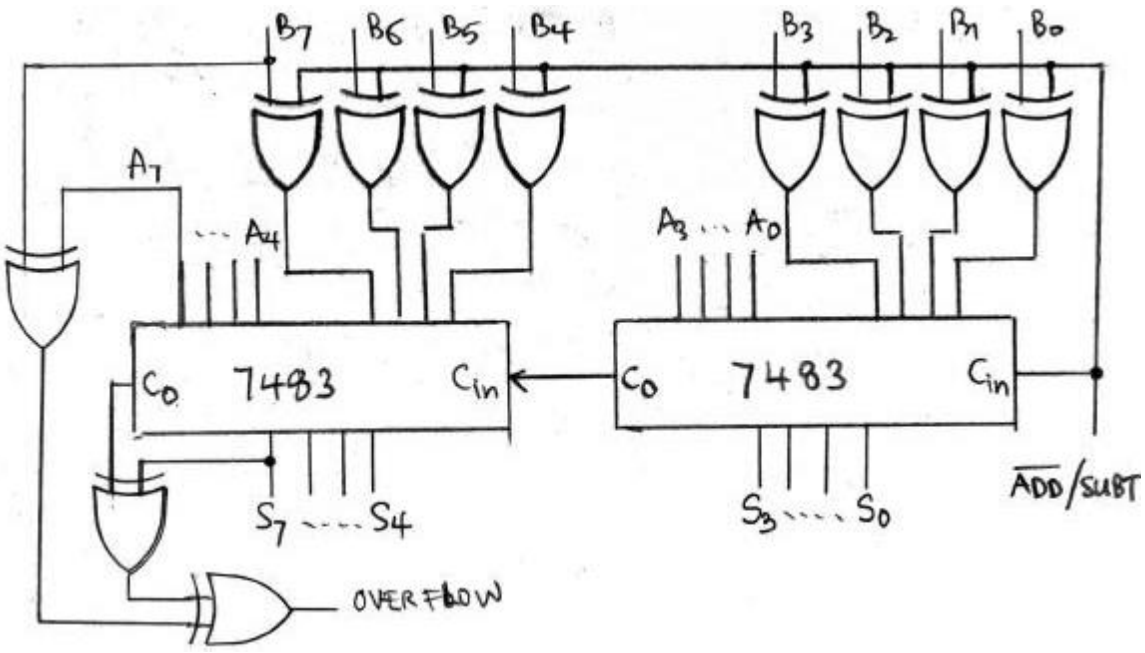
CS226-Hardware Lab

Lab 5

1. To implement a binary full-adder with a dual 4-to-1-line multiplexer and a single inverter. Simulate using Logic-sim before doing the actual implementation.

(10 points)

2. Study 7483 and design an 8-bit adder/subtractor with overflow detection using 7483s. (Simulate using Logic-sim before doing the actual implementation)



(40 points)