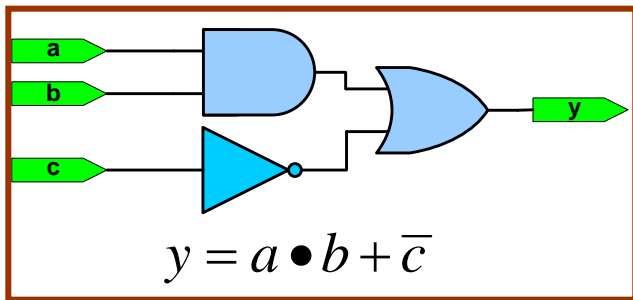


Example :Configuring LUT

- LUT is a RAM with data width of 1bit.
- The contents are programmed at power up

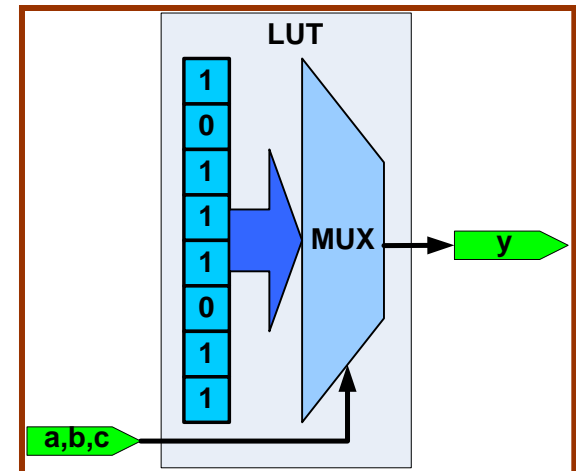
Required Function



Truth Table

| a | b | c | y |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

Programmed LUT

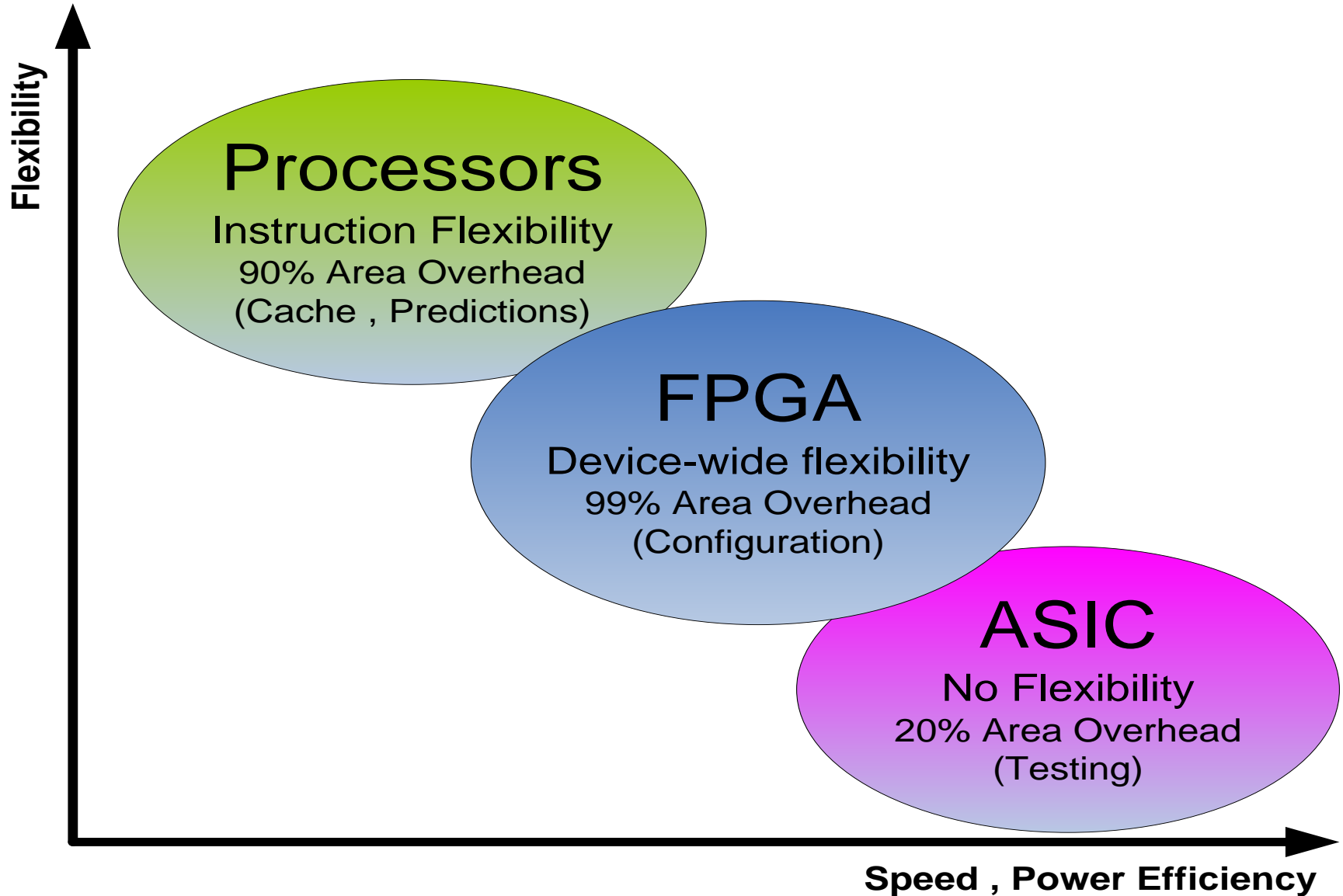


FPGA Principles

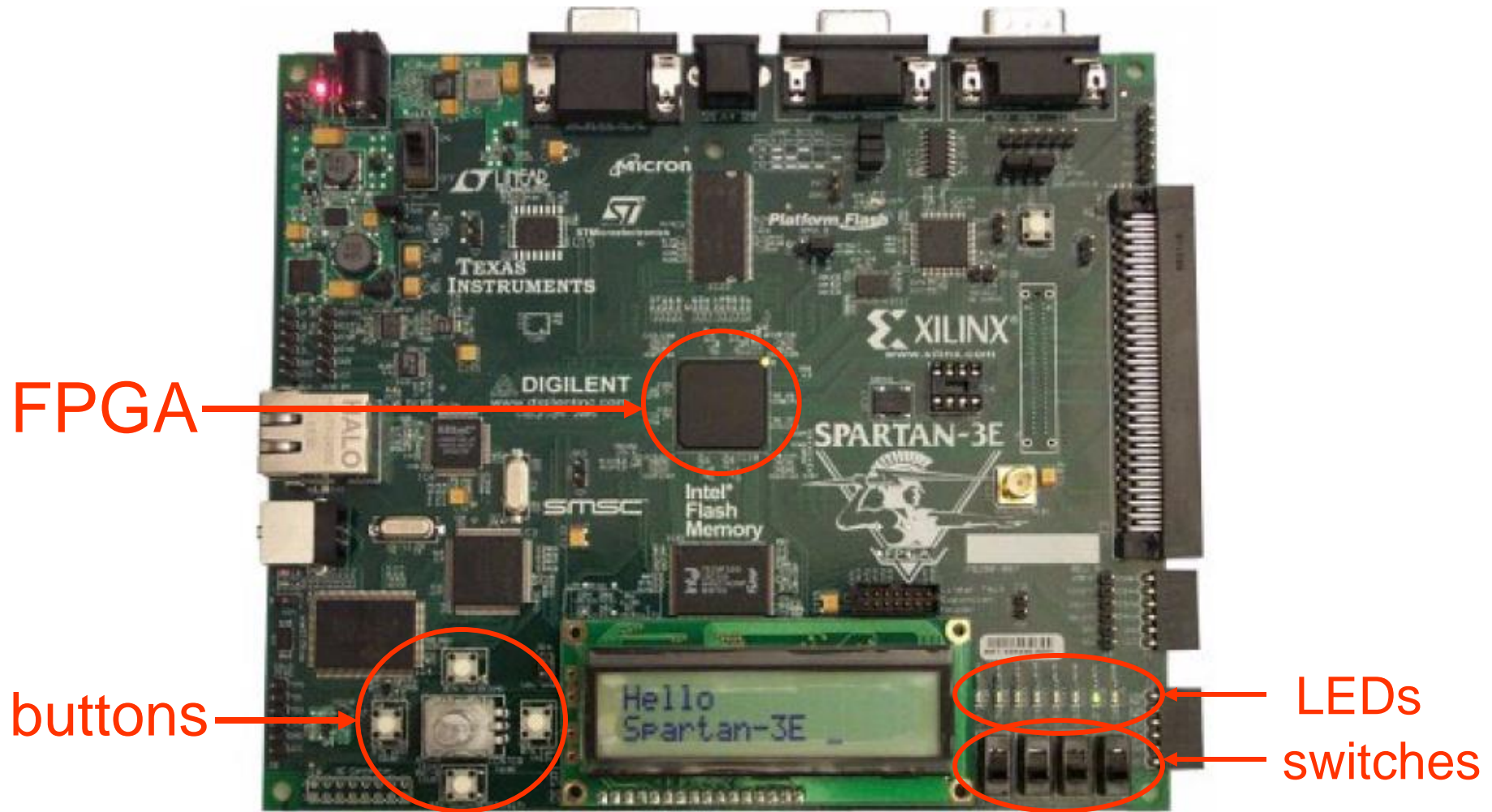
- A Field-Programmable Gate Array (FPGA) is an integrated circuit that can be configured by the user to emulate any digital circuit as long as there are enough resources
- An FPGA can be seen as an array of Configurable Logic Blocks (CLBs) connected through programmable interconnect (Switch Boxes)



Comparison



Xilinx Spartan-3E Starter Kit

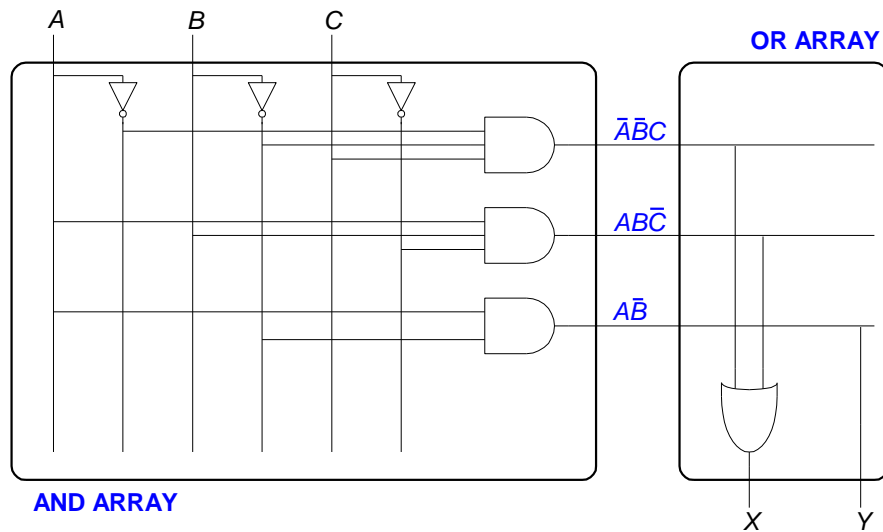
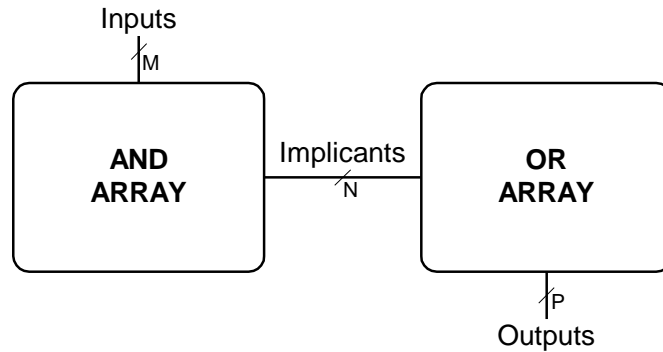


Logic Arrays

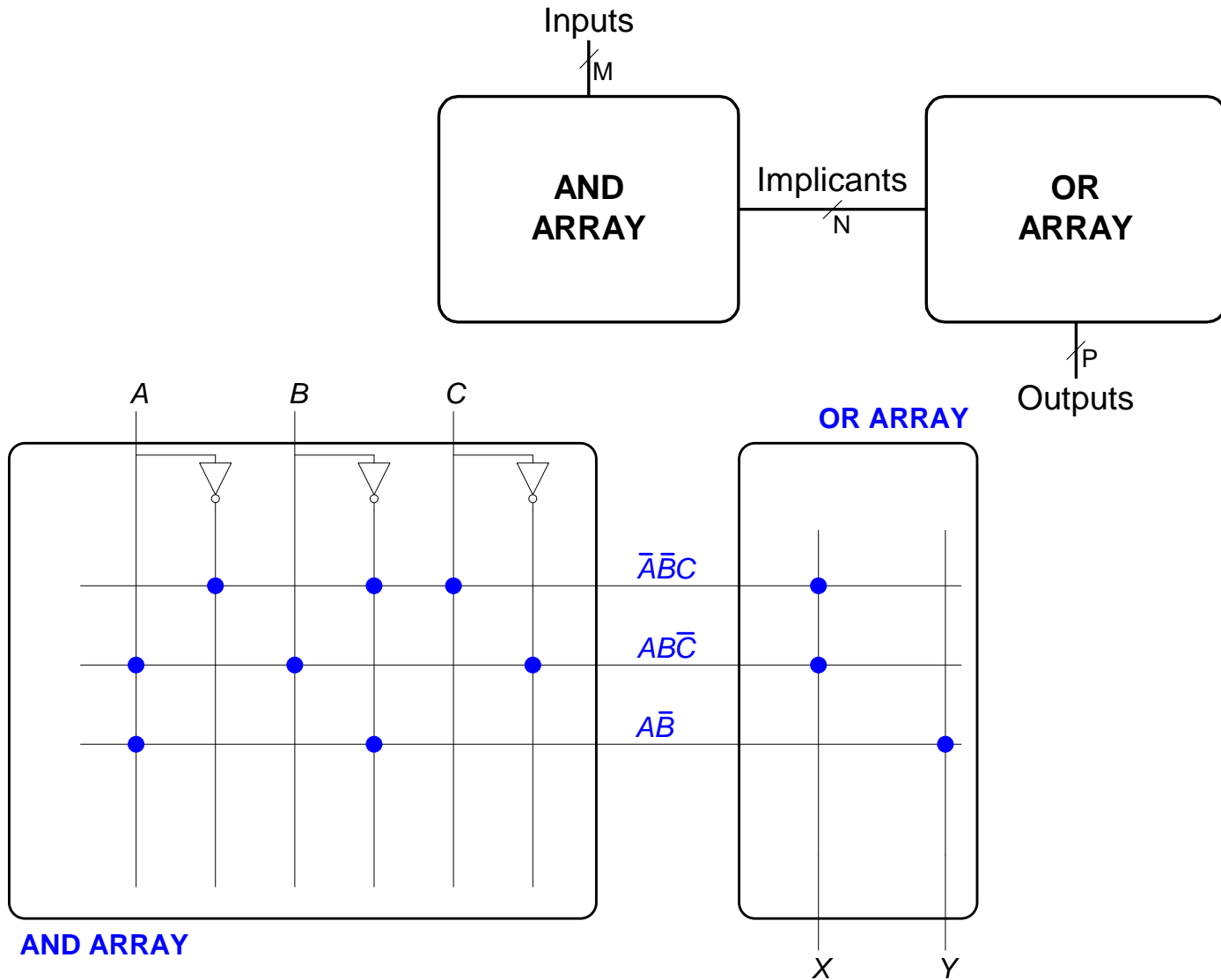
- Programmable logic arrays (PLAs)
 - AND array followed by OR array
 - Perform combinational logic only
 - Fixed internal connections
- Field programmable gate arrays (FPGAs)
 - Array of configurable logic blocks (CLBs)
 - Perform combinational and sequential logic
 - Programmable internal connections

PLAs

- $X = \bar{A}\bar{B}C + AB\bar{C}$
- $Y = A\bar{B}$



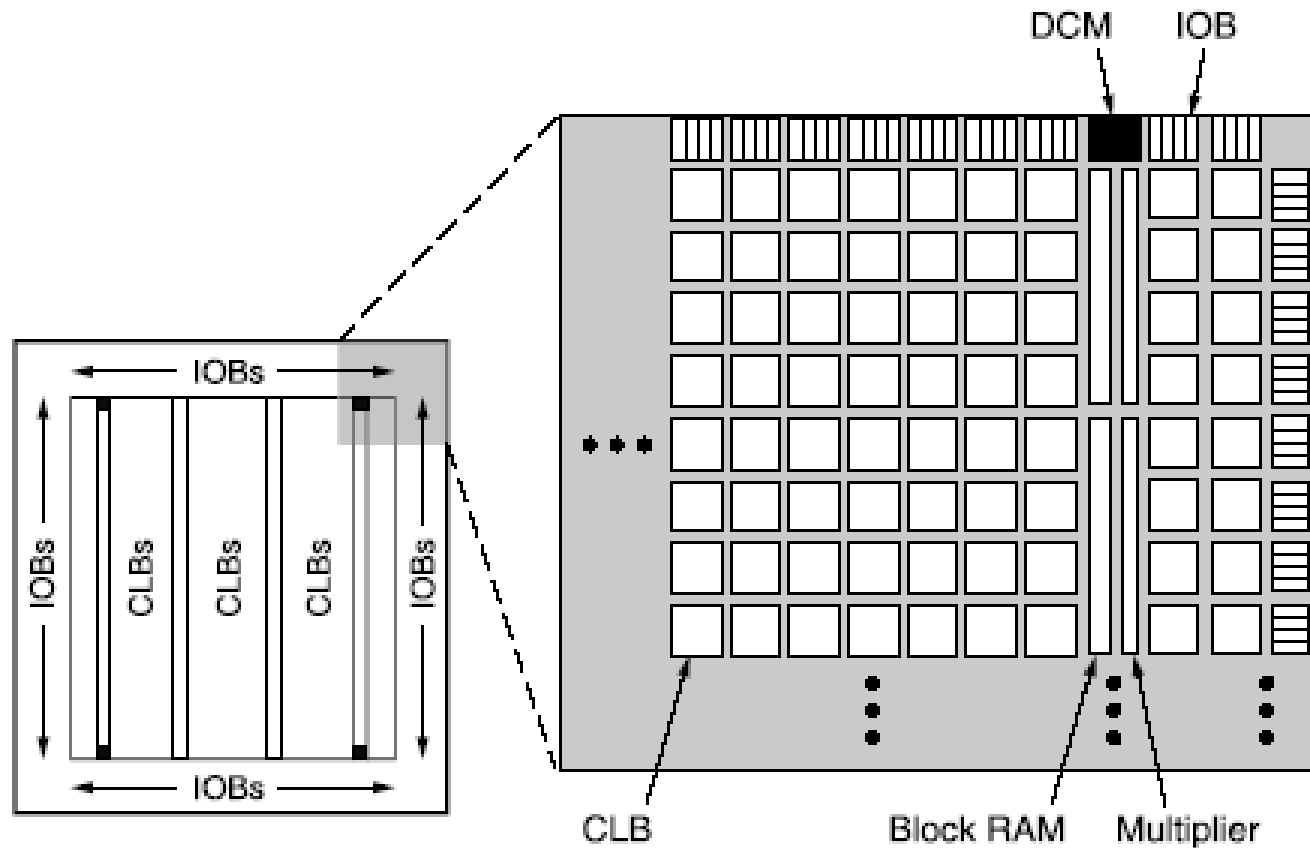
PLAs: Dot Notation



FPGAs: Field Programmable Gate Arrays

- Composed of:
 - **CLBs** (Configurable logic blocks): perform logic
 - **IOBs** (Input/output buffers): interface with outside world
 - **Programmable interconnection**: connect CLBs and IOBs
 - Some FPGAs include other building blocks such as multipliers and RAMs

Xilinx Spartan 3 FPGA Schematic

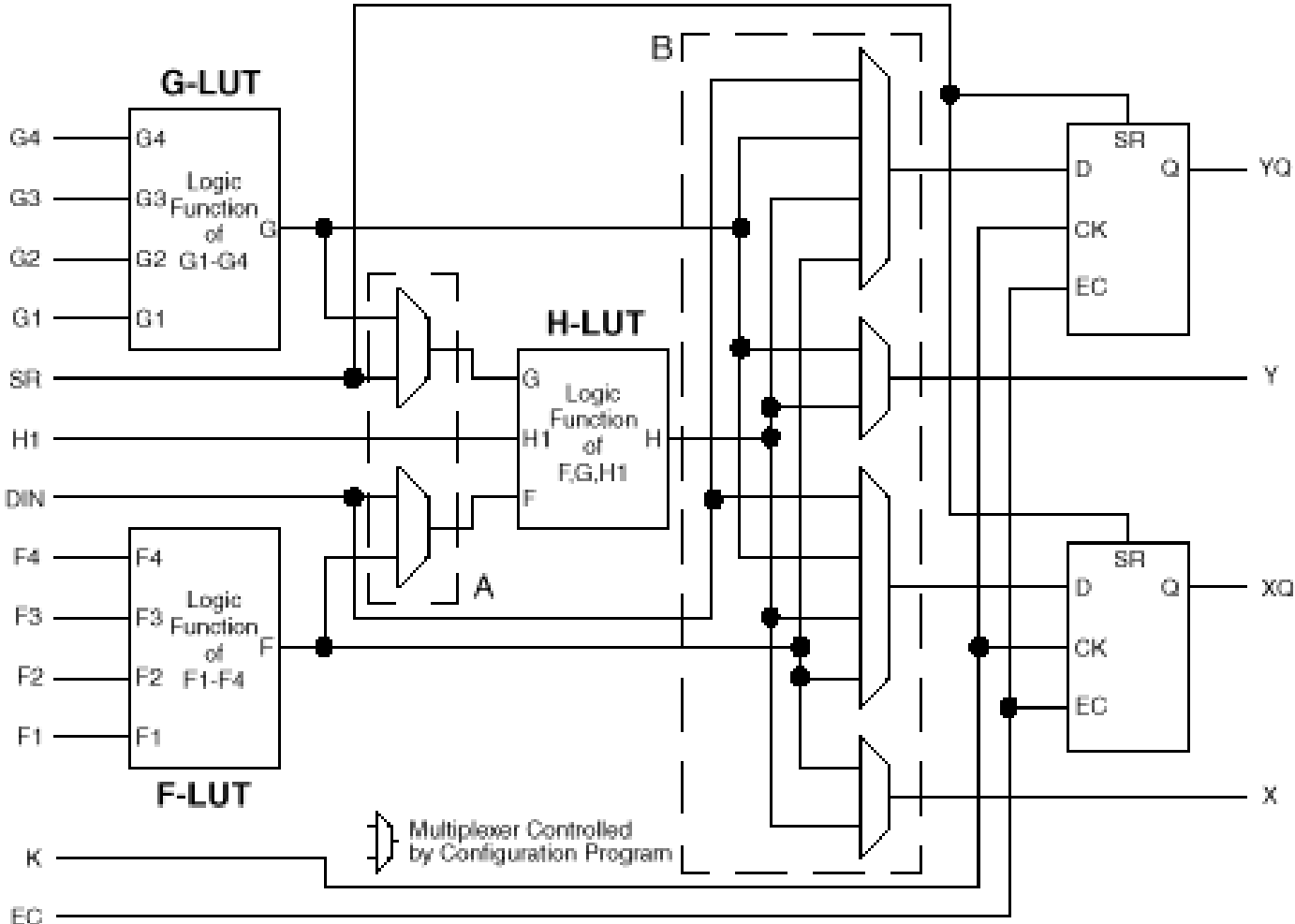


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CLBs: Configurable Logic Blocks

- Composed of:
 - LUTs (lookup tables): perform combinational logic
 - Flip-flops: perform sequential functions
 - Multiplexers: connect LUTs and flip-flops

Xilinx Spartan CLB

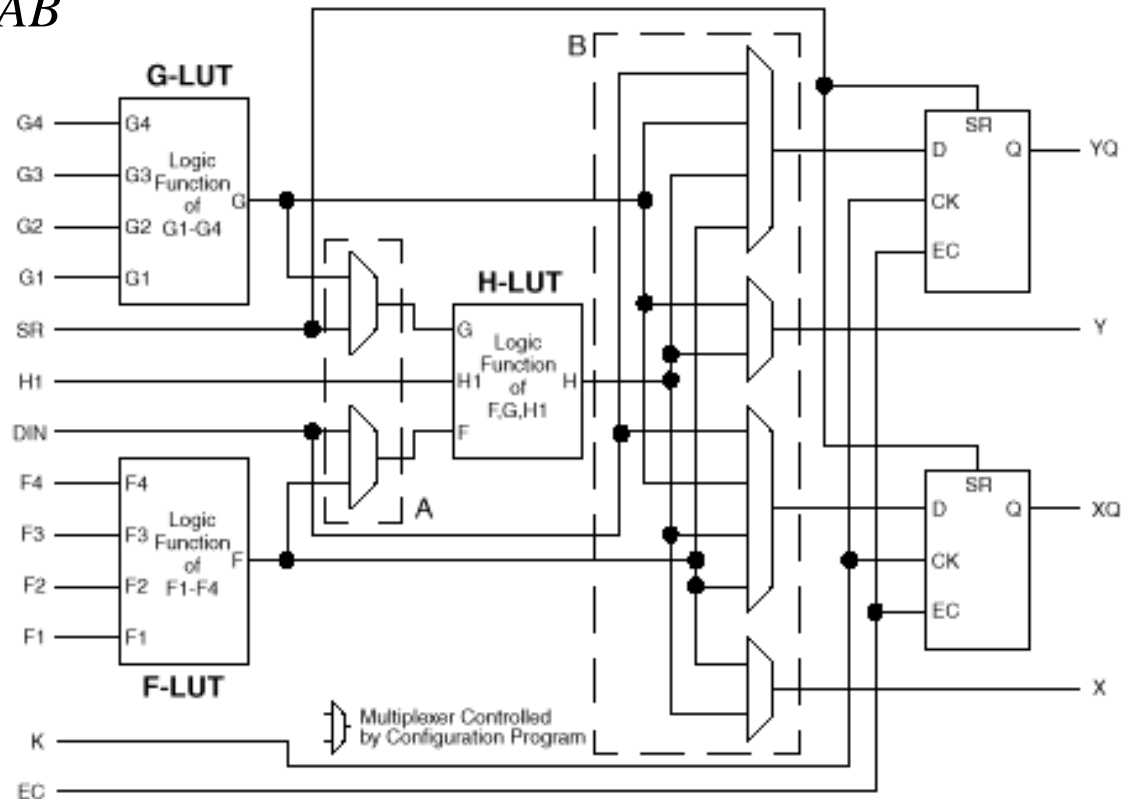


Xilinx Spartan CLB

- The Spartan CLB has:
 - 3 LUTs:
 - F-LUT (2^4 x 1-bit LUT)
 - G-LUT (2^4 x 1-bit LUT)
 - H-LUT (2^3 x 1-bit LUT)
 - 2 registered outputs:
 - XQ
 - YQ
 - 2 combinational outputs:
 - X
 - Y

CLB Configuration Example

- Show how to configure the Spartan CLB to perform the following functions:
 - $X = \overline{A}BC + A\overline{B}C$
 - $Y = A\overline{B}$

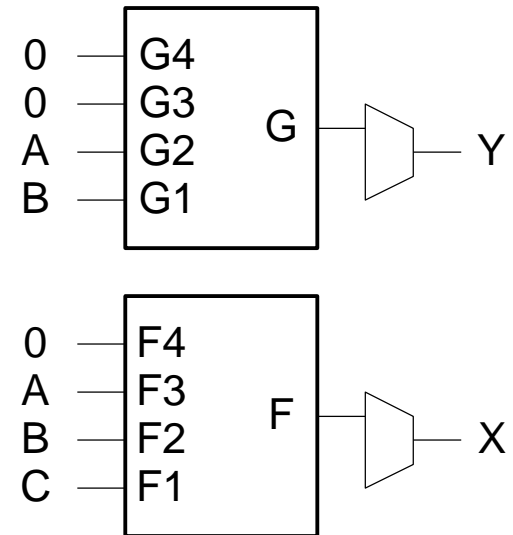


CLB Configuration Example

- Show how to configure the Spartan CLB to perform the following functions:
 - $X = \overline{A}\overline{B}C + A\overline{B}\overline{C}$
 - $Y = A\overline{B}$

| | (A) | (B) | (C) | (X) |
|----|-----|-----|-----|-----|
| F4 | F3 | F2 | F1 | F |
| X | 0 | 0 | 0 | 0 |
| X | 0 | 0 | 1 | 1 |
| X | 0 | 1 | 0 | 0 |
| X | 0 | 1 | 1 | 0 |
| X | 1 | 0 | 0 | 0 |
| X | 1 | 0 | 1 | 0 |
| X | 1 | 1 | 0 | 1 |
| x | 1 | 1 | 1 | 0 |

| | | (A) | (B) | (Y) |
|----|----|-----|-----|-----|
| G4 | G3 | G2 | G1 | G |
| X | X | 0 | 0 | 0 |
| X | X | 0 | 1 | 0 |
| X | X | 1 | 0 | 1 |
| X | X | 1 | 1 | 0 |



FPGA Design Flow

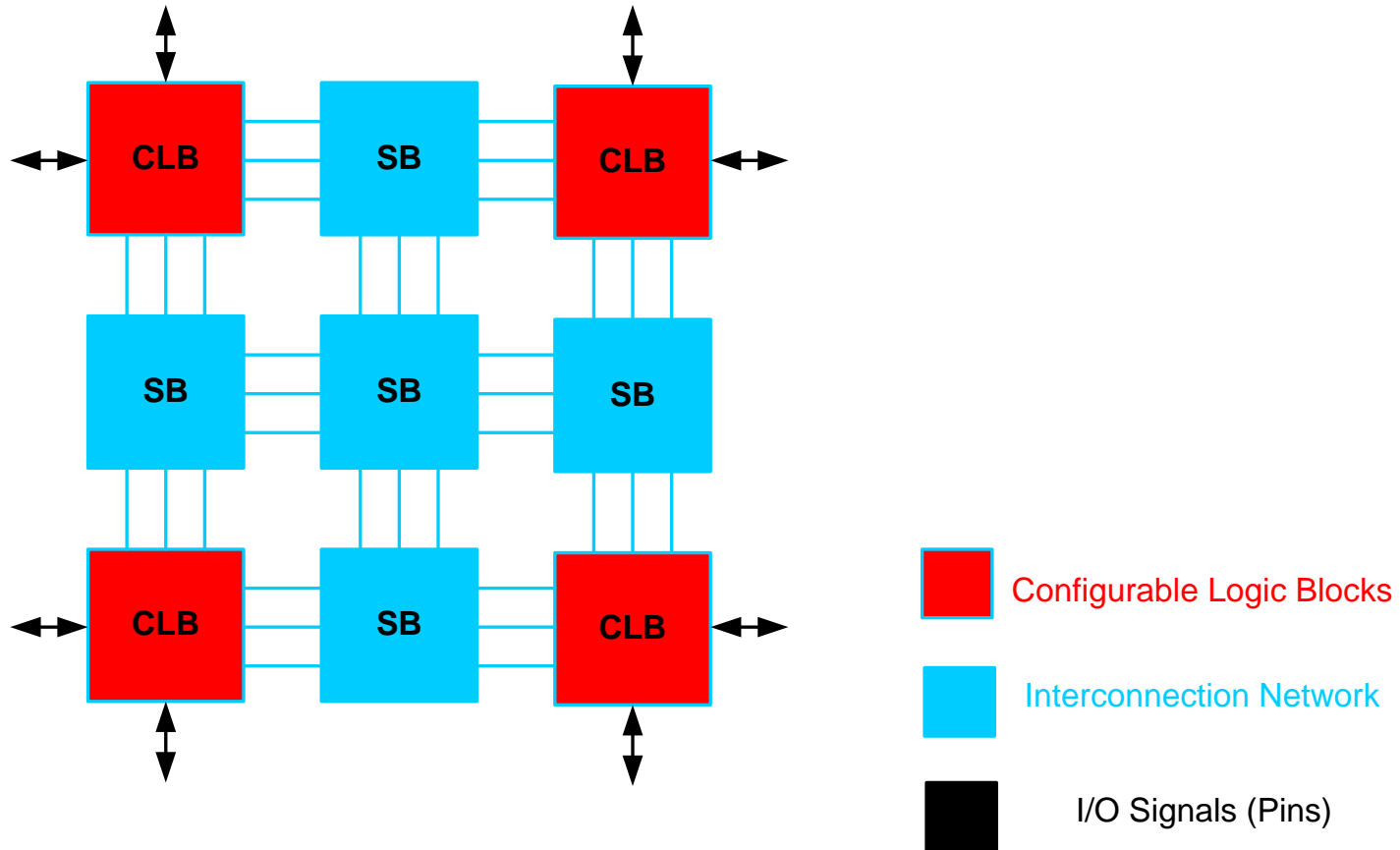
- A CAD tool (such as Xilinx Project Navigator) is used to design and implement a digital system. It is usually an iterative process.
- The user **enters the design** using schematic entry or an HDL(verilog).
- The user **simulates** the design.
- A **synthesis** tool converts the code into hardware and maps it onto the FPGA.
- The user uses the CAD tool to **download the configuration** onto the FPGA
- This configures the CLBs and the connections between them and the IOBs.

Manufacturers

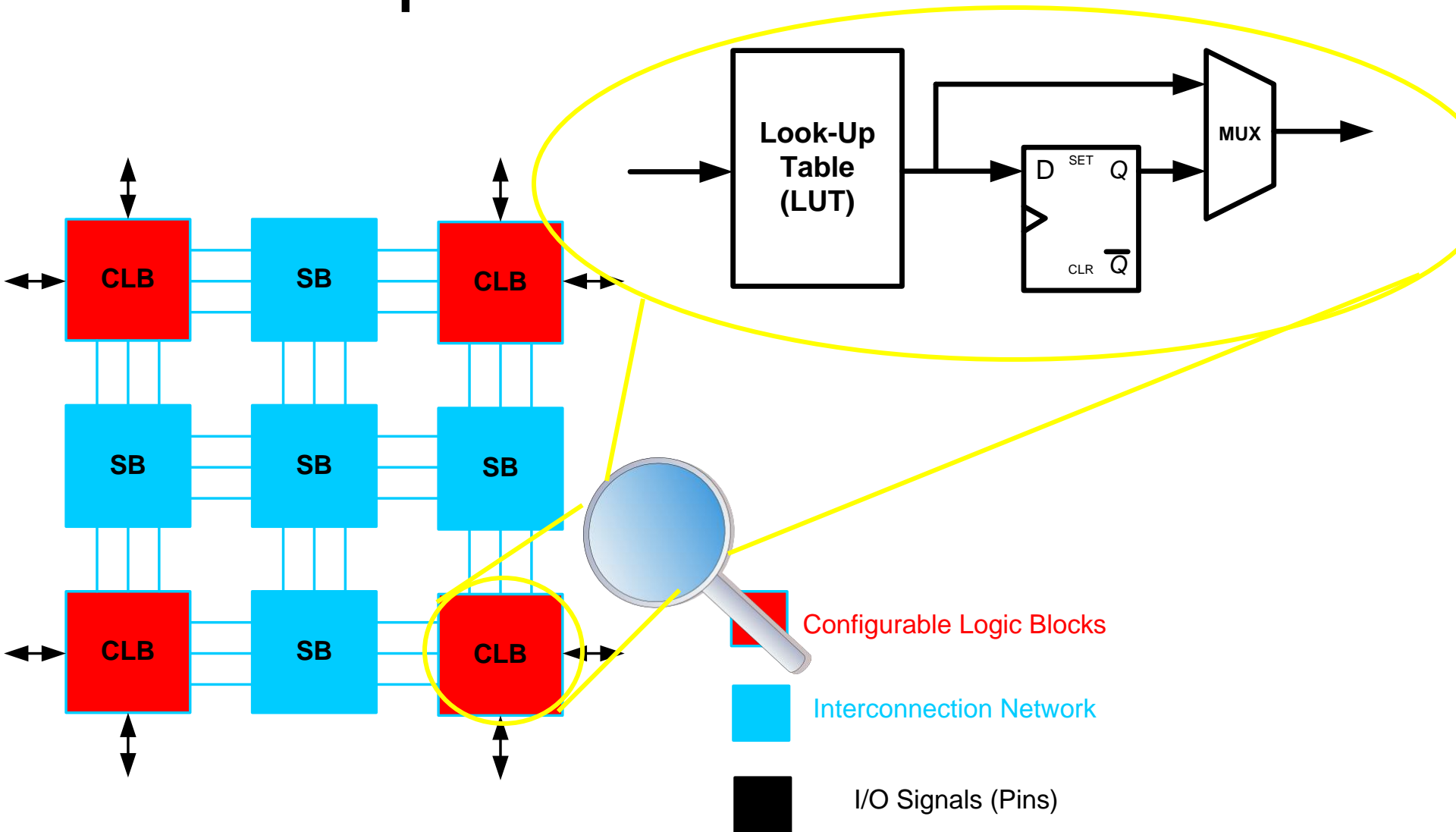
- Xilinx
- Altera
- Lattice
- Actel



FPGA structure



Simplified CLB Structure



[illegible]