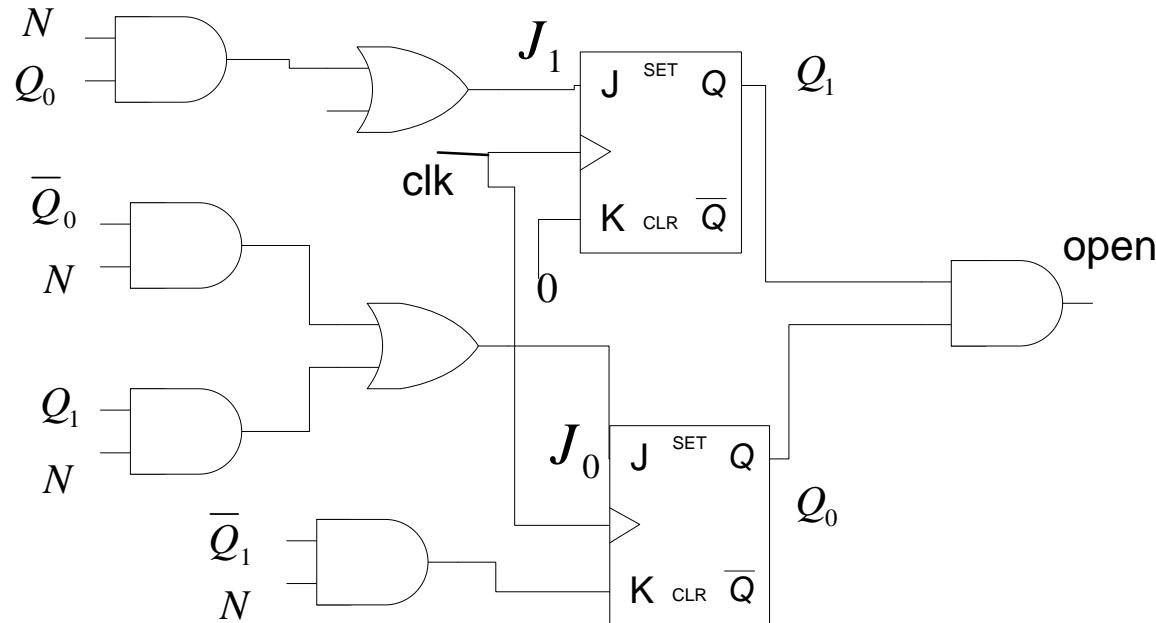


Timing

Vending Machine- J-K flip flops implementation



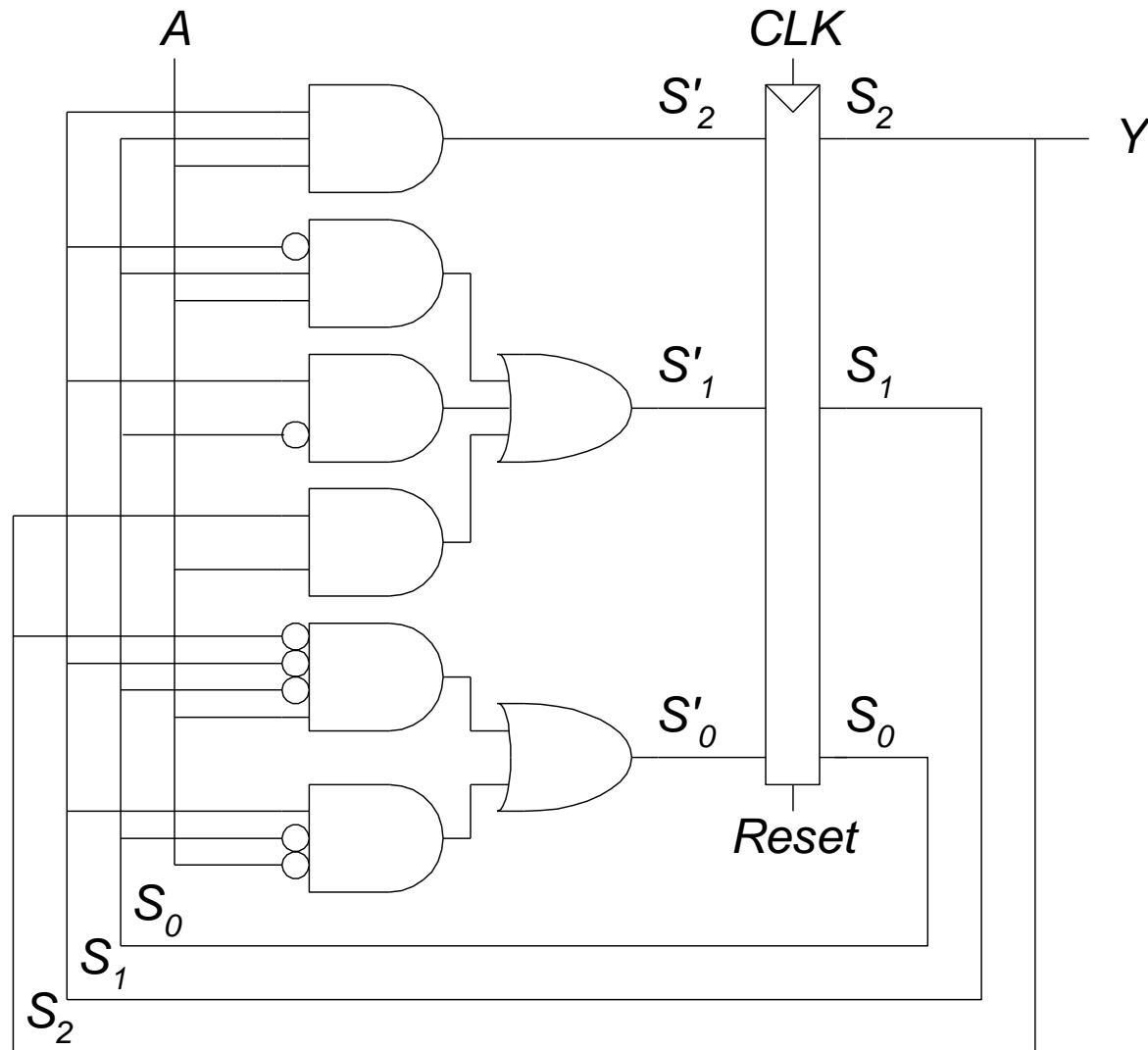
$$J_1 = D + Q_0 \cdot N$$

$$J_0 = Q_1' \cdot N + Q_1 \cdot D$$

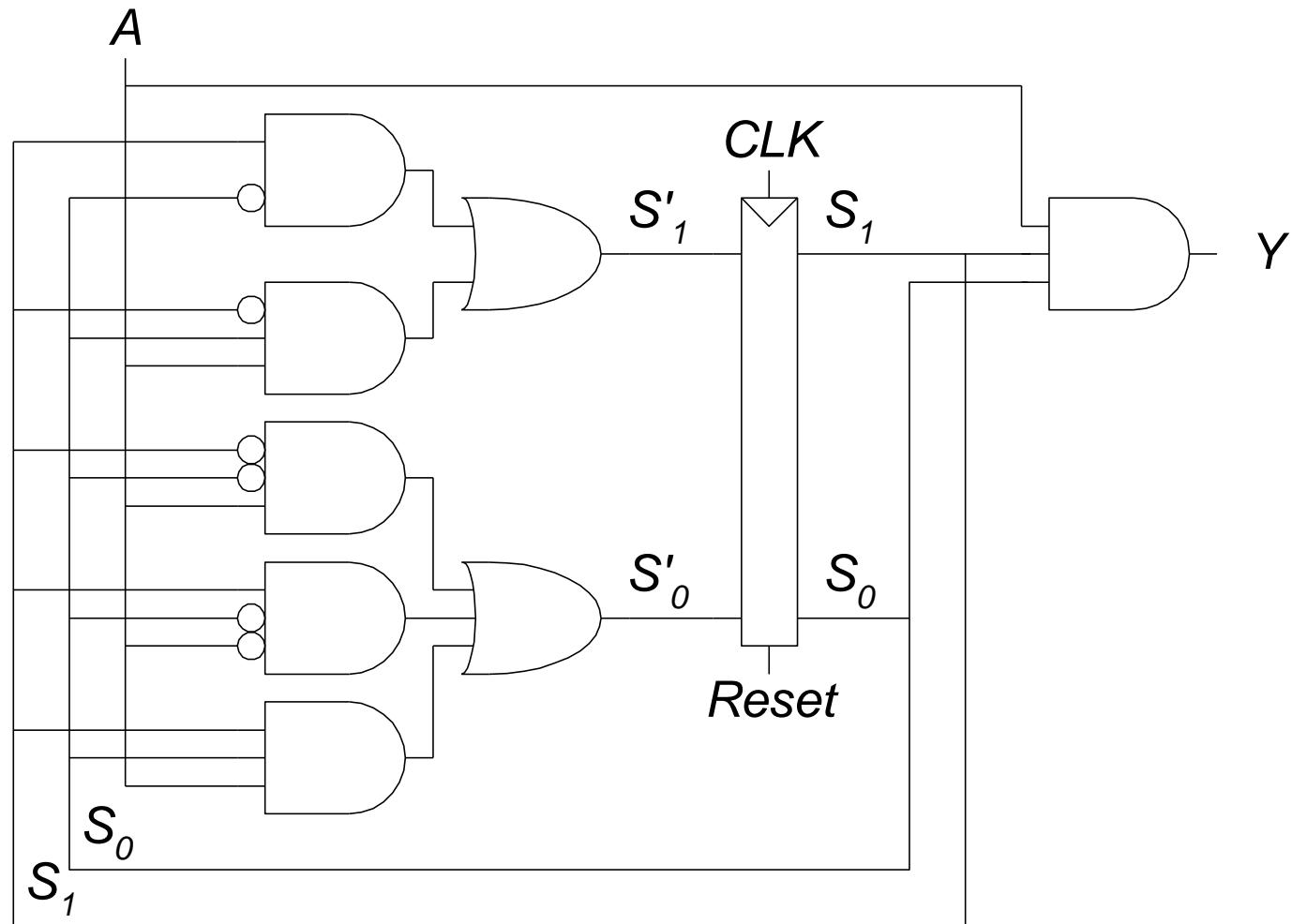
$$K_1 = 0$$

$$K_0 = Q_1' \cdot N$$

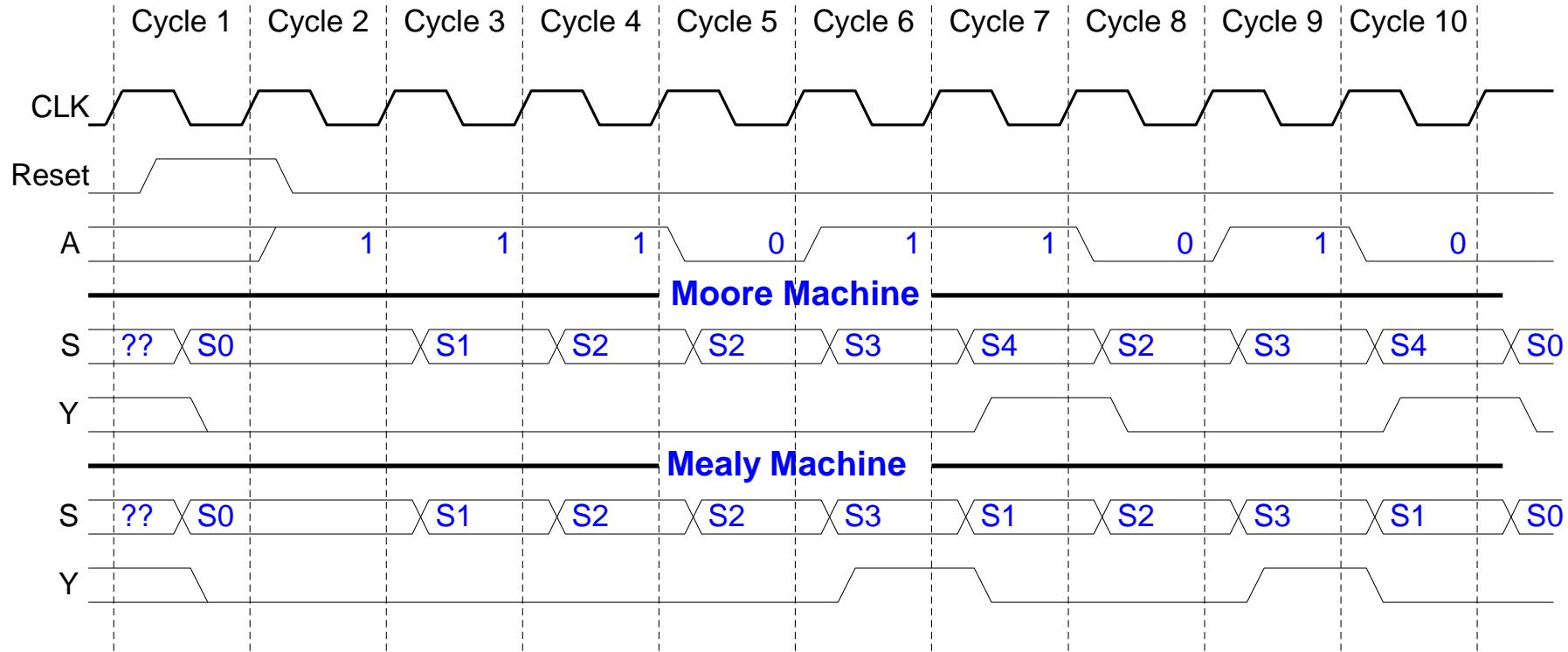
Moore FSM Schematic



Mealy FSM Schematic

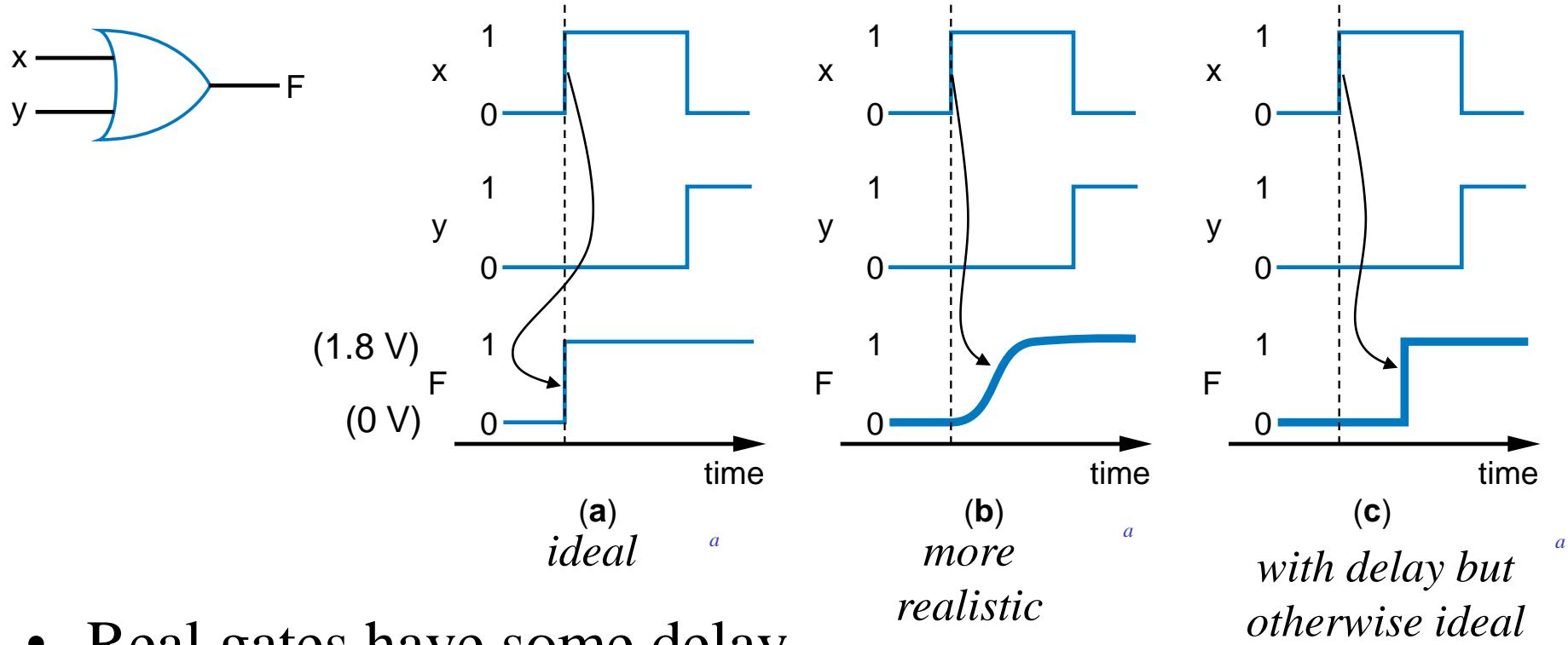


Moore and Mealy Timing Diagram



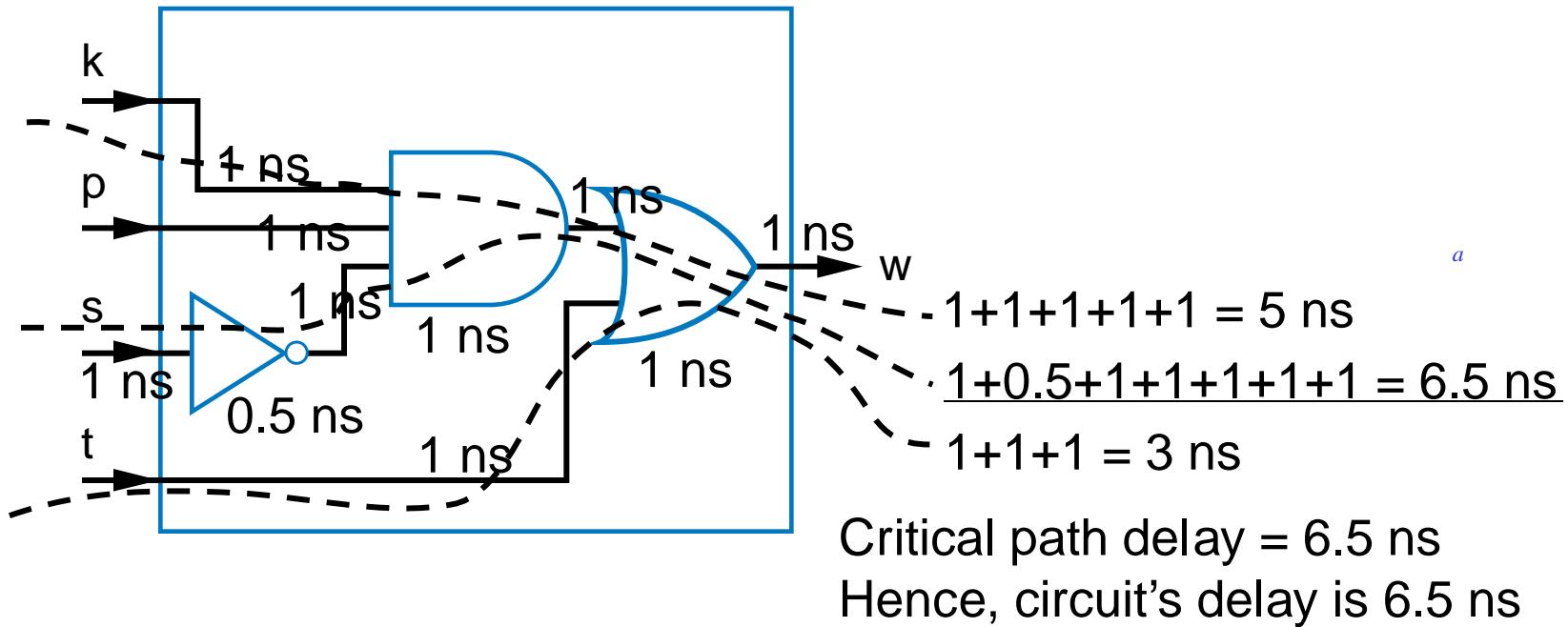
Additional Considerations

Non-Ideal Gate Behavior -- Delay



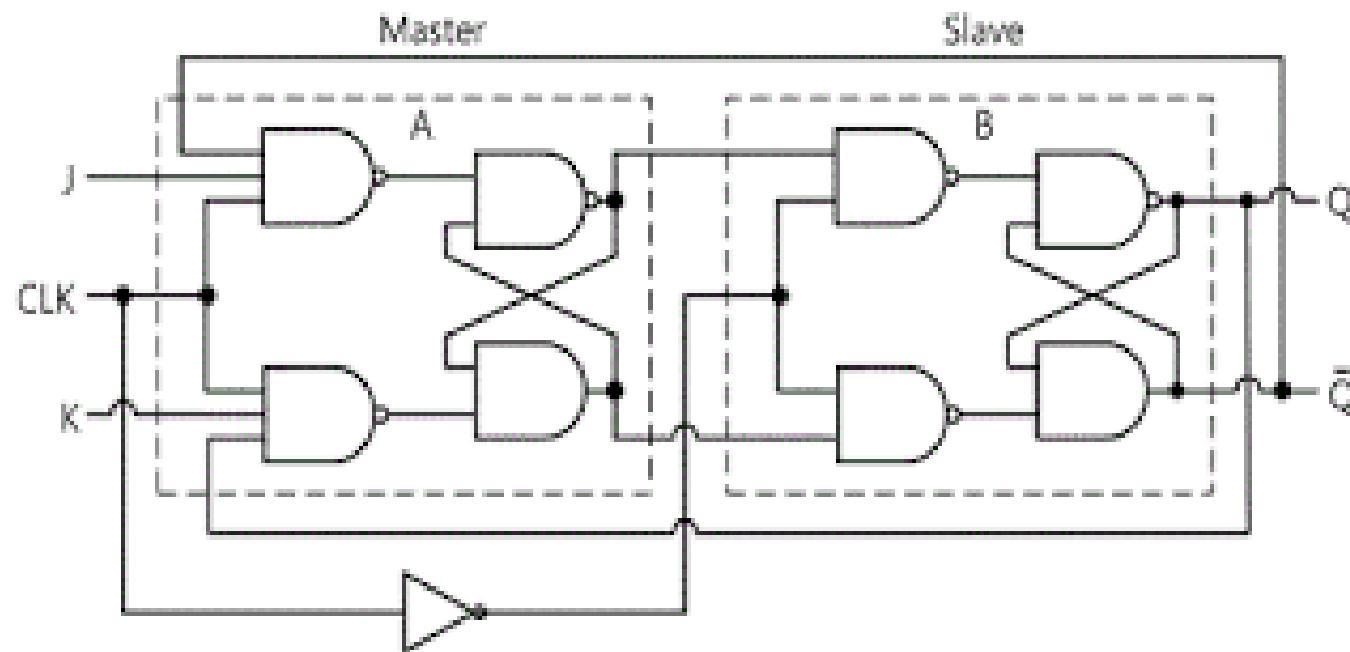
- Real gates have some delay
 - Outputs don't change immediately after inputs change

Circuit Delay and Critical Path



- Wires also have delay
- Assume gates and wires have delays as shown
- Path delay – time for input to affect output
- Critical path – path with longest path delay
- Circuit delay – delay of critical path

J-K Flip Flop

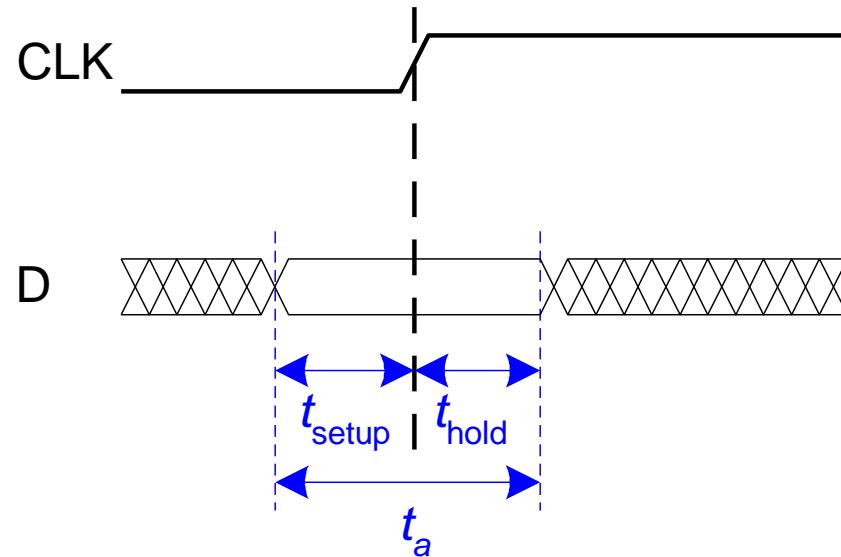


Timing

- Flip-flop samples D at clock edge
- D must be stable when it is sampled
- Similar to a photograph, D must be stable around the clock edge
- If D is changing when it is sampled, metastability can occur

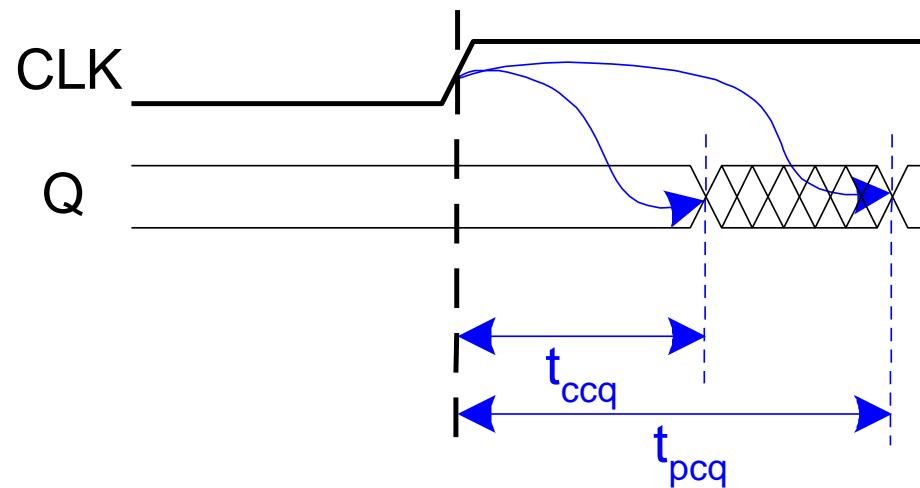
Input Timing Constraints

- Setup time: $t_{\text{setup}} = \text{time } \textit{before} \text{ the clock edge that data must be stable (i.e. not changing)}$
- Hold time: $t_{\text{hold}} = \text{time } \textit{after} \text{ the clock edge that data must be stable}$
- Aperture time: $t_a = \text{time around clock edge that data must be stable}$ ($t_a = t_{\text{setup}} + t_{\text{hold}}$)



Output Timing Constraints

- Propagation delay: t_{pcq} = time after clock edge that the output Q is guaranteed to be stable (i.e., to stop changing)
- Contamination delay: t_{ccq} = time after clock edge that Q might be unstable (i.e., start changing)

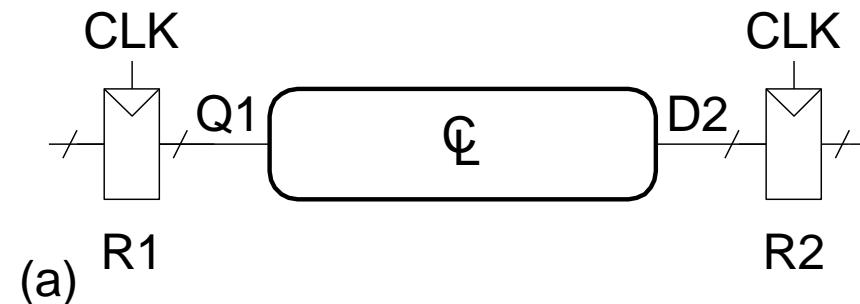


Dynamic Discipline

- The input to a synchronous sequential circuit must be stable during the aperture (setup and hold) time around the clock edge.
- Specifically, the input must be stable
 - at least t_{setup} before the clock edge
 - at least until t_{hold} after the clock edge

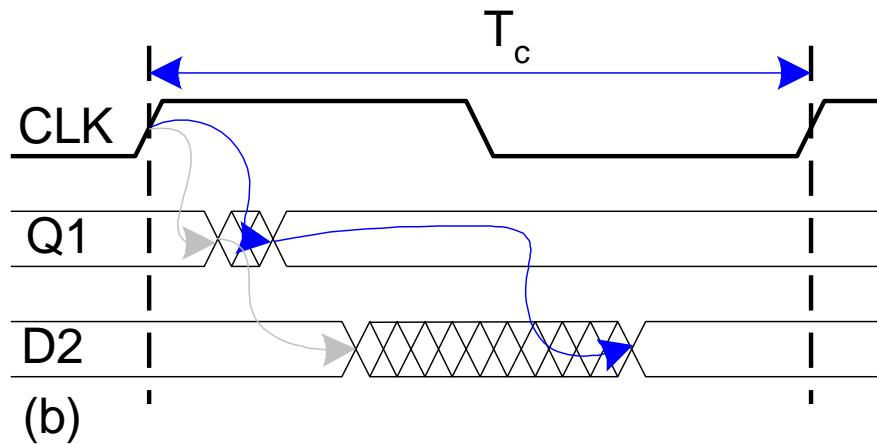
Timing

- The delay between registers has a **minimum** and **maximum** delay, dependent on the delays of the circuit elements



(a) R1

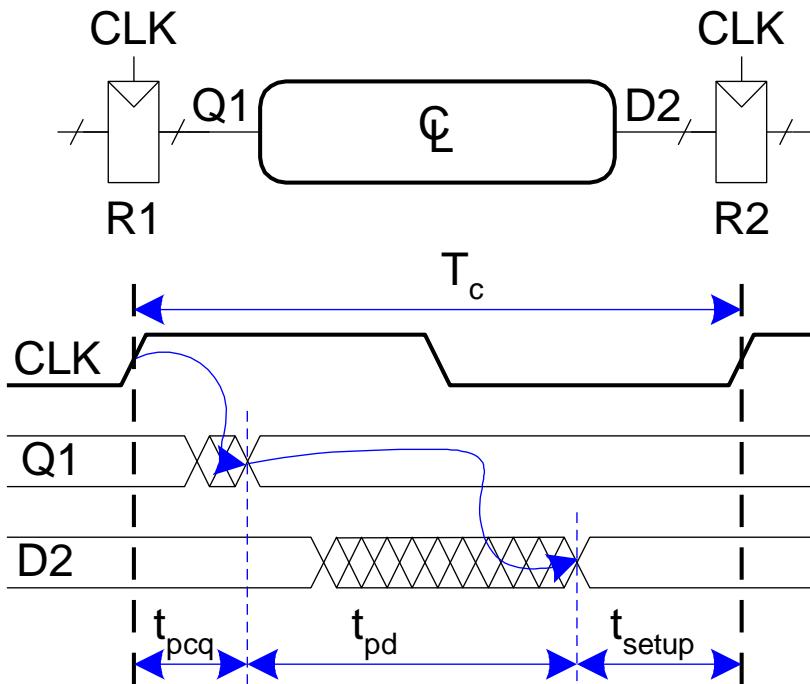
R2



(b)

Setup Time Constraint

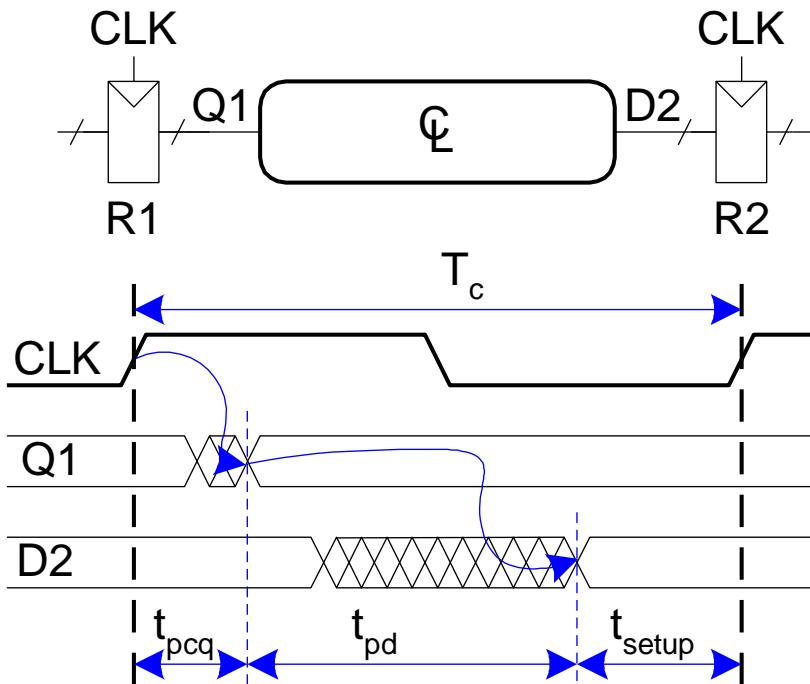
- The setup time constraint depends on the **maximum** delay from register R1 through the combinational logic.
- The input to register R2 must be stable at least t_{setup} before the clock edge.



$$T_c \geq$$

Setup Time Constraint

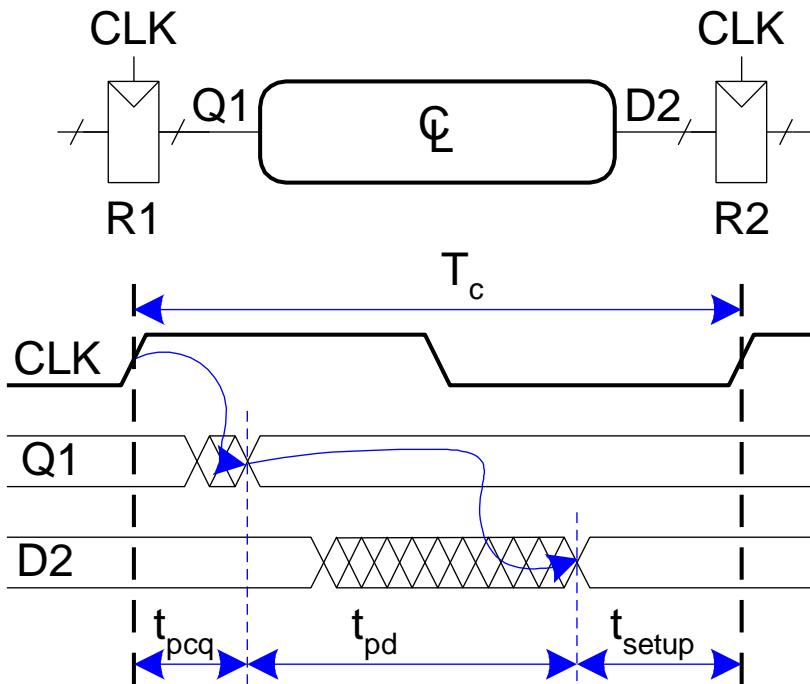
- The setup time constraint depends on the **maximum** delay from register R1 through the combinational logic.
- The input to register R2 must be stable at least t_{setup} before the clock edge.



$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}}$$
$$t_{pd} \leq$$

Setup Time Constraint

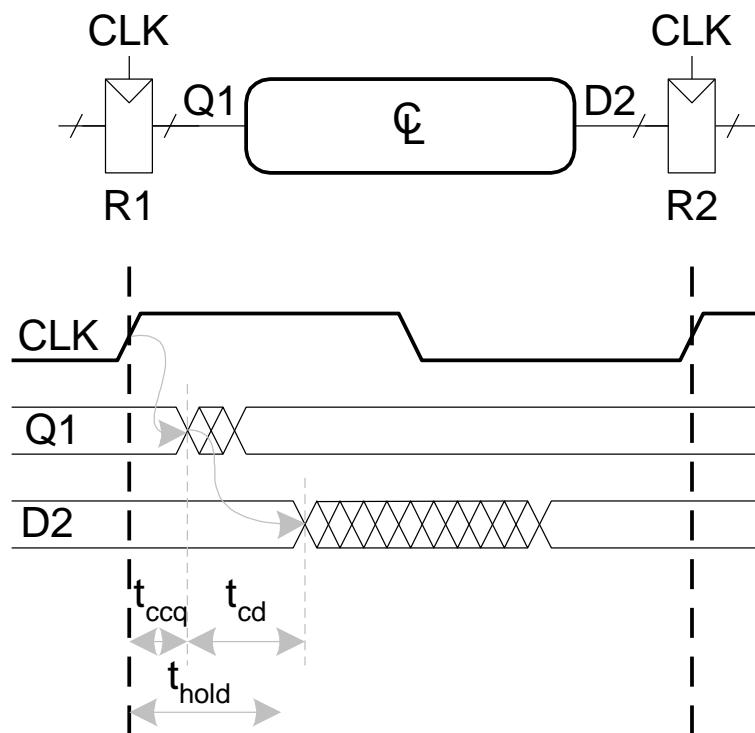
- The setup time constraint depends on the **maximum** delay from register R1 through the combinational logic.
- The input to register R2 must be stable at least t_{setup} before the clock edge.



$$T_c \geq t_{\text{pcq}} + t_{\text{pd}} + t_{\text{setup}}$$
$$t_{\text{pd}} \leq T_c - (t_{\text{pcq}} + t_{\text{setup}})$$

Hold Time Constraint

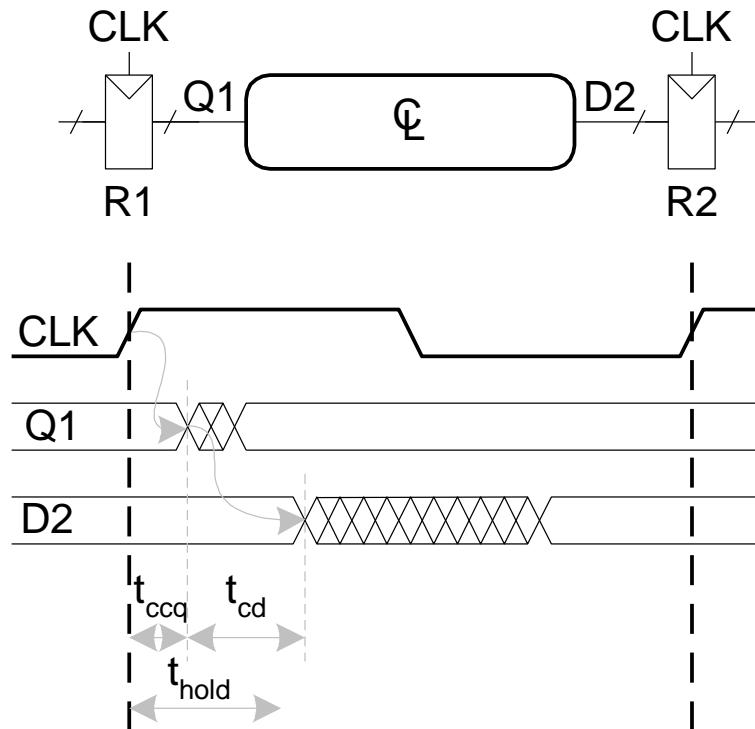
- The hold time constraint depends on the **minimum** delay from register R1 through the combinational logic.
- The input to register R2 must be stable for at least t_{hold} after the clock edge.



$t_{\text{hold}} <$

Hold Time Constraint

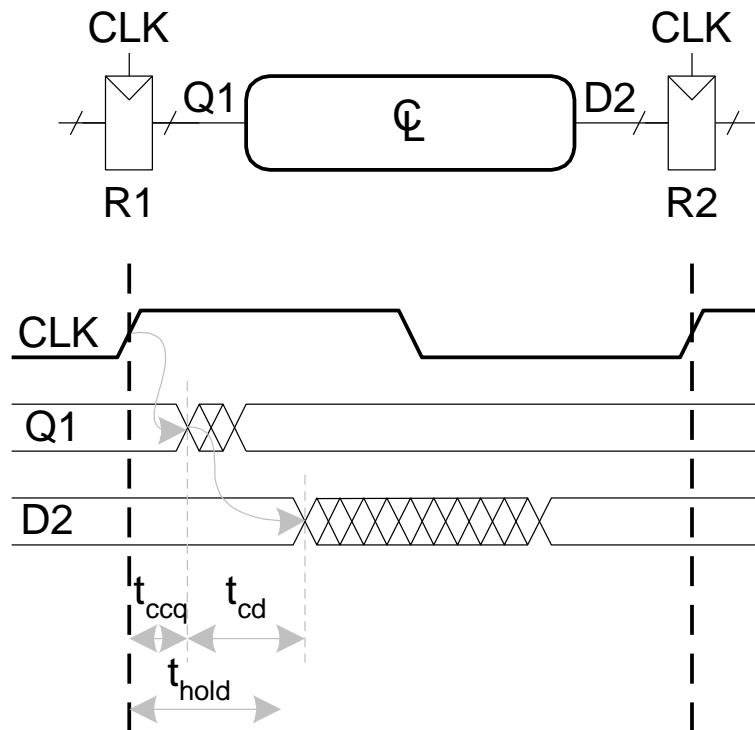
- The hold time constraint depends on the **minimum** delay from register R1 through the combinational logic.
- The input to register R2 must be stable for at least t_{hold} after the clock edge.



$$t_{hold} < t_{ccq} + t_{cd}$$
$$t_{cd} >$$

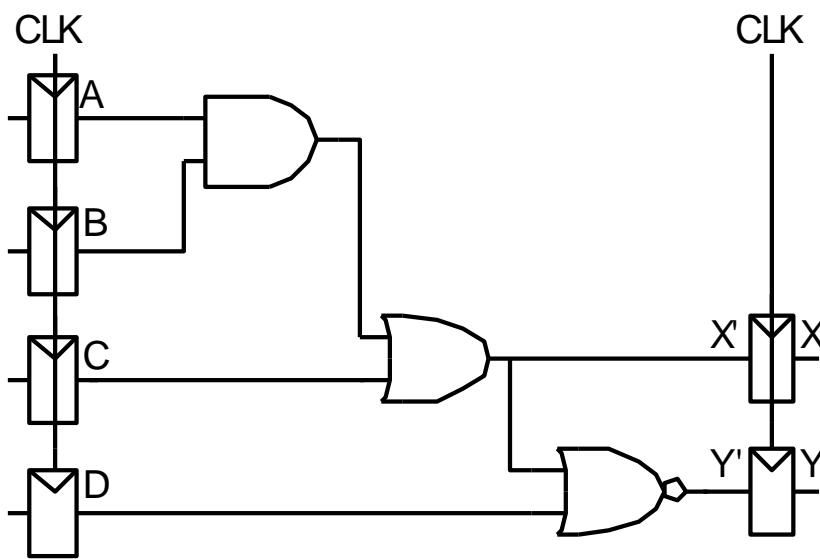
Hold Time Constraint

- The hold time constraint depends on the **minimum** delay from register R1 through the combinational logic.
- The input to register R2 must be stable for at least t_{hold} after the clock edge.



$$t_{hold} < t_{ccq} + t_{cd}$$
$$t_{cd} > t_{hold} - t_{ccq}$$

Timing Analysis



$$t_{pd} =$$

$$t_{cd} =$$

Setup time constraint:

$$T_c \geq$$

$$f_c = 1/T_c =$$

Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

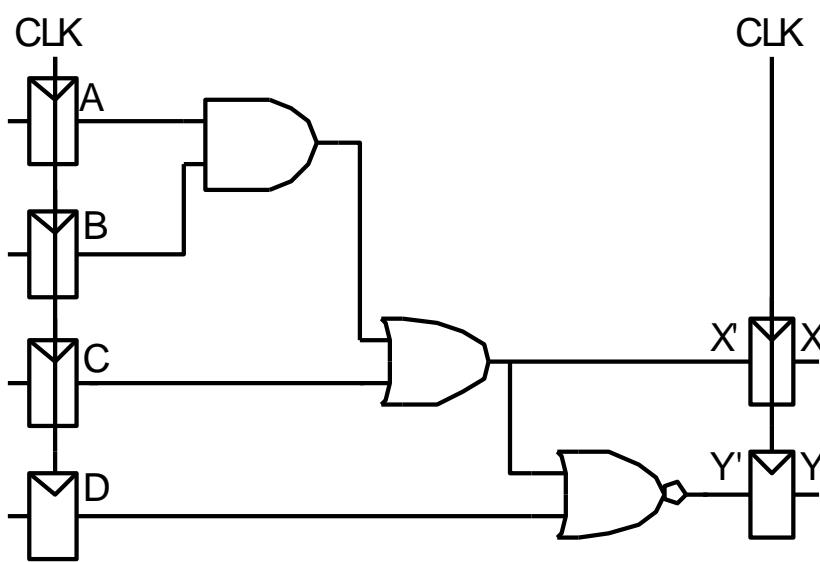
per gate

$$\begin{aligned} t_{pd} &= 35 \text{ ps} \\ t_{cd} &= 25 \text{ ps} \end{aligned}$$

Hold time constraint:

$$t_{ccq} + t_{pd} > t_{\text{hold}} ?$$

Timing Analysis



$$t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

Setup time constraint:

$$T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps}$$

$$f_c = 1/T_c = 4.65 \text{ GHz}$$

Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

per gate

$$\begin{aligned} t_{pd} &= 35 \text{ ps} \\ t_{cd} &= 25 \text{ ps} \end{aligned}$$

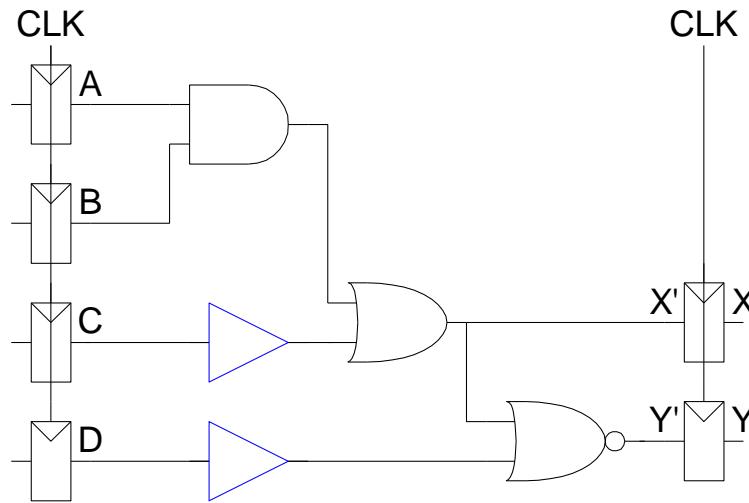
Hold time constraint:

$$t_{ccq} + t_{pd} > t_{\text{hold}} ?$$

$$(30 + 25) \text{ ps} > 70 \text{ ps} ? \text{ No!}$$

Fixing Hold Time Violation

Add buffers to the short paths:



$$t_{pd} =$$

$$t_{cd} =$$

Setup time constraint:

$$T_c \geq$$

$$f_c =$$

Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

per gate

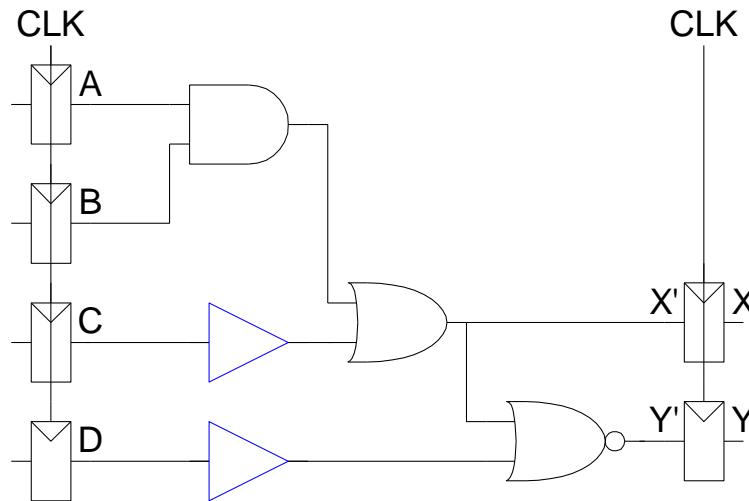
$$\begin{aligned} t_{pd} &= 35 \text{ ps} \\ t_{cd} &= 25 \text{ ps} \end{aligned}$$

Hold time constraint:

$$t_{ccq} + t_{pd} > t_{\text{hold}} ?$$

Fixing Hold Time Violation

Add buffers to the short paths:



$$t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd} = 2 \times 25 \text{ ps} = 50 \text{ ps}$$

Setup time constraint:

$$T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps}$$

$$f_c = 1/T_c = 4.65 \text{ GHz}$$

Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

per gate

$$\begin{aligned} t_{pd} &= 35 \text{ ps} \\ t_{cd} &= 25 \text{ ps} \end{aligned}$$

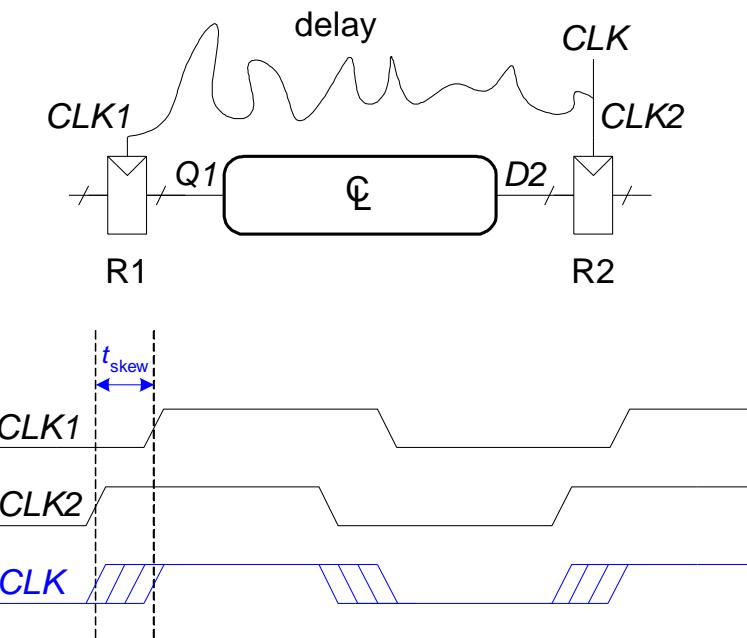
Hold time constraint:

$$t_{ccq} + t_{pd} > t_{\text{hold}} ?$$

$$(30 + 50) \text{ ps} > 70 \text{ ps} ? \text{ Yes!}$$

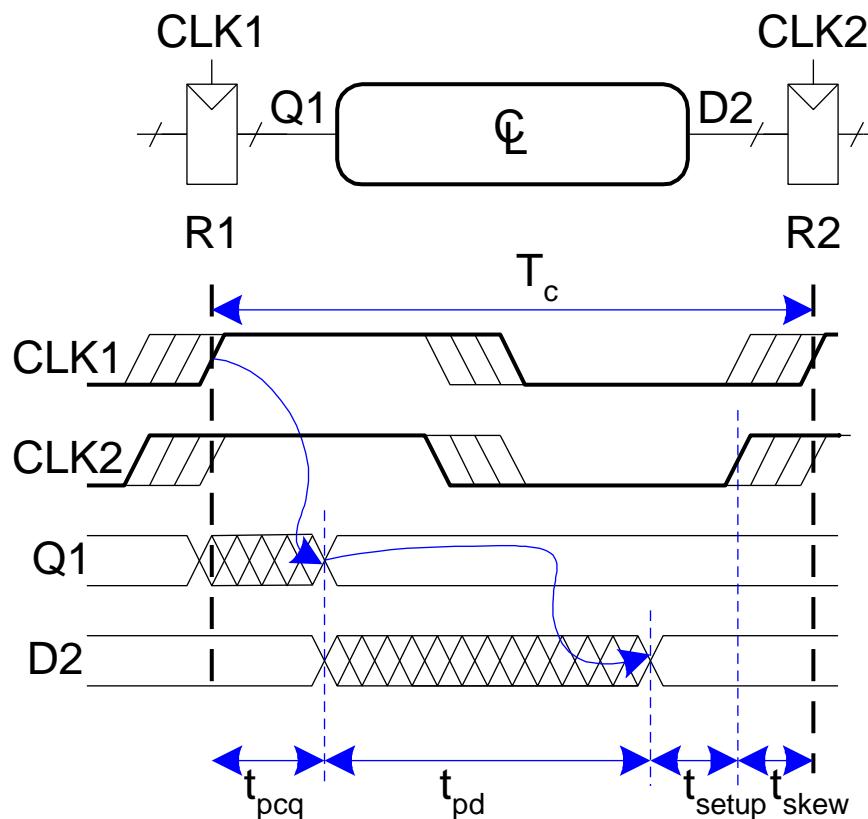
Clock Skew

- The clock doesn't arrive at all registers at the same time
- Skew is the difference between two clock edges
- Examine the worst case to guarantee that the dynamic discipline is not violated for any register – many registers in a system!



Setup Time Constraint with Clock Skew

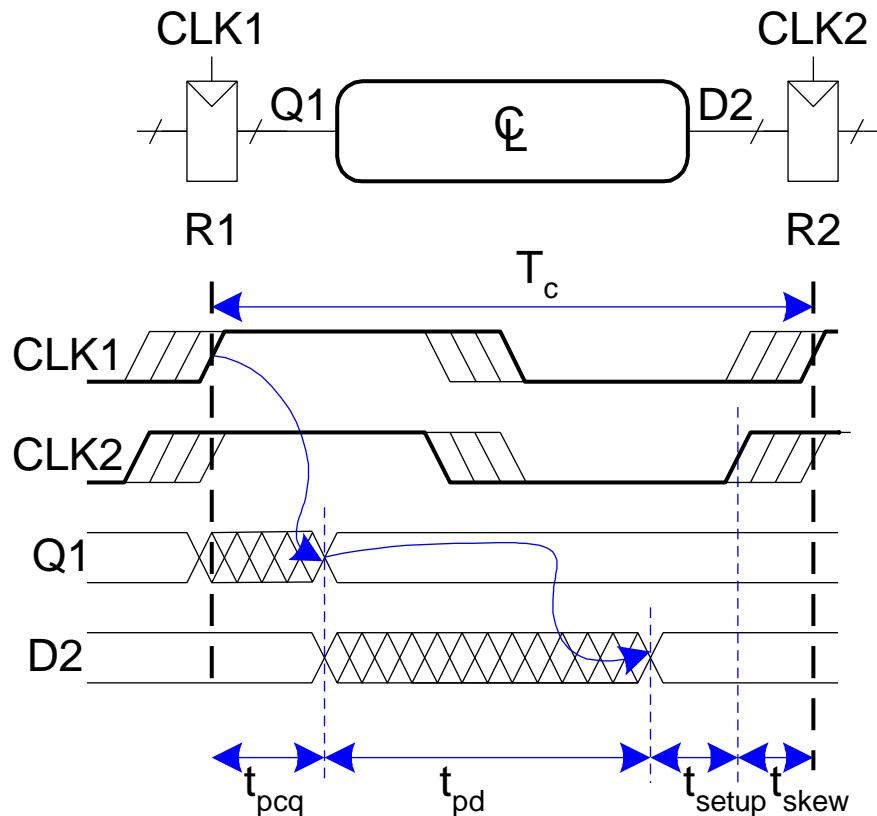
- In the worst case, the CLK2 is earlier than CLK1



$$T_c \geq$$

Setup Time Constraint with Clock Skew

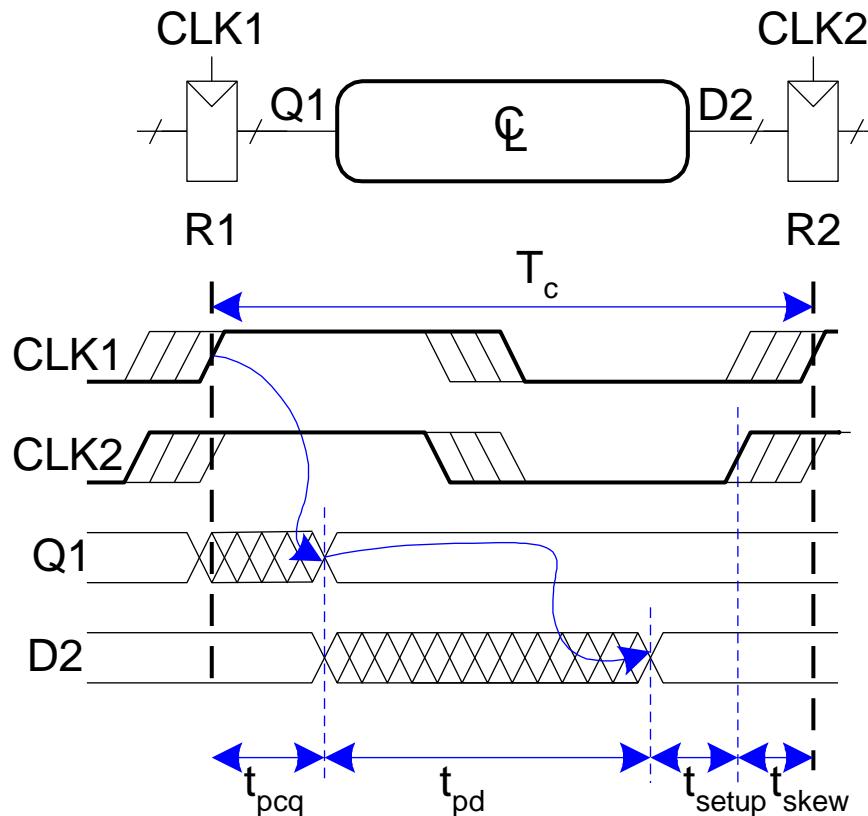
- In the worst case, the CLK2 is earlier than CLK1



$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}} + t_{\text{skew}}$$
$$t_{pd} \leq$$

Setup Time Constraint with Clock Skew

- In the worst case, the CLK2 is earlier than CLK1



$$T_c \geq t_{pcq} + t_{pd} + t_{setup} + t_{skew}$$
$$t_{pd} \leq T_c - (t_{pcq} + t_{setup} + t_{skew})$$