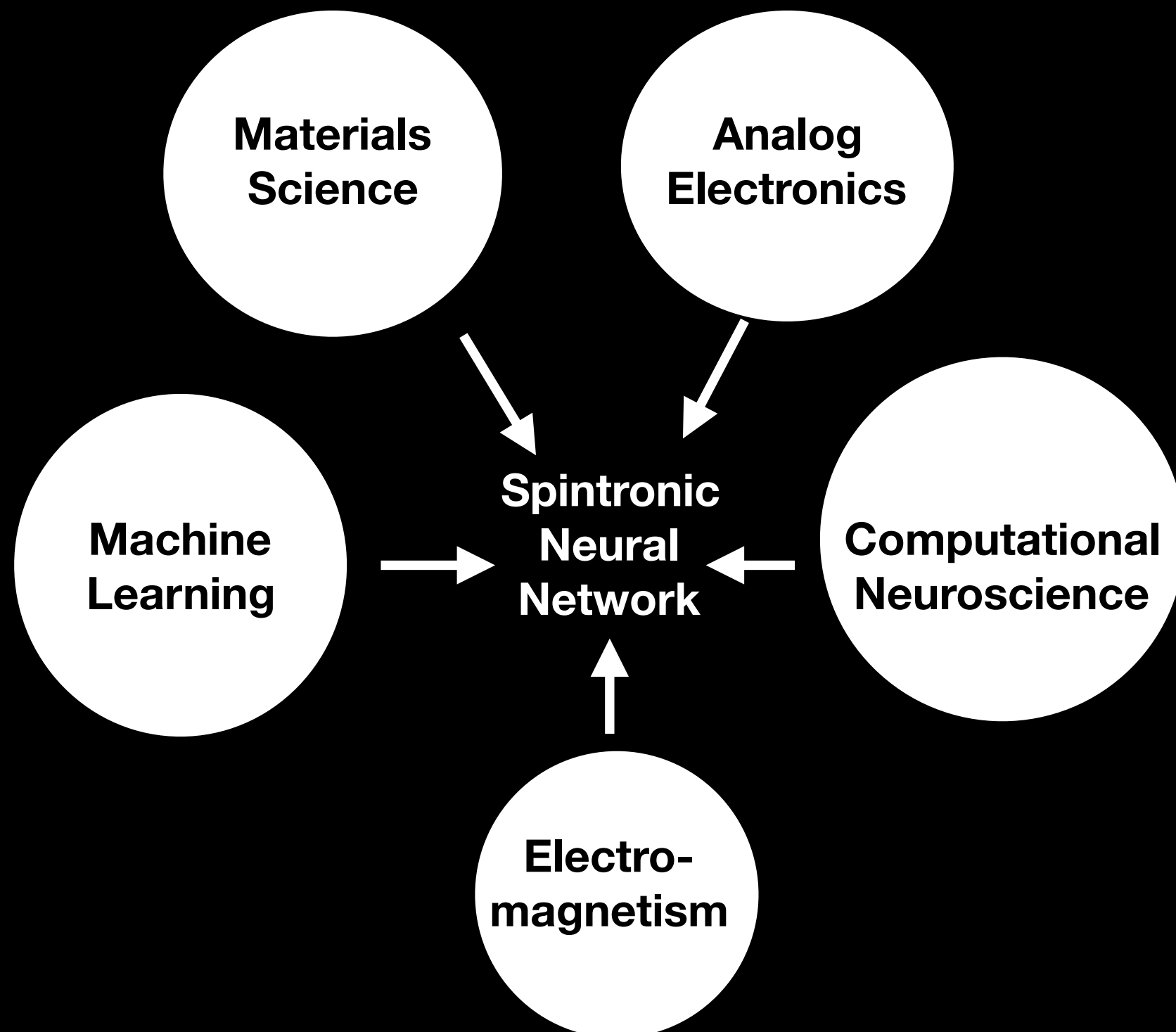


Hardware implementation of neural network algorithms, based on machine learning and neuroscience models, using spintronics

Debanjan Bhowmik
Assistant Professor

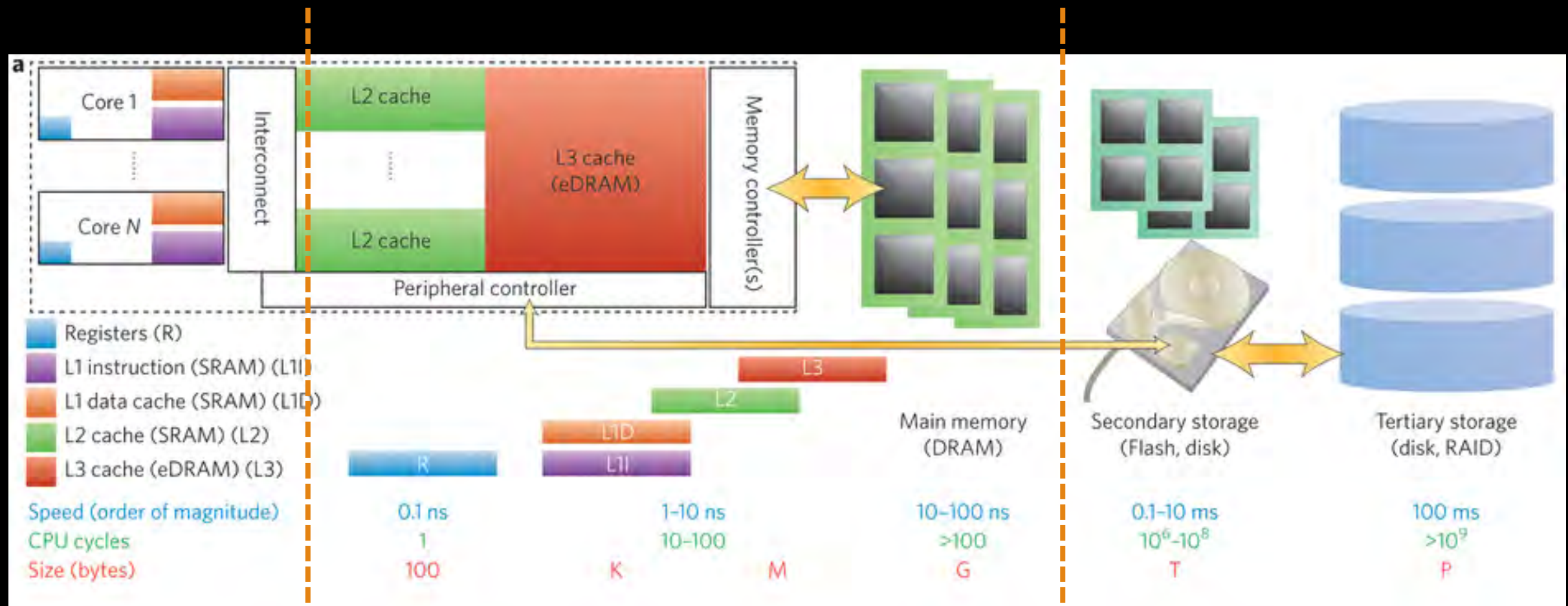
Department of Electrical Engineering
Indian Institute of Technology Delhi

Hardware implementation of neural network algorithms,
based on machine learning and neuroscience models,
using spintronics



Memory-Computing hierarchy of modern computers and role of Spintronics

Electronics using magnetic moment or spin of electrons is called spintronics.

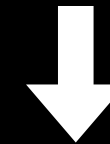
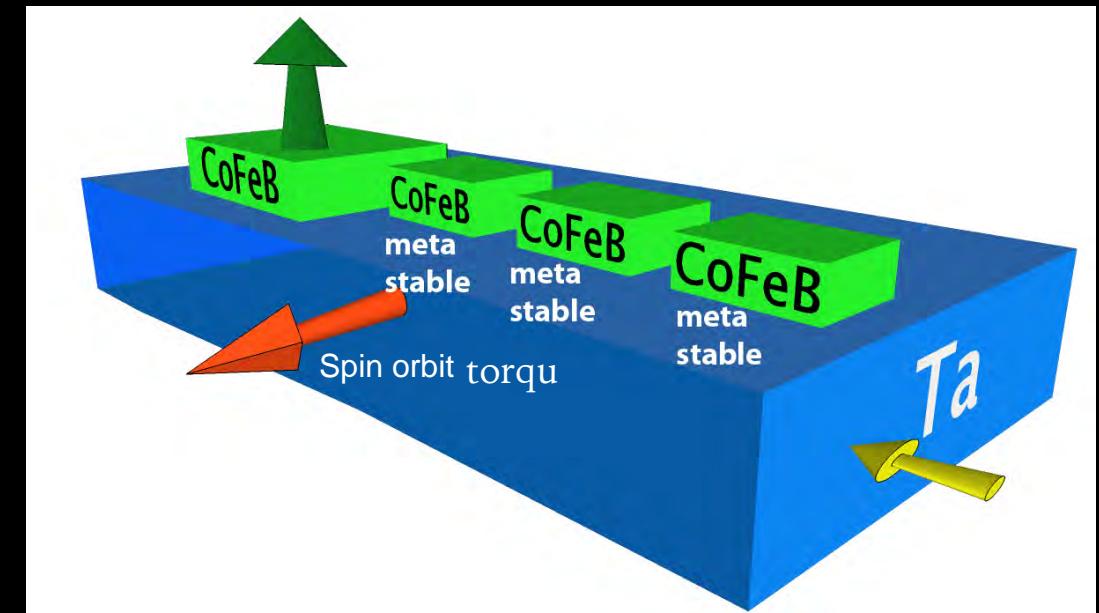
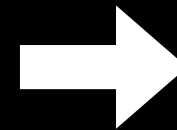
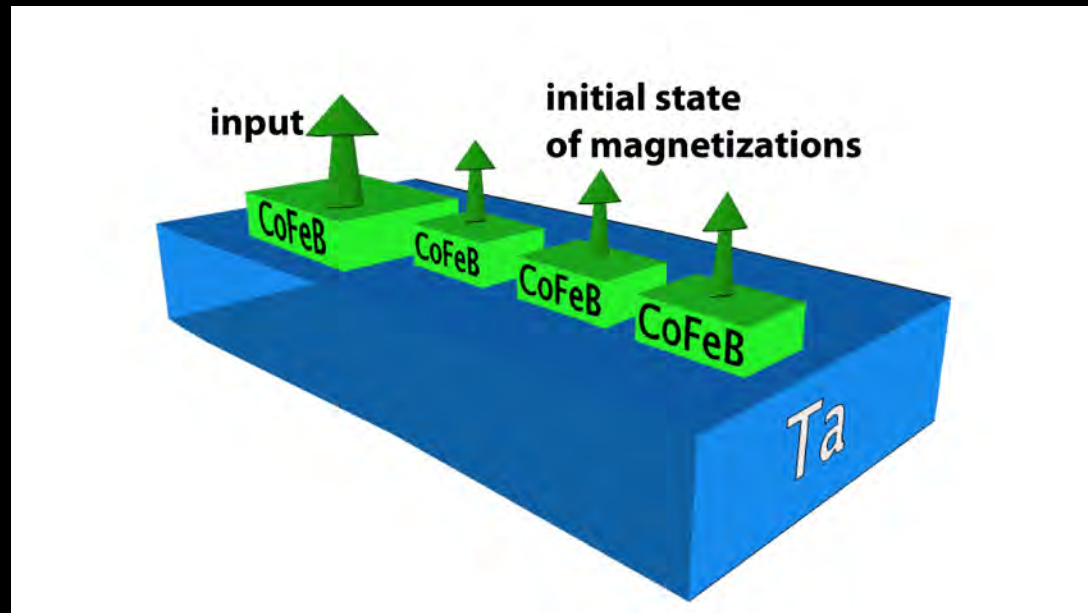


Computing
(spin FET,
nanomagnetic logic)

Memory (SpinTransferTorqueMagneticRAM,
domain wall racetrack memory)

Magnetic hard disk
widely used

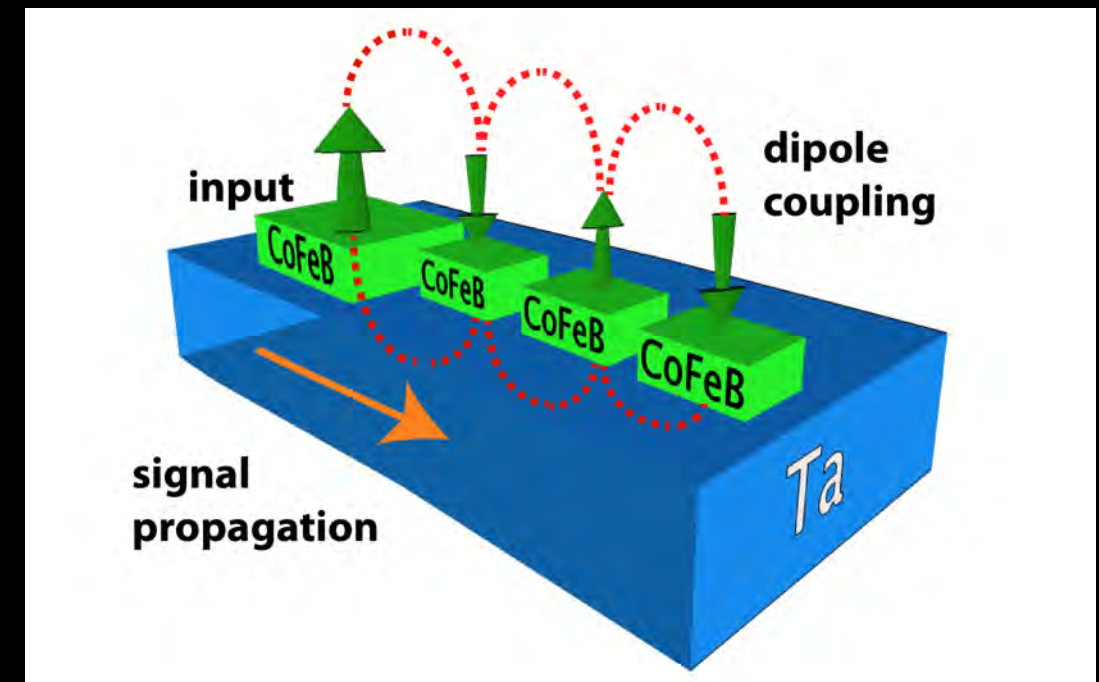
Spin orbit torque driven nanomagnetic logic (experiment)



Three 500 by 500 nm magnetic dots with a microns sized input dot separated by 30 nm each. Dipole coupling determines the final state- chain of inverters.

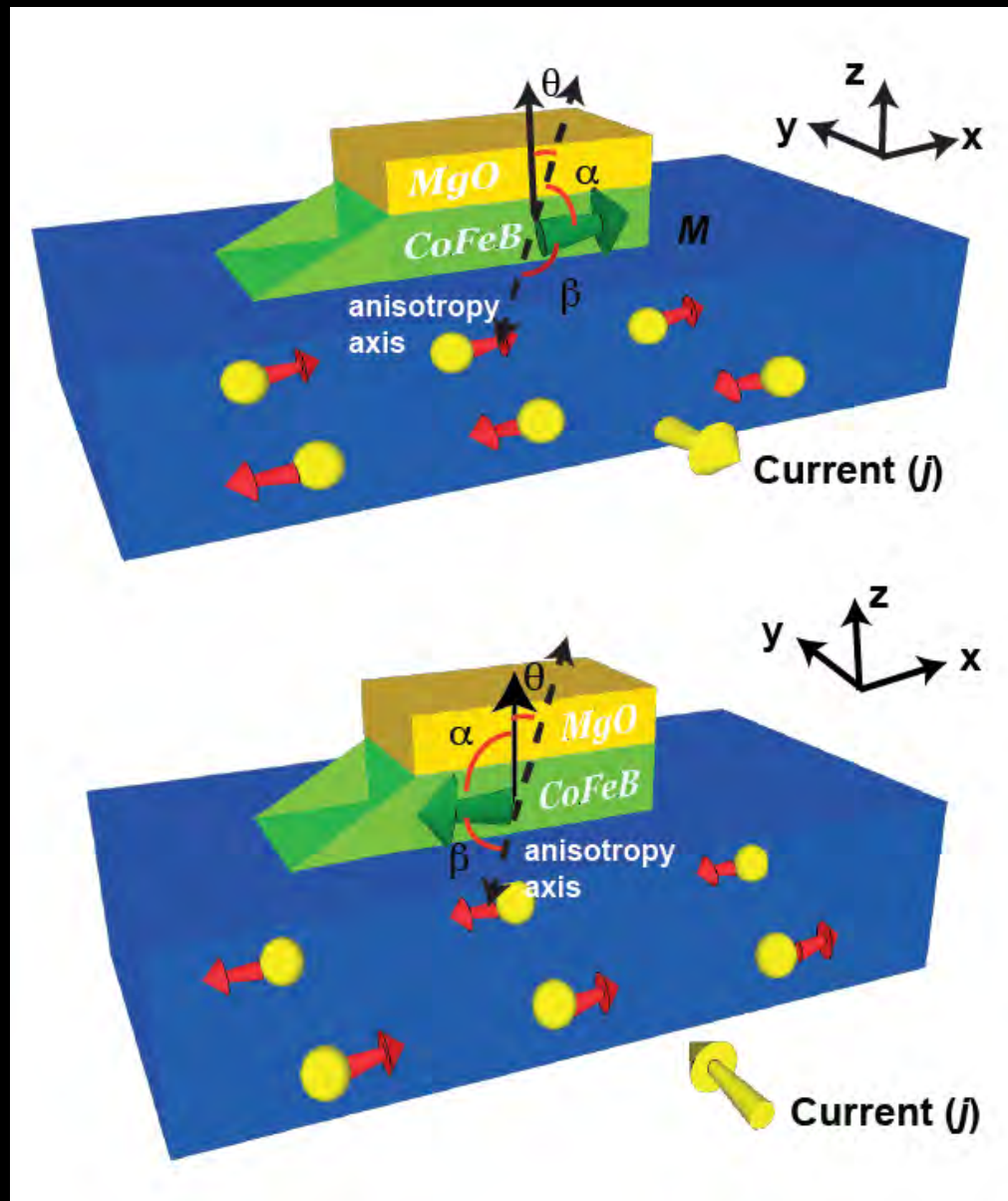
Current needed for clocking is 2mA,
While that in Oersted field clocking is
~700 mA.

Bhowmik, D. *et al.* Nature Nanotechnology 9 (2014)



Magnetic switching is too slow for logic.

Spin orbit torque driven magnetic switching for memory (simulation)



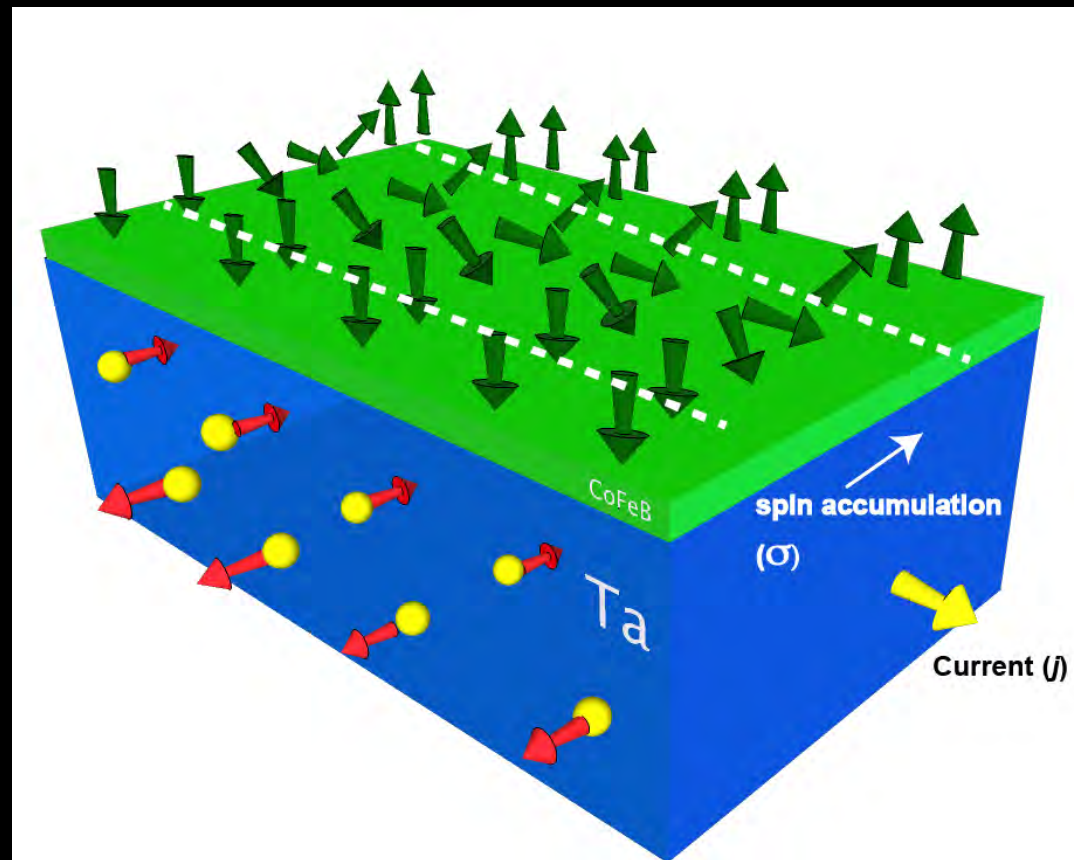
We engineer a tilt in the structure of the ferromagnet to cause deterministic switching in it by current.

Direction of magnetization M driven by spin orbit torque	Direction of final Magnetization M
+X	+Z
-X	-Z

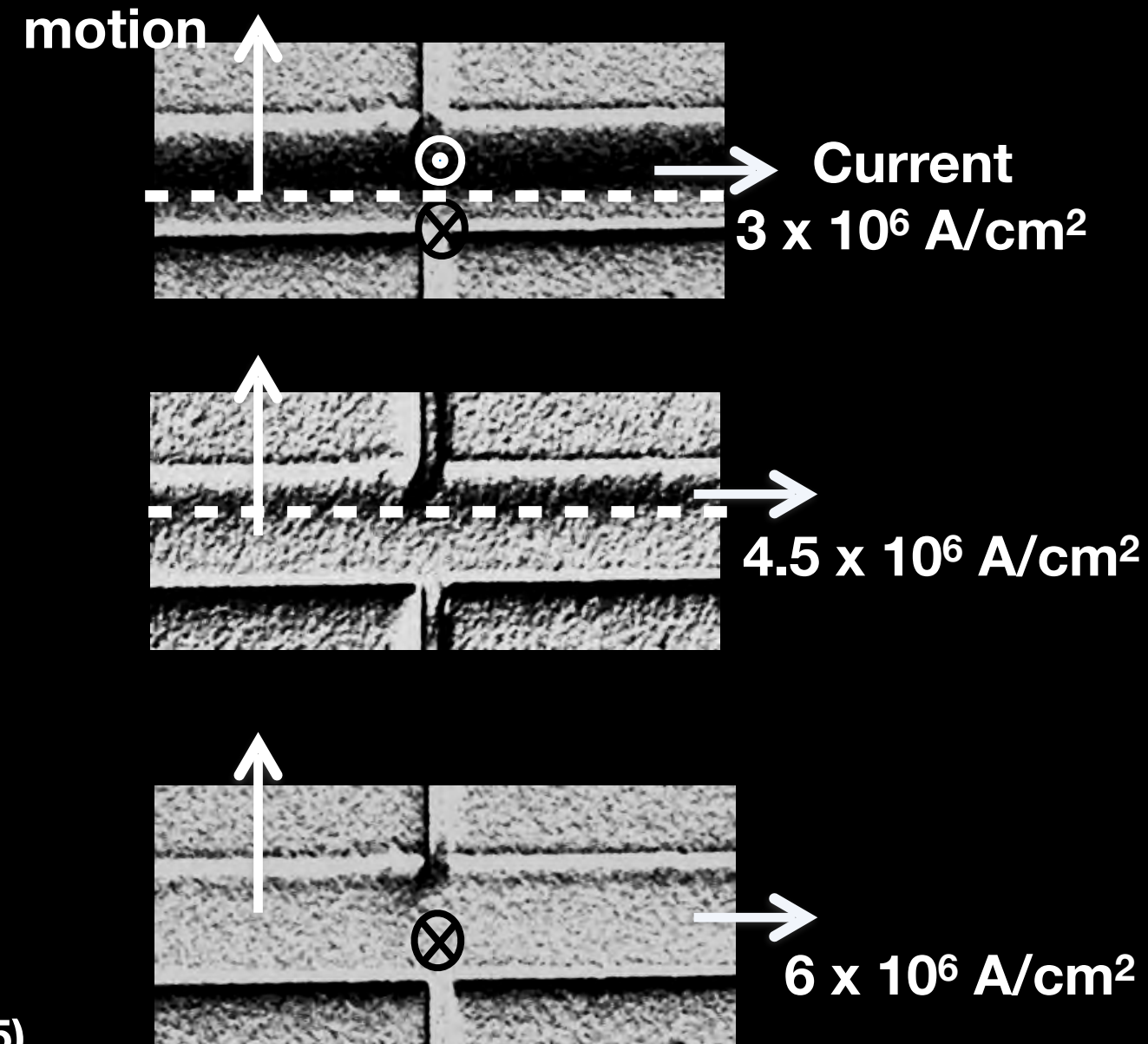
L. You, O.J. Lee, D. Bhowmik *et al.*
 Proceedings of National Academy
 of Sciences 112(33) 2015

**Spin Transfer Torque Magnetic Random
 Access Memory already being commercially made**

Spin orbit torque driven domain wall motion (simulation and experiment)



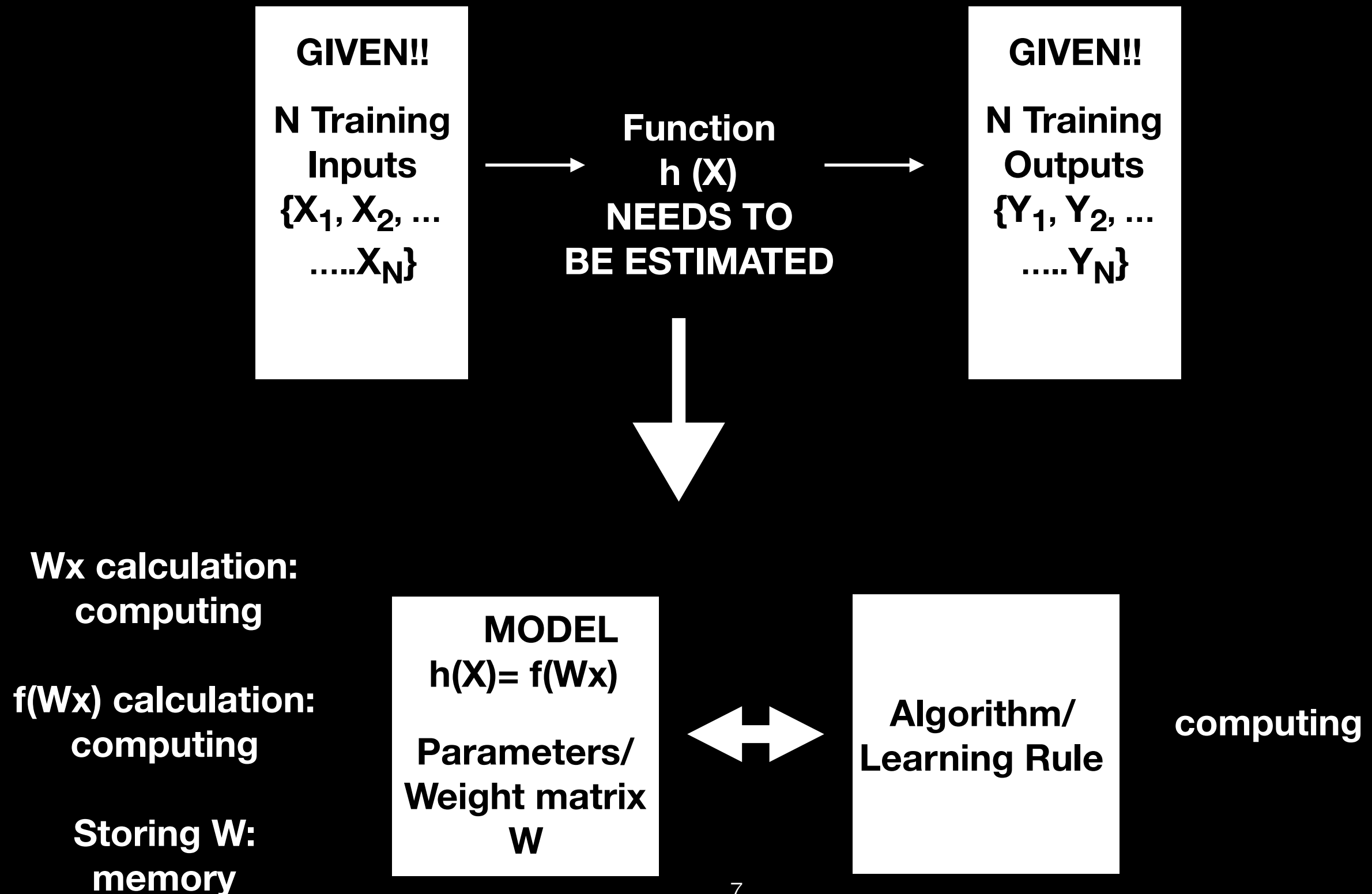
D. Bhowmik et al. Scientific Reports 5, 11823 (2015)



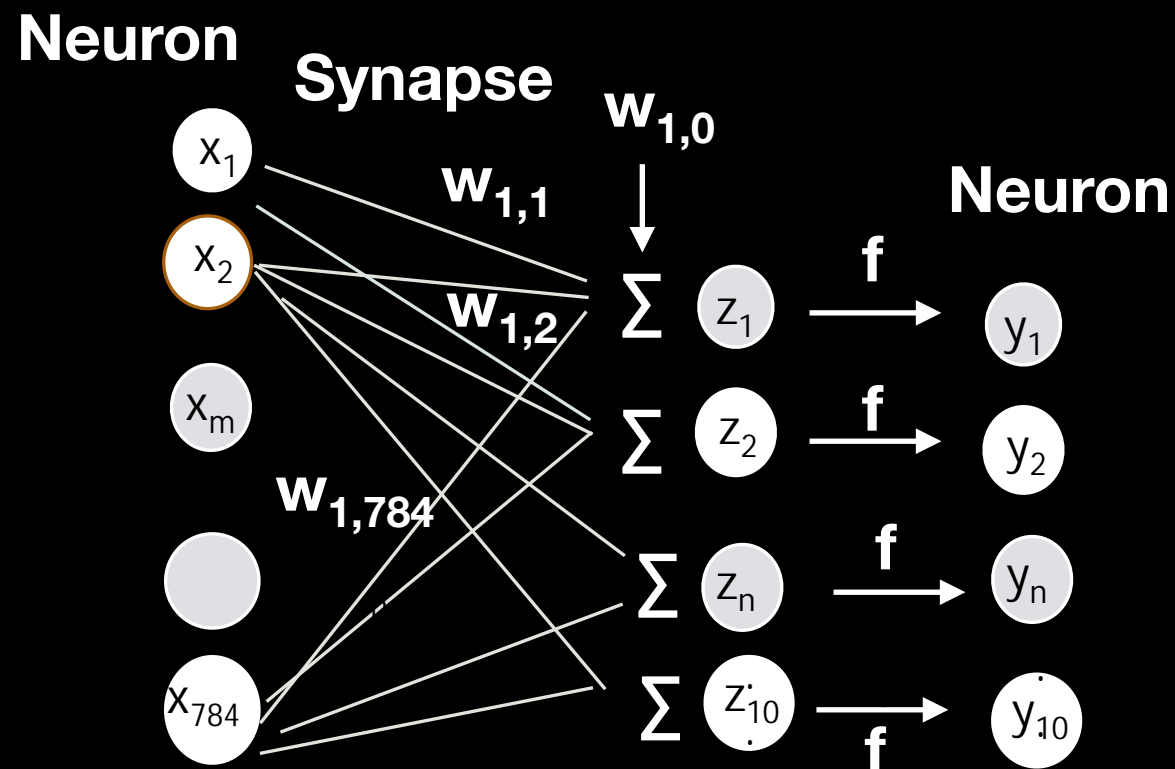
Multiple electrically controlled magnetic states can be obtained with different conductances- functional memristive behaviour.

Can this device be used for new kind of computing that combines memory and logic?
-Theme of my ongoing research

Neural Network Algorithms have memory- computing intertwined



Fully Connected Neural Network (FCNN)



Forward computation:

$$y_n = f(z_n) = \frac{2}{1 + e^{-\lambda z_n}} - 1;$$

$$z_n = w_{n,1}x_1 + w_{n,2}x_2 + \dots + w_{n,784}x_{784} + w_{n,0}$$

$$= (\sum_{m=1}^{784} w_{n,m}x_m) + w_{n,0}$$

**Stochastic Gradient Descent
(SGD) learning rule :**

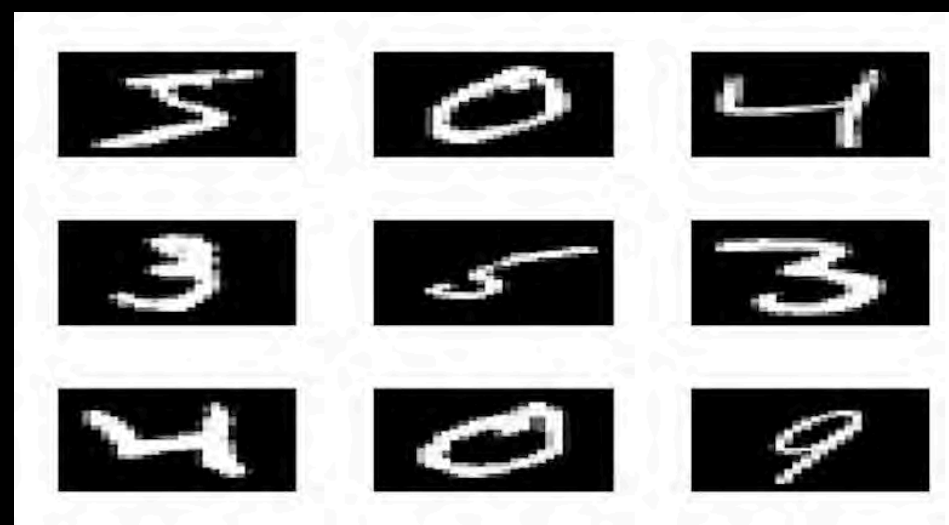
$$\epsilon_n = \frac{1}{2}(Y_n - y_n)^2$$

$$w_{n,m}^{i+1} = w_{n,m}^i - \Delta w_{n,m}$$

$$= w_{n,m}^i - \eta \frac{\partial \epsilon_n}{\partial w_{n,m}}$$

**applied over every training example,
multiple times.**

η : learning rate

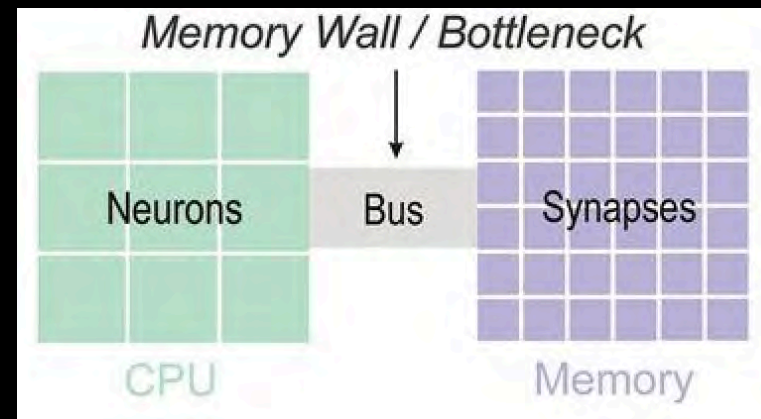


**28 by 28 pixel images
from MNIST dataset**

Theme of my
research as faculty

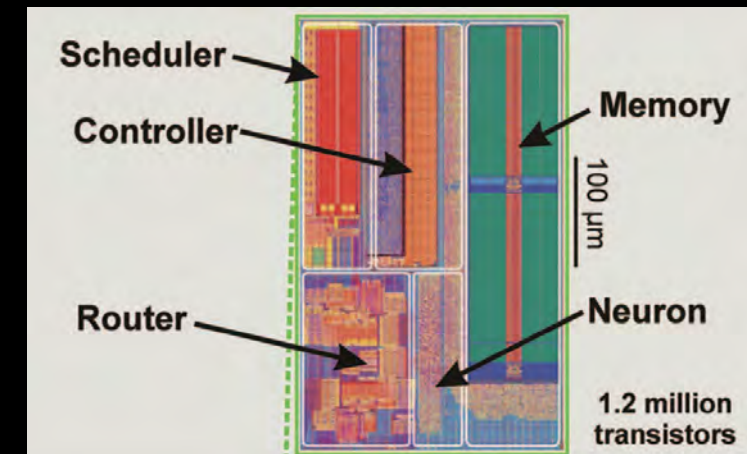
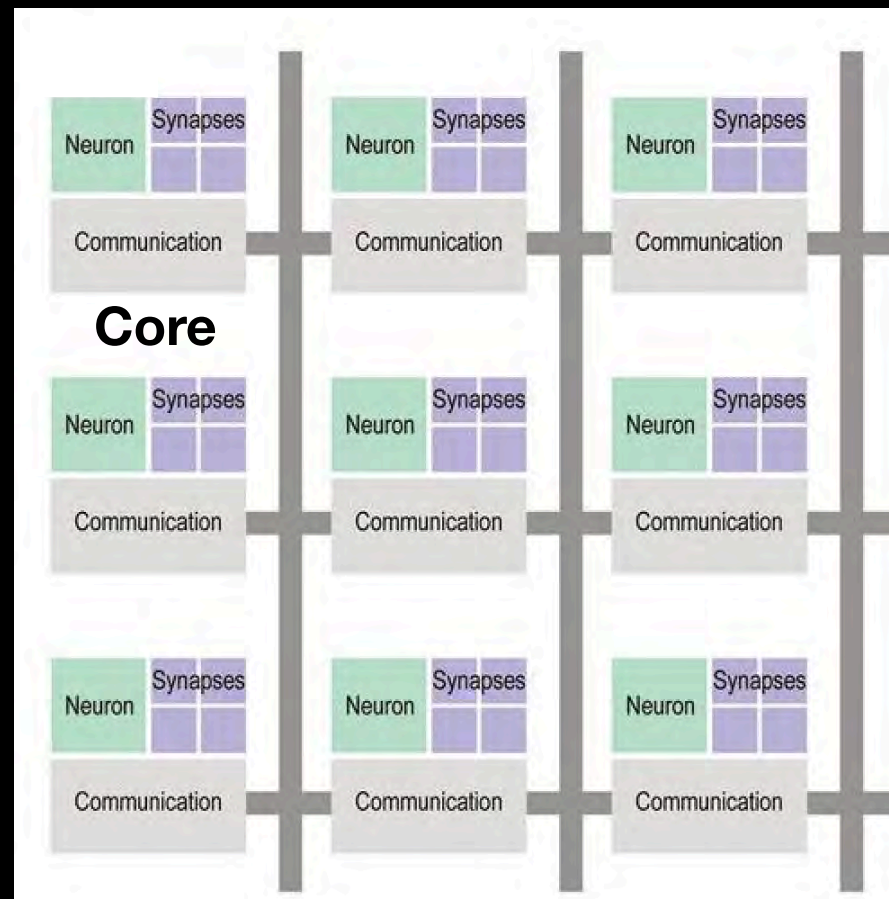
Solving FCNN on different computer architectures

**Traditional computer
architecture:
von-Neumann**



**Memory and computing
are completely separate**

Inside each core

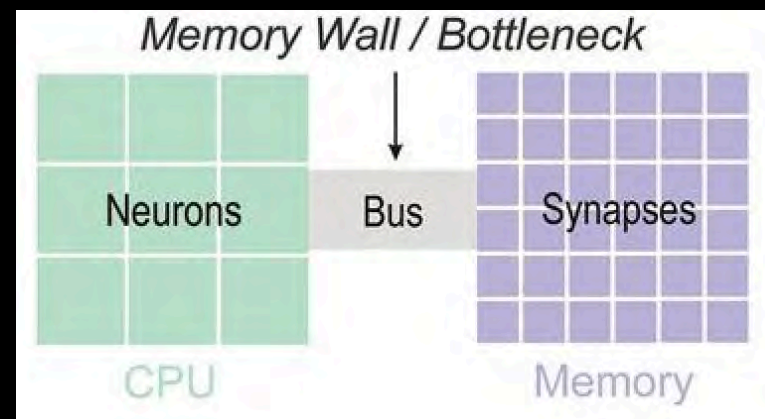


**Digital Hardware
Neural Network:
IBM True North
chip**

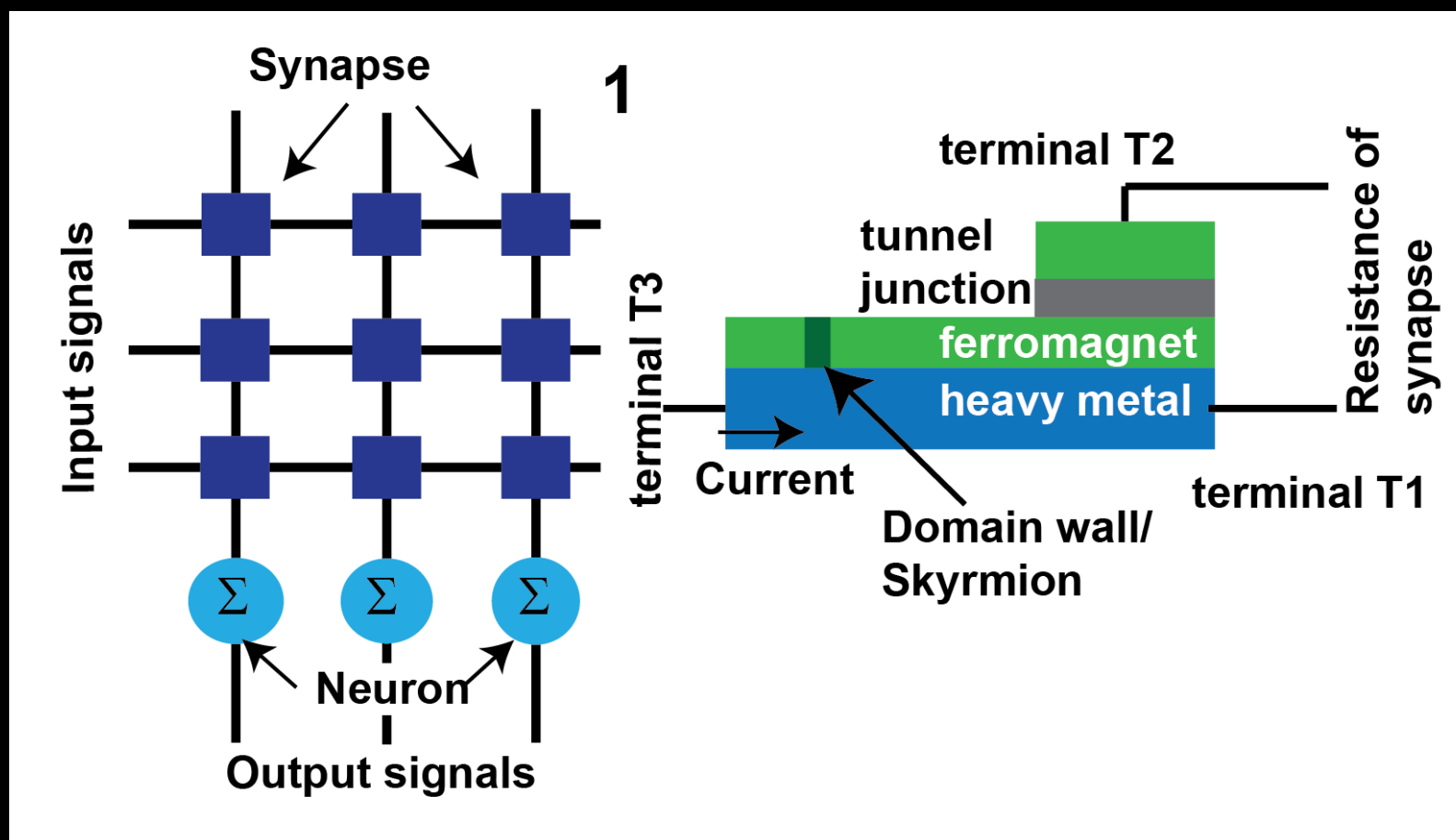
**Memory and computing
are separate inside each core,
but more intertwined
overall.**

Theme of my
research as faculty

Solving FCNN on different computer architectures



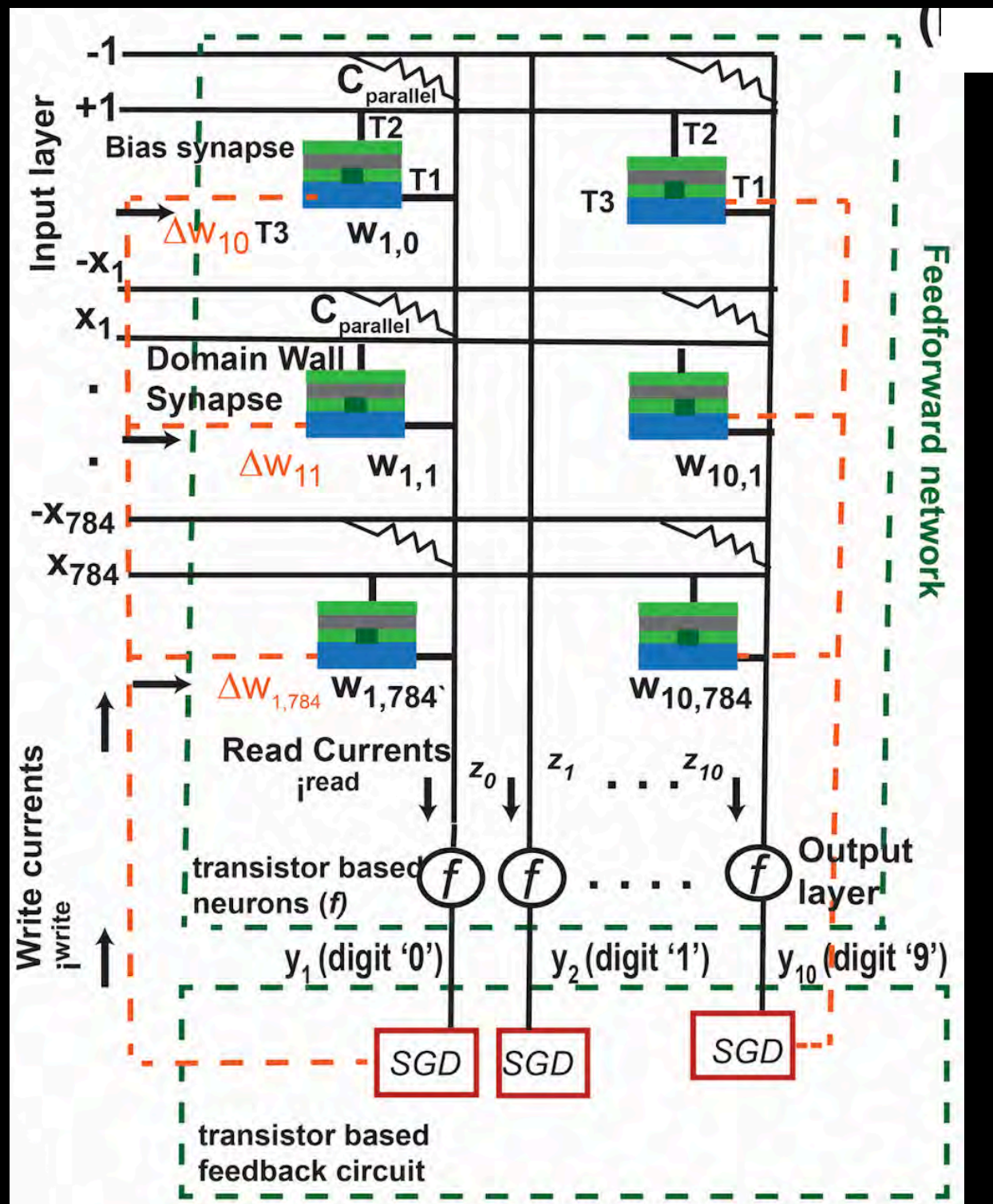
**Memory and computing
are completely separate**



**Analog Hardware
Neural Network:
Spintronic Synapse**

**Memory and computing
are completely
intertwined.**

Simulation of spintronic hardware based Fully Connected Neural Network (FCNN)



Spintronic synapses in cross-bar:

$$z_n = w_{n,1}x_1 + w_{n,2}x_2 + \dots + w_{n,784}x_{784} + w_{n,0}$$

$$= (\sum_{m=1}^{784} w_{n,m}x_m) + w_{n,0}$$

**w is adjusted at every iteration by
write current**

Transistor based neuron:

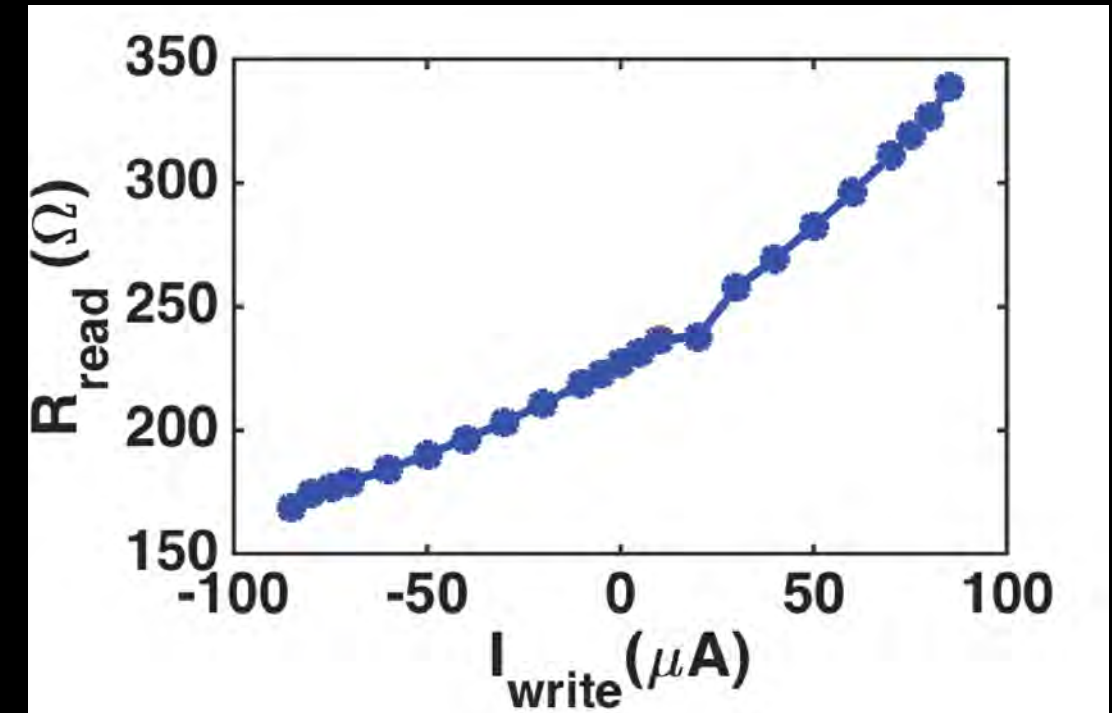
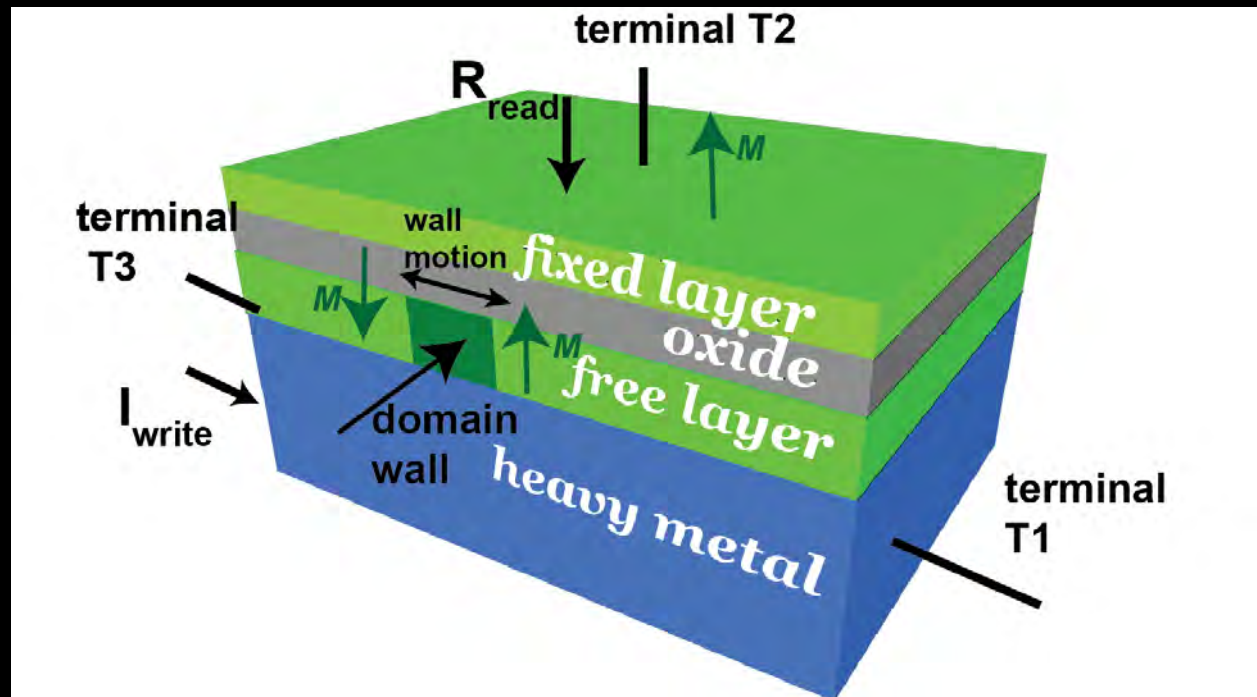
$$y_n = f(z_n) = \frac{2}{1 + e^{-\lambda z_n}} - 1$$

Transistor based SGD circuit:

$$w_{n,m}^{i+1} = w_{n,m}^i - \Delta w_{n,m}$$

$$= w_{n,m}^i - \eta \frac{\partial \epsilon_n}{\partial w_{n,m}}$$

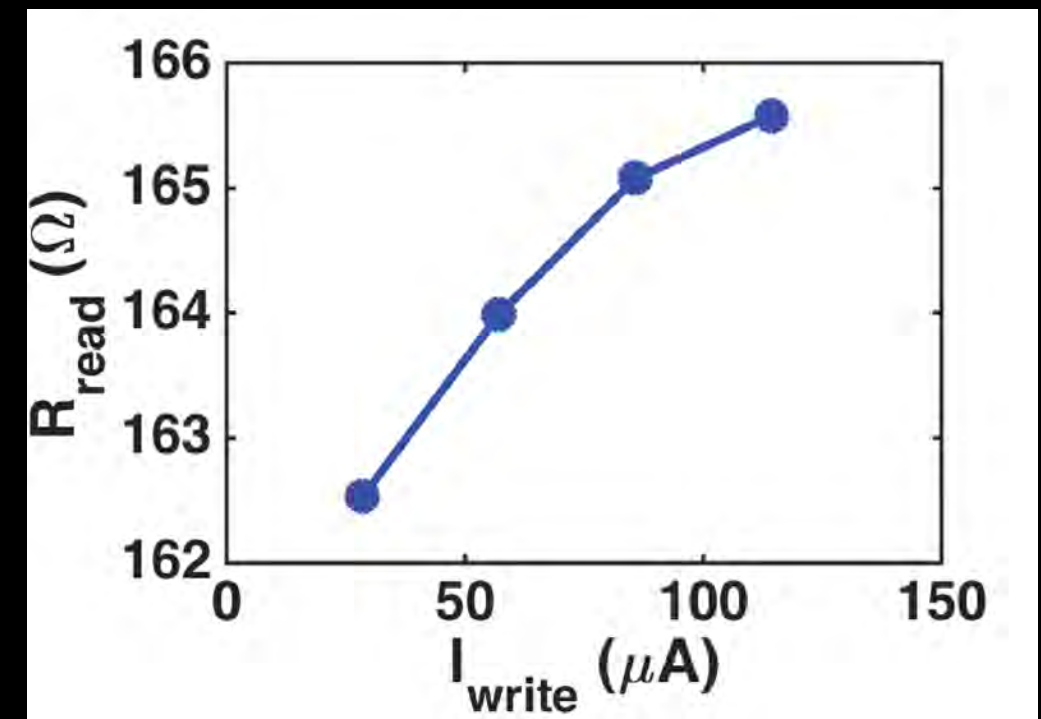
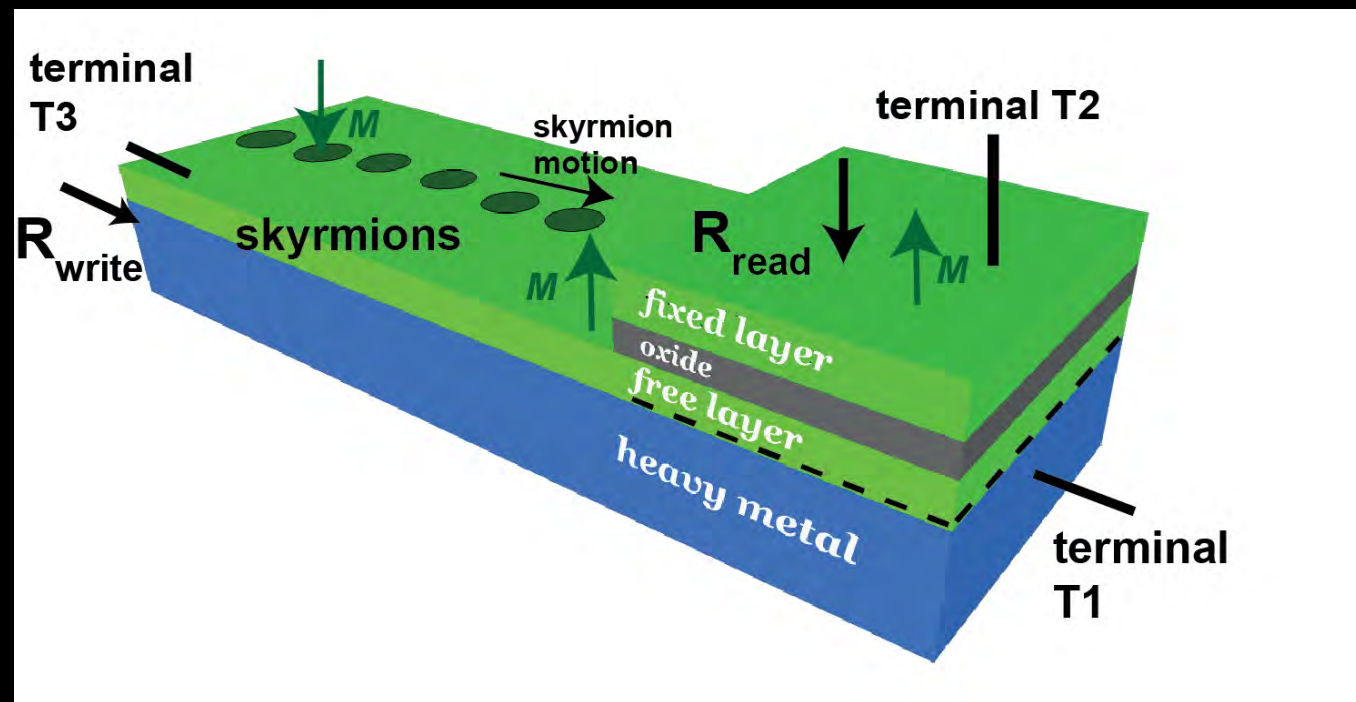
Micromagnetic simulation of domain wall synapse



**Multiple current controlled conductance states
which are non-volatile: Essential for synapse**

**simulated domain wall synapse device,
proposed by Sengupta *et al.* (2016)
on micromagnetic simulation package mumax**

Micromagnetic simulation of skyrmion synapse



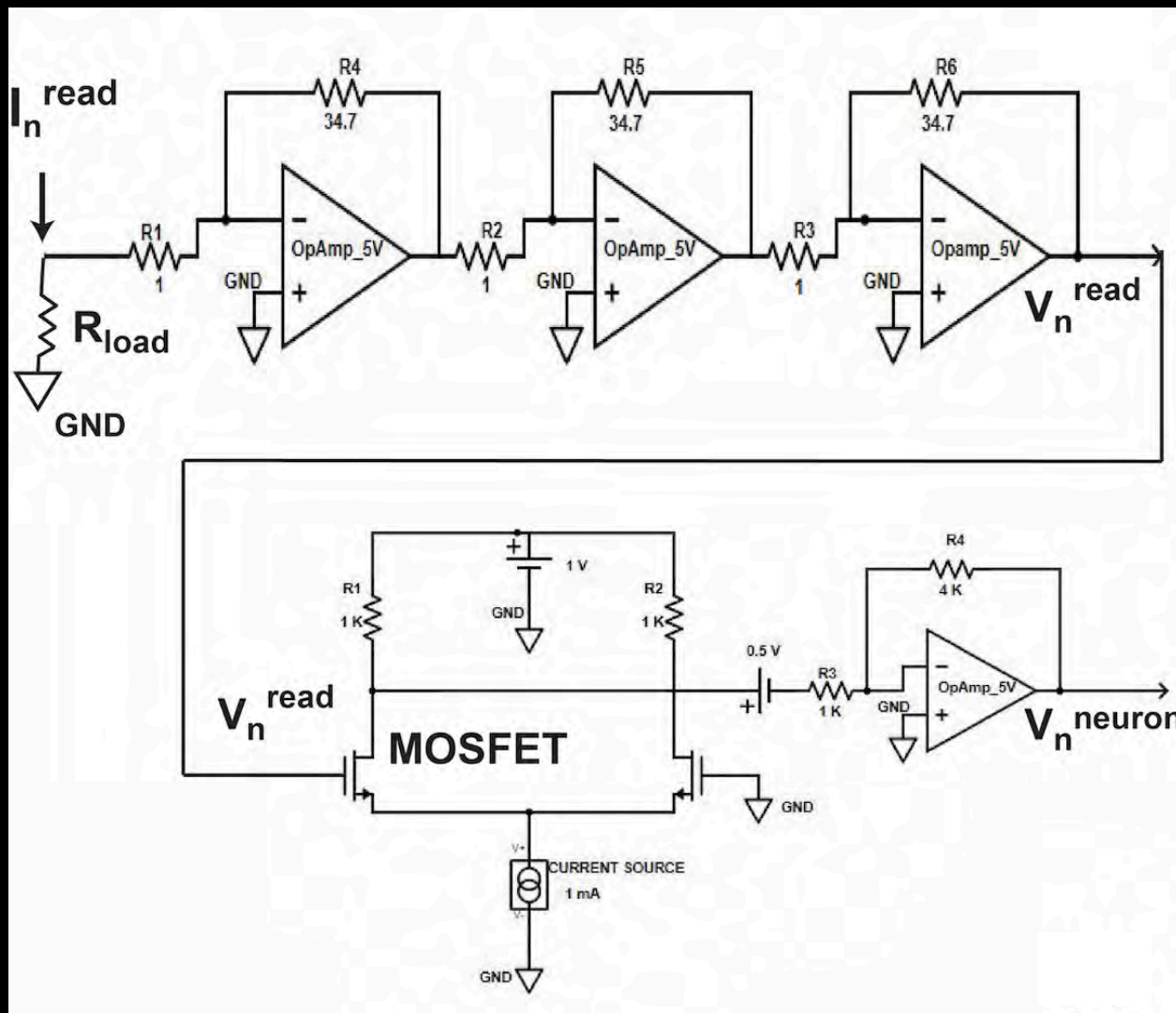
**Multiple current controlled conductance states
which are non-volatile: Essential for synapse**

**proposed and simulated skyrmionic synapse
on micromagnetic simulation package mumax.**

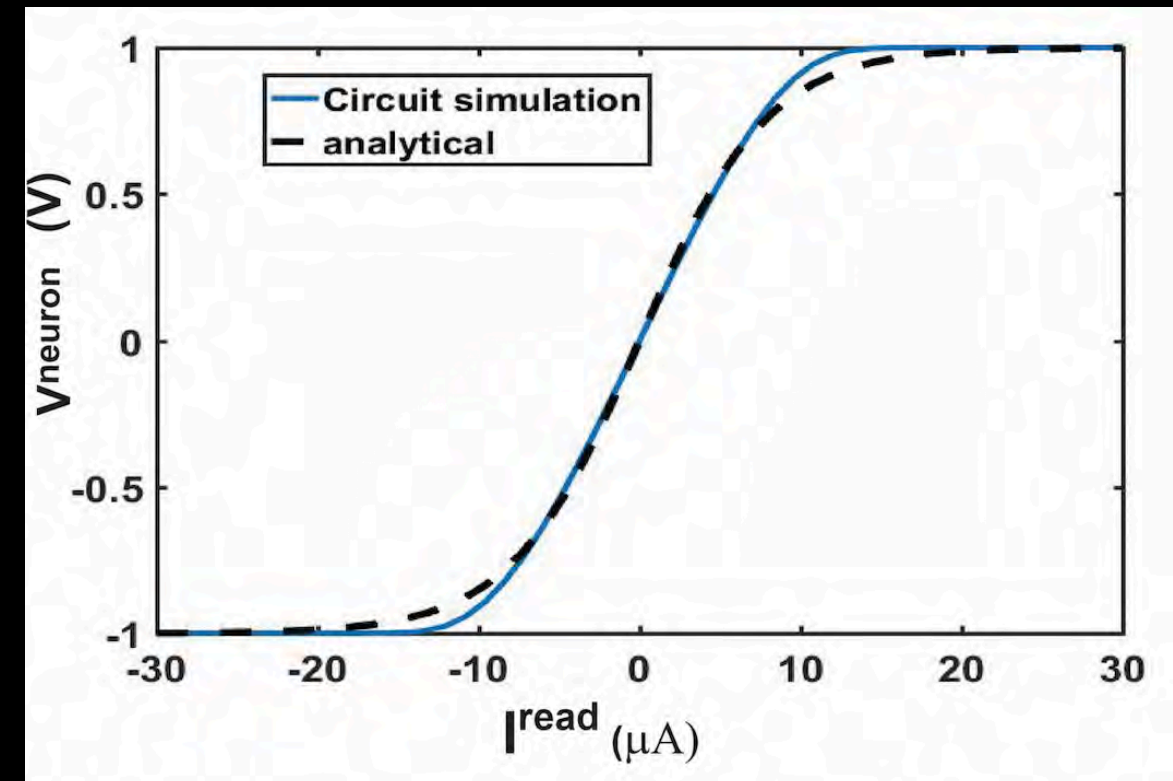
**showed that it consumes lower energy than
domain wall synapse if operated with low current.**

*U. Saxena et al. IEEE Transactions
on Magnetics, vol. 44, no. 11 (2018).*

Transistor based Neuron circuit



op-amp and differential amplifier based
analog circuit for neuron

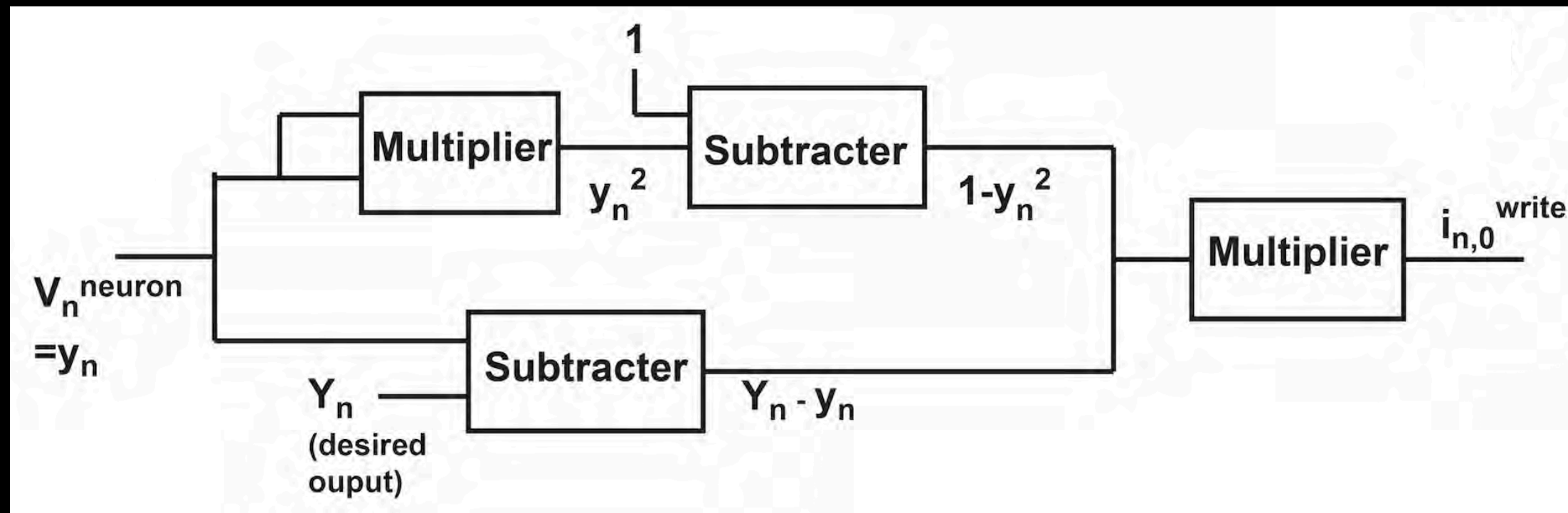


tan sigmoid activation function:

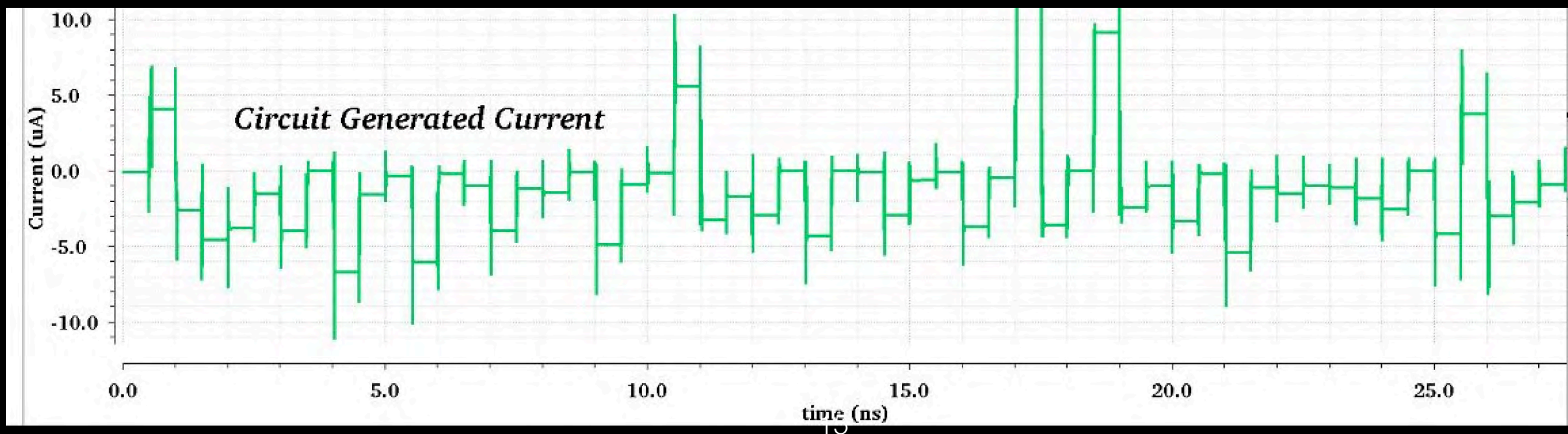
$$y_n = f(z_n) = \frac{2}{1 + e^{-\lambda z_n}} - 1$$

Results from
our research
group

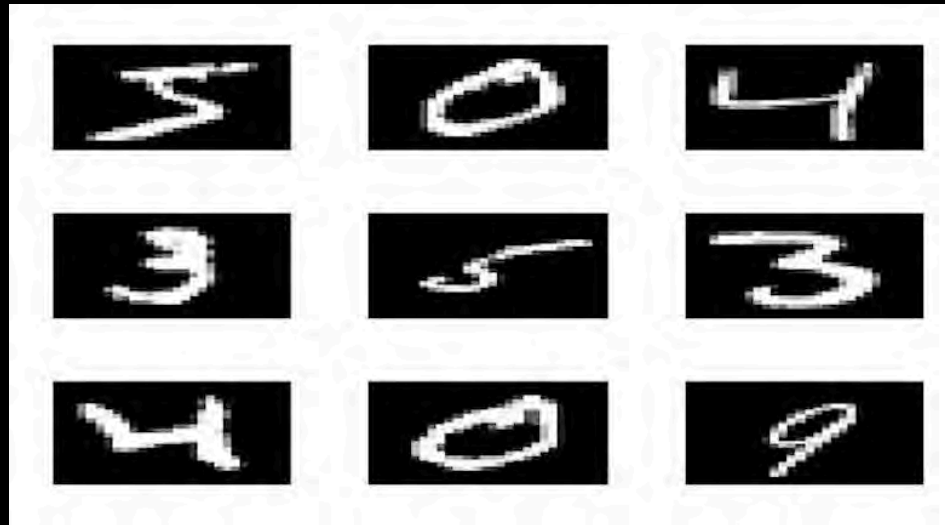
On chip learning of spintronic FCNN on MNIST dataset



SGD calculation and write current
generation circuit



On chip learning of spintronic FCNN on MNIST dataset



1000 train samples, 100 test samples.
10,000 epochs

Train accuracy: 97 %

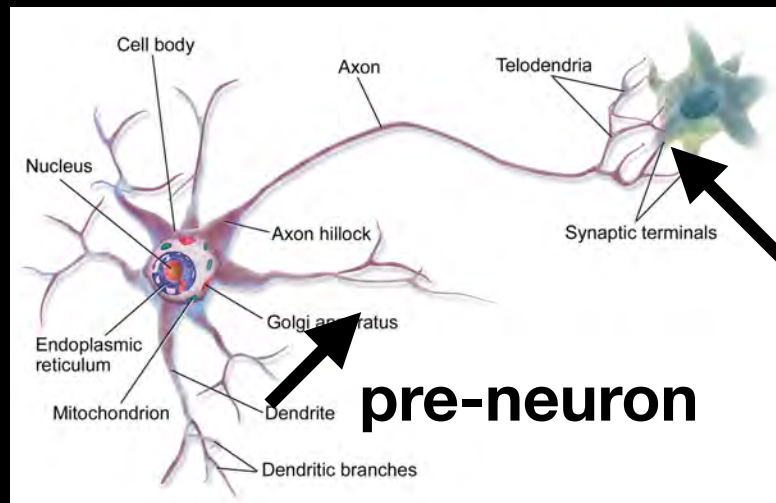
Test accuracy: ~ 65%

A. Dankar et al. , under preparation

- To improve test accuracy hidden layers will be needed, but then implementing SGD calculation circuit (backpropagation) in hardware is hard because weights of synapses are needed in the calculation.
- We turn towards hardware neural network that already exists in nature: the brain.

Theme of my
research as faculty

Brain Inspired Spiking Neural Network (SNN)

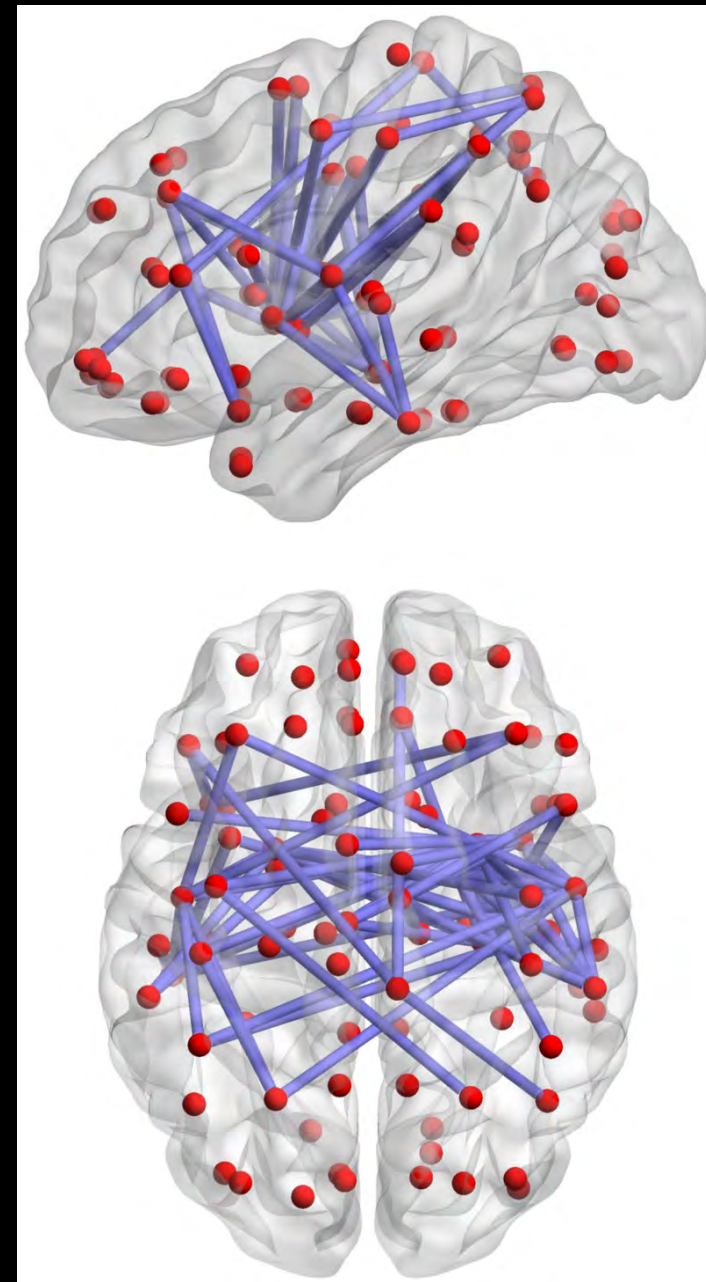


post-neuron

synapse

pre-neuron

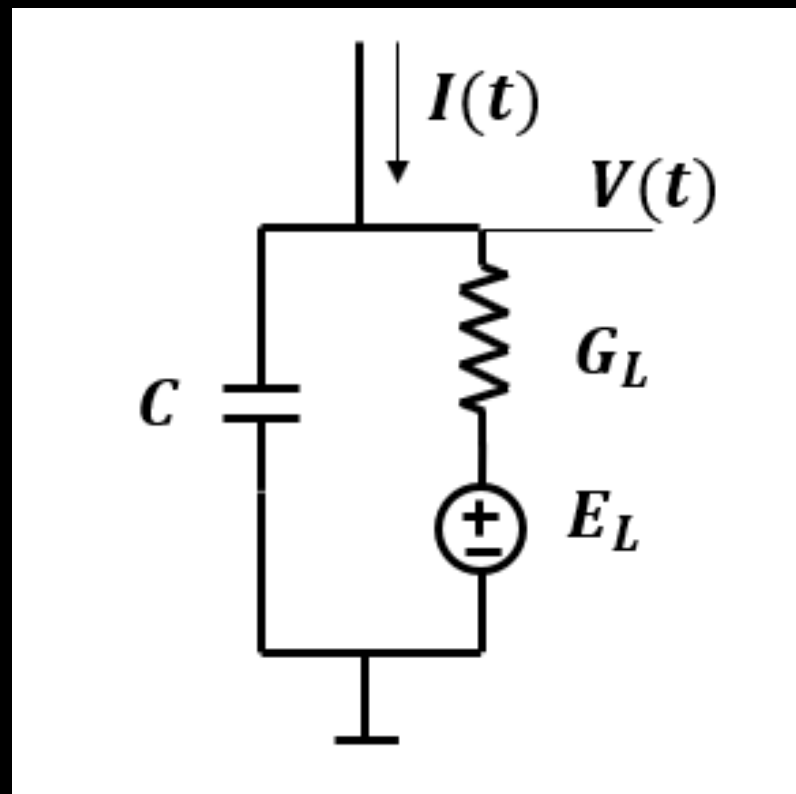
Neuron connected to another neuron
by synapse



10^{11} neurons interconnected through
 10^{15} synapses

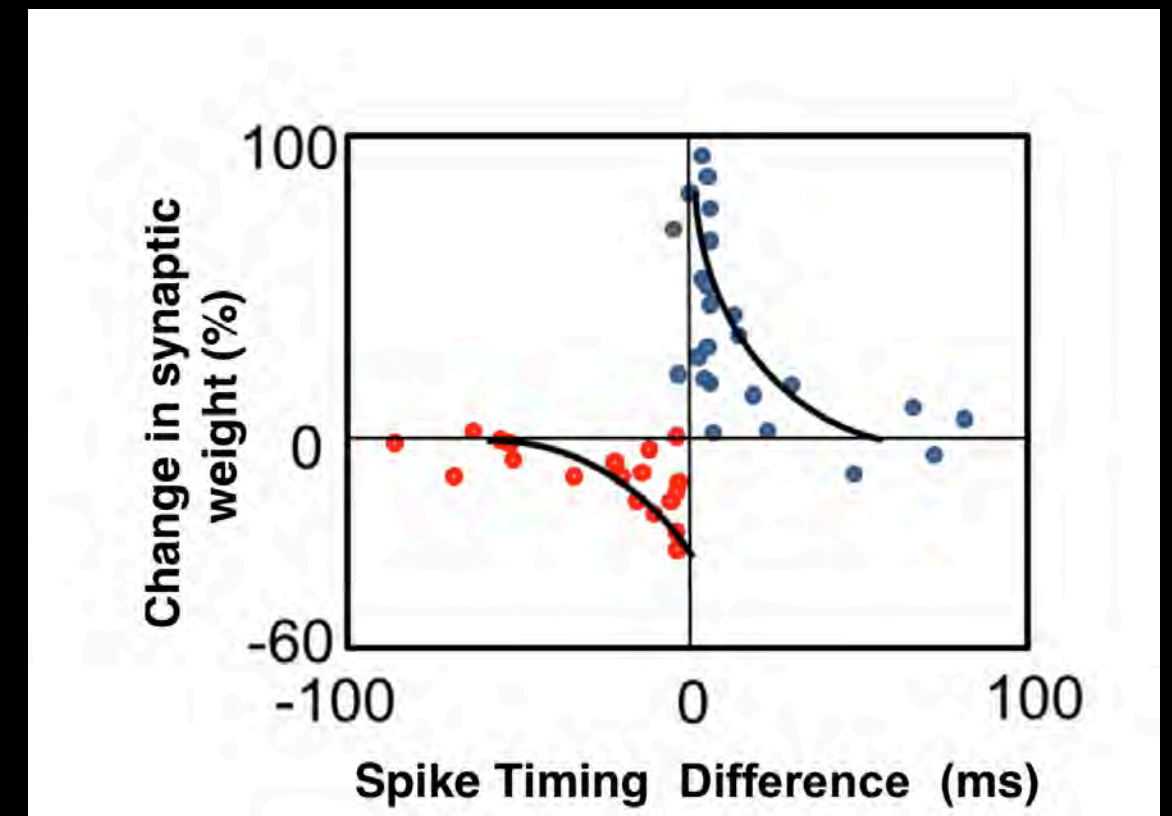
Brain Inspired Spiking Neural Network (SNN)

Model for neuron:
Leaky Integrate and Fire (LIF)



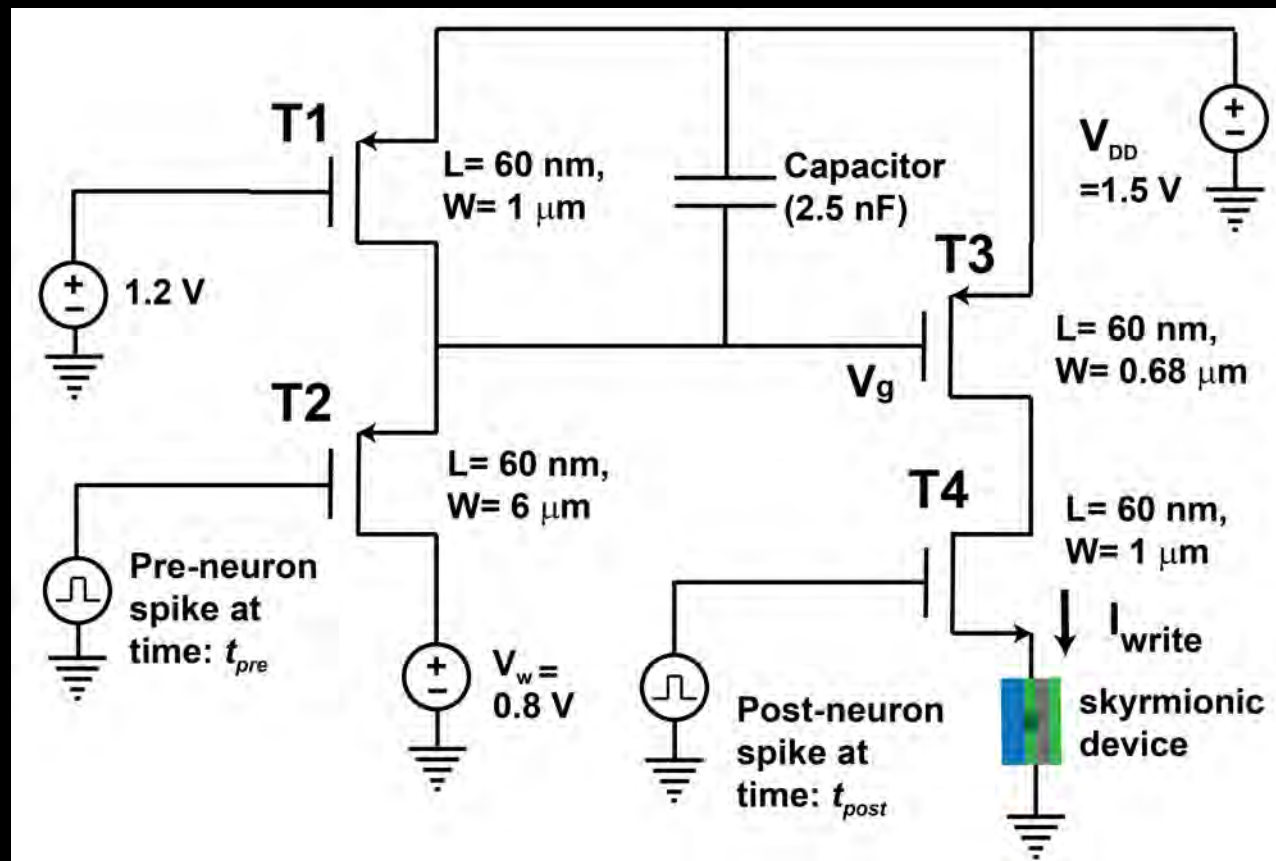
Whenever $V(t)$ reaches a threshold,
it spikes and goes back to rest
potential E_L

Model for synapse:
Spike Time Dependent Plasticity (STDP)

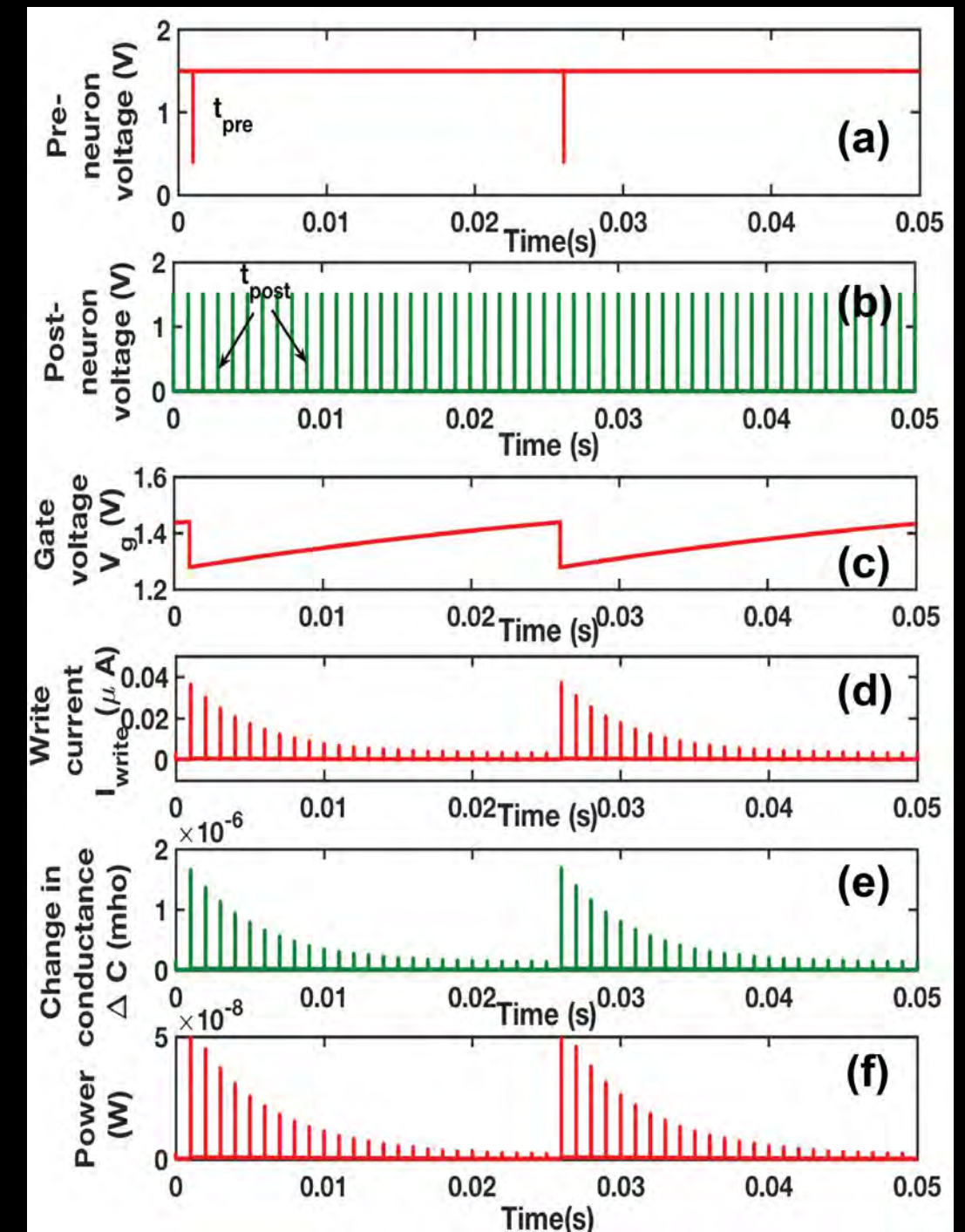


Data obtained from rat's hippocampus
(*Bi, Poo, J. Neuroscience 1998*)
Increase in weight of synapse decreases
exponentially with time gap between
pre- neuron and post neuron spike

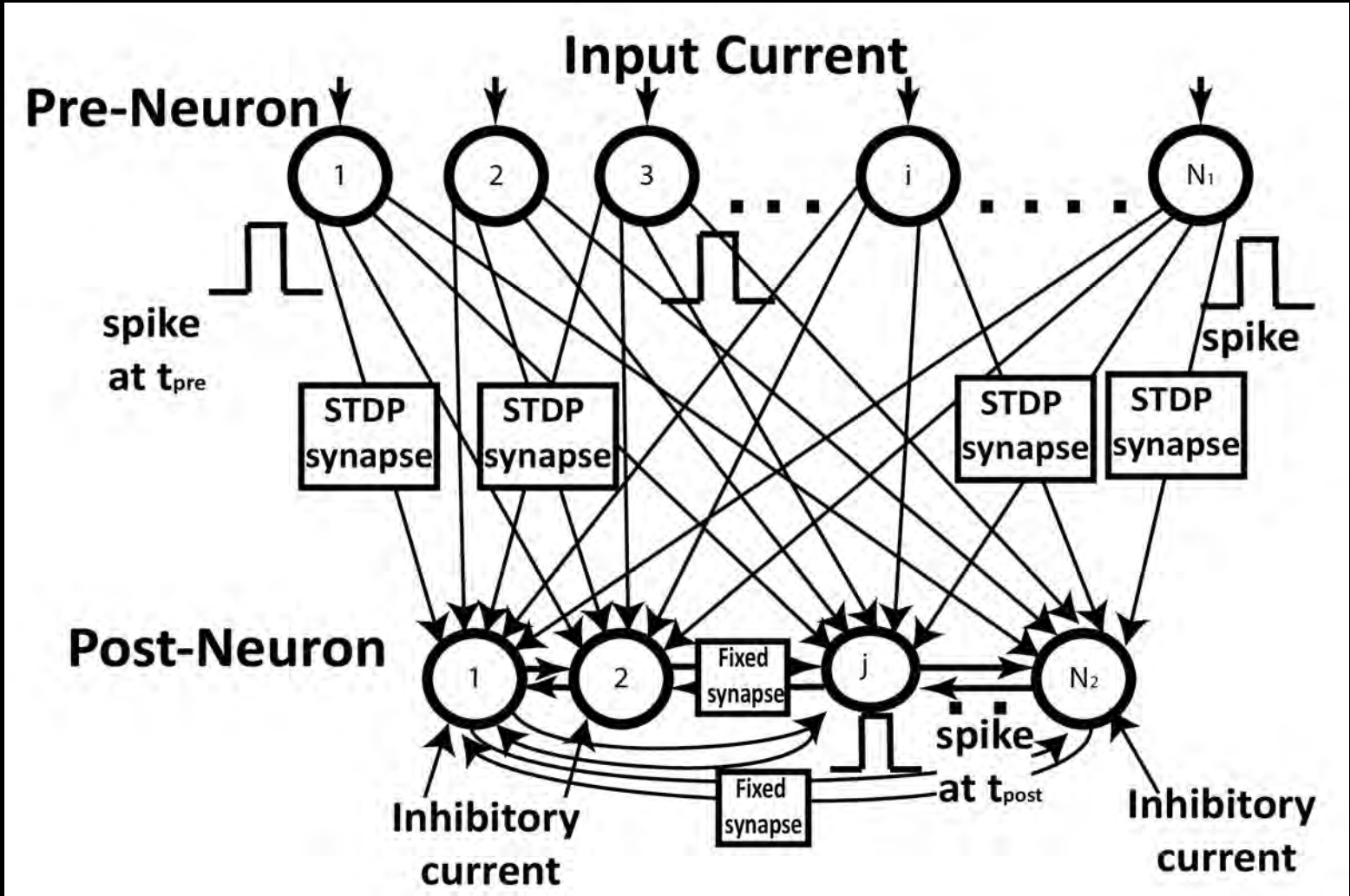
Design of spintronic- transistor circuit to emulate STDP



Since write current (I_{write}) decays exponentially with $(t_{post} - t_{pre})$ conductance decays exponentially too and so does weight of the synapse (STDP).



Design of spintronic- transistor circuit based STDP enabled SNN

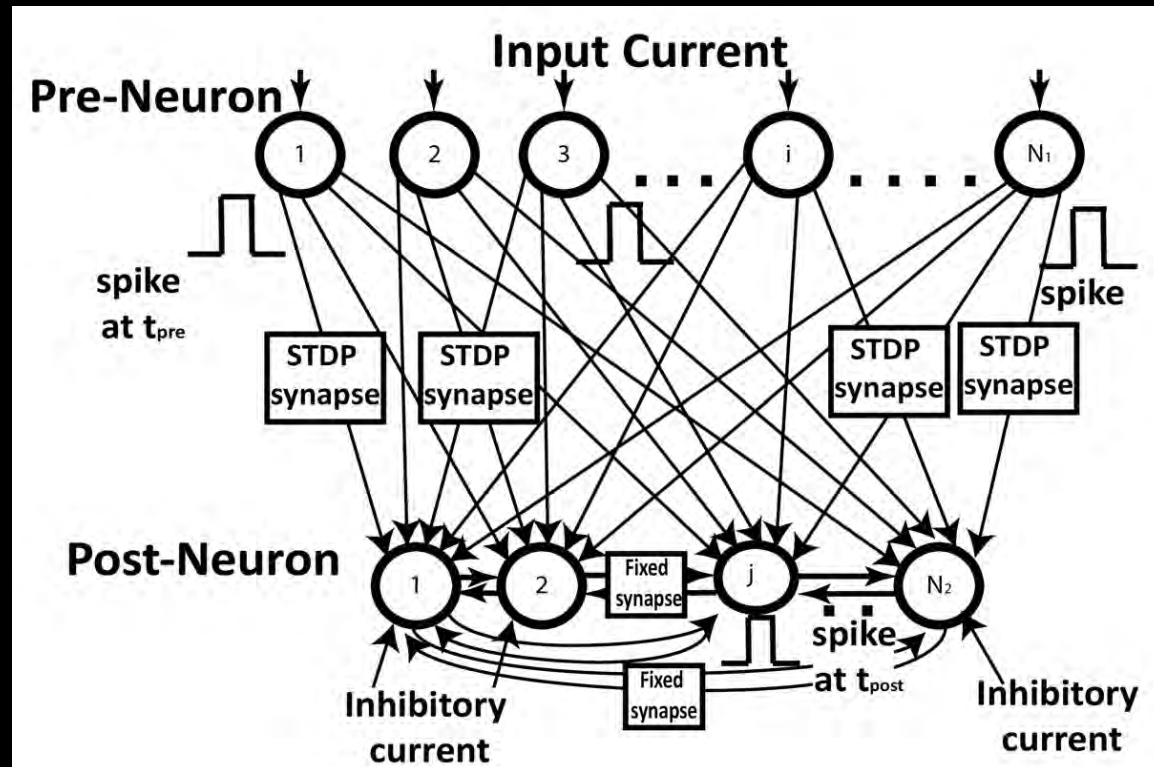


Performance on popular machine learning datasets:

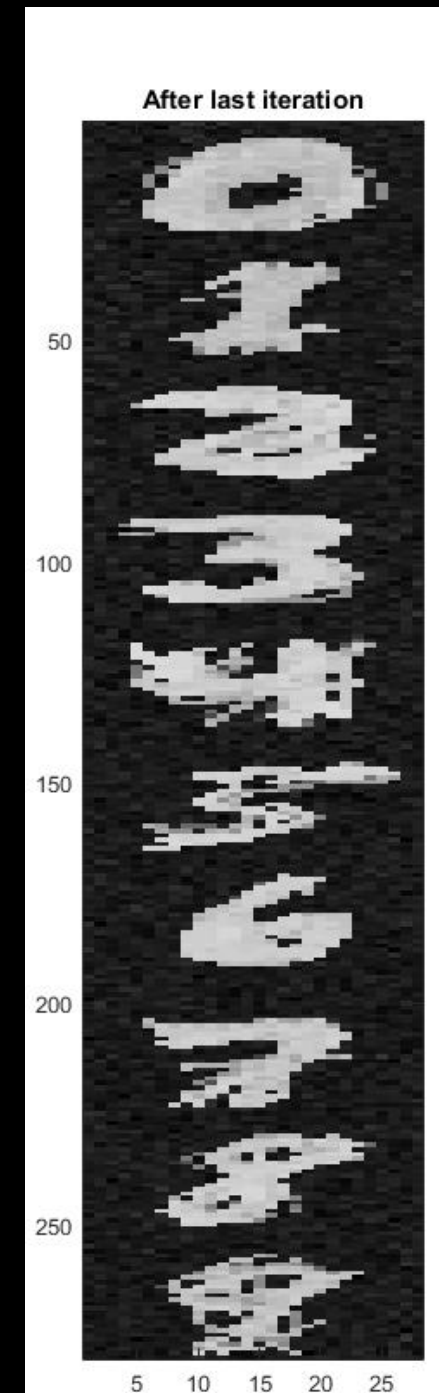
Dataset	Number of epochs	Training Accuracy(%)	Test accuracy(%)	Total Energy (nJ)	Average Energy per weight update (fJ)
Fisher's Iris	10	87	93	0.59	8.83
WBC	10	91	91	0.56	0.745

Results from
our research
group

Training STDP enabled SNN on MNIST dataset



Direct visualization of weights
of the synapses



100 train samples, 100 test samples.
50 epochs

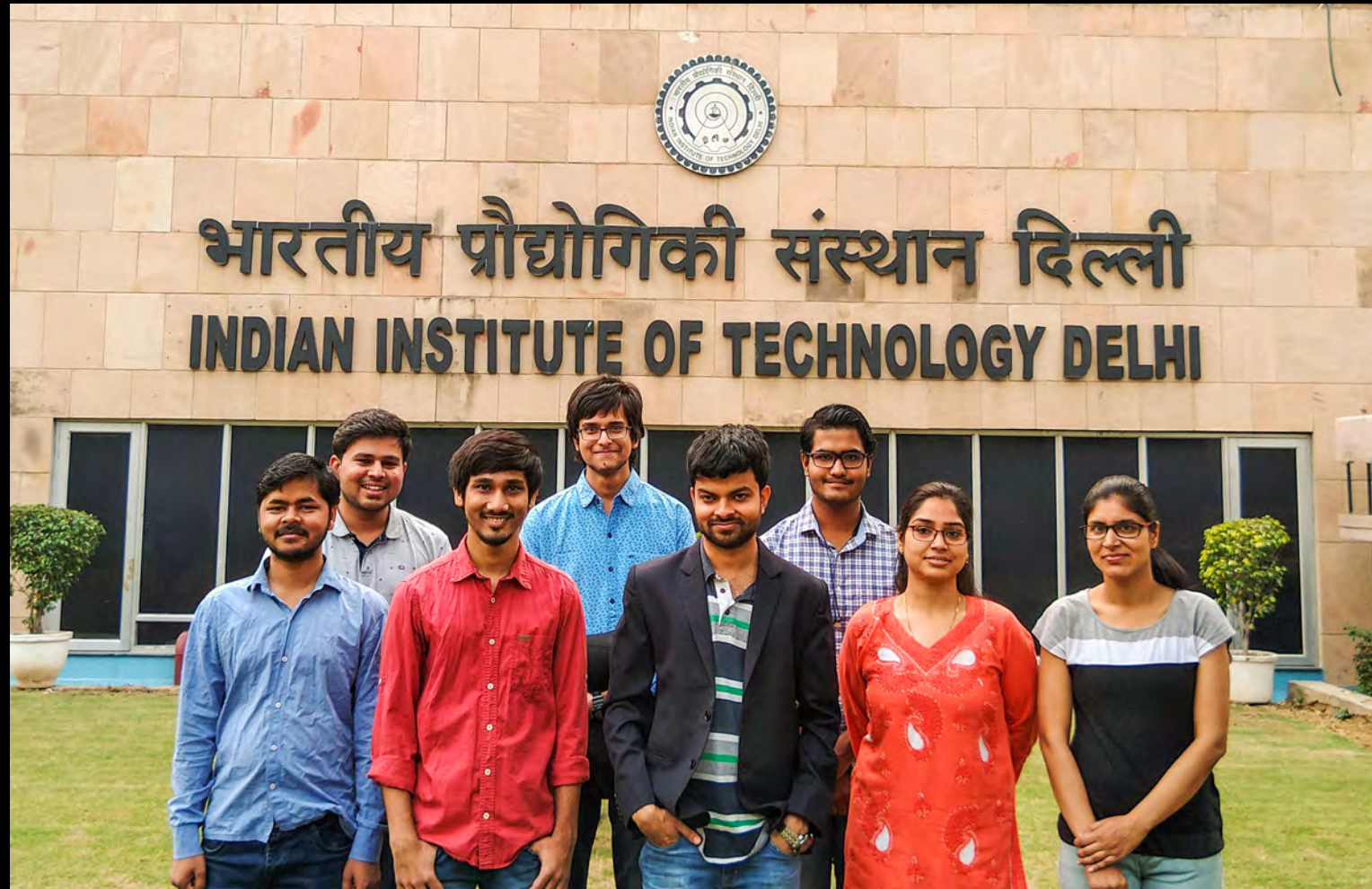
Train accuracy: 91 %
Test accuracy: 55%

In collaboration with Prof.
Udayan Ganguly, IIT Bombay

Summary of Results and Future Work

- Simulated spintronic synapse devices through micromagnetics and benchmarked them against experiments.
- Implemented in simulations on-chip learning of different types of neural networks using spintronics.
- Future goal: Fabricate and characterize such spintronic neural networks.
- Future goal: Explore more learning paradigms closer to actual functioning of the brain.

Natural and Artificial Intelligence Through Spintronics (NAITS) Group



Thanks to Indian Academy of Sciences
for the Associateship and organising the seminar

Thank you for you attention!