Implementation of Cmos Buffer Along With Multiplexer with Adder/Subtractor for Signal Shaping Operation

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***Abstract*—In this paper, An sine wave generator along with cmos buffer is used to generate signals. Output is fed to 4x1 multiplexer. An Adder/subtractor circuit is design to give either sum and carry or borrow and difference to input signals for mux. The output of mux signal is AND-ed with input signal for modifing signal according to mux output.**

I. Circuit Details

Sine wave is generated passed to cmos buffer to generate signals. Half Adder is the adder that adds two inputs and produces two outputs. The first 2 inputs are A and B . The output carry is designated as C-OUT and the normal output is designated as S which is SUM. A Half subtractor is a combinational circuit that performs subtraction of 2 bits, one is minuend and other is subtrahend, This circuit has two inputs and two outputs. The two inputs A, B denote the minuend and subtrahend respectively. The two outputs, D and Bout represent the difference and output borrow, respectively. This output is fed to 4x1Multiplexer. Multiplexer is a combinational circuit which has maximum of 2n data inputs, 'n' selection lines and single output line. Among these data inputs only one will be connected to the output based on the select line values. So, a 4x1 mux have 4 data input lines, 2 select lines and one output line. So, based on the output of input signals the corresponding data line is connected to the output line. This mux output is AND-ed with input signal. So based on select line either sum/difference or carry/borrow or remaining data lines will be AND-ed with input signal to produce desired output. Figure 1 shows the reference circuit diagram and Figure 2 shows the resultant waveforms.

II. Circuit Diagram

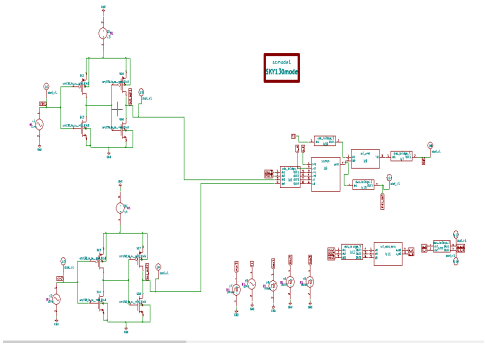

Figure 1. Circuit Diagram

III. Circuit Waveform

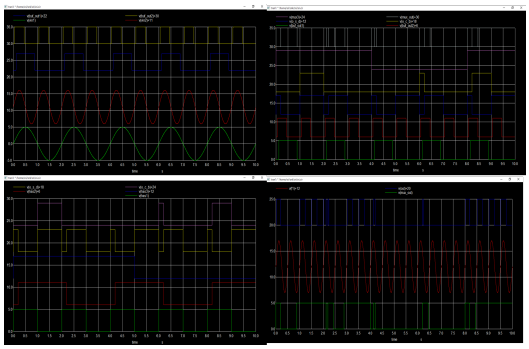

Figure 2. circuit waveform

References

[1] J. Park, J. Song, S. Lim and S. Kim, "A high speed and low power 41 multiplexer with cascoded clock control," 2010 IEEE Asia Pacific Conference on Circuits and Systems, 2010.
[2] https://www.geeksforgeeks.org/full-subtractor-in-digital-logic/