RISC-V cheatsheet

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By: Carl van Heezik

All RISC-V processors must implement the base integer instruction set known under the acronym RV32I. The encoding of RISC-V base integer instructions is 32 bits wide. A RISC-V processor has 32 general purpose x-registers and a program counter register. This cheatsheet shows an overview of the assembly instructions.

RISC-V registers

register	ABI	description
pc	pc	program counter

register	ABI	description	register	ABI	description
x0	zero	always zero	x16	a6	function argument 6
x1	ra	call return address	x17	a7	function argument 7
x2	sp	stack pointer	x18	s2	saved register 2
x3	gp	global pointer	x19	s3	saved register 3
x4	tp	thread pointer	x20	s4	saved register 4
x5	t0	temporary register 0	x21	s5	saved register 5
x6	t1	temporary register 1	x22	s6	saved register 6
x7	t2	temporary register 2	x23	s7	saved register 7
x8	s0	saved register 0	x24	s8	saved register 8
x9	s1	saved register 1	x25	s9	saved register 9
x10	a0	function argument 0	x26	s10	saved register 10
x11	a1	function argument 1	x27	s11	saved register 11
x12	a2	function argument 2	x28	t3	temporary register 3
x13	a3	function argument 3	x29	t4	temporary register 4
x14	a4	function argument 4	x30	t5	temporary register 5
x15	a5	function argument 5	x31	t6	temporary register 6

RV32I instructions

Acronyms

- xD : Destination register x0...x31
- xS : Source register x0...x31
- xL : Left register x0...x31
- xR : Right register x0...x31
- xB : Base register x0...x31

Register-register instructions

mnemonic	destination register	source 1 register	source 2 register	description
ADD	xD,	xL,	xR	Add
SUB	xD,	xL,	xR	Subtract
AND	xD,	xL,	xR	AND
OR	xD,	xL,	xR	OR
XOR	xD,	xL,	xR	XOR
SLT	xD,	xL,	xR	Set Less Than
SLTU	xD,	xL,	xR	Set Less Than Unsigned
SLL	xD,	xL,	xR	Shift Left Logical
SRL	xD,	xL,	xR	Shift Right Logical
SRA	xD,	xL,	xR	Shift Right Arithmetic

Immediate instructions

mnemonic	destination register	source 1 register	immediate	description
ADDI	xD,	xL,	CONSTANT	Add Immediate
ANDI	xD,	xL,	CONSTANT	AND Immediate
ORI	xD,	xL,	CONSTANT	OR Immediate
XORI	xD,	xL,	CONSTANT	XOR Immediate
SLTI	xD,	xL,	CONSTANT	Set Less Than Immediate
SLLI	xD,	xL,	SHIFT	Shift Left Logical Immediate
SRLI	xD,	xL,	SHIFT	Shift Right Logical Immediate
SRAI	xD,	xL,	SHIFT	Shift Right Arithmetic Immediate

Conditional branches

mnemonic	source 1 register	source 2 register	immediate	description
BEQ	xL,	xR,	OFFSET	Branch Equal
BNE	xL,	xR,	OFFSET	Branch Not Equal
BLT	xL,	xR,	OFFSET	Branch Less Than
BGE	xL,	xR,	OFFSET	Branch Greater Equal
BLTU	xL,	xR,	OFFSET	Branch Less Than Unsigned
BGEU	xL,	xR,	OFFSET	Branch Greater Equal Unsigned

Upper immediate instructions

mnemonic	destination register	immediate		description
LUI	xD,	UPPER		Load Upper Immediate
AUIPC	xD,	UPPER		Add Upper Immediate to PC

Unconditional jumps

mnemonic	destination register	immediate		description
JAL	xD,	OFFSET		Jump AND Link

Indirect jump instruction

mnemonic	destination register	source 1 register	immediate	description
JALR	xD,	xL,	OFFSET	Jump and Link Register

Load and store instruction

mnemonic	destination register	immediate	source 1 register	description
LB	xD,	OFFSET	(xB)	Load Byte
LH	xD,	OFFSET	(xB)	Load Half
LW	xD,	OFFSET	(xB)	Load word
LBU	xD,	OFFSET	(xB)	Load Byte Unsigned
LHU	xD,	OFFSET	(xB)	Load Half Unsigned

mnemonic	source 2 register	immediate	source 1 register	description
SB	xS,	OFFSET	(xB)	Store Byte
SH	xS,	OFFSET	(xB)	Store Half
SW	xS,	OFFSET	(xB)	Store word
SBU	xS,	OFFSET	(xB)	Store Byte Unsigned
SHU	xS,	OFFSET	(xB)	Store Half Unsigned

Memory ordering instructions

mnemonic	predecessor	successor		description
FENCE	IORW,	IORW		Fence
FENCE.I				Fence instruction

RV32I encoding

[31:25] 7	[24:20] 5	[19:15] 5	[14:12] 3	[11:7] 5	[6:0] 7
function 7	source 2	source 1	function 3	destination	opcode
0000000	xR	xL	000 : ADD	xD	0110011 : OP
0100000	xR	xL	000 : SUB	xD	0110011 : OP
0000000	xR	xL	001 : SLL	xD	0110011 : OP
0000000	xR	xL	010 : SLT	xD	0110011 : OP
0000000	xR	xL	011 : SLTU	xD	0110011 : OP
0000000	xR	xL	100 : XOR	xD	0110011 : OP
0000000	xR	xL	101 : SRL	xD	0110011 : OP
0100000	xR	xL	101 : SRA	xD	0110011 : OP
0000000	xR	xL	110 : OR	xD	0110011 : OP
0000000	xR	xL	111 : AND	xD	0110011 : OP

[31:20] 12	[19:15] 5	[14:12] 3	[11:7] 5	[6:0] 7
IMMEDIATE[11:0]	source 1	function 3	destination	opcode
CONSTANT[11:0]	xL	000 : ADDI	xD	0010011 : OP-IMM
CONSTANT[11:0]	xL	010 : SLTI	xD	0010011 : OP-IMM
CONSTANT[11:0]	xL	011 : SLTIU	xD	0010011 : OP-IMM
CONSTANT[11:0]	xL	100 : XORI	xD	0010011 : OP-IMM
CONSTANT[11:0]	xL	110 : ORI	xD	0010011 : OP-IMM
CONSTANT[11:0]	xL	111 : ANDI	xD	0010011 : OP-IMM

[31:25] 7	[24:20] 5	[19:15] 5	[14:12] 3	[11:7] 5	[6:0] 7
IMMEDIATE[11:5]	IMMEDIATE[4:0]	source 1	function 3	destination	opcode
0000000	SHIFT	xL	001 : SLLI	xD	0010011 : OP-IMM
0000000	SHIFT	xL	101 : SRLI	xD	0010011 : OP-IMM
0100000	SHIFT	xL	101 : SRAI	xD	0010011 : OP-IMM

[31] 1	[30:25] 6	[24:20] 5	[19:15] 5	[14:12] 3	[11:8] 4	[7] 1	[6:0] 7
I[12]	I[10:5]	source 2	source 1	function 3	I[4:1]	I[11]	opcode
O[12]	O[10:5]	xR	xL	000 : BEQ	O[4:1]	O[11]	1100011 : BRANCH
O[12]	O[10:5]	xR	xL	001 : BNE	O[4:1]	O[11]	1100011 : BRANCH
O[12]	O[10:5]	xR	xL	100 : BLT	O[4:1]	O[11]	1100011 : BRANCH
O[12]	O[10:5]	xR	xL	101 : BGE	O[4:1]	O[11]	1100011 : BRANCH
O[12]	O[10:5]	xR	xL	110 : BLTU	O[4:1]	O[11]	1100011 : BRANCH
O[12]	O[10:5]	xR	xL	111 : BGEU	O[4:1]	O[11]	1100011 : BRANCH

[31:12] 20	[11:7] 5	[6:0] 7
IMMEDIATE[31:12]	destination	opcode
UPPER[31:12]	xD	0110111 : LUI
UPPER[31:12]	xD	0010111 : AUIPC

[31] 1	[30:21] 10	[20] 1	[19:12] 8	[11:7] 5	[6:0] 7
I[20]	I[10:1]	I[11]	IMMEDIATE[19:12]	destination	opcode
O[20]	O[10:1]	O[11]	O[19:12]	xD	1101111 : JAL

[31:20] 12	[19:15] 5	[14:12] 3	[11:7] 5	[6:0] 7
IMMEDIATE[11:0]	source 1	function 3	destination	opcode
OFFSET[11:0]	xL	0	xD	1100111 : JALR

[31:20] 12	[19:15] 5	[14:12] 3	[11:7] 5	[6:0] 7
IMMEDIATE[11:0]	source 1	function 3	destination	opcode
OFFSET[11:0]	xB	000 : LB	xD	0000011 : LOAD
OFFSET[11:0]	xB	001 : LH	xD	0000011 : LOAD
OFFSET[11:0]	xB	010 : LW	xD	0000011 : LOAD
OFFSET[11:0]	xB	100 : LBU	xD	0000011 : LOAD
OFFSET[11:0]	xB	101 : LHU	xD	0000011 : LOAD

[31:25] 7	[24:20] 5	[19:15] 5	[14:12] 3	[11:7] 5	[6:0] 7
IMMEDIATE[11:5]	source 2	source 1	function 3	IMMEDIATE[4:0]	opcode
OFFSET[11:5]	xS	xB	000 : SB	OFFSET	0100011 : STORE
OFFSET[11:5]	xS	xB	001 : SH	OFFSET	0100011 : STORE
OFFSET[11:5]	xS	xB	010 : SW	OFFSET	0100011 : STORE
OFFSET[11:5]	xS	xB	100 : SBU	OFFSET	0100011 : STORE
OFFSET[11:5]	xS	xB	101 : SHU	OFFSET	0100011 : STORE

[31:28] 4	[27] 1	[26] 1	[25] 1	[24] 1	[23] 1	[22] 1	[21] 1	[20] 1	[19:15] 5	[14:12] 3	[11:7] 5	[6:0] 7
FM	PI	PO	PR	PW	SI	SO	SR	SW	source 1	function 3	destination	opcode
0000	PI	PO	PR	PW	SI	SO	SR	SW	00000	000: FENCE	00000	0001111 : MISC-MEM
0000	0	0	0	0	0	0	0	0	00000	001: FENCE.I	00000	0001111 : MISC-MEM

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