Note:

- Technology $\lambda = 11nm$.
- Model File: 22nm PTM
- Assignments are to be submitted individually
- Project is to be done in groups of three
- Reference CMOS Inverter : NMOS $W/L = 4\lambda/2\lambda$ and PMOS $W/L = 8\lambda/2\lambda$
- V_{DD} and GND lines are to be laid out in Metal-2/3 with a standard cell height of 50λ

Problem Statement

Design a signed 8 bit carry save multiplier with a single stage pipeline. The idea is to show that the frequency of operation can be doubled and data can be fed to the multiplier at twice the rate through pipelining. This would require the following components

- NAND2/ AND2 gate
- Full adder
  - Carry out generation circuit
  - Sum generation circuit
- Flip flop for pipelining

You have built your library with the above components and submitted each one as an assignment. Now you need to put them together and make the top level circuit.

1 Final Submission: 8 Bit Multiplier Design with and without Pipelining - Due 26 Nov 2021

Using the CSM that you have built, show that you can approximately double the operating clock frequency of a pipelined CSM by suitably inserting a flop at the right location as shown in the figure below.

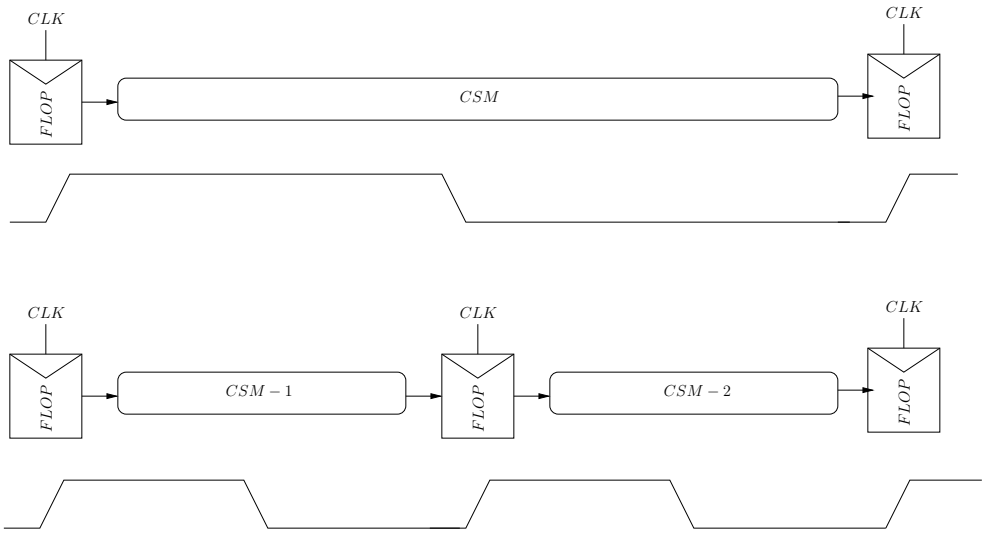
1.1 Deliverables

- Transistor schematic of an 8 bit signed multiplier, with and without pipelining, with the components you built
- DRC and LVS clean layout of the CSM without pipeline flops.

1.2 Submission - To be shown to your TA

The complete ELECTRIC library(.jelib) with

- Schematic of the 8 bit Carry Save Multipler (CSM) without a pipeline
- Schematic of the 8 bit CSM with a single stage pipeline
- Schematic and layout of all sub blocks from previous assignments - DRC and LVS clean. Flip flop does not need a layout.



- DRC and LVS clean CSM without pipeline
- SPICE simulation of one test pattern that exercises the critical path with
  - Schematic only
  - Top level schematic + RC-extracted netlist for all sub-blocks
- Alternate adder schematics to speed up the final Vector Merging- Layout not necessary

1.3 Submission - To be uploaded on Moodle

A single PDF with

- A table summarizing the following information
  - Maximum clock frequency w/o pipelining for the schematic and the layout extracted netlist
  - Maximum clock frequency with pipelining using the layout extracted netlist
  - Area of the DRC and LVS clean CSM.
  - Number of test patterns you verified the functionality of your CSM against
- Block diagram of the 8 bit Carry Save Multipler (CSM) - Highlight how you used inverting and non-inverting adders to optimize delay
- Area of the CSM layout
- Maximum operating frequency of the CSM (without Pipeline)
- Location of the flip flop to double the frequency of operation
- SPICE simulation showing the frequency of operation with and without pipelining using RC extracted netlists for all sub-blocks (you should have the layout of all sub-blocks)
- Input combinations that you tested your CSM to see if it's functionally correct - Showing different kinds of multiplications
- SPICE simulations showing how the use of a faster adder in the Vector merge stage sped up over all delay of the CSM.

1.4 Evaluation Rubric

Table 1 explains how the projects will be graded. To understand this table, read column-wise to figure out the bar for your submission in order to be rated accordingly. For example, a Good project should necessarily

- Be functional and verified against carefully chosen input combinations to check various signed multiplication cases
- Pass DRC and LVS for all sub-blocks
- Use inverting adders to optimize for delay
- Have a delay of the extracted netlist being about $2-3X$ of the schematic simulation - This is a measure of your layout efficiency
- Use pipelining with the flip flops placed in the correct location
- Nearly allow doubling of the clock frequency - 1.5X - 2X is also acceptable

Metric	Very Poor	Poor	Fair	Good	Excellent
#Test patterns to verify Functionality	Not Functional	0	1	Carefully chosen input combinations	Carefully chosen input combinations
Cell DRC and LVS	No Layout	Fail	Pass	Pass	Pass
CSM LVS	No Layout	Fail	Pass	Pass	Pass
CSM DRC	No Layout	Fail	Pass	Pass	Pass
Use of Inverting Adders	Not used	Not Used	Used	Used	Used
Extracted netlist delay vs Schematic delay	N.A	$> 5X$	$3-5X$	$2-3X$	$1-2X$
Pipelining	No	No	Used but not optimally	Used correctly	Used correctly
Max Clock Frequency with and w/o Pipelining	N.A	N.A.	$1-1.5X$	$1.5-2X$	$1.5-2X$
Alternate Vector Merge Adders	-	-	-	-	Yes
Other optimization	-	-	-	-	Yes

Table 1: Rubric for Project Evaluation