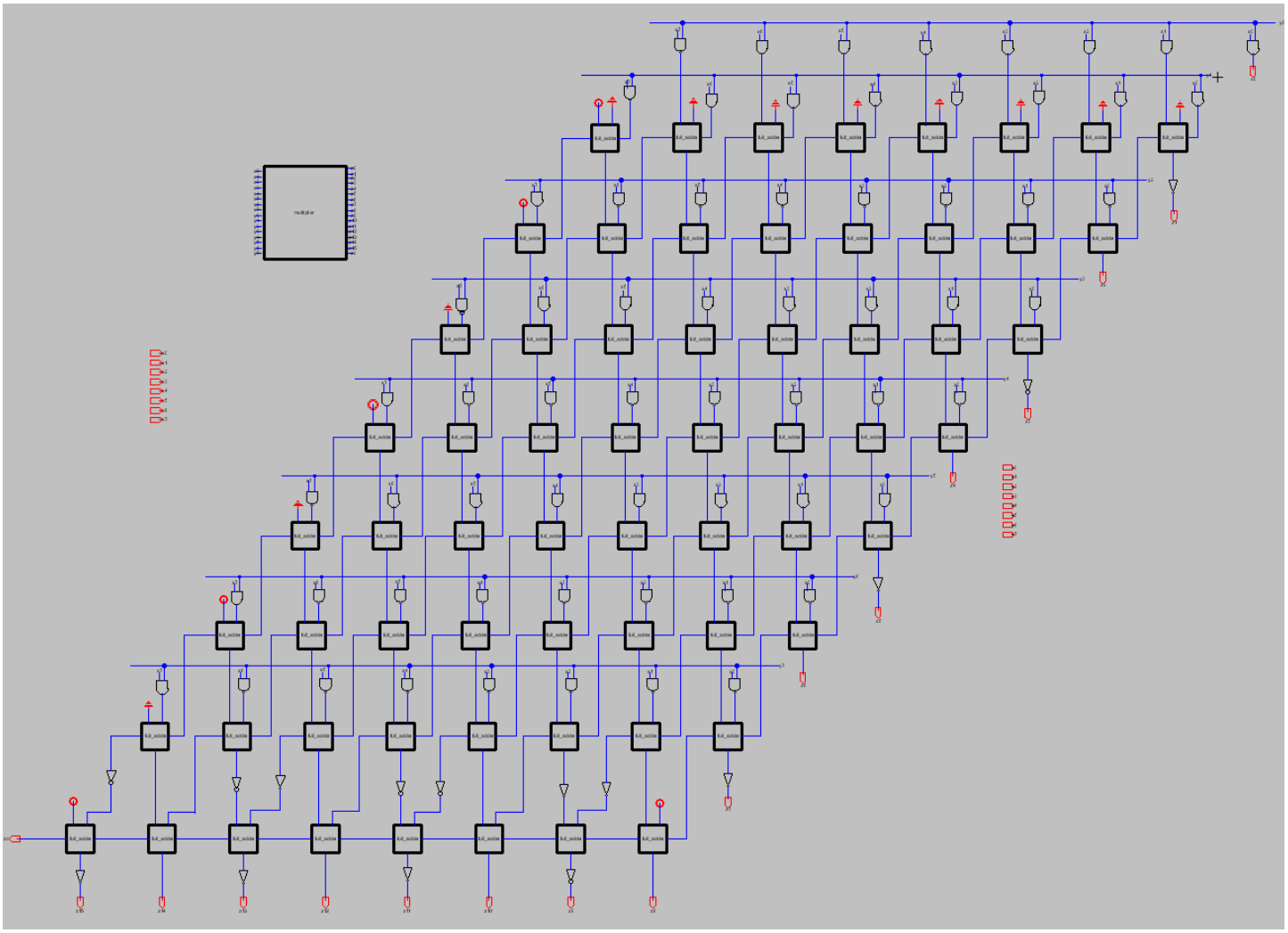
EE5311 - Digital IC Design

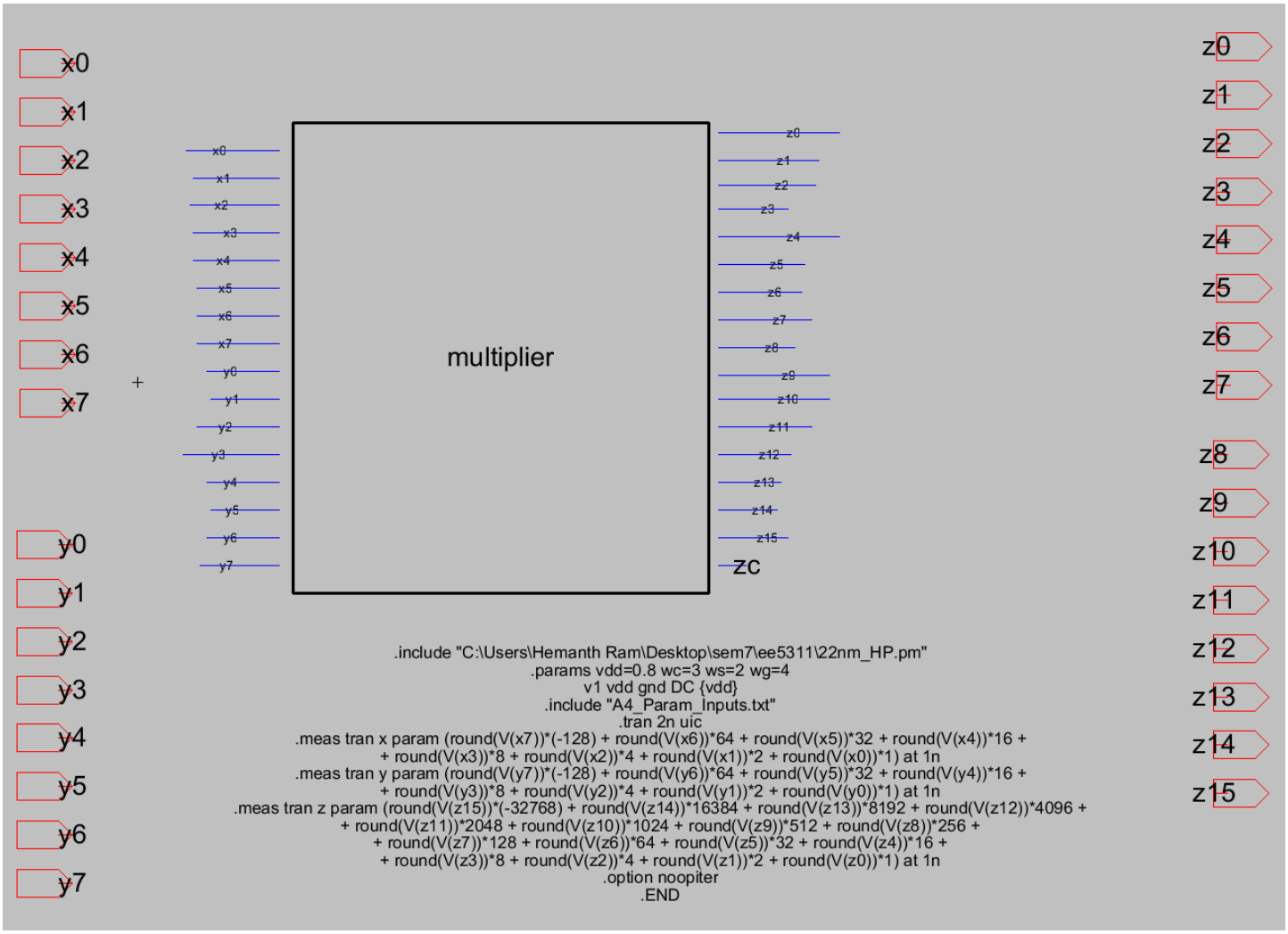
Assignment 4 - Schematic of a signed 8-bit Carry Save Multiplier

Member 1: Srivenkat A(EE18B038)
Member 2: Hemanth Ram G K(EE18B132)
Member 3: Sidesh S(EE18B032)

Schematic of CSM

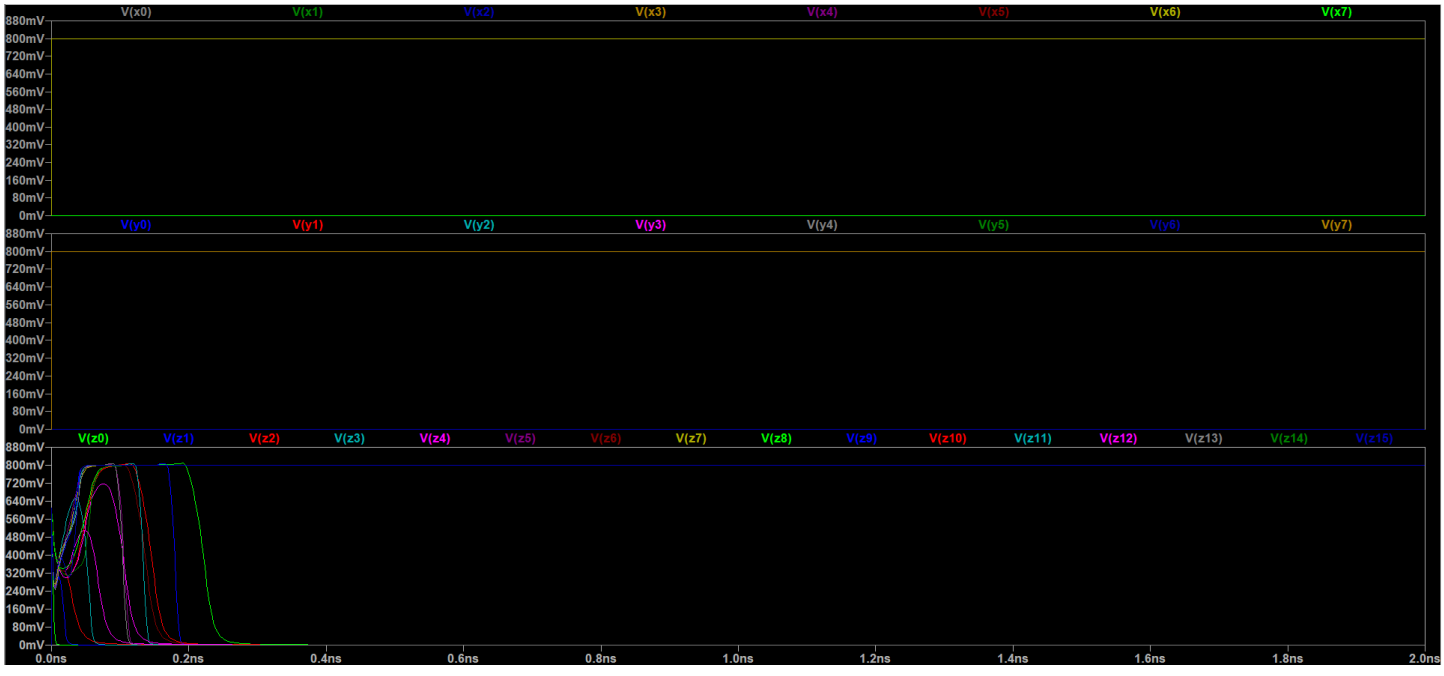


Multiplier Testbench




```
.include "C:\Users\Hemanth Ram\Desktop\sem7\ee5311\22nm_HP.pm"
.params vdd=0.8 wc=3 ws=2 wg=4
v1 vdd gnd DC {vdd}
.include "A4_Param_Inputs.txt"
.tran 2n uic
.meas tran x param (round(V(x7))*(-128) + round(V(x6))*64 + round(V(x5))*32 + round(V(x4))*16 +
+ round(V(x3))*8 + round(V(x2))*4 + round(V(x1))*2 + round(V(x0))*1) at 1n
.meas tran y param (round(V(y7))*(-128) + round(V(y6))*64 + round(V(y5))*32 + round(V(y4))*16 +
+ round(V(y3))*8 + round(V(y2))*4 + round(V(y1))*2 + round(V(y0))*1) at 1n
.meas tran z param (round(V(z15))*(-32768) + round(V(z14))*16384 + round(V(z13))*8192 + round(V(z12))*4096 +
+ round(V(z11))*2048 + round(V(z10))*1024 + round(V(z9))*512 + round(V(z8))*256 +
+ round(V(z7))*128 + round(V(z6))*64 + round(V(z5))*32 + round(V(z4))*16 +
+ round(V(z3))*8 + round(V(z2))*4 + round(V(z1))*2 + round(V(z0))*1) at 1n
.option noopiter
.END
```

Simulation output for 127 * -128



Interpreted voltage values for 127 * -128

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=127
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=-128
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 +  round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 +  round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 +  round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 + round(v(z0))*1)=-
16256
```

Interpreted voltage values for -128 * 127

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=-128
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=127
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 +  round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 +  round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 +  round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 + round(v(z0))*1)=-
16256
```

Interpreted voltage values for 0 * 127

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=0
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=127
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 +  round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 +  round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 +  round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 + round(v(z0))*1)=0
```

Interpreted voltage values for -128 * 0

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=-128
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=0
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 +  round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 +  round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 +  round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 + round(v(z0))*1)=0
```

Interpreted voltage values for -12 * 13

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=-12
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=13
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 +  round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 +  round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 +  round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 + round(v(z0))*1)=-
156
```

Interpreted voltage values for -1 * -1

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=-1
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=-1
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 +  round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 +  round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 +  round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 + round(v(z0))*1)=1
```

Interpreted voltage values for -128 * -128

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=-128
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=-128
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 +  round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 +  round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 +  round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 +
round(v(z0))*1)=16384
```

Interpreted voltage values for 103 * -57

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=103
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=-57
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 +  round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 +  round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 +  round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 + round(v(z0))*1)=-
5871
```

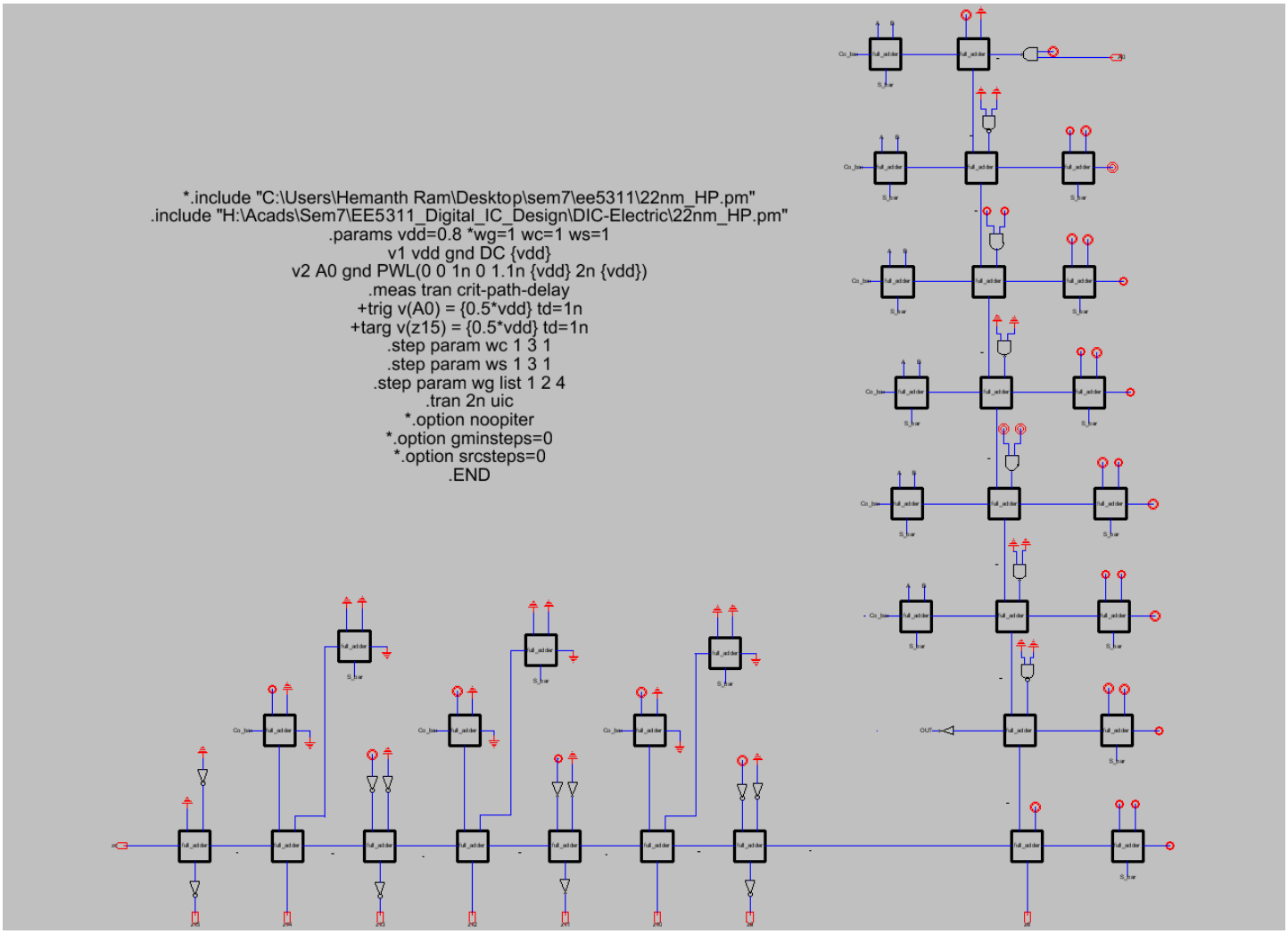
Interpreted voltage values for -50 * 50

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=-50
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=50
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 +  round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 +  round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 +  round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 + round(v(z0))*1)=-
2500
```

Interpreted voltage values for 79 * 81

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=79
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=81
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 +  round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 +  round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 +  round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 +
round(v(z0))*1)=6399
```

Critical Path of CSM modelled separately



Inputs to Full Adders in Critical Path

1. Input A is closer than B to output and critical input is connected to A in every full adder.
2. For an edge in A, sum delay for different combinations of B, Ci in a Full Adder:

Inputs to (B, Cin) \ Edge Type	Rising	Falling
00	48.9ps	75.7ps
01	25.9ps	106ps
10	133ps	129ps
11	99.9ps	29.5ps

So, for both rising/falling edge in A, B=1, Cin=0 for max delay in sum propagation

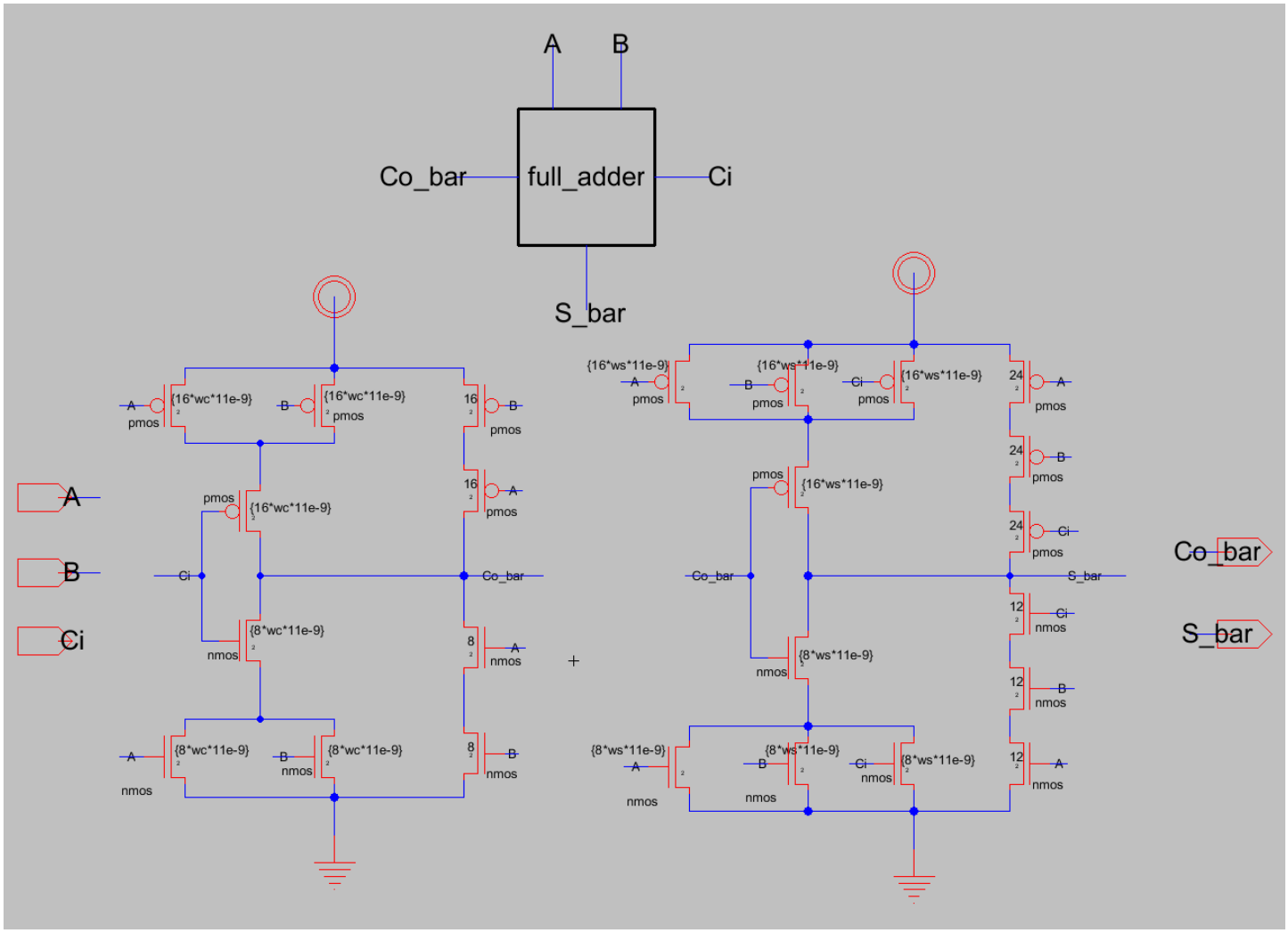
3. For an edge in Carry in, Full Adder should be in propagation stage for max delay. Delays for different combinations of A/B in Full Adder:

Inputs to (A, B) \ Edge Type	Rising	Falling
01	29.9ps	10.6ps
10	28.4ps	10.5ps

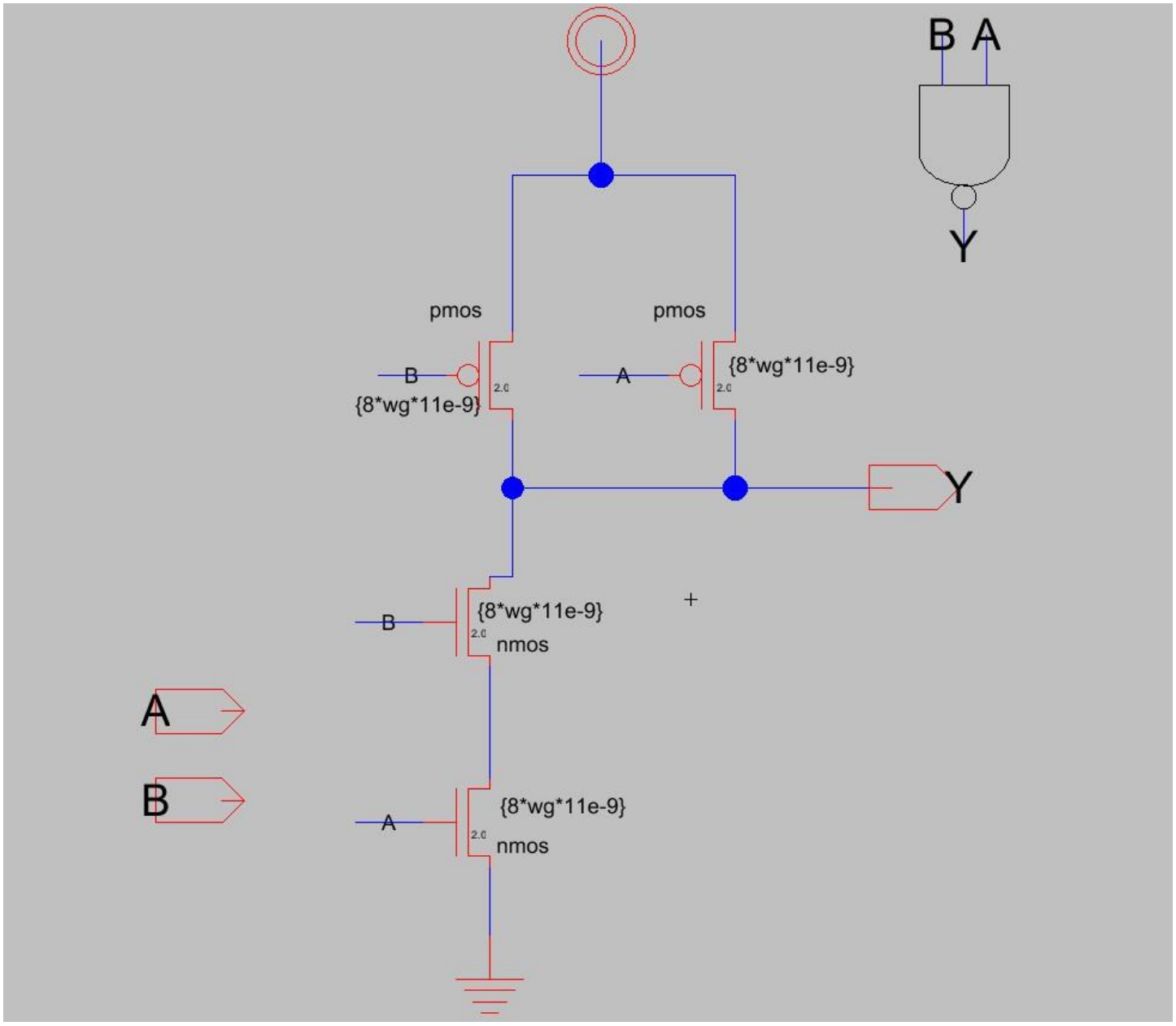
So, for rising/falling edge in Cin, A=0, B=1 for max delay in carry propagation

Sizes of FA, NAND, AND and INV gates used are parameterised

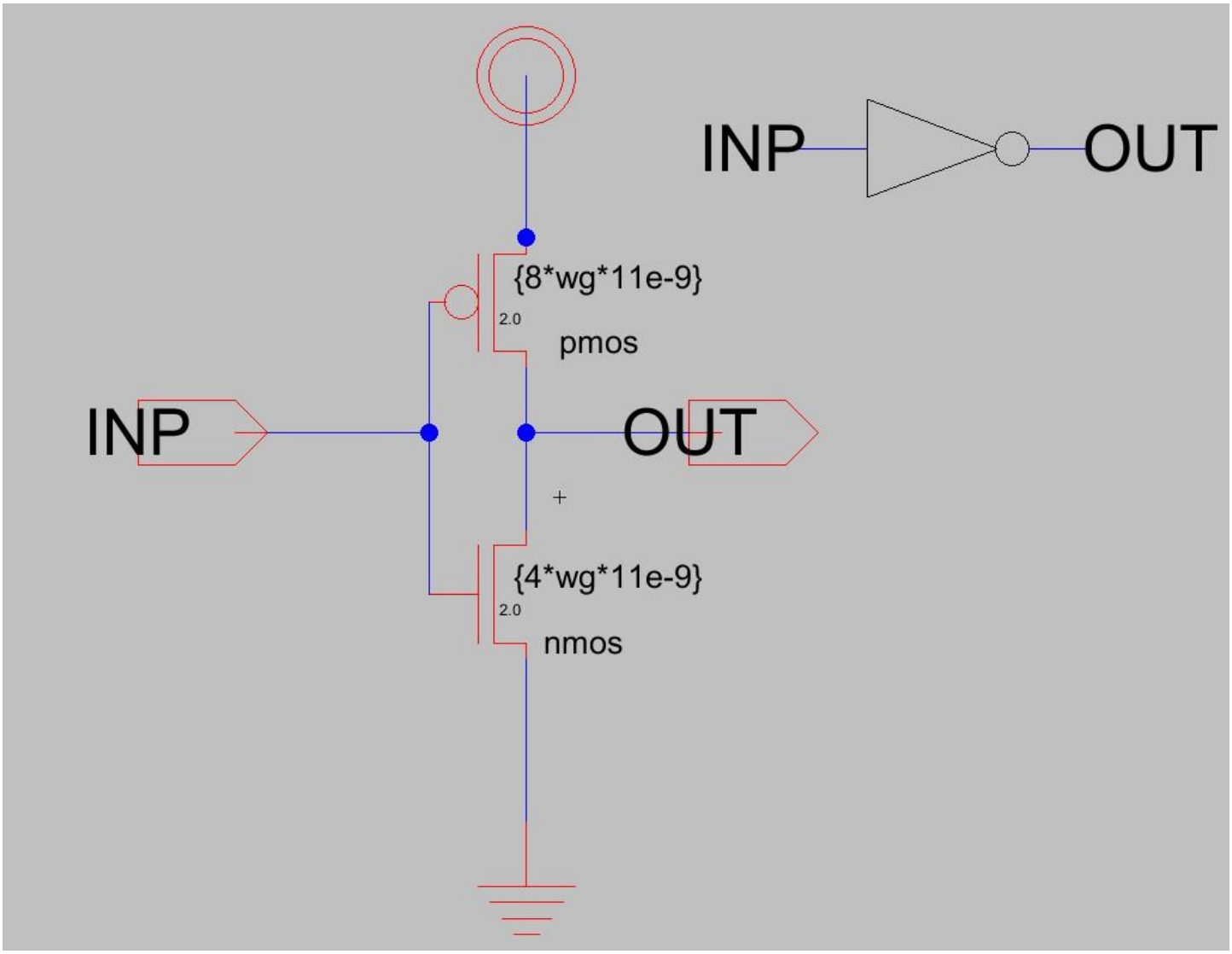
Schematic of Full Adder used



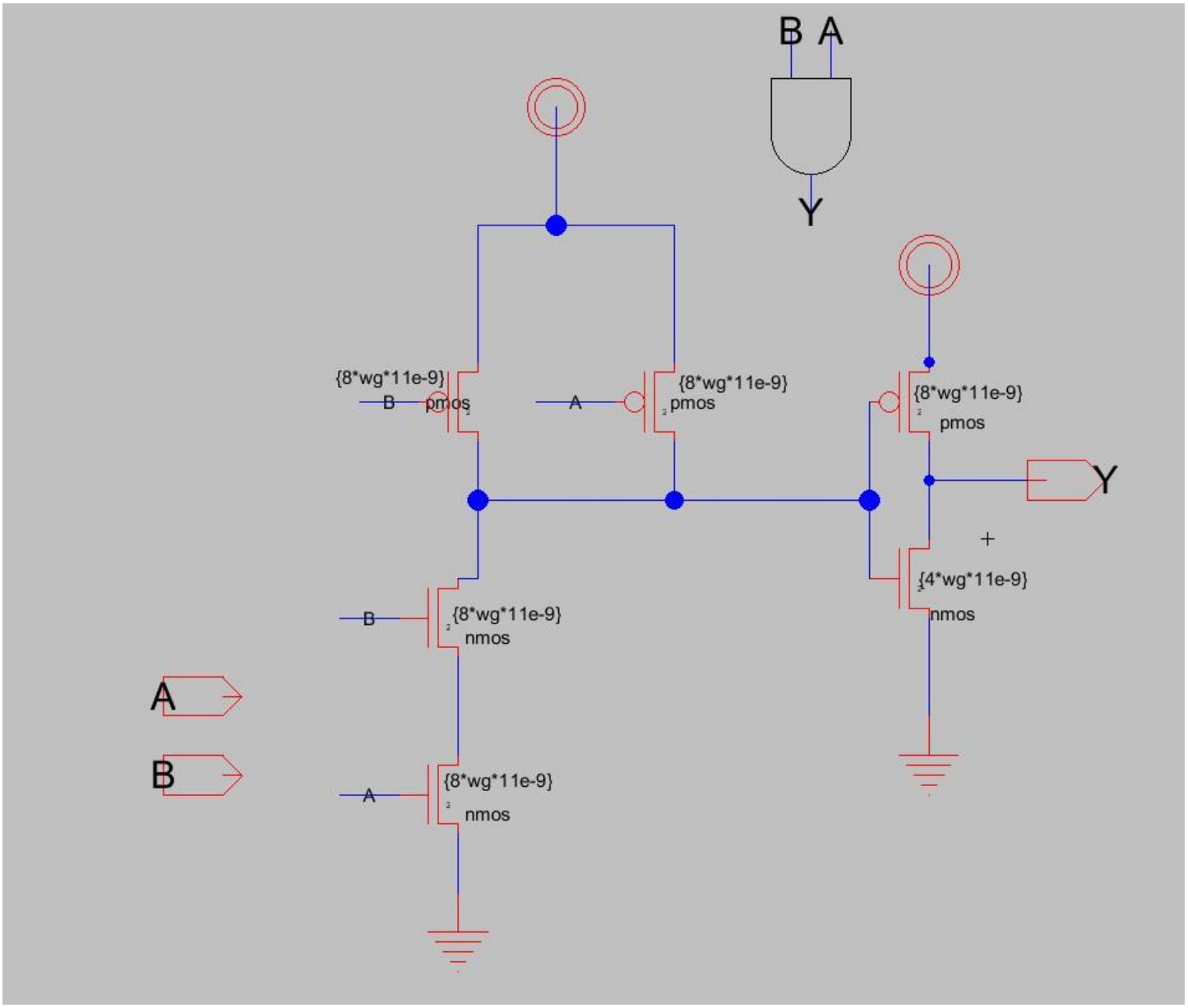
Schematic of NAND gate used



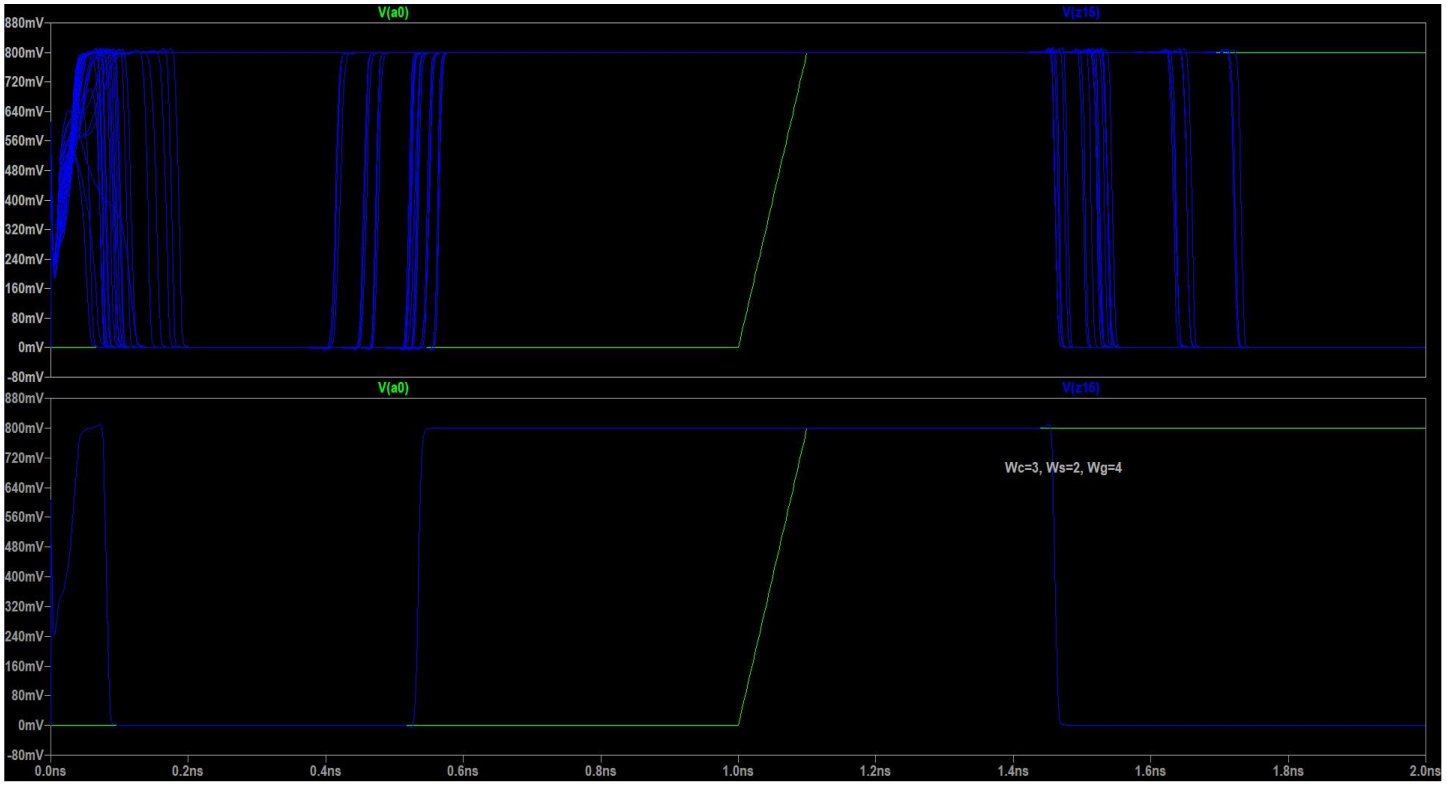
Schematic of Inverter used



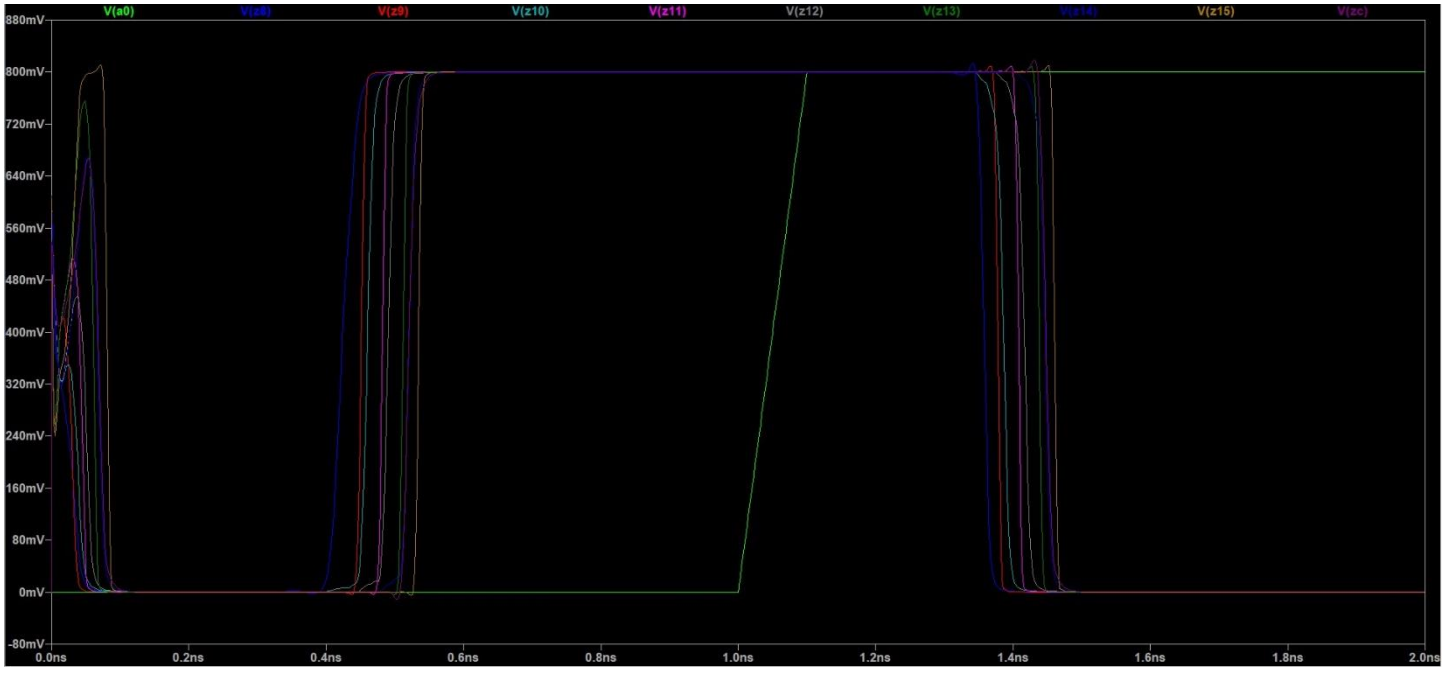
Schematic of AND gate used



Simulation of Critical Path Delay swept across possible gate size combinations



Simulation of Vector Merge outputs for critical input



Critical Path Delay tabulated across gate size combinations

step				crit-path-delay	FROM	TO
1	wc=1	ws=1	wg=1	5.87E-10	1.05E-09	1.64E-09
2	wc=2	ws=1	wg=1	4.94E-10	1.05E-09	1.54E-09
3	wc=3	ws=1	wg=1	4.82E-10	1.05E-09	1.53E-09
4	wc=1	ws=2	wg=1	6.09E-10	1.05E-09	1.66E-09
5	wc=2	ws=2	wg=1	4.63E-10	1.05E-09	1.51E-09
6	wc=3	ws=2	wg=1	4.25E-10	1.05E-09	1.48E-09
7	wc=1	ws=3	wg=1	6.81E-10	1.05E-09	1.73E-09
8	wc=2	ws=3	wg=1	4.87E-10	1.05E-09	1.54E-09
9	wc=3	ws=3	wg=1	4.29E-10	1.05E-09	1.48E-09
10	wc=1	ws=1	wg=2	5.83E-10	1.05E-09	1.63E-09
11	wc=2	ws=1	wg=2	4.88E-10	1.05E-09	1.54E-09
12	wc=3	ws=1	wg=2	4.74E-10	1.05E-09	1.52E-09
13	wc=1	ws=2	wg=2	6.02E-10	1.05E-09	1.65E-09
14	wc=2	ws=2	wg=2	4.54E-10	1.05E-09	1.50E-09
15	wc=3	ws=2	wg=2	4.15E-10	1.05E-09	1.46E-09
16	wc=1	ws=3	wg=2	6.72E-10	1.05E-09	1.72E-09
17	wc=2	ws=3	wg=2	4.76E-10	1.05E-09	1.53E-09
18	wc=3	ws=3	wg=2	4.17E-10	1.05E-09	1.47E-09
19	wc=1	ws=1	wg=4	5.85E-10	1.05E-09	1.64E-09
20	wc=2	ws=1	wg=4	4.87E-10	1.05E-09	1.54E-09
21	wc=3	ws=1	wg=4	4.73E-10	1.05E-09	1.52E-09
22	wc=1	ws=2	wg=4	6.02E-10	1.05E-09	1.65E-09
23	wc=2	ws=2	wg=4	4.51E-10	1.05E-09	1.50E-09
24	wc=3	ws=2	wg=4	4.11E-10	1.05E-09	1.46E-09
25	wc=1	ws=3	wg=4	6.71E-10	1.05E-09	1.72E-09
26	wc=2	ws=3	wg=4	4.72E-10	1.05E-09	1.52E-09
27	wc=3	ws=3	wg=4	4.11E-10	1.05E-09	1.46E-09

Chosen Gate sizes

Full Adder:

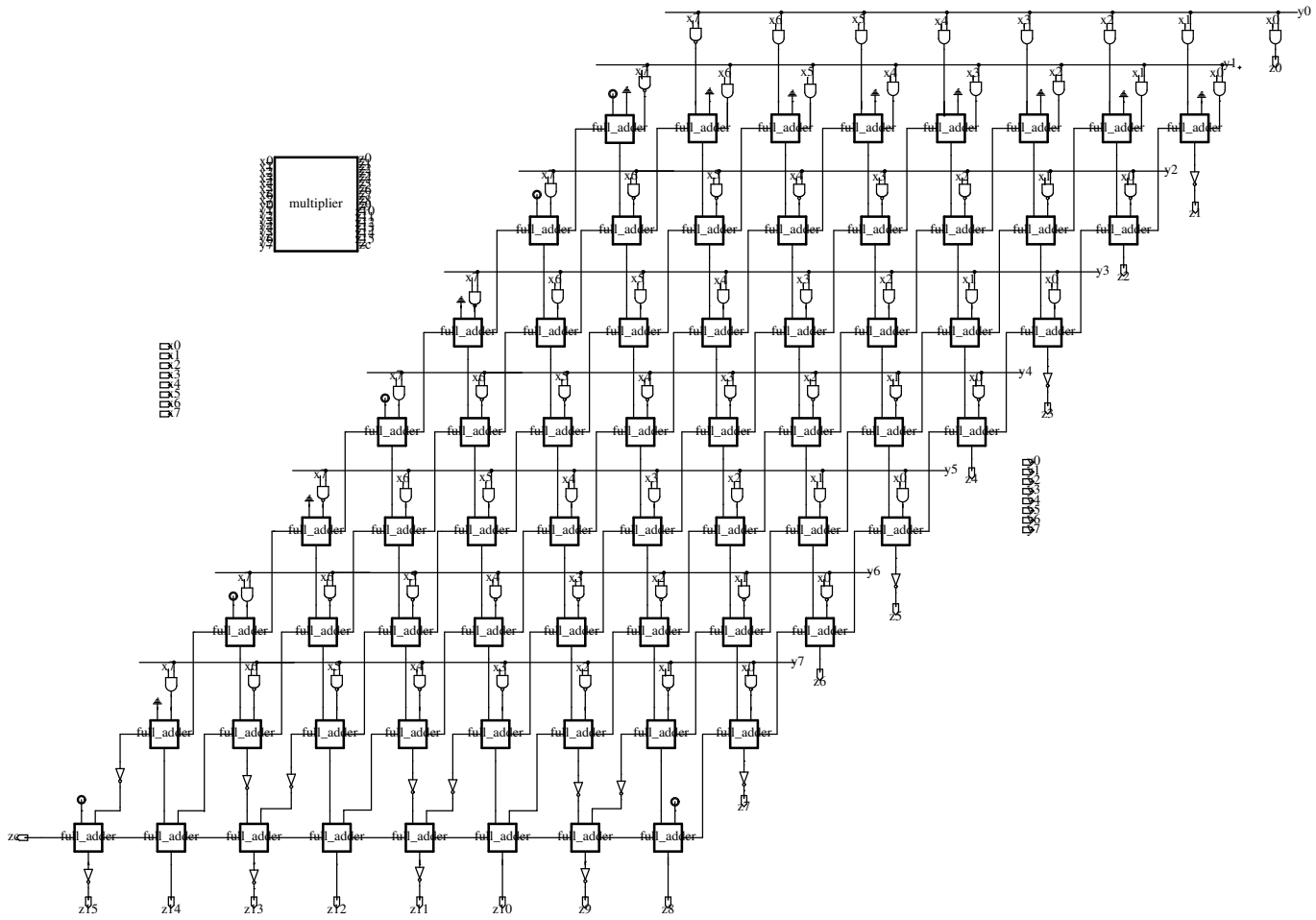
Cout-bar: 3x

Sum-bar: 2x

Standard Cells:

NAND, AND, INV: 4x

--End--


multiplier
full_adder
x0
x1
x2
x3
x4
x5
x6
x7
y0
y1
y2
y3
y4
y5
y6
y7
z0
z1
z2
z3
z4
z5
z6
z7
z8
z9
zY0
zY1
zY2
zY3
zY4
zY5