EE5311 - Digital IC Design

Assignment 1 - Inverter, NAND2 and AND2

Member 1: Srivenkat A(EE18B038)

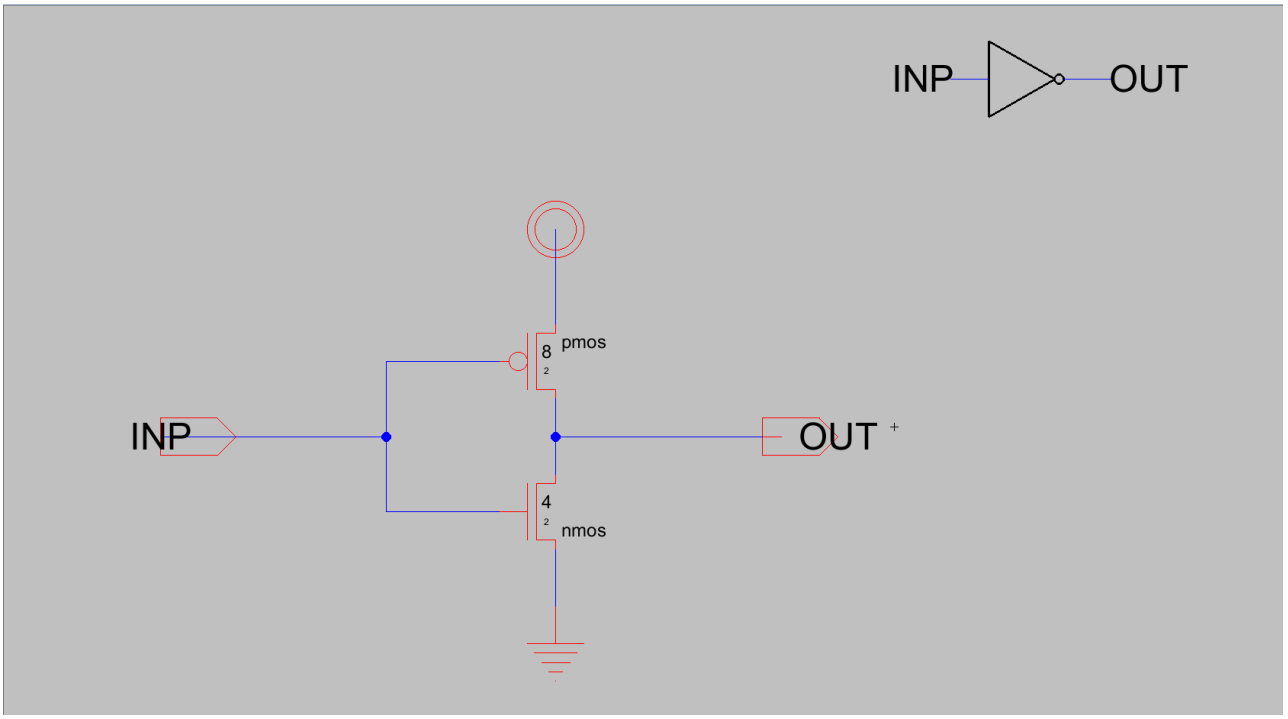
Member 2: Hemanth Ram G K(EE18B132)

Member 3: Sidesh S(EE18B032)

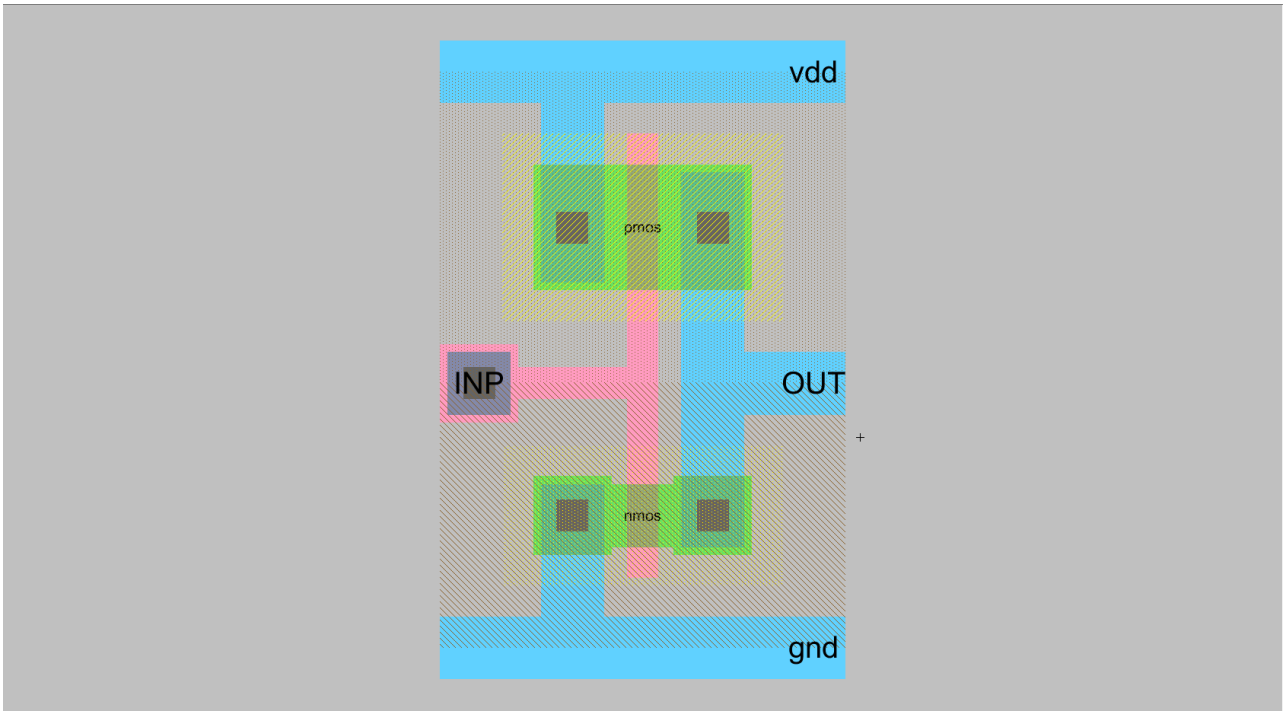
Part A - Inverter

Inverter 1x

Dimensions: L=2λ, Wn=4λ, Wp=8λ



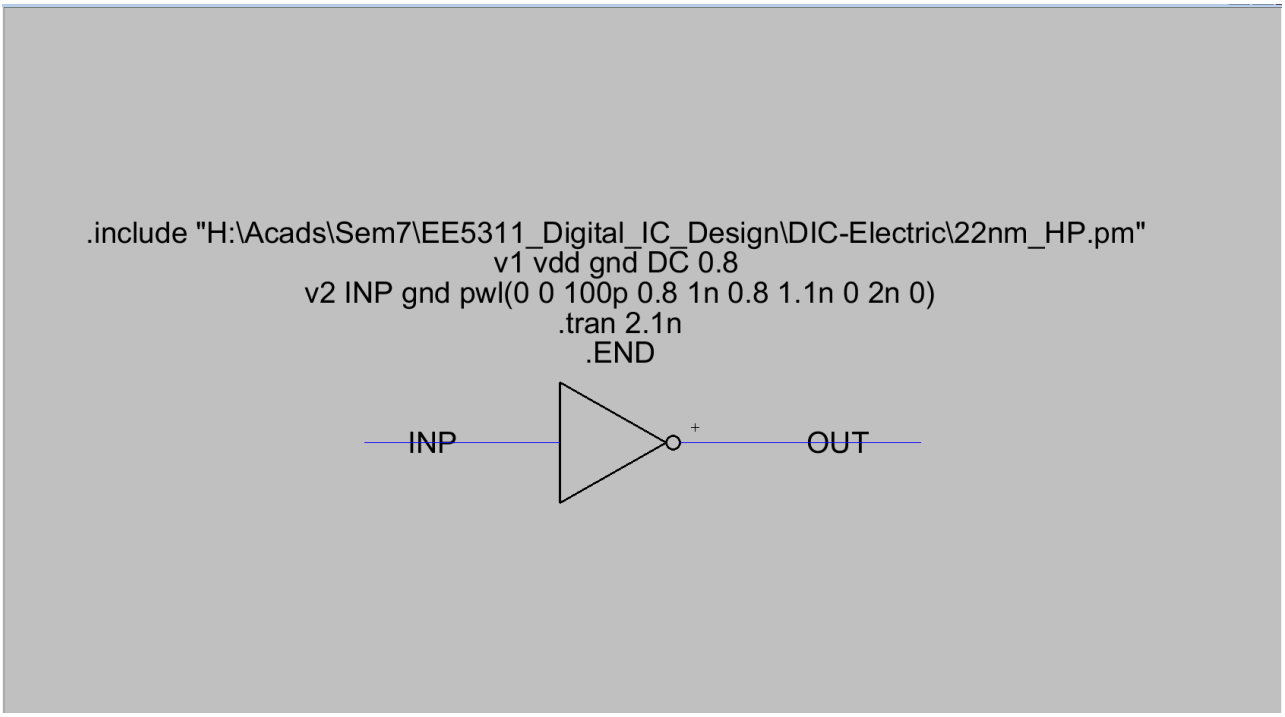
Schematic



Layout

```
================================22================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 7 networks
0 errors and 0 warnings found (took 0.001 secs)
================================16================================
Hierarchical NCC every cell in the design: cell 'inverter{sch}'  cell 'inv-lx__inverter{lay}'
Comparing: inv-lx:inverter{sch} with: inv-lx:inv-lx__inverter{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.003 seconds.
================================17================================
```

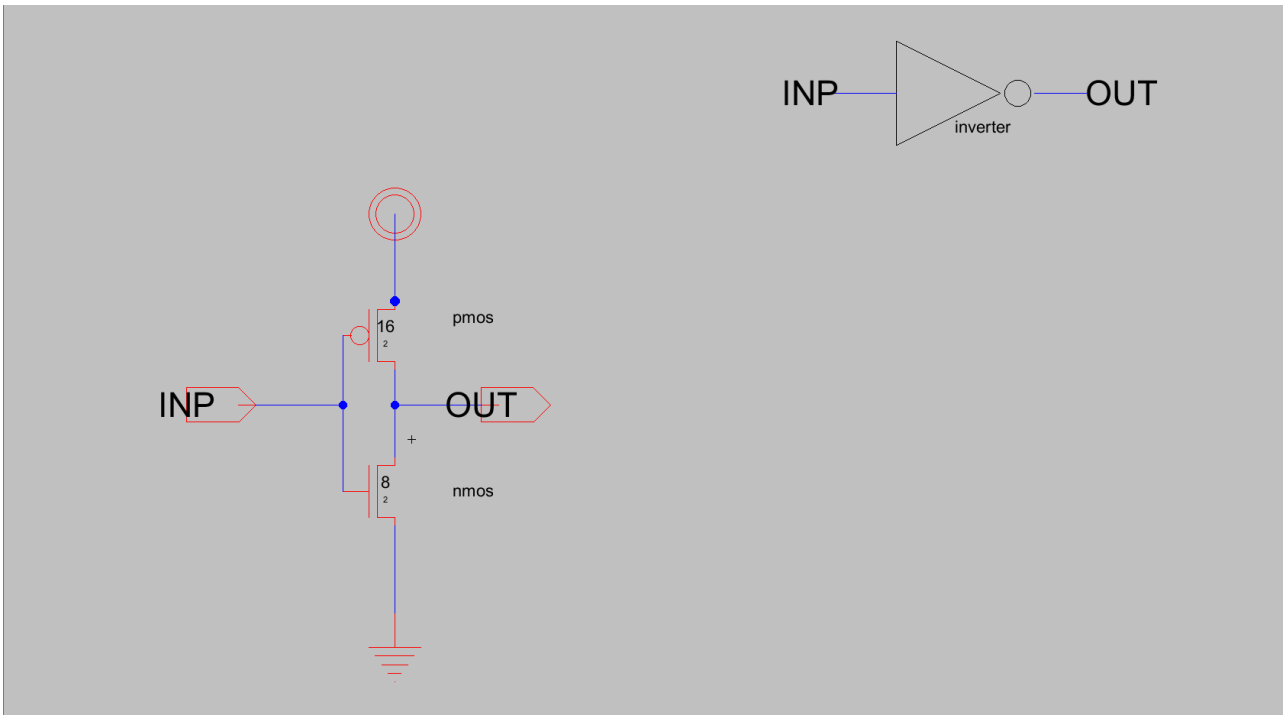
DRS LVS Clean Screenshot



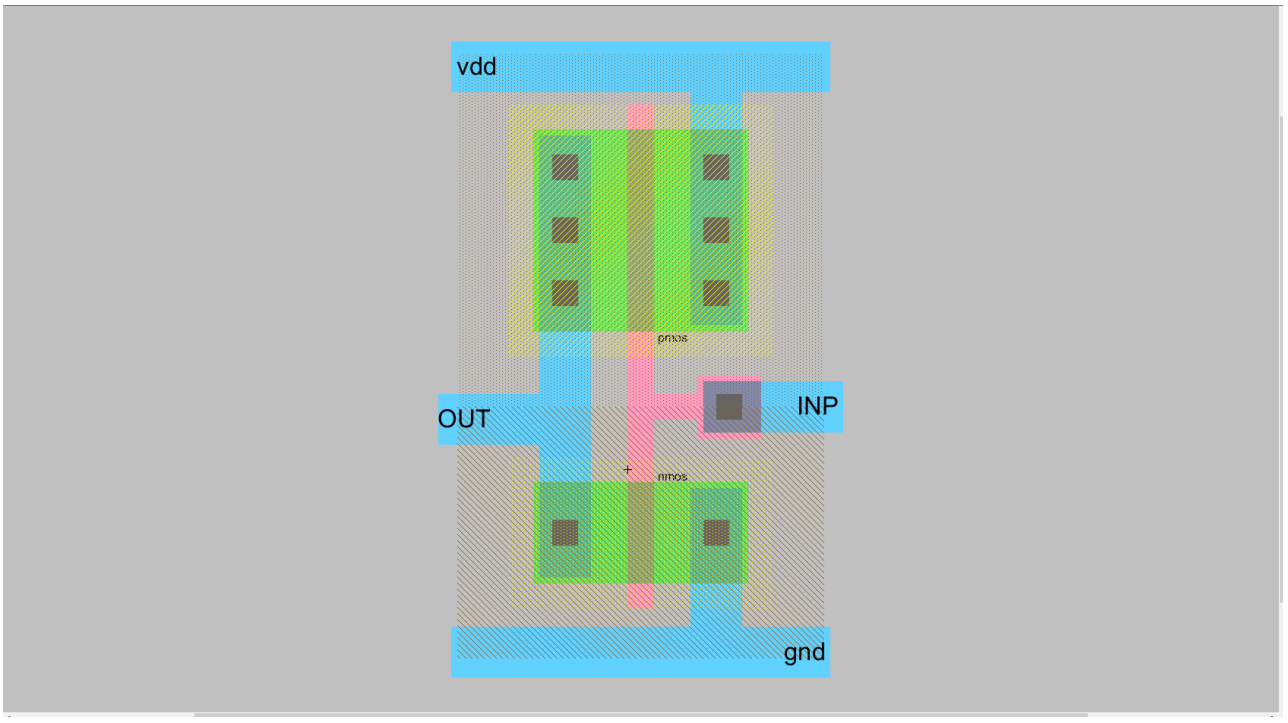
Testbench

Inverter 2x

Dimensions: L=2λ, Wn=8λ, Wp=16λ



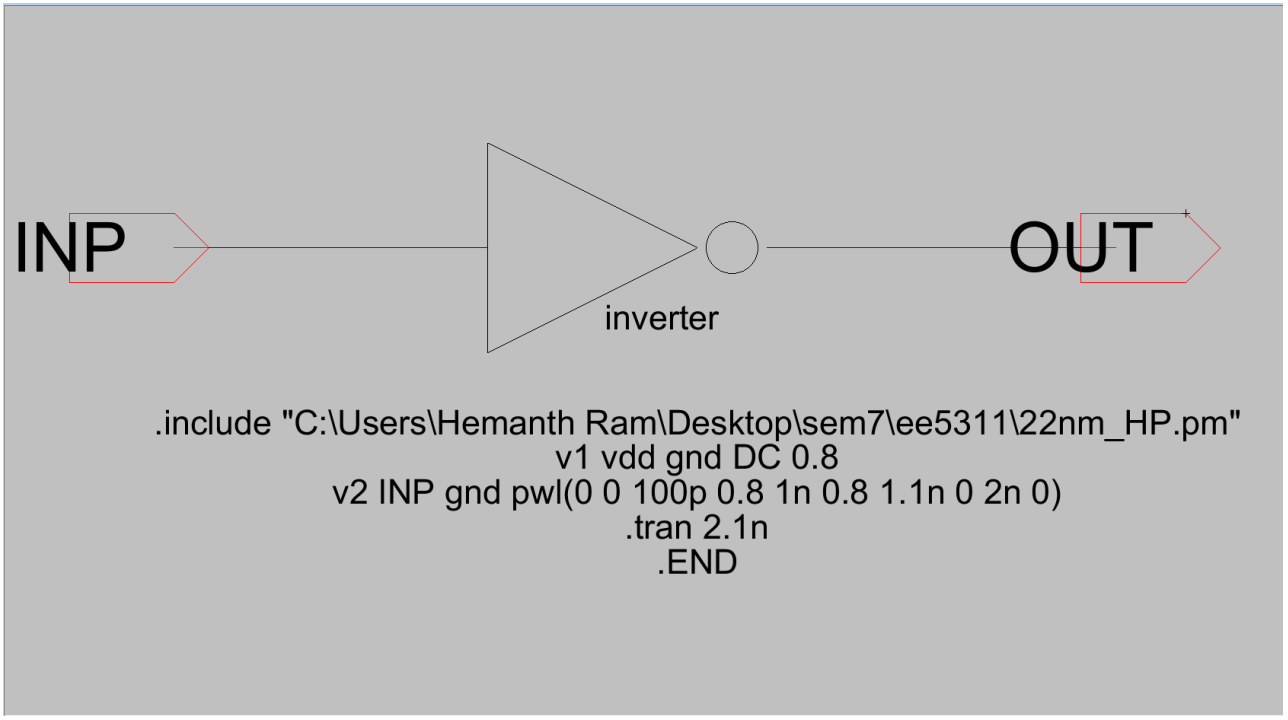
Schematic



Layout

```
================================6================================
Hierarchical NCC every cell in the design: cell 'inverter{sch}'  cell 'test_inverter{lay}'
Comparing: not_2x:inverter{sch} with: not_2x:test_inverter{lay}
  exports match, topologies match, sizes not checked in 0.001 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.002 seconds.
================================7================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 7 networks
0 errors and 0 warnings found (took 0.002 secs)
```

DRS LVS Clean Screenshot

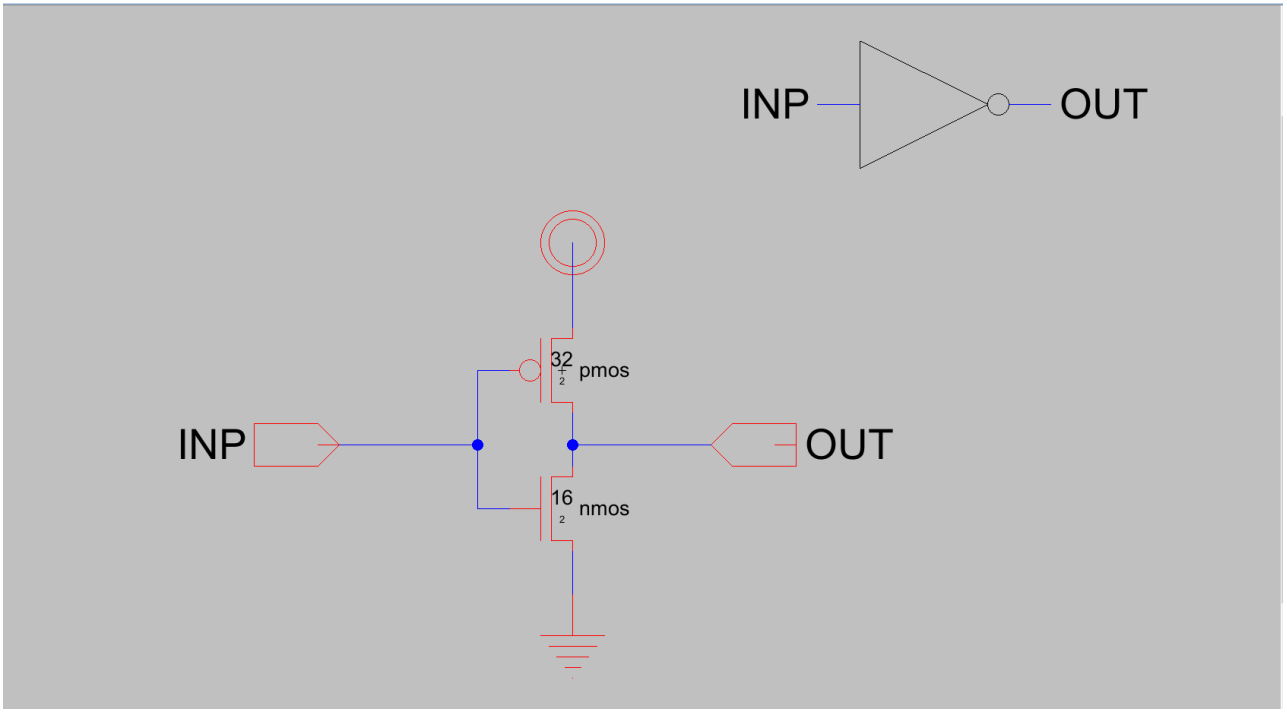


Testbench

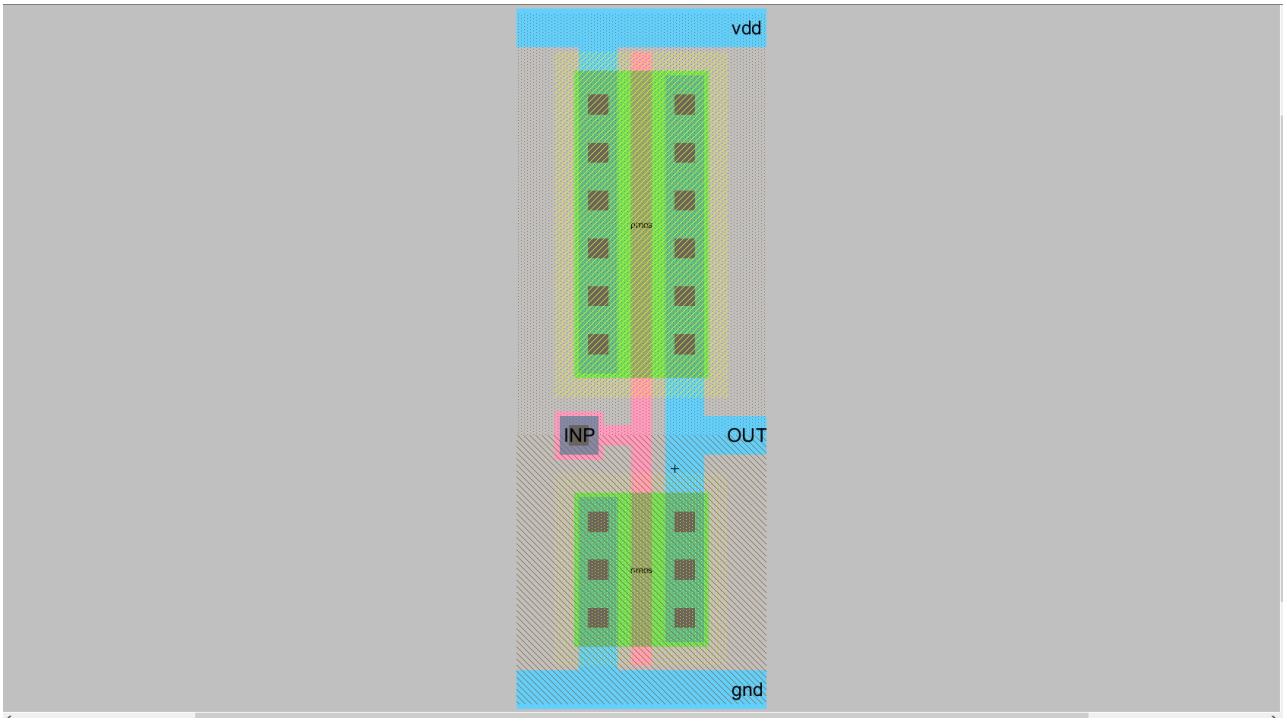
z

Inverter 4x

Dimensions: L=2λ, Wn=16λ, Wp=32λ



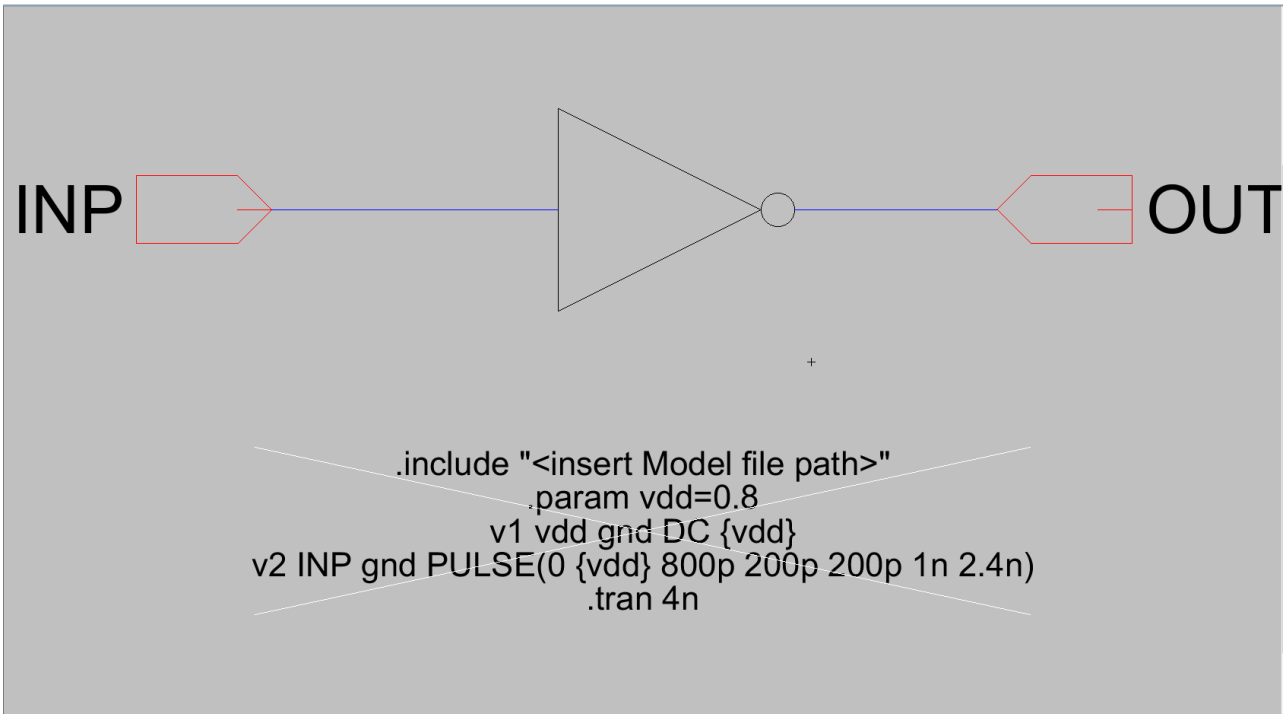
Schematic



Layout

```
================================5================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 7 networks
Checking cell 'inv_4x__inv{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.035 secs)
================================6================================
Hierarchical NCC every cell in the design: cell 'inv{sch}'  cell 'inv_4x__inv{lay}'
Comparing: inv_4x:inv{sch} with: inv_4x:inv_4x__inv{lay}
  exports match, topologies match, sizes match in 0.016 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.032 seconds.
```

DRS LVS Clean Screenshot

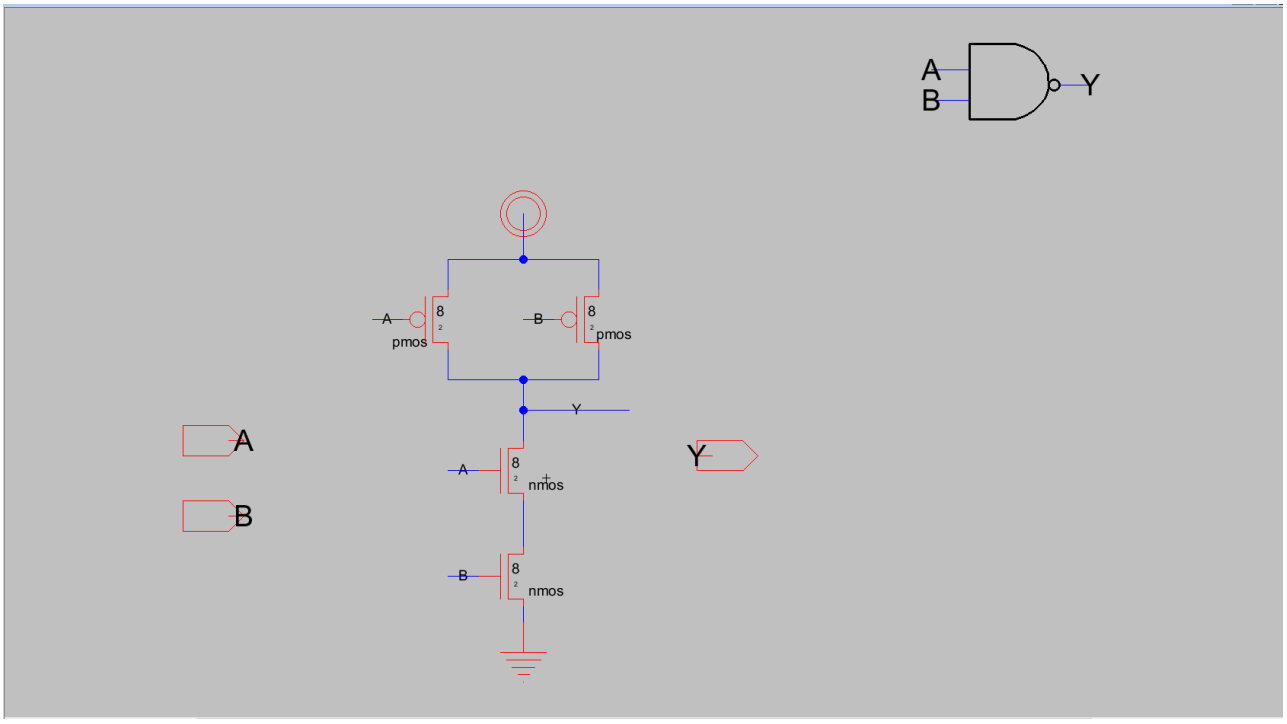


Testbench

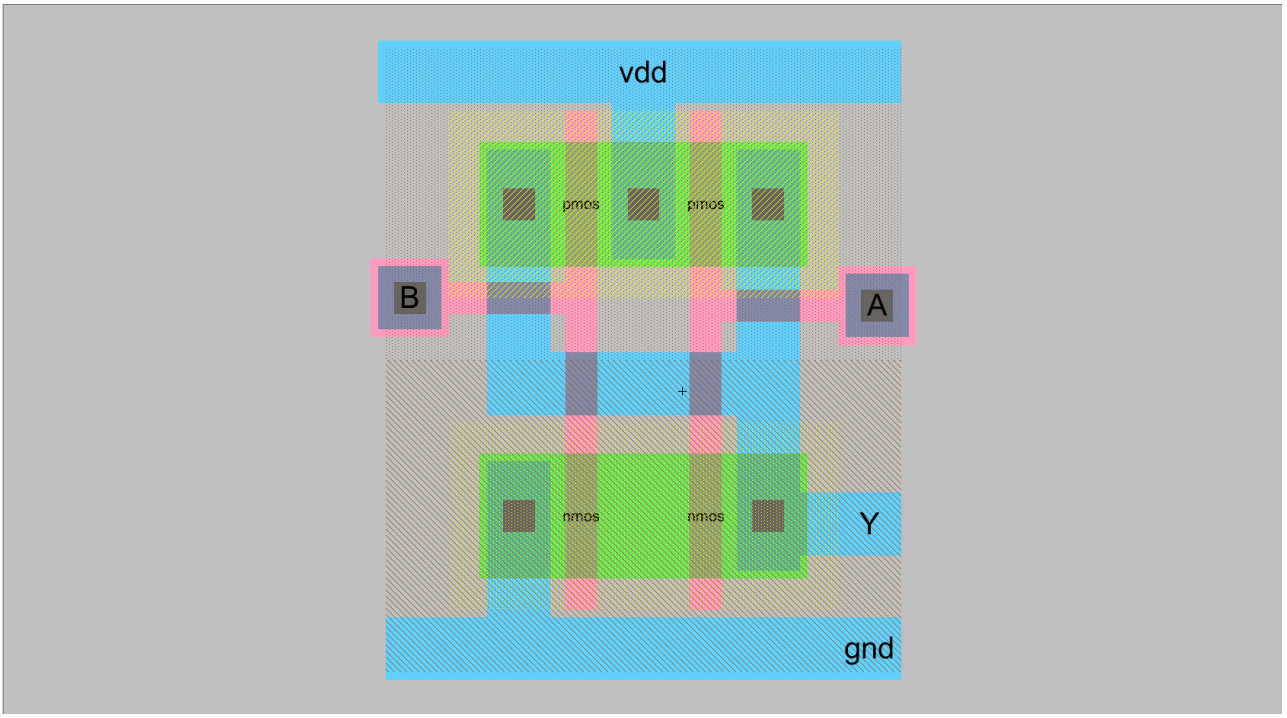
Part B - NAND2

NAND2 1x

Dimensions: L=2λ, Wn=8λ, Wp=8λ



Schematic

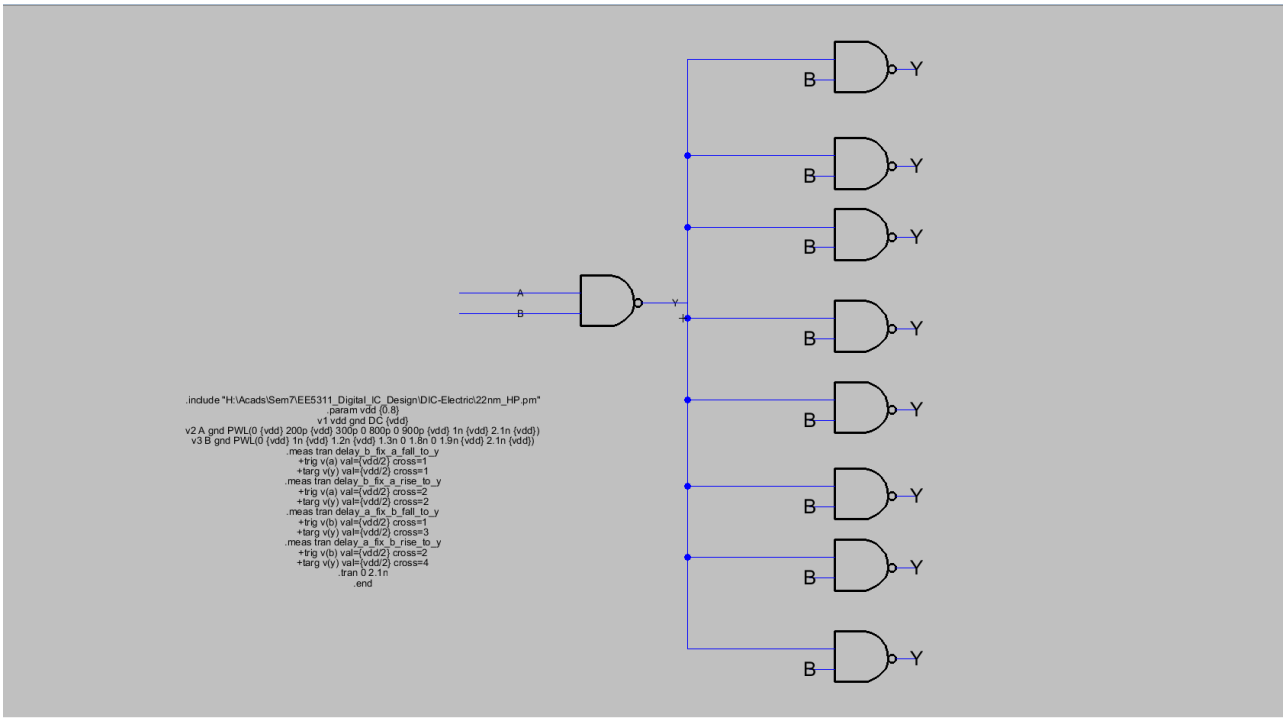


Layout

```
================================24================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 11 networks
0 errors and 0 warnings found (took 0.002 secs)

================================13================================
Hierarchical NCC every cell in the design: cell 'nand2{sch}'  cell 'nand2-1x__nand2{lay}'
Comparing: nand2-1x:nand2{sch} with: nand2-1x:nand2-1x__nand2{lay}
  exports match, topologies match, sizes not checked in 0.028 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.037 seconds.
================================14================================
```

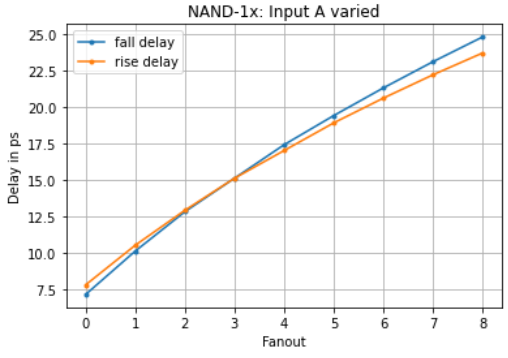
DRS LVS Clean Screenshot

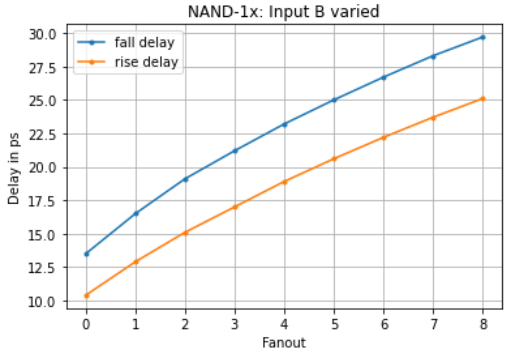


Testbench

Delay - NAND2 1x					
Fanout Count	Delay Name	Delay Type	Fixed Input(High)	Transitioning Input	Delay Value
0	delay_b_fixed_a_fall	Rise	B	A (1->0)	7.78E-12
	delay_b_fixed_a_rise	Fall	B	A(0->1)	7.12E-12
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.04E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.35E-11
1	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.05E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	1.01E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.29E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.65E-11
2	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.29E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	1.28E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.51E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.91E-11
3	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.51E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	1.51E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.70E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.12E-11
4	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.70E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	1.74E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.89E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.32E-11
5	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.89E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	1.94E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.06E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.50E-11
6	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.06E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.13E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.22E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.67E-11
7	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.22E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.31E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.37E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.83E-11
8	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.37E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.48E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.51E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.97E-11

Delay Values

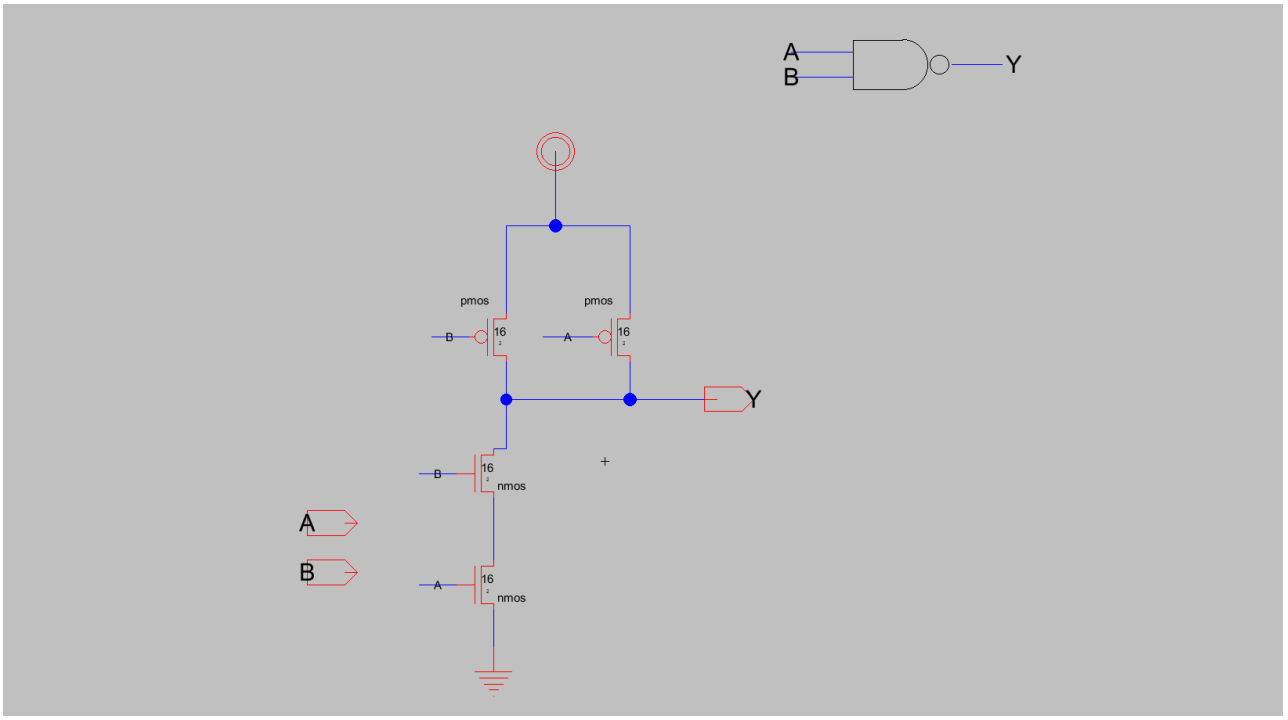




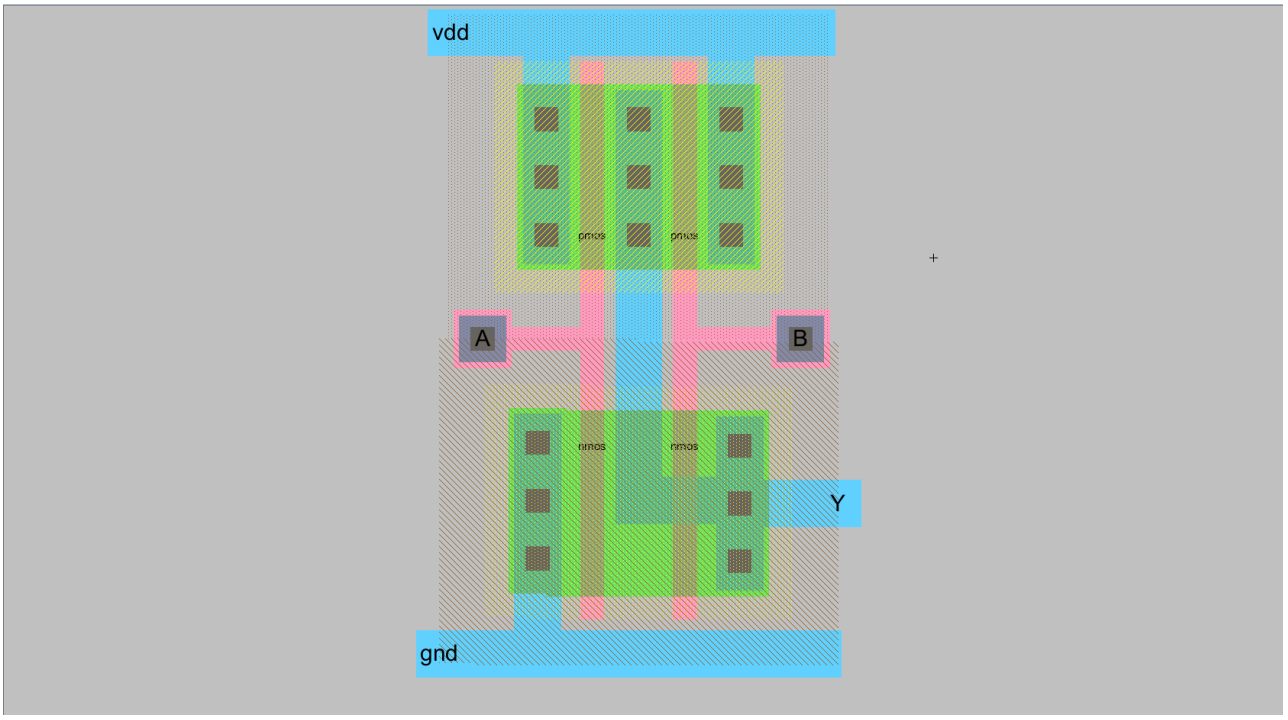
Delay vs Fanout

NAND2 2x

Dimensions: L=2λ, Wn=16λ, Wp=16λ



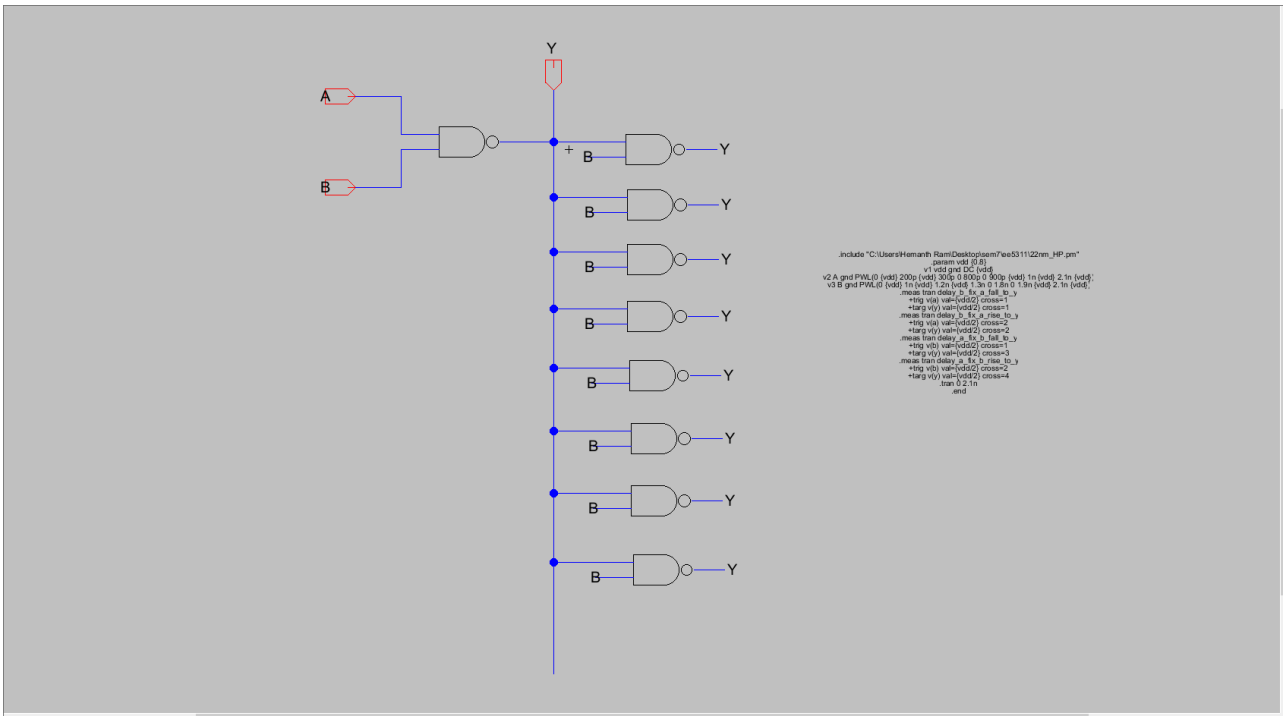
Schematic



Layout

```
================================3================================
Hierarchical NCC every cell in the design: cell 'nand2{sch}'  cell 'nand2_nand2{lay}'
Comparing: nand2_2x:nand2{sch} with: nand2_2x:nand2_nand2{lay}
  exports match, topologies match, sizes not checked in 0.035 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.043 seconds.
================================4================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.001 secs)
Found 11 networks
0 errors and 0 warnings found (took 0.02 secs)
```

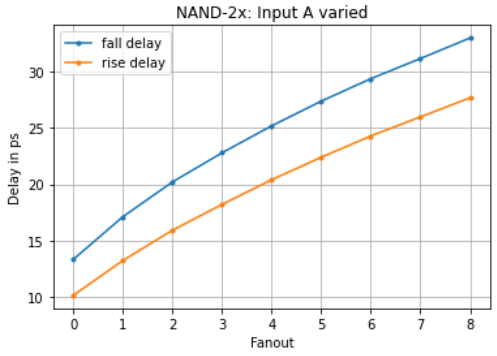
DRS LVS Clean Screenshot

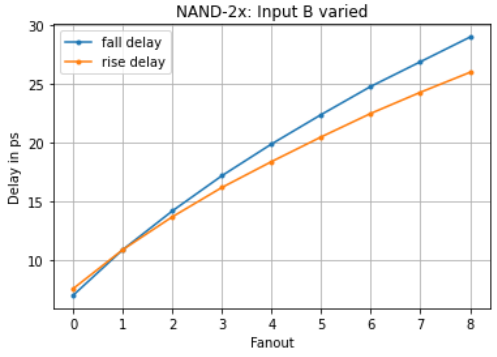


Testbench

Delay - NAND2 2x					
Fanout Count	Delay Name	Delay Type	Fixed Input(High)	Transitioning Input	Delay Value
0	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.01E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	1.33E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	7.58E-12
	delay_a_fixed_b_rise	Fall	A	B(0->1)	7.02E-12
1	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.32E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	1.71E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.09E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.09E-11
2	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.59E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.02E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.37E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.42E-11
3	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.82E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.28E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.62E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.72E-11
4	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.04E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.52E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.84E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.99E-11
5	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.24E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.74E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.05E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.24E-11
6	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.43E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.94E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.25E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.48E-11
7	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.60E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	3.12E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.43E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.69E-11
8	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.77E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	3.30E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.60E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.90E-11

Delay Values

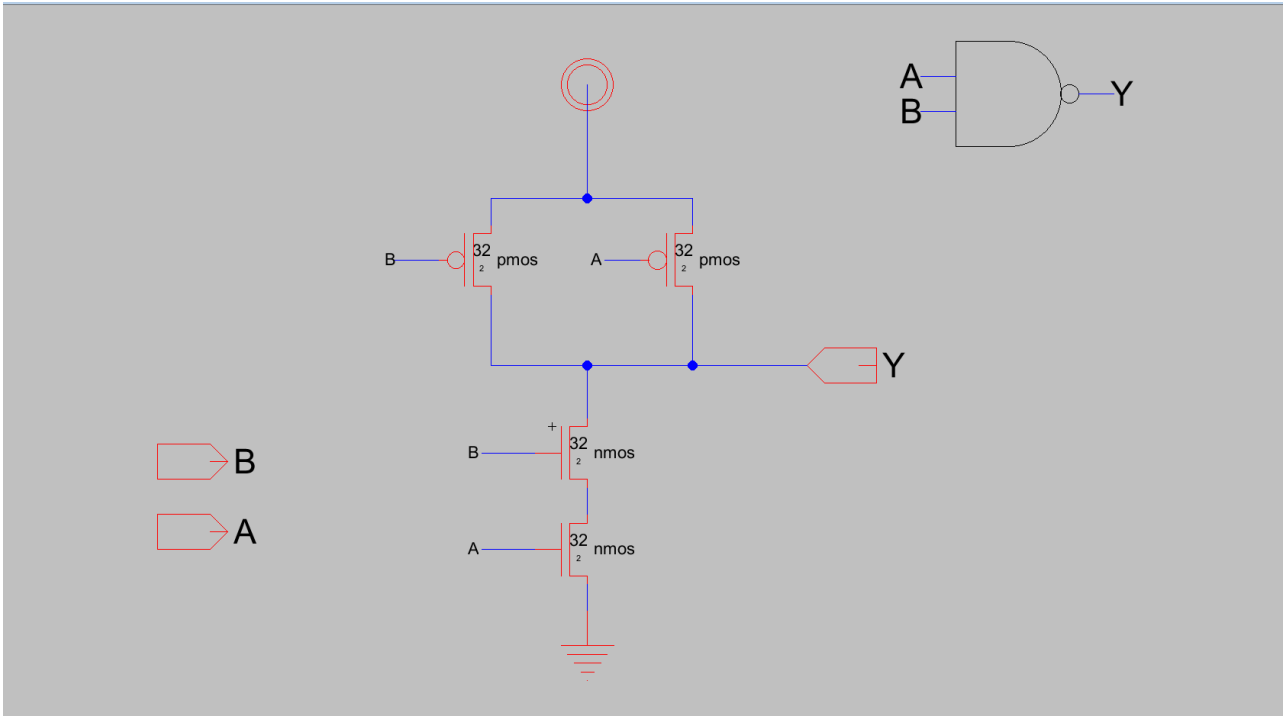




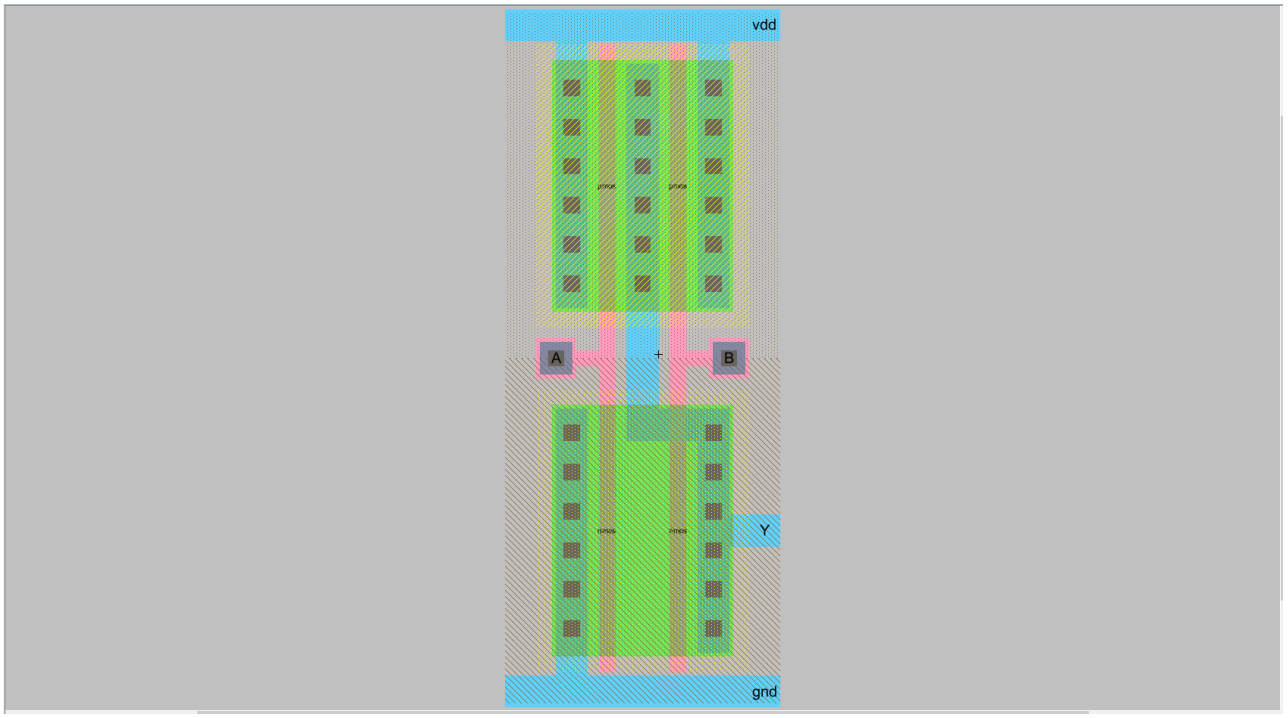
Delay vs Fanout

NAND2 4x

Dimensions: L=2λ, Wn=32λ, Wp=32λ



Schematic

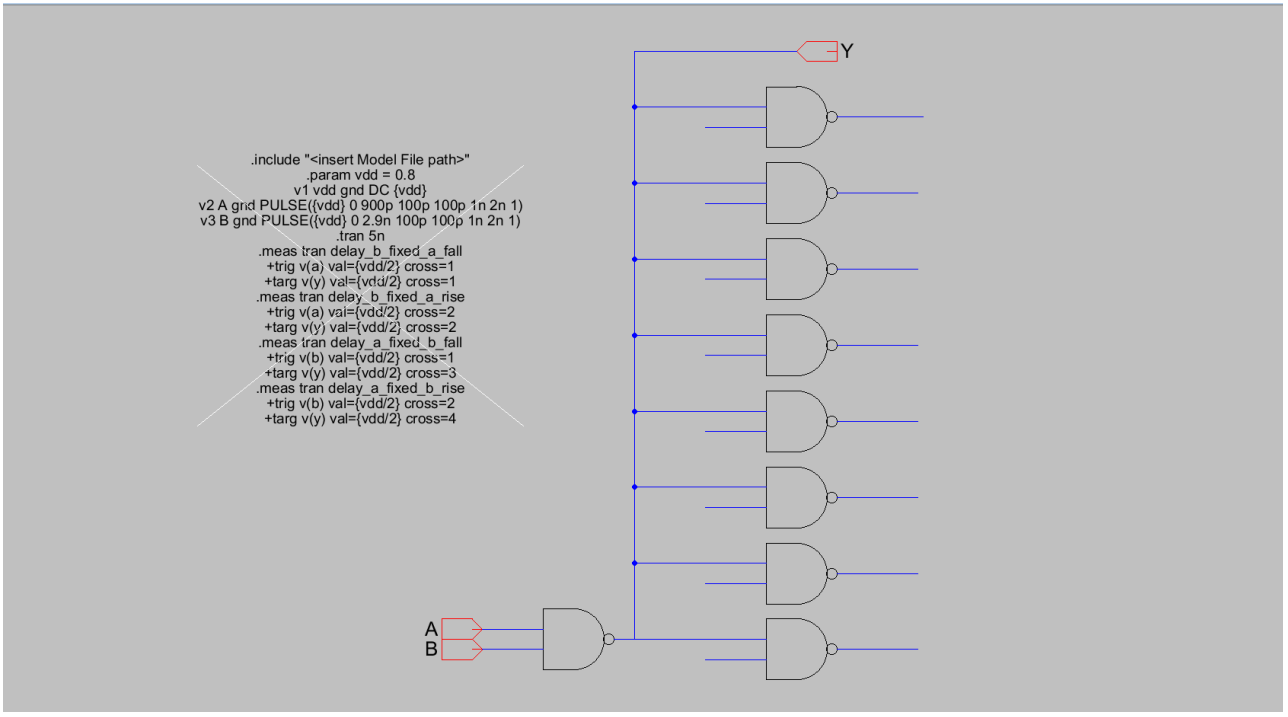


Layout

Electric Messages

```
Electric's log file is C:\WINDOWS\system32\electric.log.
================================1================================
Library /C:/Users/welcome/Documents/Academics/7th%20Sem/EE5311%20-%20Digital%20IC%20Design/Assignments/Assignment1/Size-4x/nand2_4x.jelib read, took 0.024 secs
Checking library 'nand2_4x' for repair... library checked
No errors found
================================2================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.002 secs)
Found 11 networks
0 errors and 0 warnings found (took 0.017 secs)
================================3================================
Hierarchical NCC every cell in the design: cell 'nand2{sch}'  cell 'nand2_4x__nand2{lay}'
Comparing: nand2_4x:nand2{sch} with: nand2_4x:nand2_4x__nand2{lay}
  exports match, topologies match, sizes match in 0.025 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.032 seconds.
================================4================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 11 networks
0 errors and 0 warnings found (took 0.002 secs)
================================5================================
Hierarchical NCC every cell in the design: cell 'nand2{sch}'  cell 'nand2_4x__nand2{lay}'
Comparing: nand2_4x:nand2{sch} with: nand2_4x:nand2_4x__nand2{lay}
  exports match, topologies match, sizes match in 0.003 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.003 seconds.
```

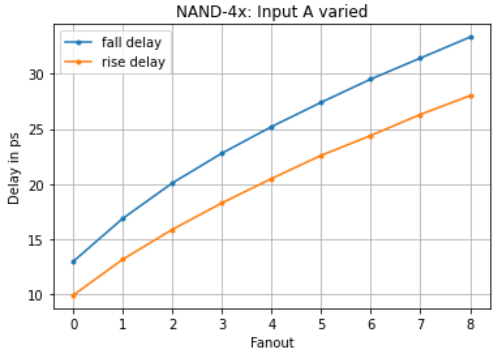
DRS LVS Clean Screenshot

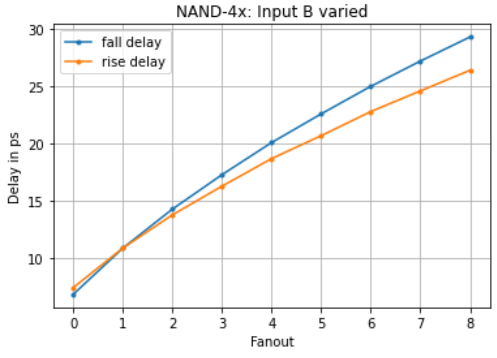


Testbench

Delay - NAND2 4x					
Fanout Count	Delay Name	Delay Type	Fixed Input(High)	Transitioning Input	Delay Value
0	delay_b_fixed_a_fall	Rise	B	A (1->0)	9.95E-12
	delay_b_fixed_a_rise	Fall	B	A(0->1)	1.30E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	7.46E-12
	delay_a_fixed_b_rise	Fall	A	B(0->1)	6.87E-12
1	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.32E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	1.69E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.09E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.09E-11
2	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.59E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.01E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.38E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.43E-11
3	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.83E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.28E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.63E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.73E-11
4	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.05E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.52E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.87E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.01E-11
5	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.26E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.74E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.07E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.26E-11
6	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.44E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.95E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.28E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.50E-11
7	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.63E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	3.14E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.46E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.72E-11
8	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.80E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	3.33E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.64E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.93E-11

Delay Values

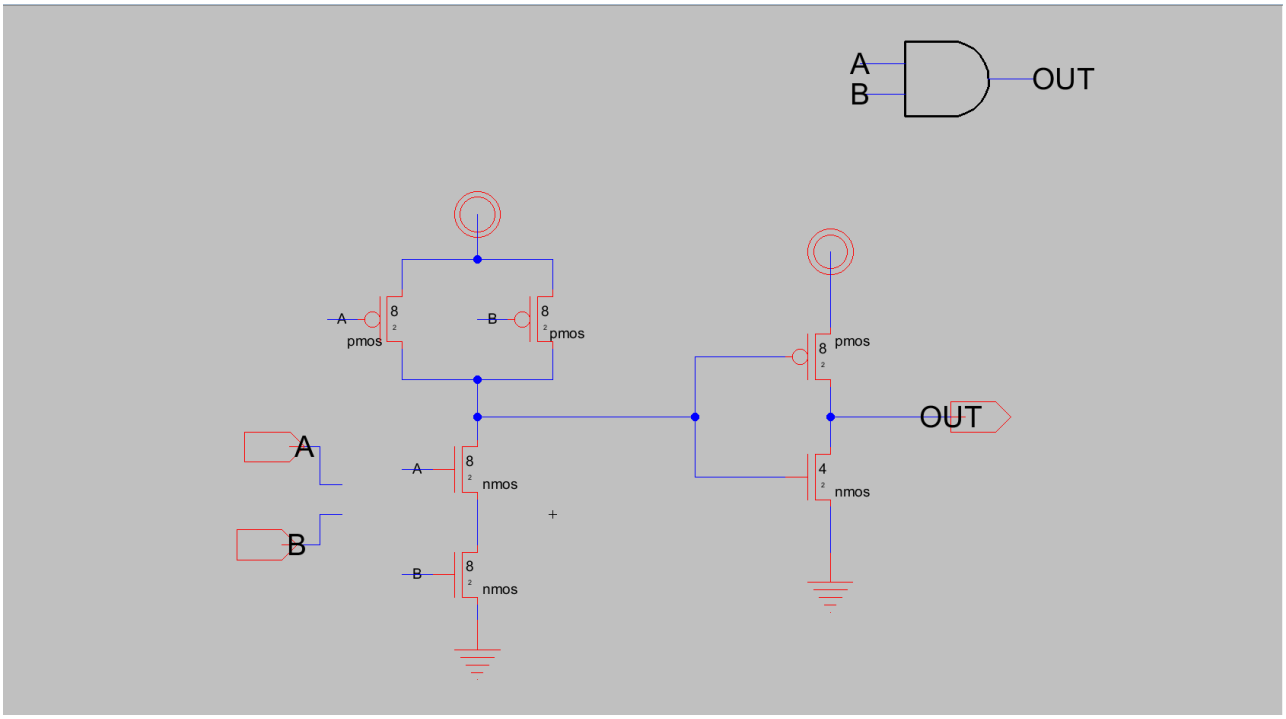




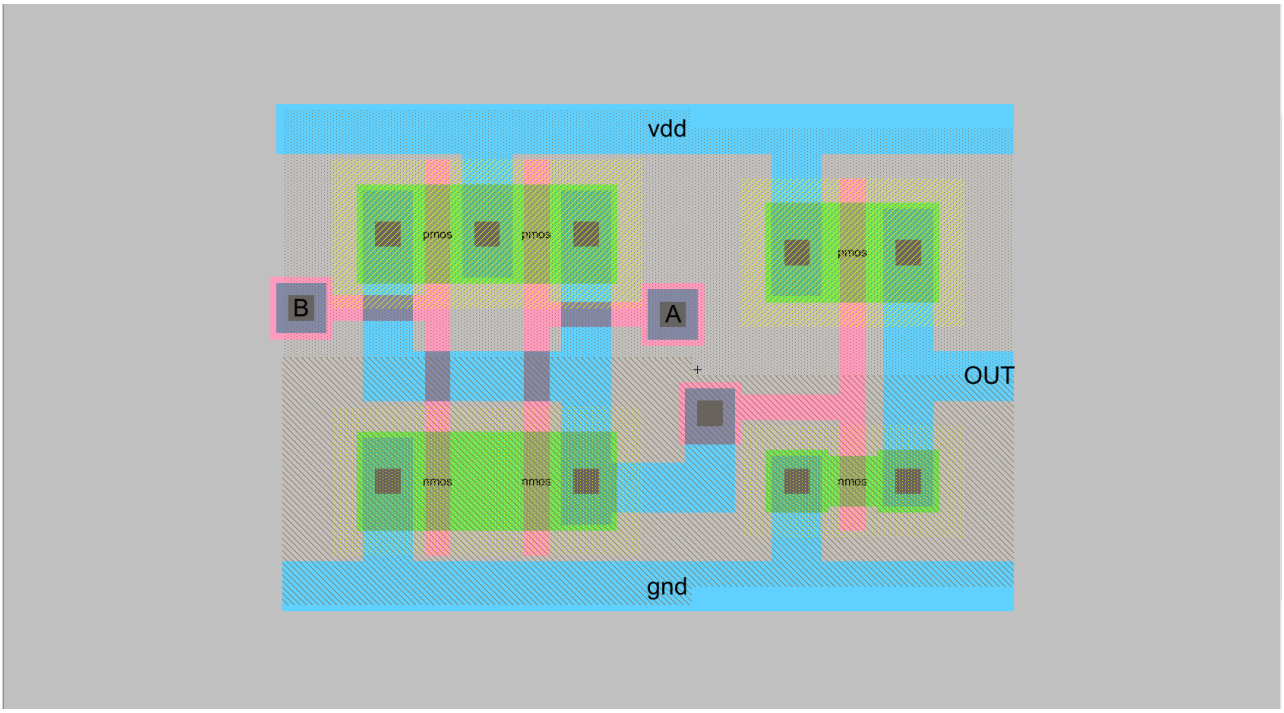
Delay vs Fanout

Part C - AND2

AND2 1x



Schematic

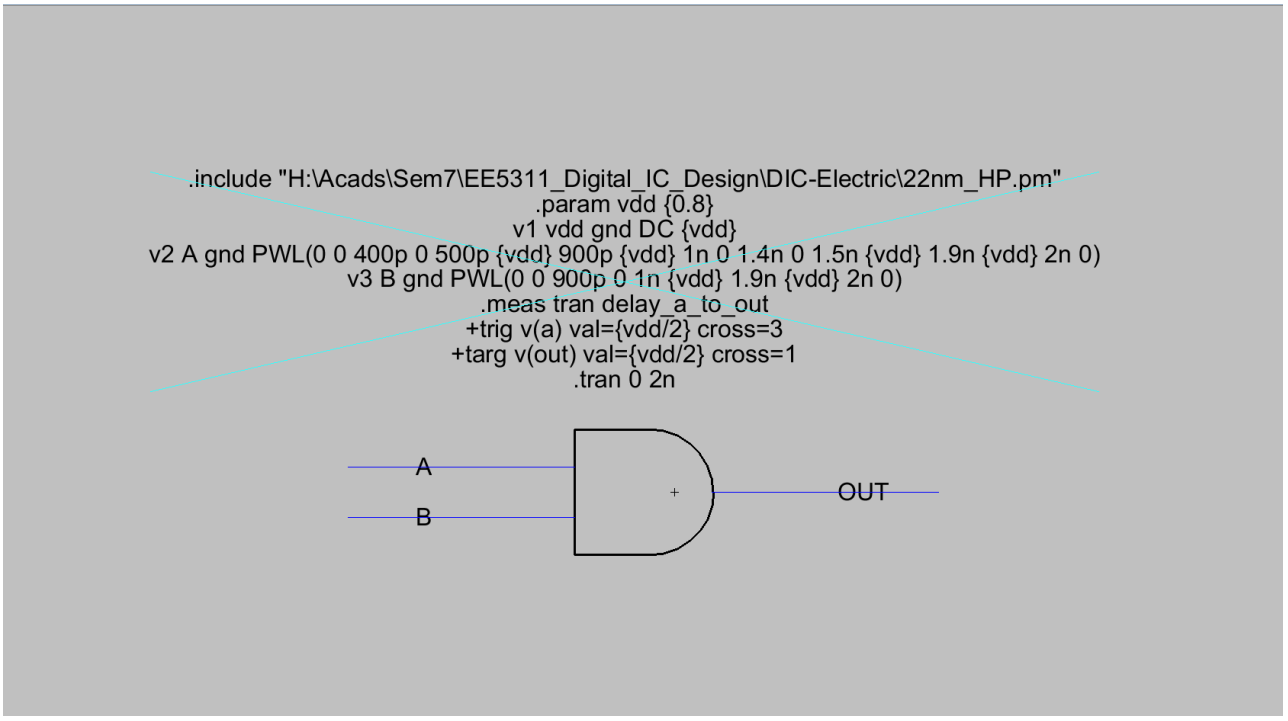


Layout

```
================================21================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 14 networks
0 errors and 0 warnings found (took 0.002 secs)
```

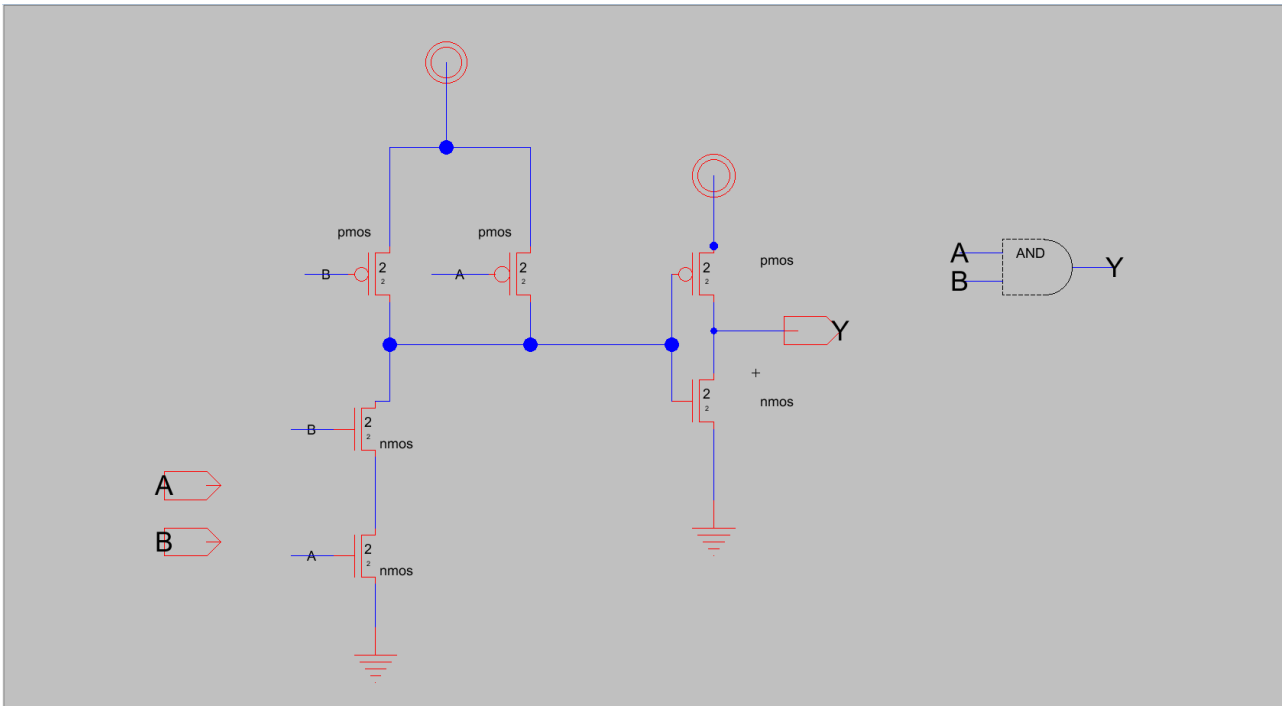
```
================================17================================
Hierarchical NCC every cell in the design: cell 'and2-1x:and2{sch}'  cell 'and2-1x:and2-1x__and2{lay}'
Comparing: and2-1x:and2{sch} with: and2-1x:and2-1x__and2{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.002 seconds.
================================18================================
```

DRS LVS Clean Screenshot

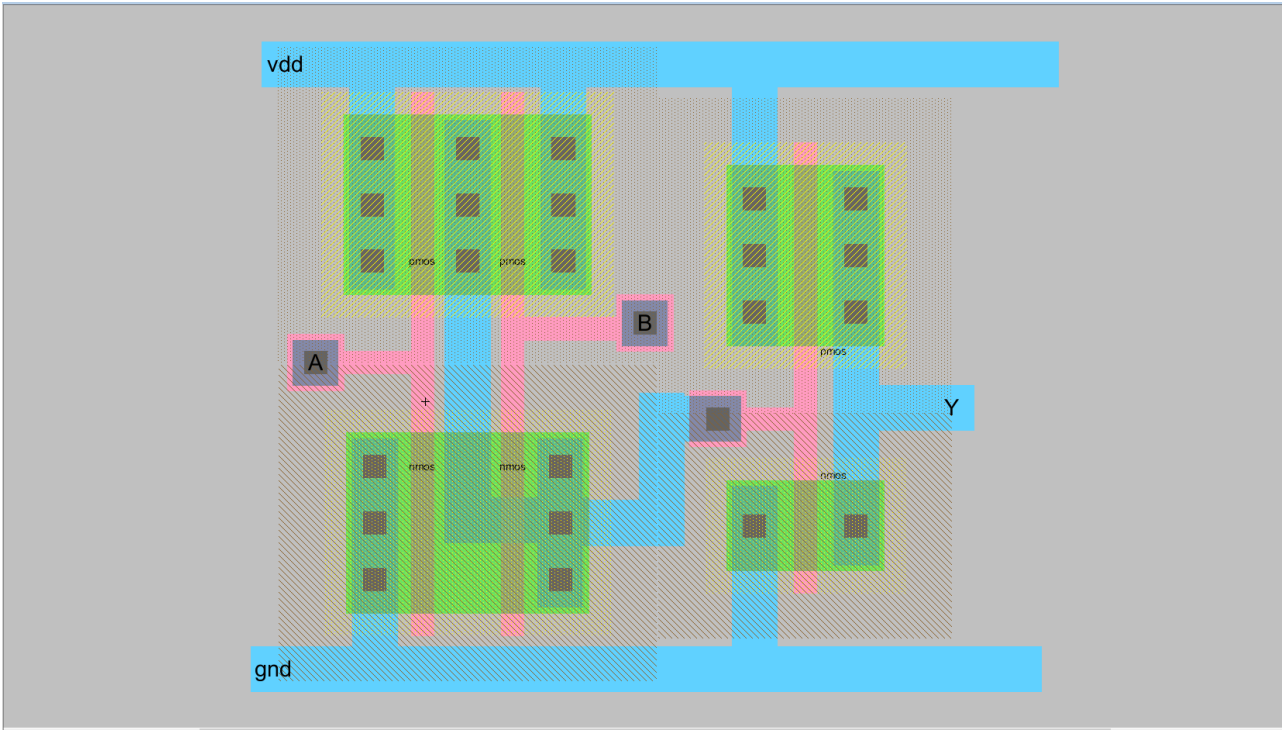


Testbench

AND2 2x



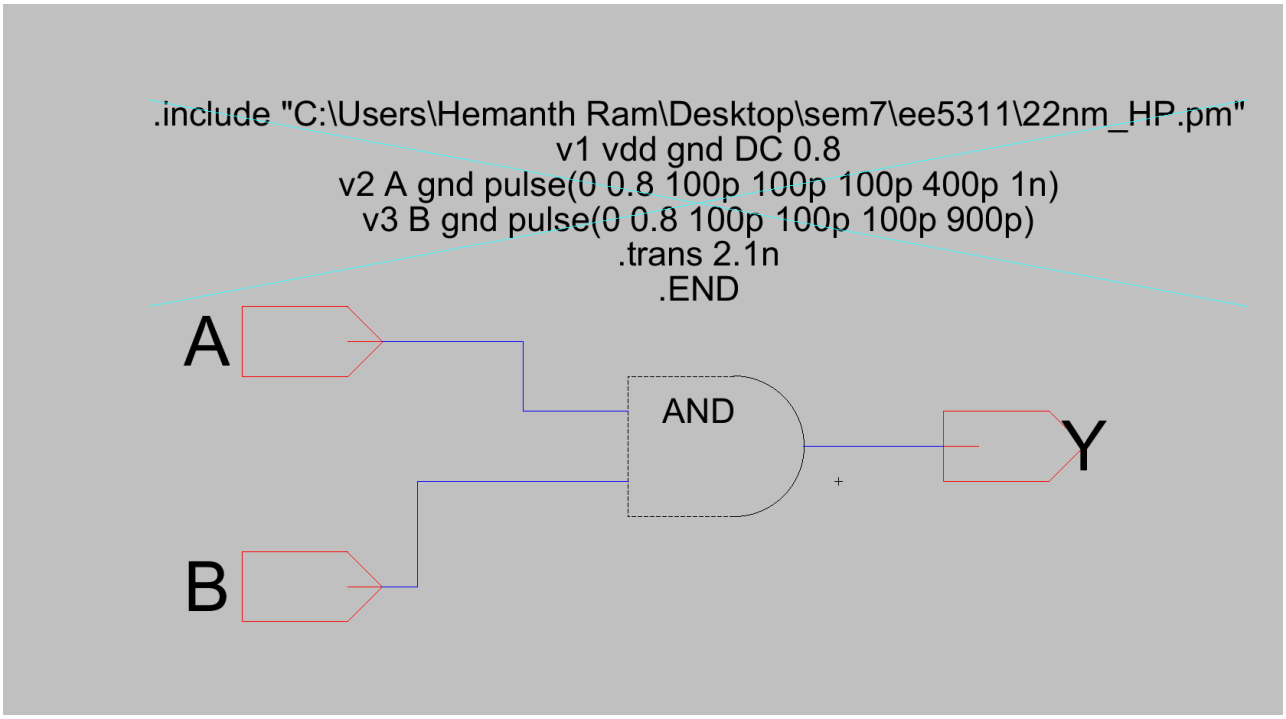
Schematic



Layout

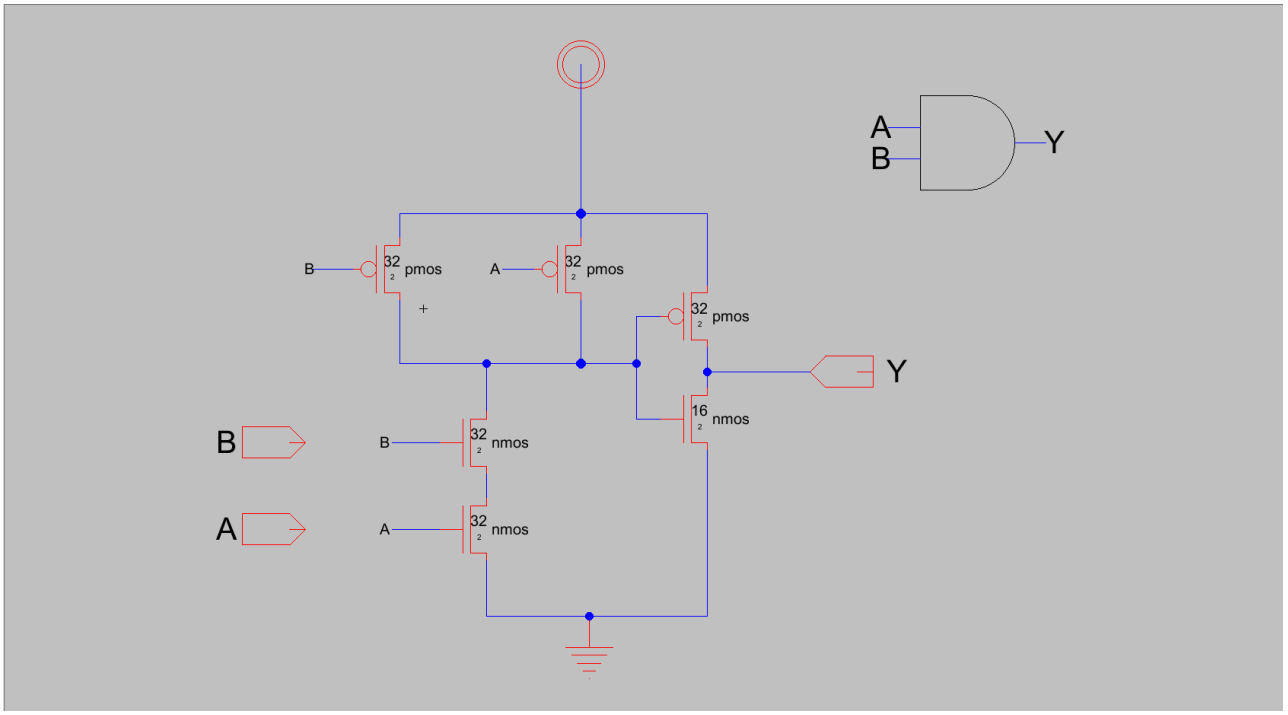
```
================================30================================
Hierarchical NCC every cell in the design: cell 'and{sch}'  cell 'and_and{lay}'
Comparing: and2_2x:and{sch} with: and2_2x:and_and{lay}
  exports match, topologies match, sizes not checked in 0.003 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.003 seconds.
================================31================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 14 networks
0 errors and 0 warnings found (took 0.002 secs)
```

DRS LVS Clean Screenshot

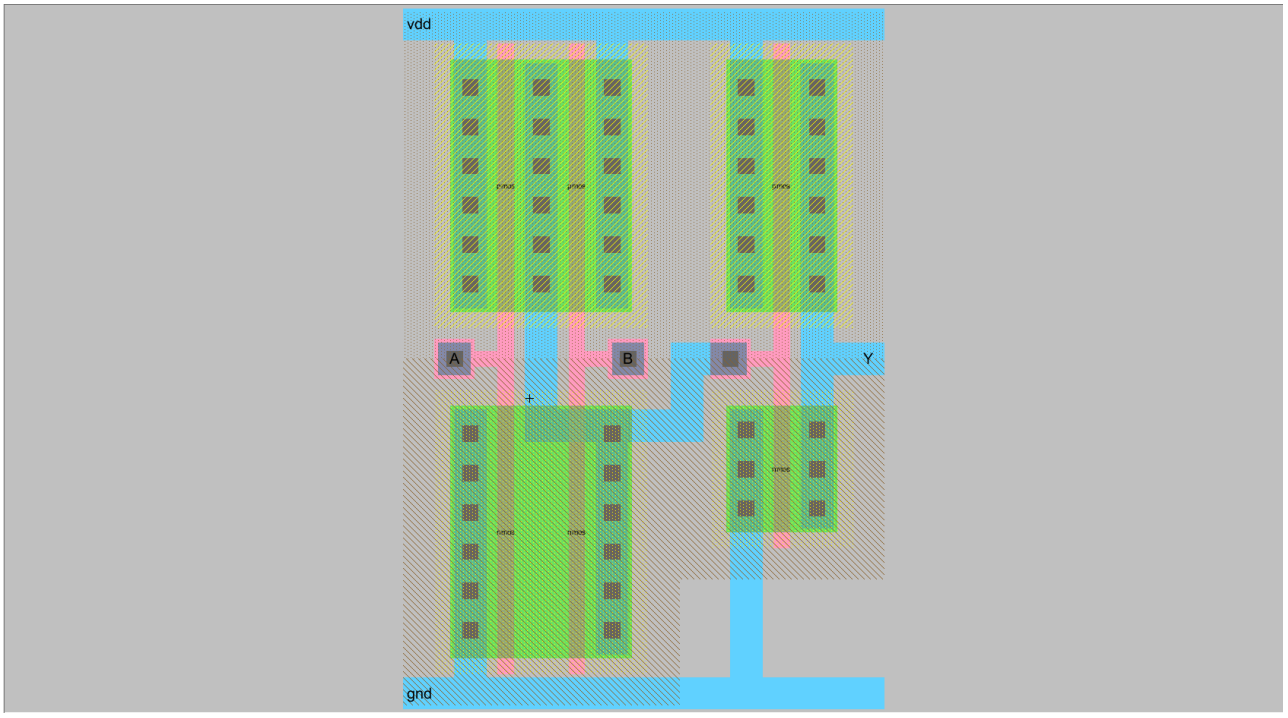


Testbench

AND2 4x



Schematic

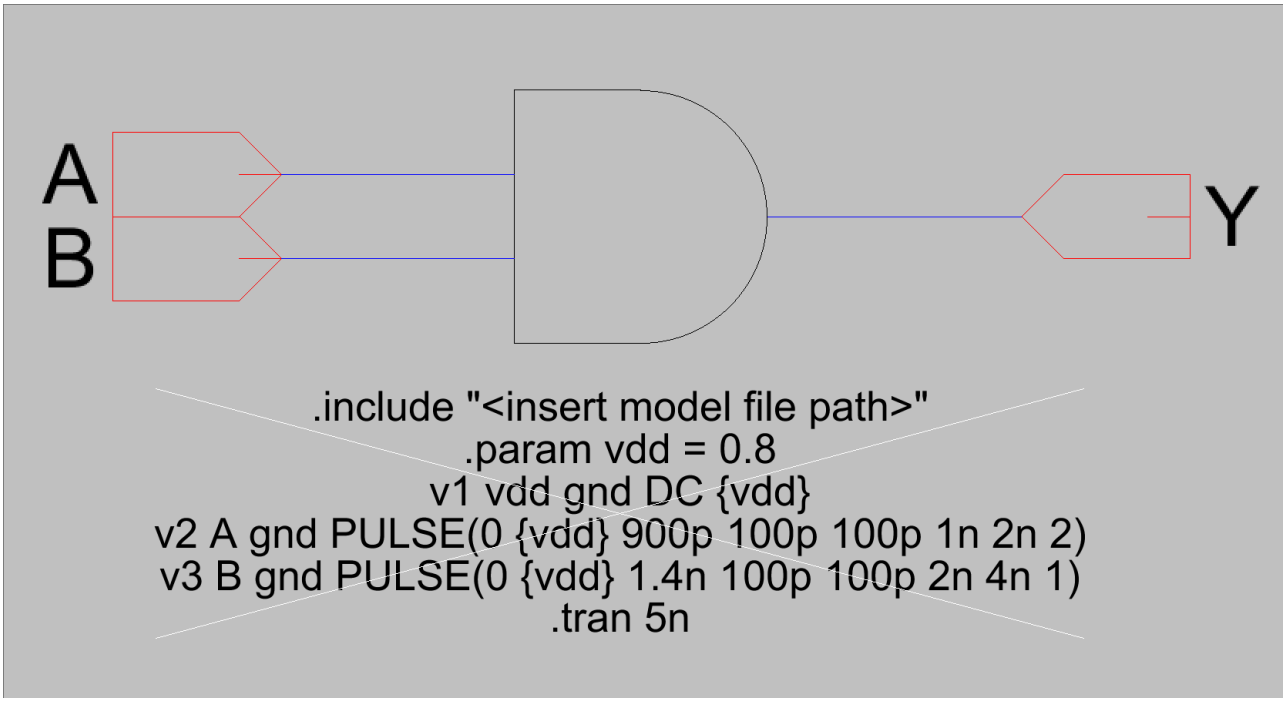


Layout

Electric Messages

```
Electric's log file is C:\WINDOWS\system32\electric.log.
================================1================================
Library /C:/Users/welcome/Documents/Academics/7th%20Sem/EE5311%20-%20Digital%20IC%20Design/Assignments/Assignment1/Size-4x/and2_4x.jelib read, took 0.023 secs
Checking library 'and2_4x' for repair... library checked
No errors found
================================2================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.003 secs)
Found 14 networks
Checking cell 'and2{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.112 secs)
================================3================================
Hierarchical NCC every cell in the design: cell 'and2{sch}'  cell 'and2{lay}'
Comparing: and2_4x:and2{sch} with: and2_4x:and2{lay}
  exports match, topologies match, sizes match in 0.028 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.035 seconds.
```

DRS LVS Clean Screenshot



Testbench
