
EE5311 - Digital IC Design

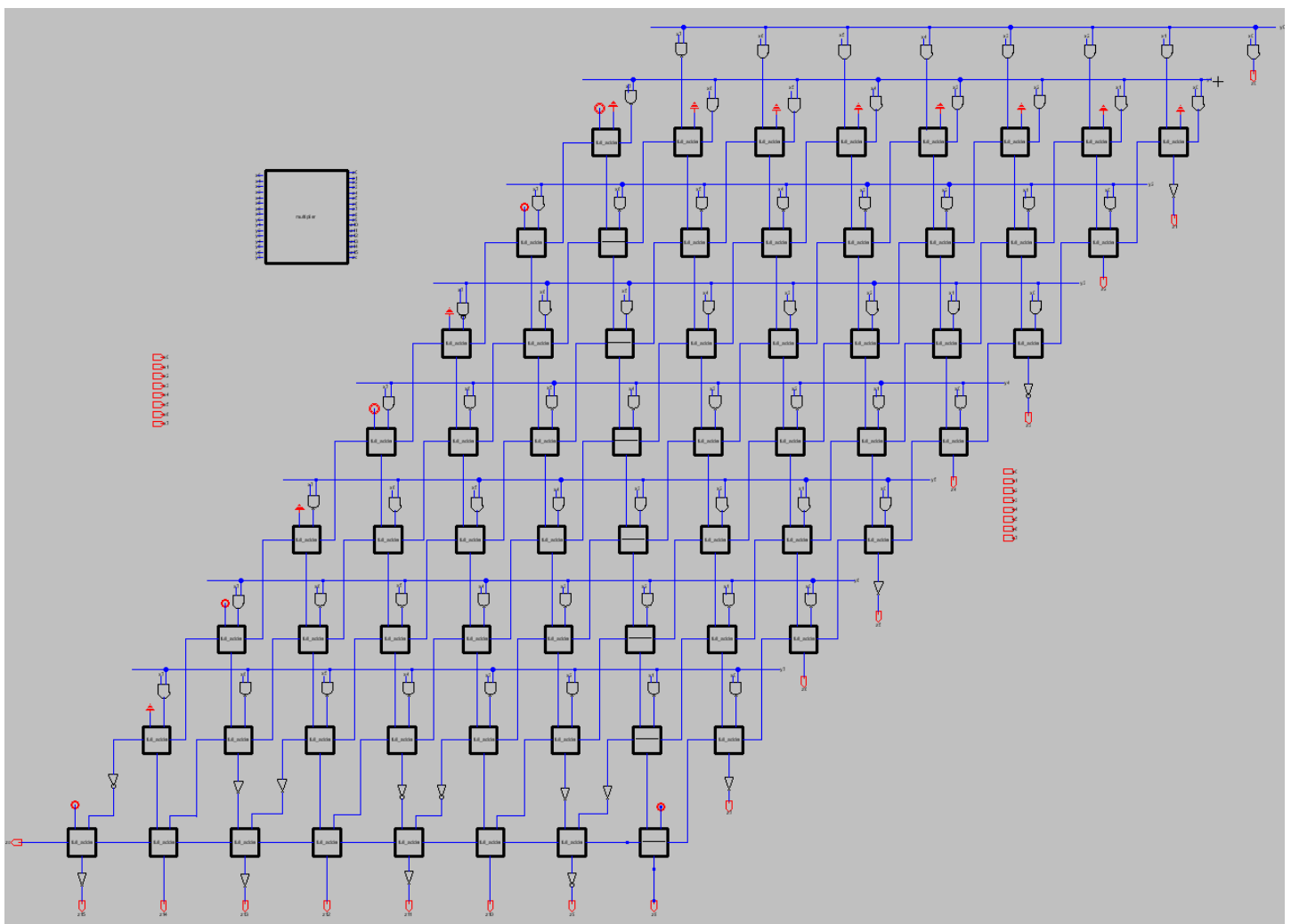
Assignment 4 - Schematic of a signed 8-bit Carry Save Multiplier

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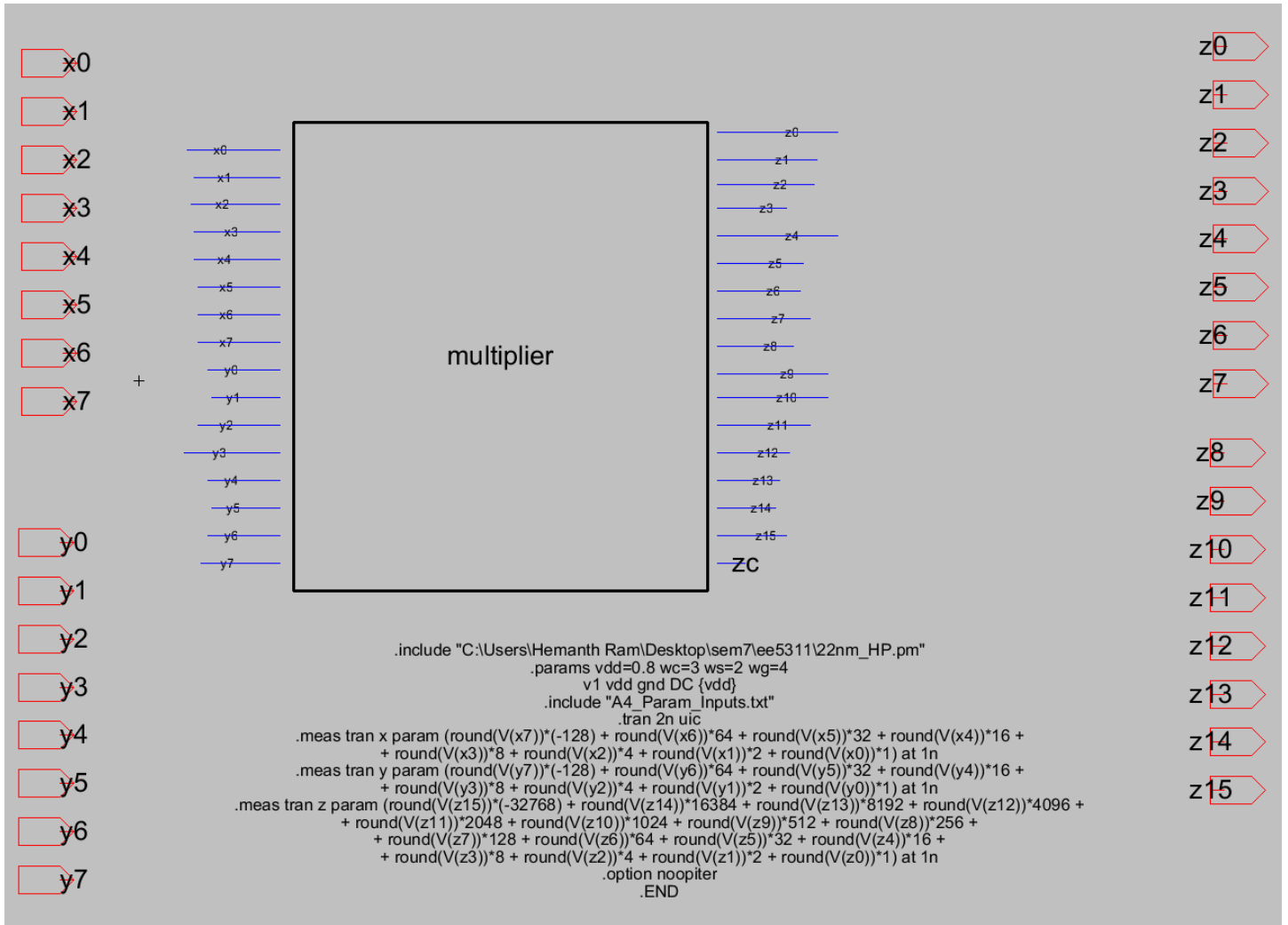
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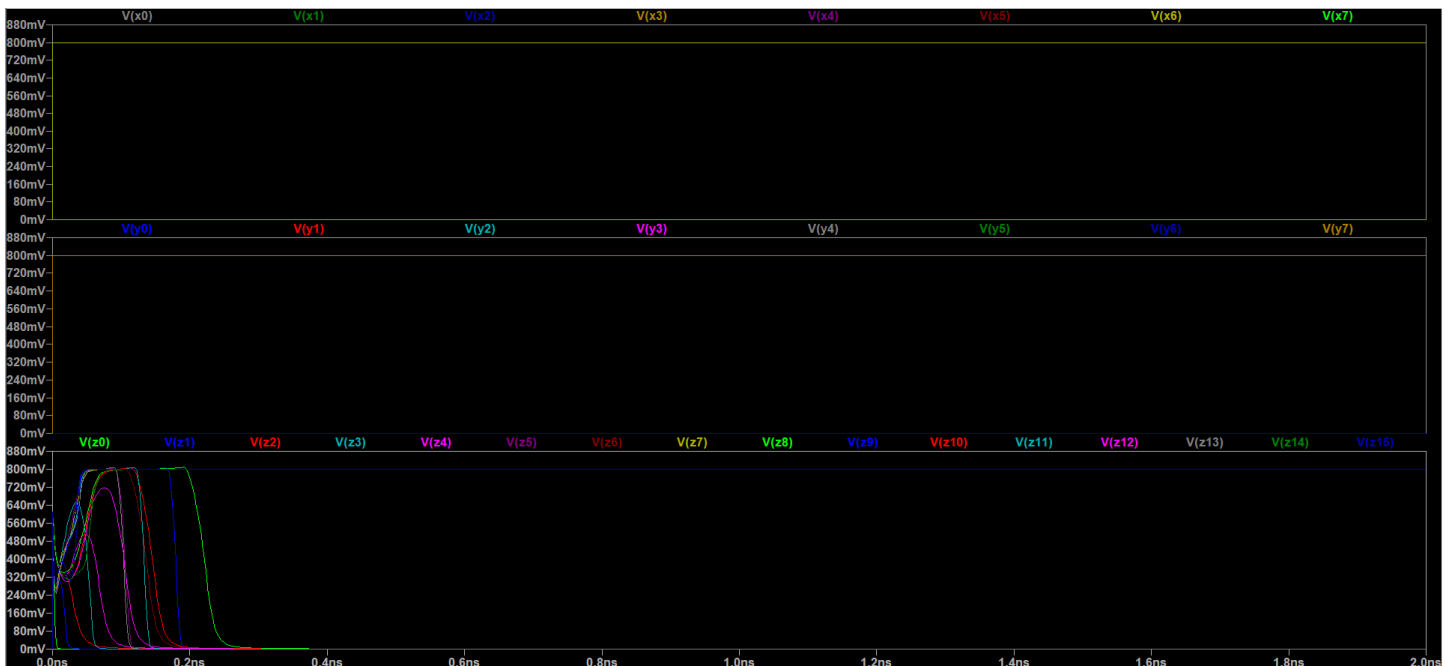
Schematic of CSM



Multiplier Testbench



Simulation output for $127 * -128$



Interpreted voltage values for 127 * -128

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=127
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=-128
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 + round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 + round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 + round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 + round(v(z0))*1)=-
16256
```

Interpreted voltage values for -128 * 127

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=-128
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=127
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 + round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 + round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 + round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 + round(v(z0))*1)=-
16256
```

Interpreted voltage values for 0 * 127

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=0
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=127
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 + round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 + round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 + round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 + round(v(z0))*1)=0
```

Interpreted voltage values for -128 * 0

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=-128
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=0
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 + round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 + round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 + round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 + round(v(z0))*1)=0
```

Interpreted voltage values for -12 * 13

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=-12
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=13
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 + round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 + round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 + round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 + round(v(z0))*1)=-
156
```

Interpreted voltage values for -1 * -1

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=-1
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=-1
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 + round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 + round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 + round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 + round(v(z0))*1)=1
```

Interpreted voltage values for -128 * -128

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=-128
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=-128
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 + round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 + round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 + round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 +
round(v(z0))*1)=16384
```

Interpreted voltage values for 103 * -57

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=103
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=-57
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 + round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 + round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 + round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 + round(v(z0))*1)=-
5871
```

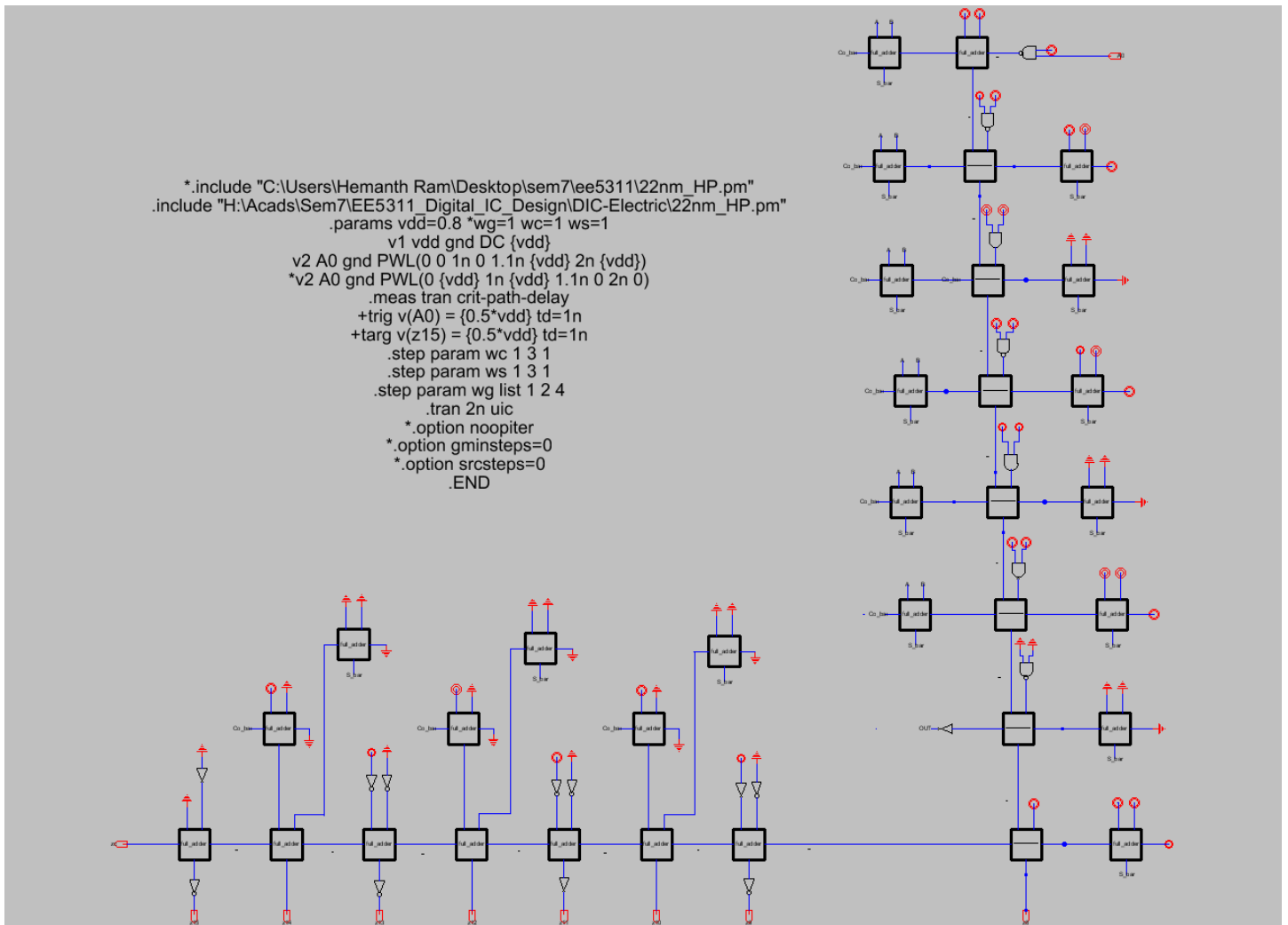
Interpreted voltage values for -50 * 50

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=-50
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=50
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 + round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 + round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 + round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 + round(v(z0))*1)=-
2500
```

Interpreted voltage values for 79 * 81

```
x: (round(v(x7))*(-128) + round(v(x6))*64 + round(v(x5))*32 + round(v(x4))*16 +
round(v(x3))*8 + round(v(x2))*4 + round(v(x1))*2 + round(v(x0))*1)=79
y: (round(v(y7))*(-128) + round(v(y6))*64 + round(v(y5))*32 + round(v(y4))*16 +
round(v(y3))*8 + round(v(y2))*4 + round(v(y1))*2 + round(v(y0))*1)=81
z: (round(v(z15))*(-32768) + round(v(z14))*16384 + round(v(z13))*8192 +
round(v(z12))*4096 + round(v(z11))*2048 + round(v(z10))*1024 + round(v(z9))*512 +
round(v(z8))*256 + round(v(z7))*128 + round(v(z6))*64 + round(v(z5))*32 +
round(v(z4))*16 + round(v(z3))*8 + round(v(z2))*4 + round(v(z1))*2 +
round(v(z0))*1)=6399
```

Critical Path of CSM modelled separately



Inputs to Full Adders in Critical Path

- Input Cin is closer than A, B to output and critical input is connected to Cin in every full adder.
- For an edge in Cin, sum delay for different combinations of A, B in a Full Adder:

Inputs to (A,B) \ Cin Edge Type	Rising	Falling
00	28.5ps	44.8ps
01	41.1ps	28.5ps
10	38.8ps	28.9ps
11	75.6ps	18.7ps

So, for both rising edge in Cin, A=1, B=1 and for falling edge in Cin, A=0, B=0 for max delay in sum propagation

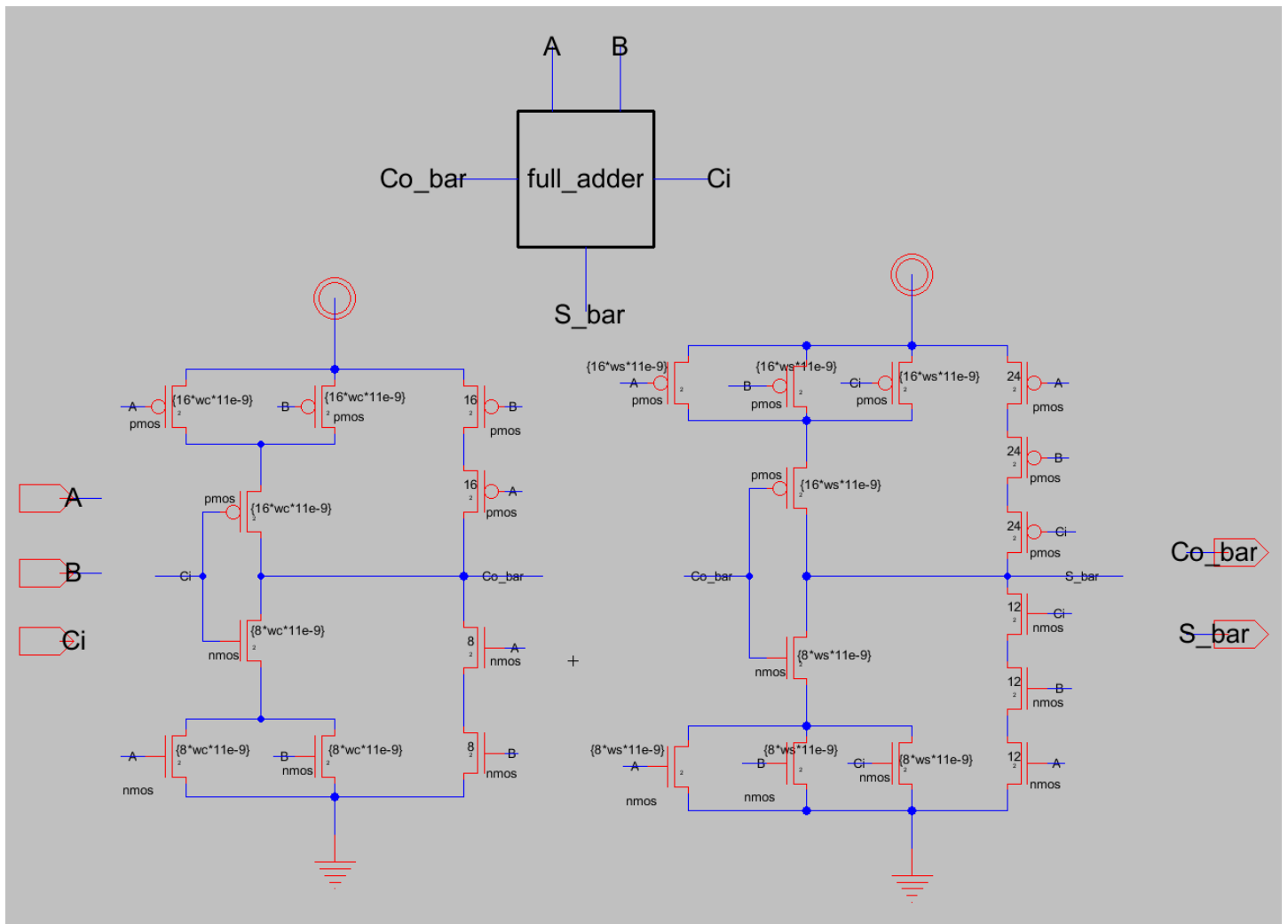
- For an edge in Carry in, Full Adder should be in propagation stage for max delay. Delays for different combinations of A/B in Full Adder:

Inputs to (A, B) \ Cin Edge Type	Rising	Falling
01	29.9ps	10.6ps
10	28.4ps	10.5ps

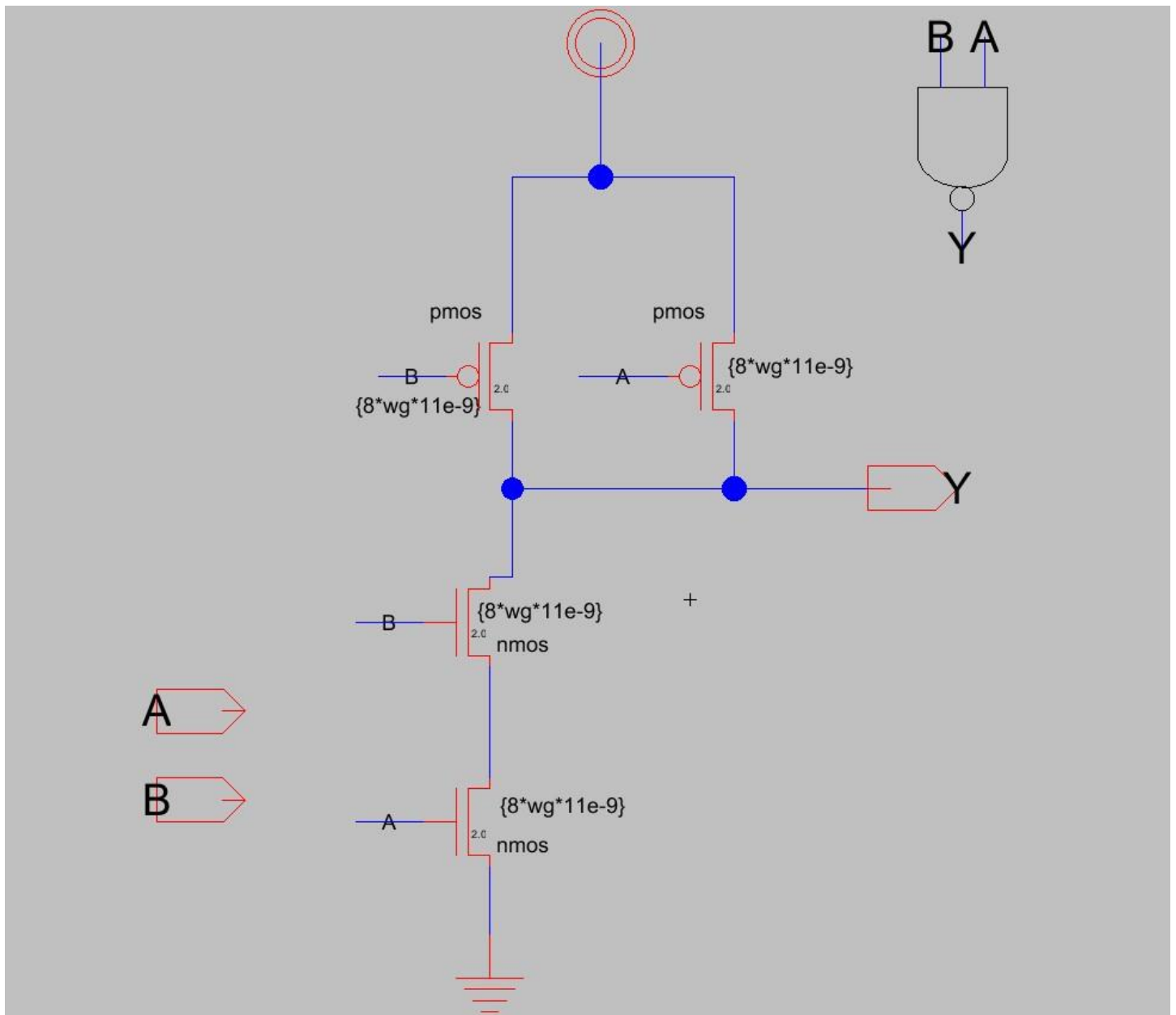
So, for rising/falling edge in Cin, A=0, B=1 for max delay in carry propagation

Sizes of FA, NAND, AND and INV gates used are parameterised

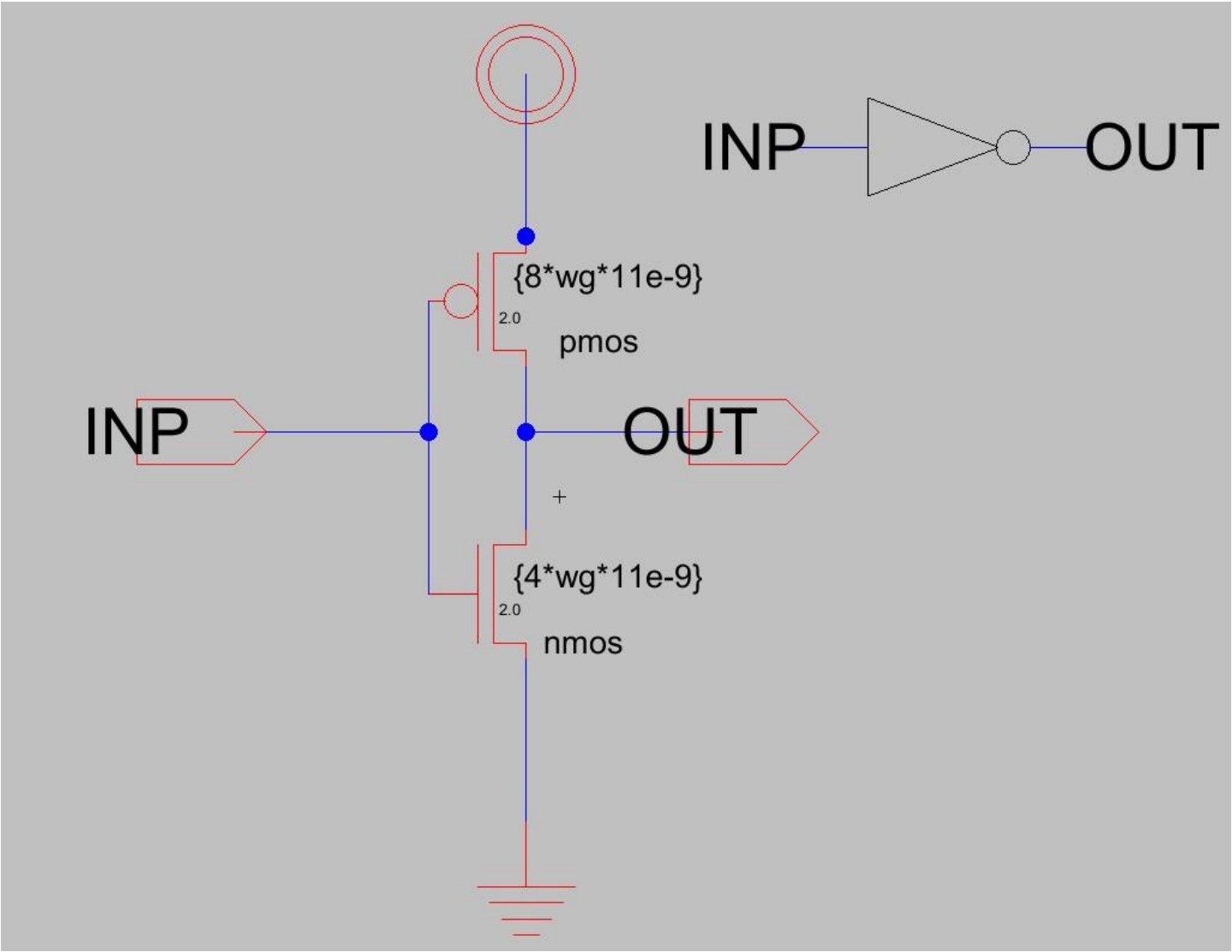
Schematic of Full Adder used



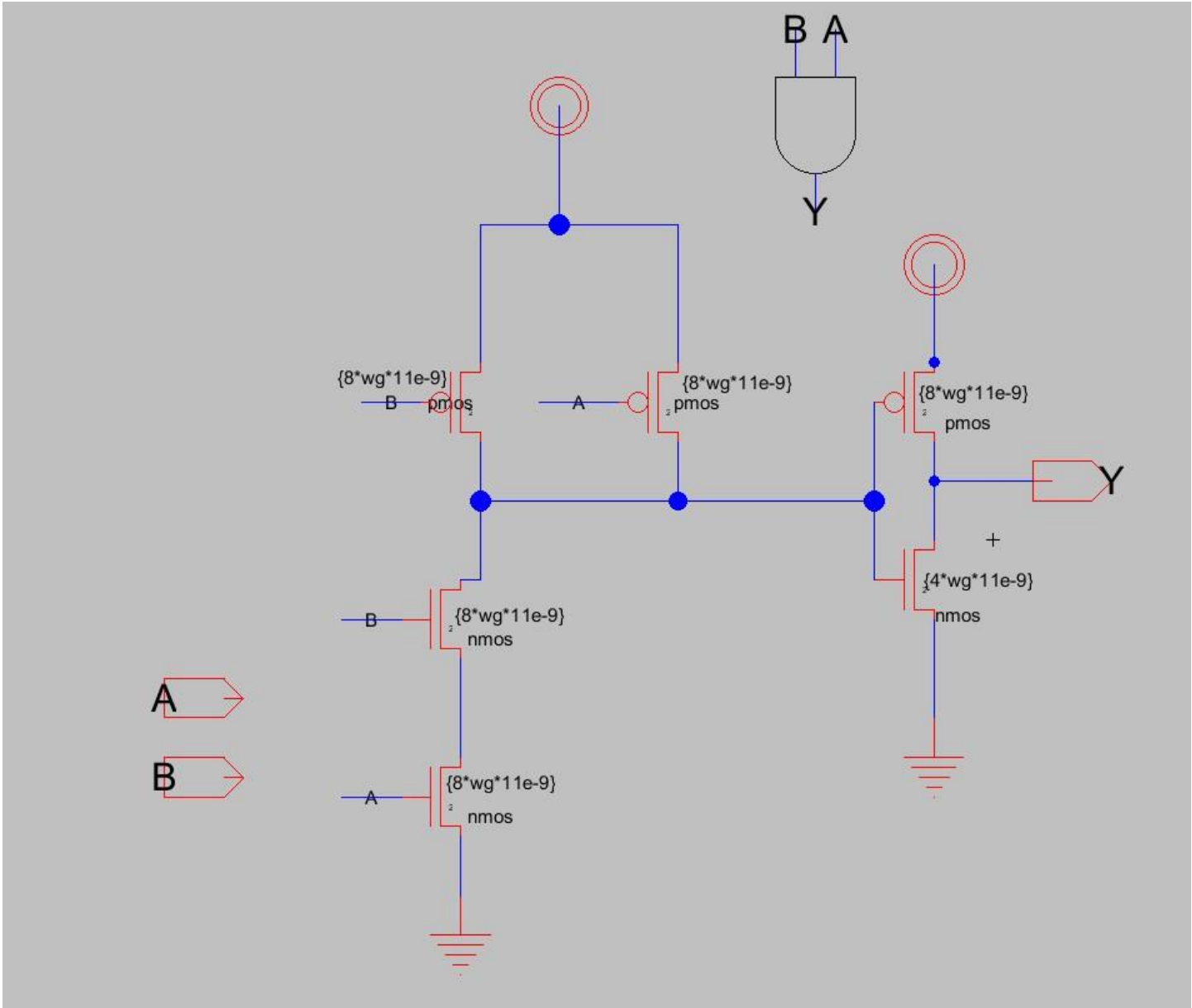
Schematic of NAND gate used



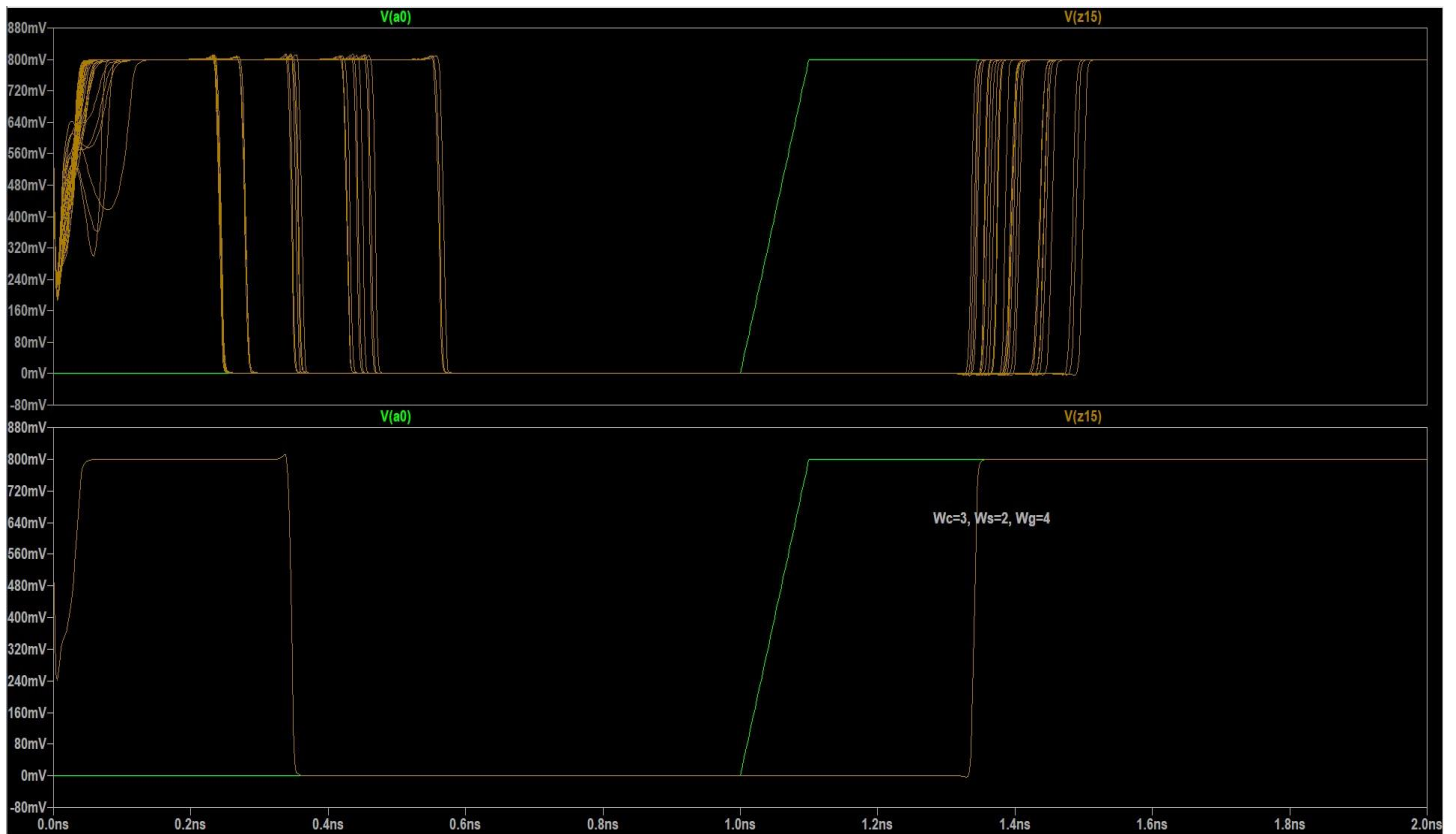
Schematic of Inverter used



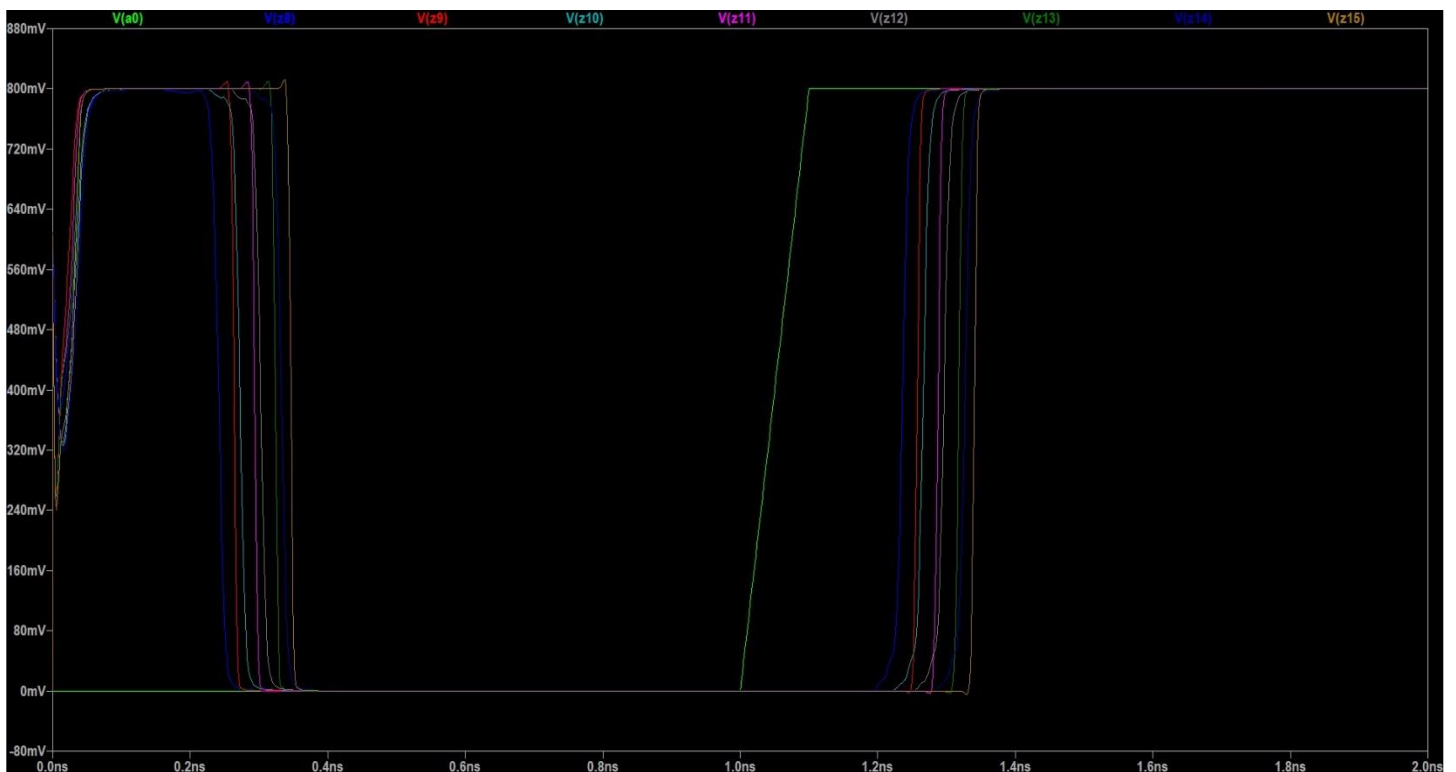
Schematic of AND gate used



Simulation of Critical Path Delay swept across possible gate size combinations



Simulation of Vector Merge outputs for critical input



Critical Path Delay tabulated across gate size combinations

1	wc=1	ws=1	wg=1	3.92E-10	1.05E-09	1.44E-09
2	wc=2	ws=1	wg=1	3.53E-10	1.05E-09	1.40E-09
3	wc=3	ws=1	wg=1	3.56E-10	1.05E-09	1.41E-09
4	wc=1	ws=2	wg=1	4.04E-10	1.05E-09	1.45E-09
5	wc=2	ws=2	wg=1	3.24E-10	1.05E-09	1.37E-09
6	wc=3	ws=2	wg=1	3.06E-10	1.05E-09	1.36E-09
7	wc=1	ws=3	wg=1	4.49E-10	1.05E-09	1.50E-09
8	wc=2	ws=3	wg=1	3.36E-10	1.05E-09	1.39E-09
9	wc=3	ws=3	wg=1	3.06E-10	1.05E-09	1.36E-09
10	wc=1	ws=1	wg=2	3.87E-10	1.05E-09	1.44E-09
11	wc=2	ws=1	wg=2	3.46E-10	1.05E-09	1.40E-09
12	wc=3	ws=1	wg=2	3.48E-10	1.05E-09	1.40E-09
13	wc=1	ws=2	wg=2	3.96E-10	1.05E-09	1.45E-09
14	wc=2	ws=2	wg=2	3.14E-10	1.05E-09	1.36E-09
15	wc=3	ws=2	wg=2	2.96E-10	1.05E-09	1.35E-09
16	wc=1	ws=3	wg=2	4.39E-10	1.05E-09	1.49E-09
17	wc=2	ws=3	wg=2	3.25E-10	1.05E-09	1.37E-09
18	wc=3	ws=3	wg=2	2.93E-10	1.05E-09	1.34E-09
19	wc=1	ws=1	wg=4	3.86E-10	1.05E-09	1.44E-09
20	wc=2	ws=1	wg=4	3.44E-10	1.05E-09	1.39E-09
21	wc=3	ws=1	wg=4	3.45E-10	1.05E-09	1.40E-09
22	wc=1	ws=2	wg=4	3.92E-10	1.05E-09	1.44E-09
23	wc=2	ws=2	wg=4	3.10E-10	1.05E-09	1.36E-09
24	wc=3	ws=2	wg=4	2.87E-10	1.05E-09	1.34E-09
25	wc=1	ws=3	wg=4	4.34E-10	1.05E-09	1.48E-09
26	wc=2	ws=3	wg=4	3.19E-10	1.05E-09	1.37E-09
27	wc=3	ws=3	wg=4	2.87E-10	1.05E-09	1.34E-09

Chosen Gate sizes

Full Adder:

Cout-bar: 3x

Sum-bar: 2x

Standard Cells:

NAND, AND, INV: 4x

--End--