EE5311 – Digital IC Design

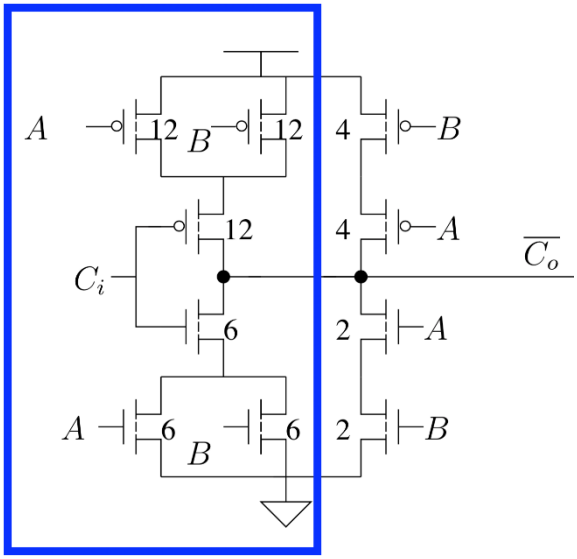
July – November 2021

Assignment – 2

Member 1 - Srivenkat (EE18B038), Member 2 - Hemanth Ram (EE18B132), Member 3 - Sidesh (EE18B032)

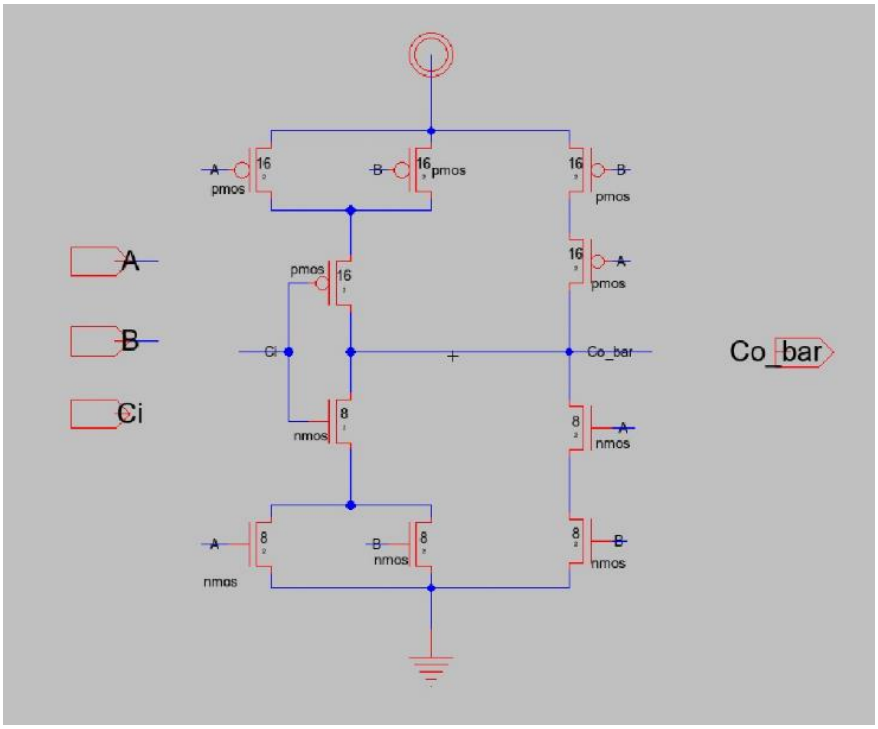
Overview

In this assignment we design the Carry Out Circuit of a Full Adder shown below.

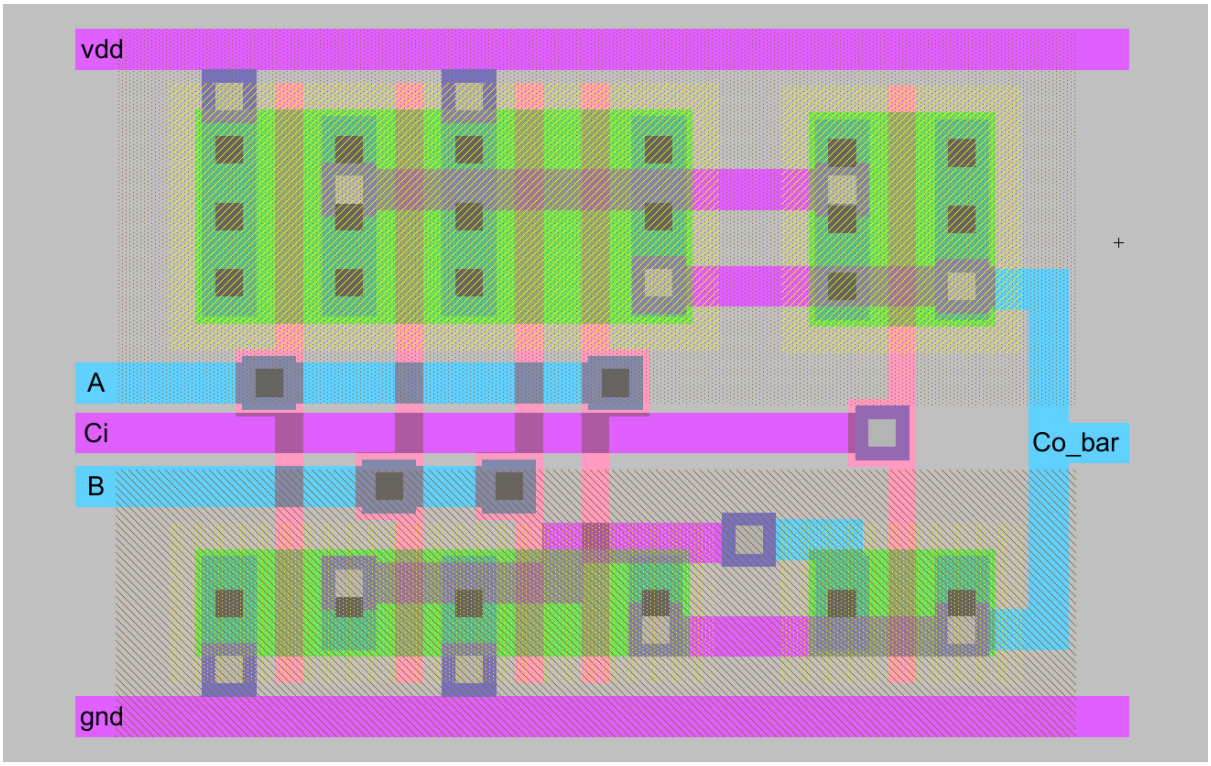


Part 1 - Size 1x

Schematic



Layout



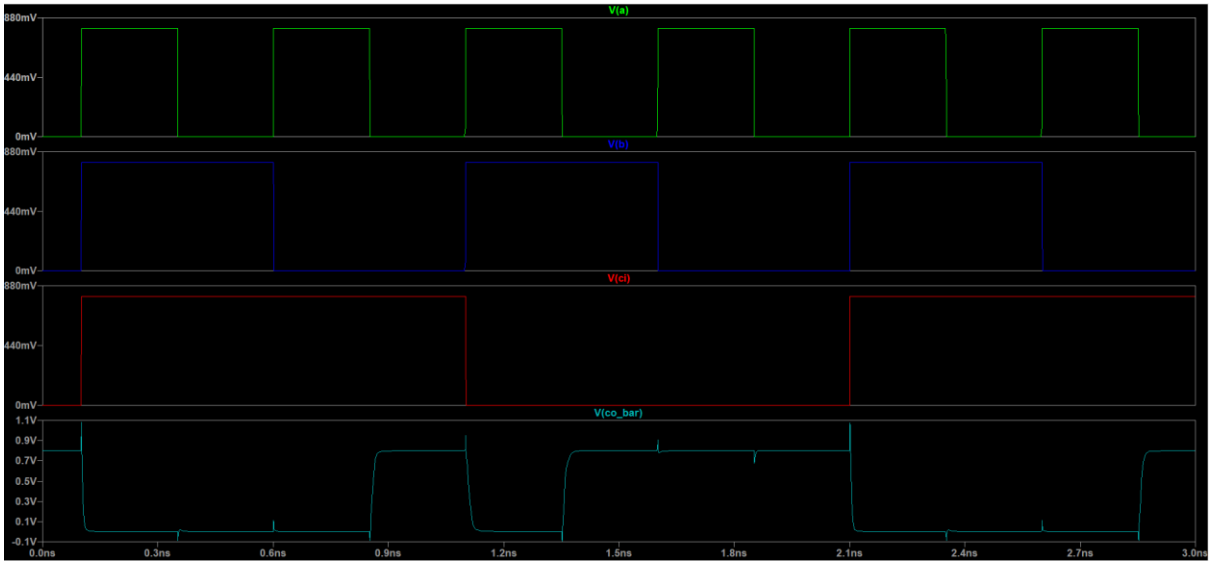
DRS LVS Check

```
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.002 secs)
Found 21 networks
0 errors and 0 warnings found (took 0.022 secs)
================================4================================
Hierarchical NCC every cell in the design: cell 'carryout{sch}'  cell 'carryout{lay}'
Comparing: carryout-lx:carryout{sch} with: carryout-lx:carryout{lay}
  exports match, topologies match, sizes match in 0.038 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.048 seconds.
```

SPICE Code

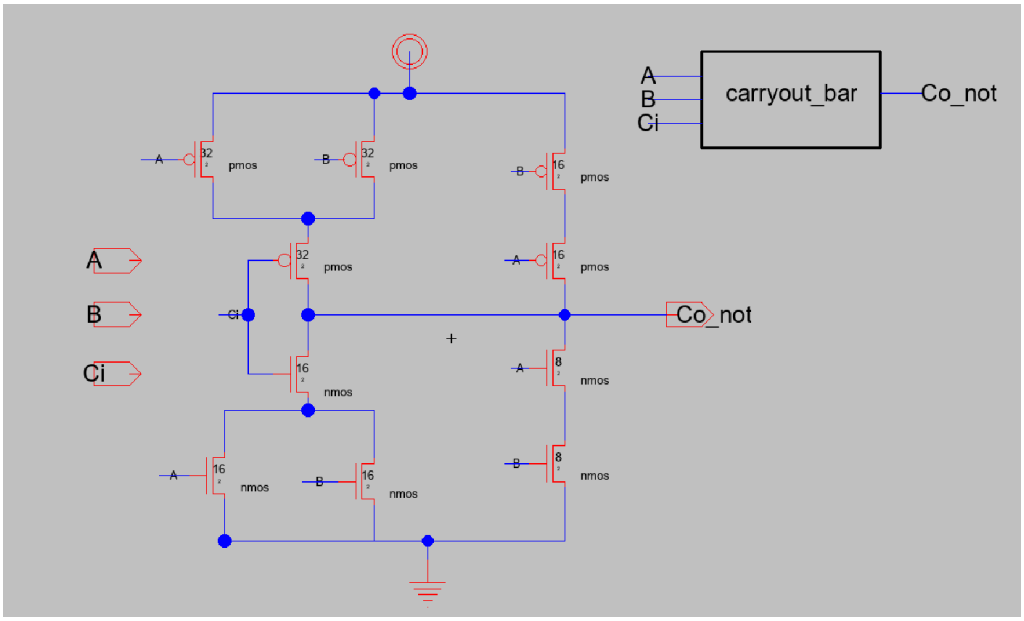
```
* Spice Code nodes in cell cell 'test_carryout{sch}'
.include "H:\Acads\Sem7\EE5311_Digital_IC_Design\DIC-Electric\22nm_HP.pm"
.param vdd {0.8}
v1 vdd gnd DC {vdd}
v2 A gnd PULSE(0 {vdd} 100p 1p 1p 250p 500p 20)
v3 B gnd PULSE(0 {vdd} 100p 1p 1p 500p 1000p 20)
v4 Ci gnd PULSE(0 {vdd} 100p 1p 1p 1000p 2000p 20)
.tran 0 3n
.end
.END
```

Simulation Output



Part 2 - Size 2x

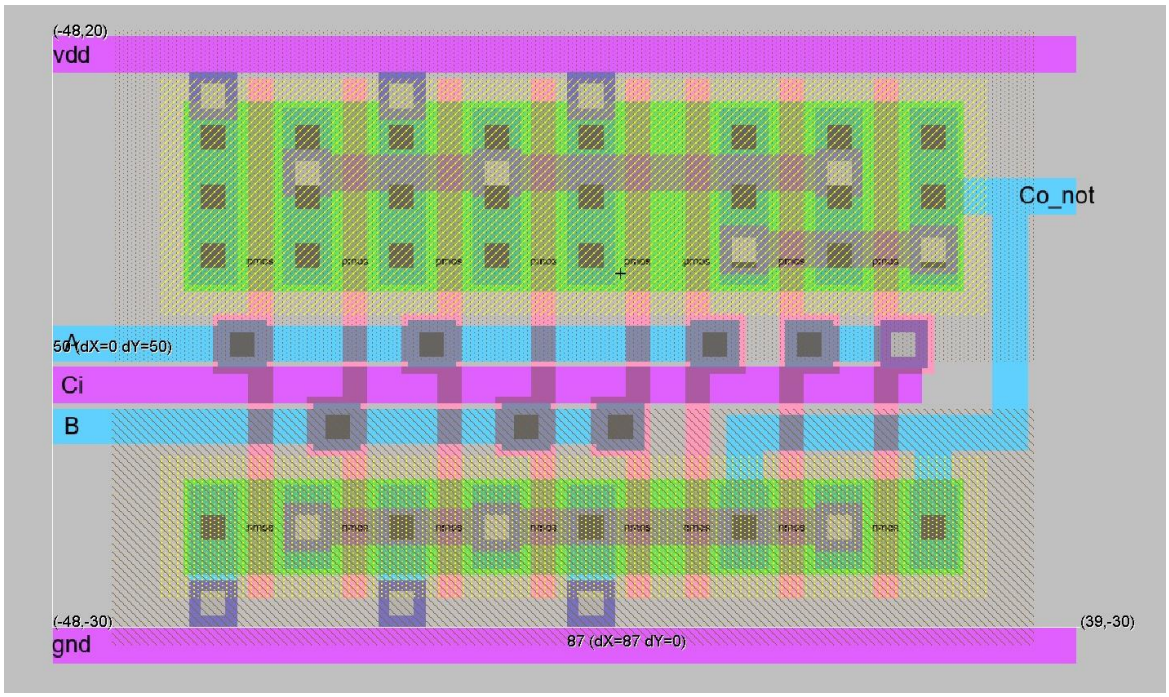
Schematic



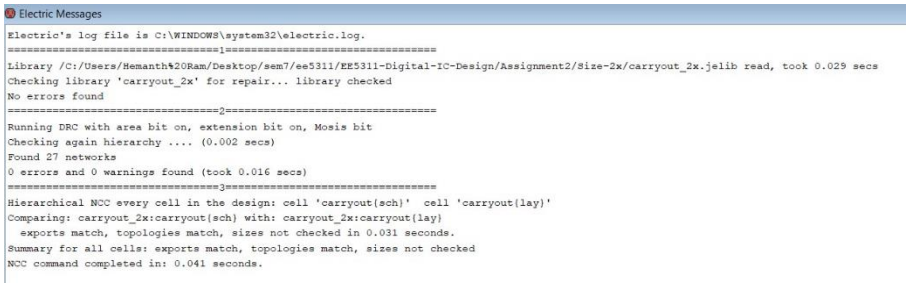
SPICE Code

```
* Spice Code nodes in cell cell 'carryout_bar_2x_test{sch}'
.include "C:\Users\Hemanth Ram\Desktop\sem7\ee5311\22nm_HP.pm"
.param vdd {0.8}
v1 vdd gnd DC {vdd}
v2 A gnd PULSE(0 {vdd} 100p 1p 1p 250p 500p 20)
v3 B gnd PULSE(0 {vdd} 100p 1p 1p 500p 1000p 20)
v4 Ci gnd PULSE(0 {vdd} 100p 1p 1p 1000p 2000p 20)
.tran 0 3n
.end
.END
```

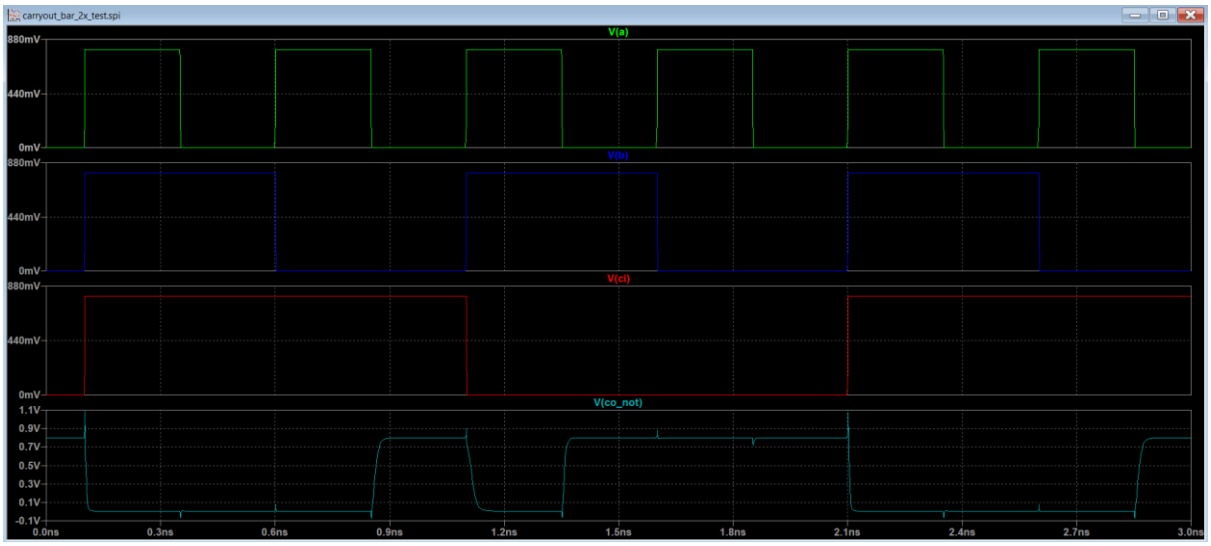
Layout



DRC LVS Check

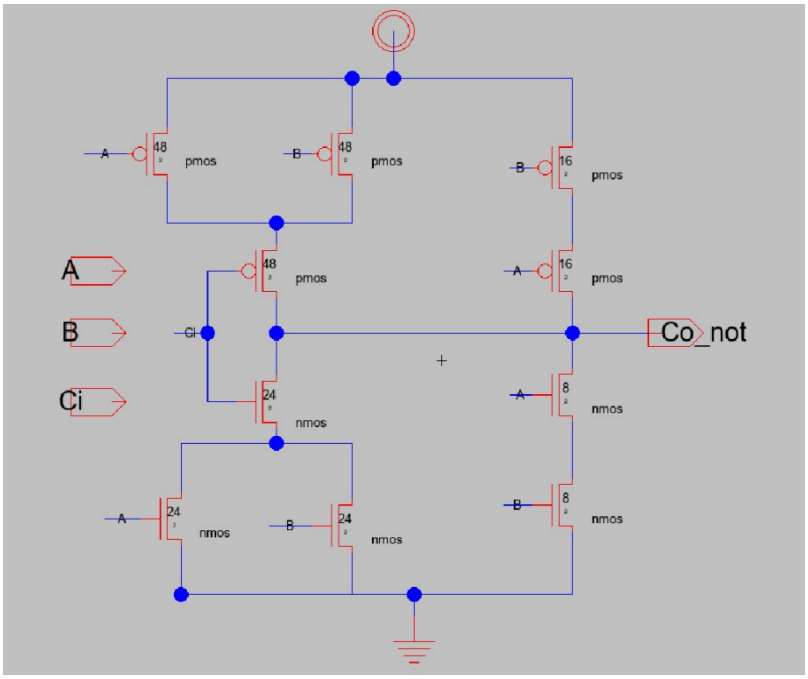


Simulation Output



Part 3 - Size 3x

Schematic



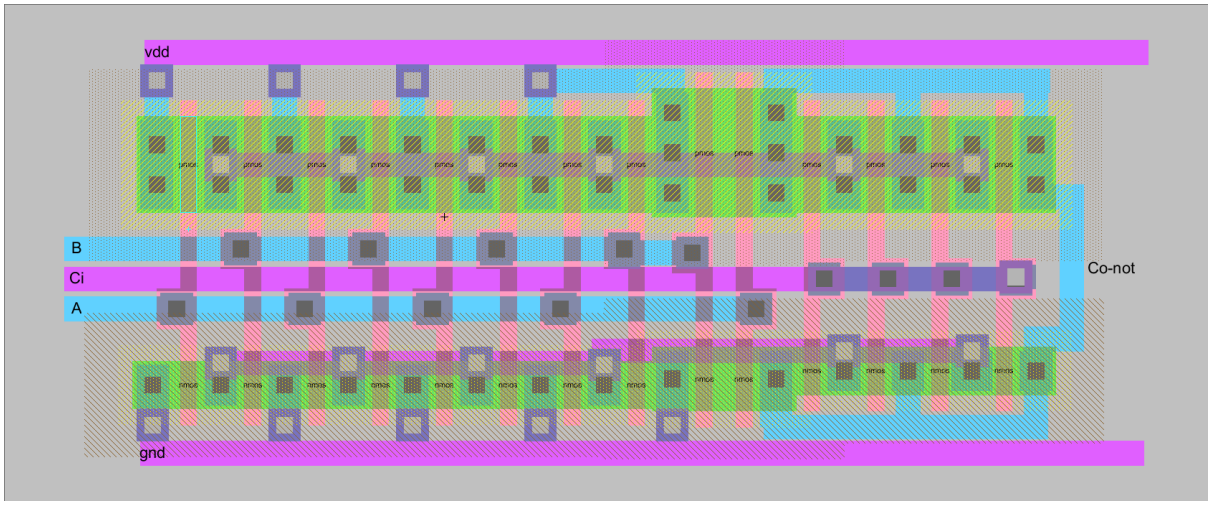
SPICE Code

```
* Spice Code nodes in cell cell 'carryout{lay}'
.include "D:\Program_Files\22nm_HP.pm"
.param VDD = 0.8
v1 VDD GND DC {VDD}
v2 A gnd PULSE(0 {VDD} 0.5n 100p 100p 0.5n 1.2n 4)
v3 B gnd PULSE(0 {VDD} 0.5n 100p 100p 1n 2.2n 2)
v4 Ci gnd PULSE(0 {VDD} 0.5n 100p 100p 2n 4.2n 1)
.tran 5n
.END
```

DRC LVS Check

```
================================230================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 39 networks
Checking cell 'carryout{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.059 secs)
================================231================================
Hierarchical NCC every cell in the design: cell 'carryout{sch}'  cell 'carryout{lay}'
Comparing: carryout-3x:carryout{sch} with: carryout-3x:carryout{lay}
  exports match, topologies match, sizes match in 0.066 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.081 seconds.
```

Layout



Simulation Output