

# EE5311 - Digital IC Design

## Assignment 1 - Inverter, NAND2 and AND2

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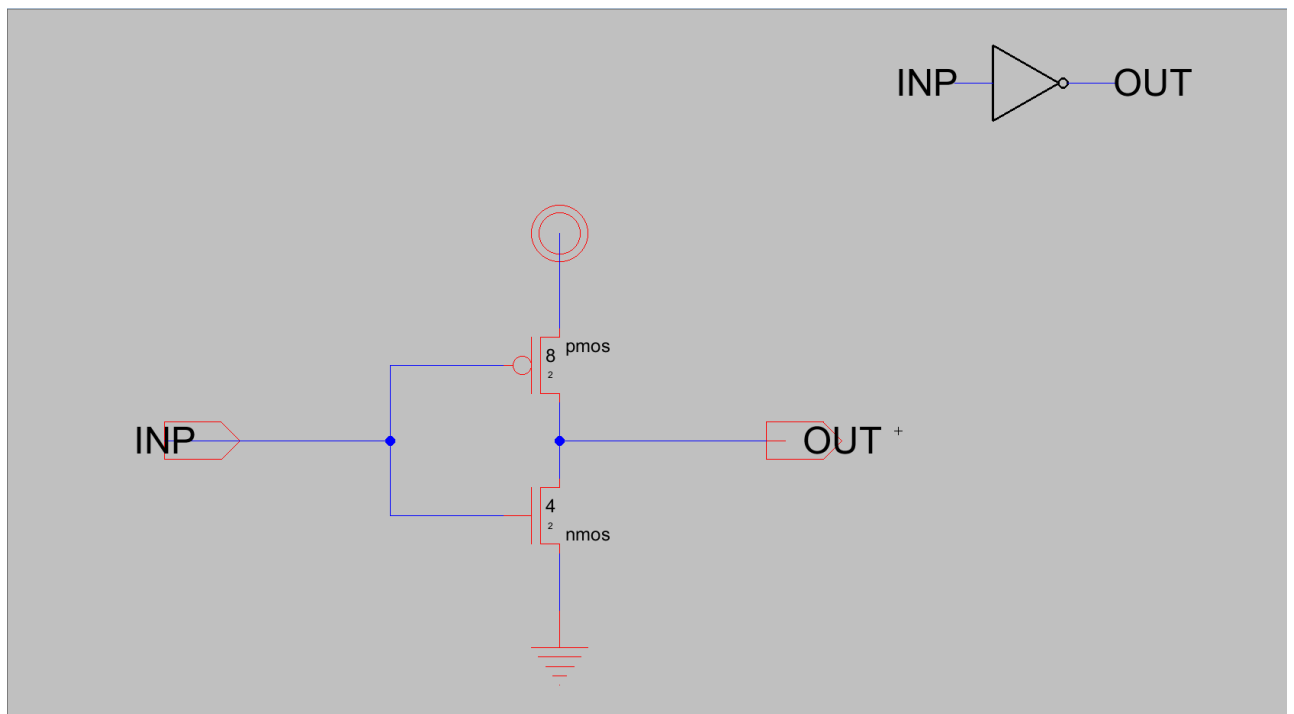
Member 2: **Hemanth Ram G K**(EE18B132)

Member 3: **Sidesh S**(EE18B032)

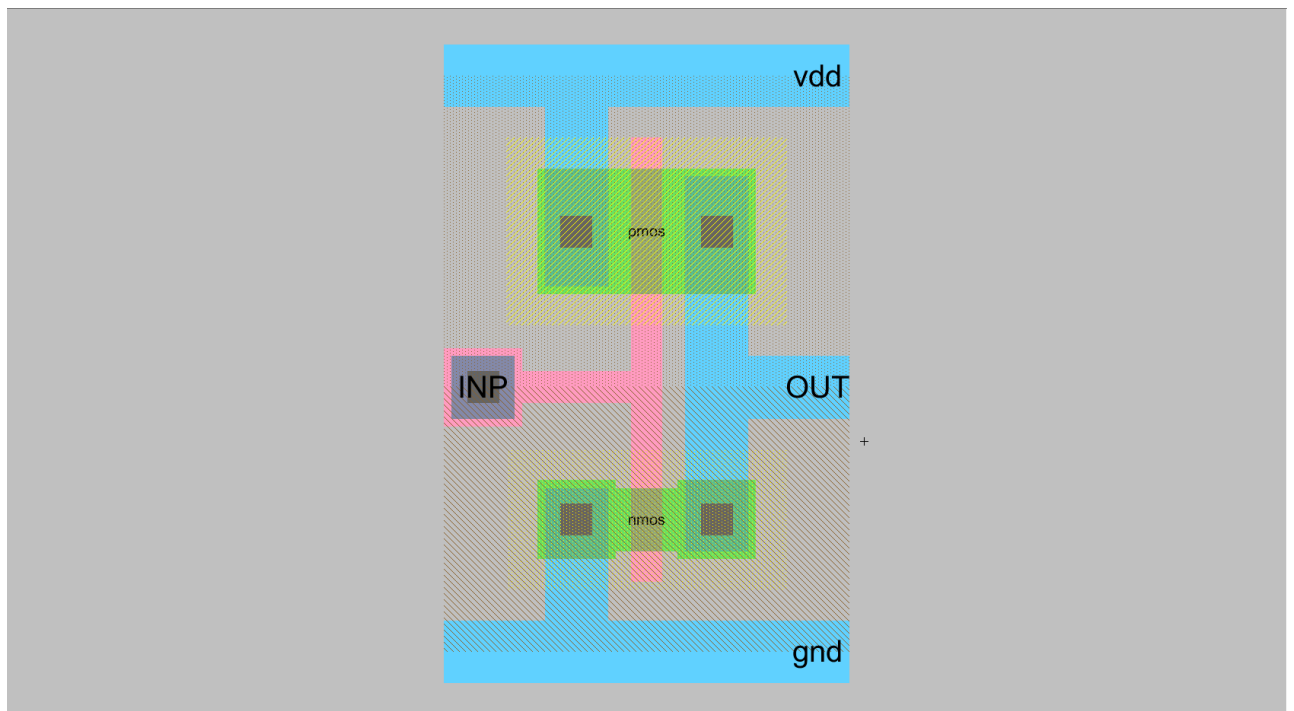
### Part A - Inverter

#### Inverter 1x

Dimensions:  $L=2\lambda$ ,  $W_n=4\lambda$ ,  $W_p=8\lambda$



Schematic



Layout

```

=====22=====
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 7 networks
0 errors and 0 warnings found (took 0.001 secs)
=====10=====
Hierarchical NCC every cell in the design: cell 'inverter[sch]' cell 'inv-lx_inverter[lay]'
Comparing: inv-lx:inverter[sch] with: inv-lx:inv-lx_inverter[lay]
    exports match, topologies match, sizes not checked in 0.002 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.003 seconds.
=====17=====

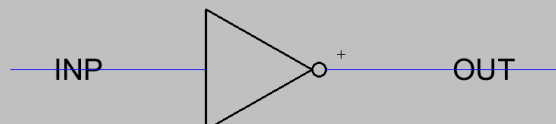
```

DRC LVS Clean Screenshot

```

.include "H:\Acads\Sem7\EE5311_Digital_IC_Design\DIC-Electric\22nm_HP.pm"
v1 vdd gnd DC 0.8
v2 INP gnd pwl(0 0 100p 0.8 1n 0.8 1.1n 0 2n 0)
.tran 2.1n
.END

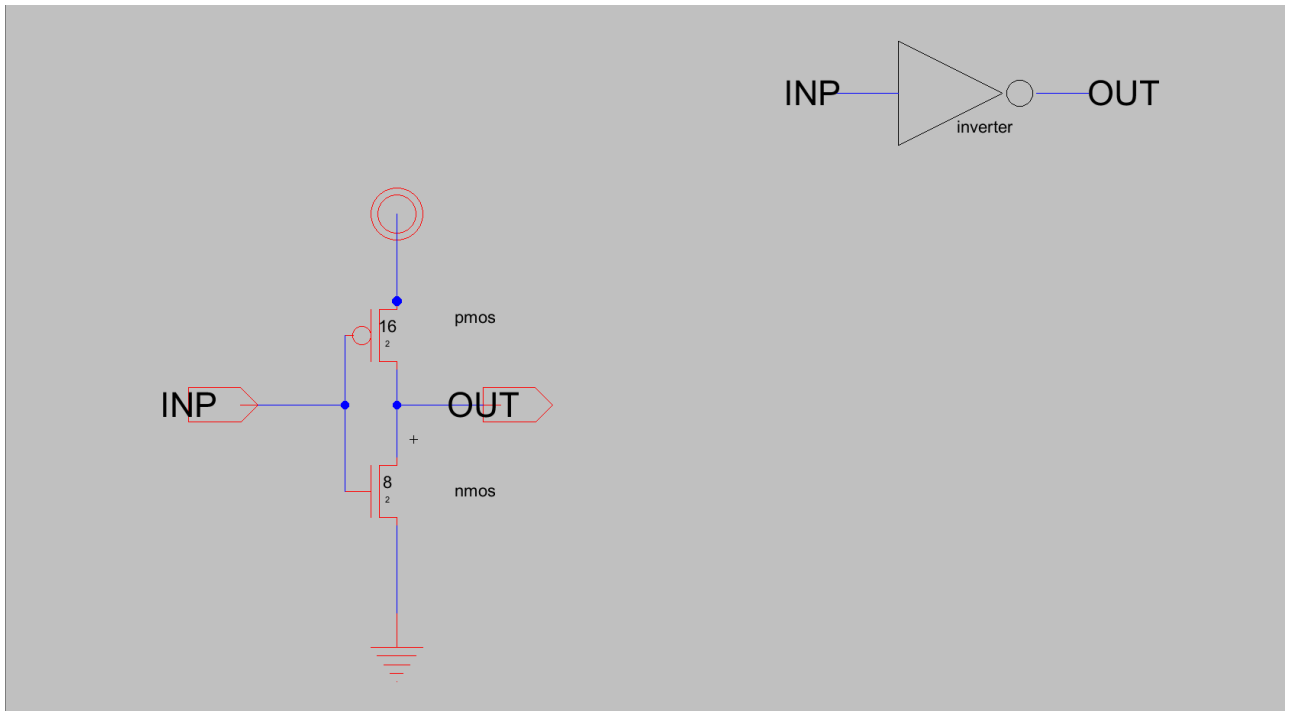
```



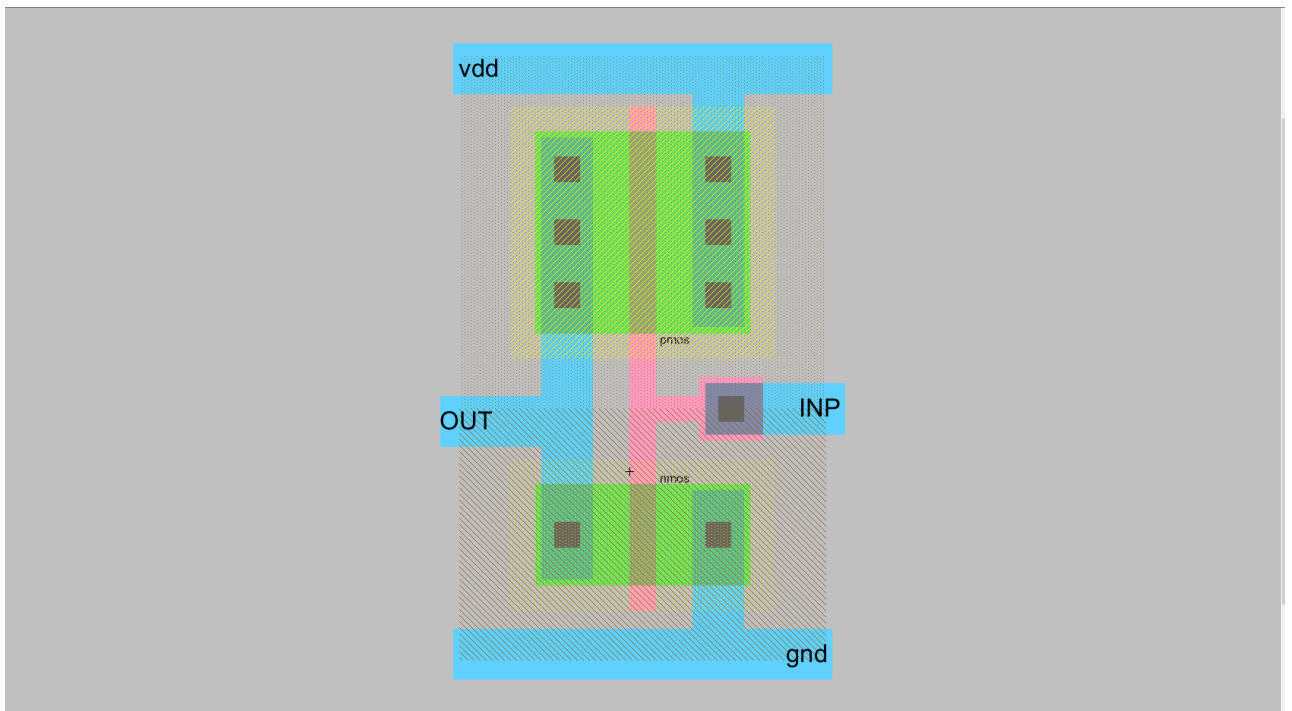
Testbench

## Inverter 2x

Dimensions:  $L=2\lambda$ ,  $W_n=8\lambda$ ,  $W_p=16\lambda$



## Schematic



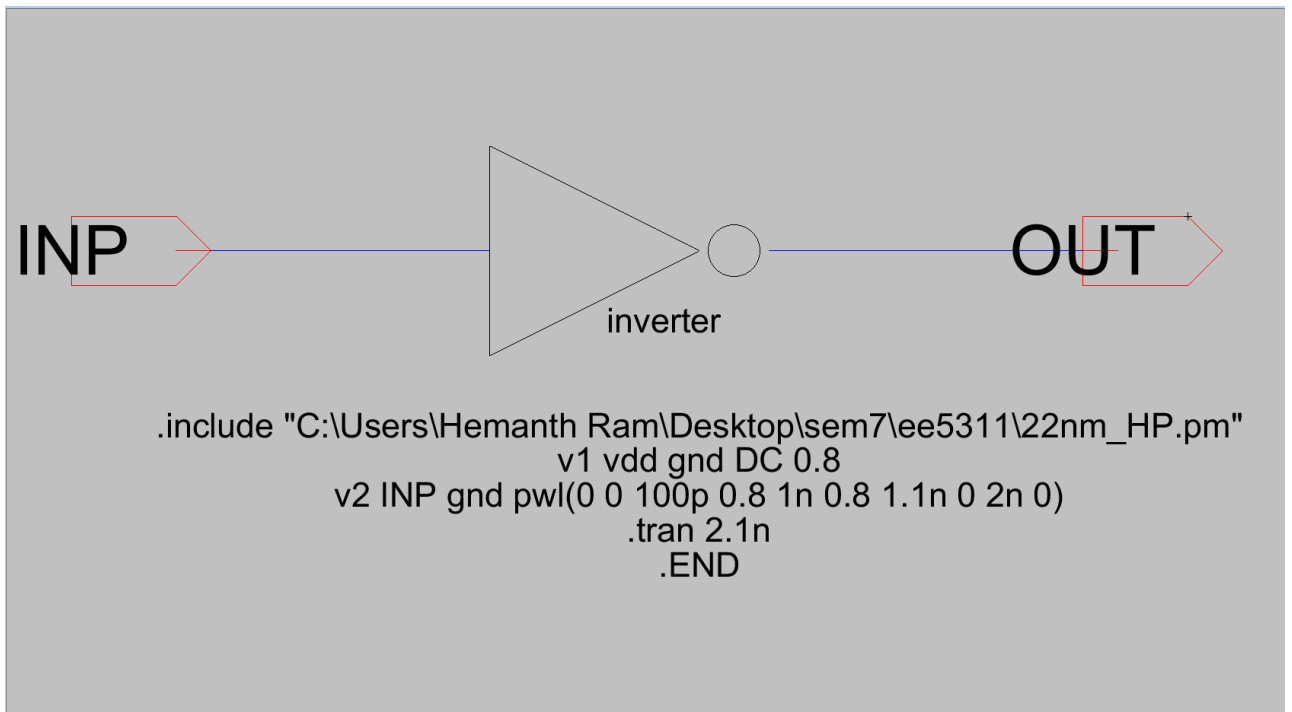
## Layout

```

=====6=====
Hierarchical NCC every cell in the design: cell 'inverter[sch]' cell 'test_inverter[lay]'
Comparing: not_2x:inverter[sch] with: not_2x:test_inverter[lay]
  exports match, topologies match, sizes not checked in 0.001 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.002 seconds.
=====7=====
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)|
Found 7 networks
0 errors and 0 warnings found (took 0.002 secs)

```

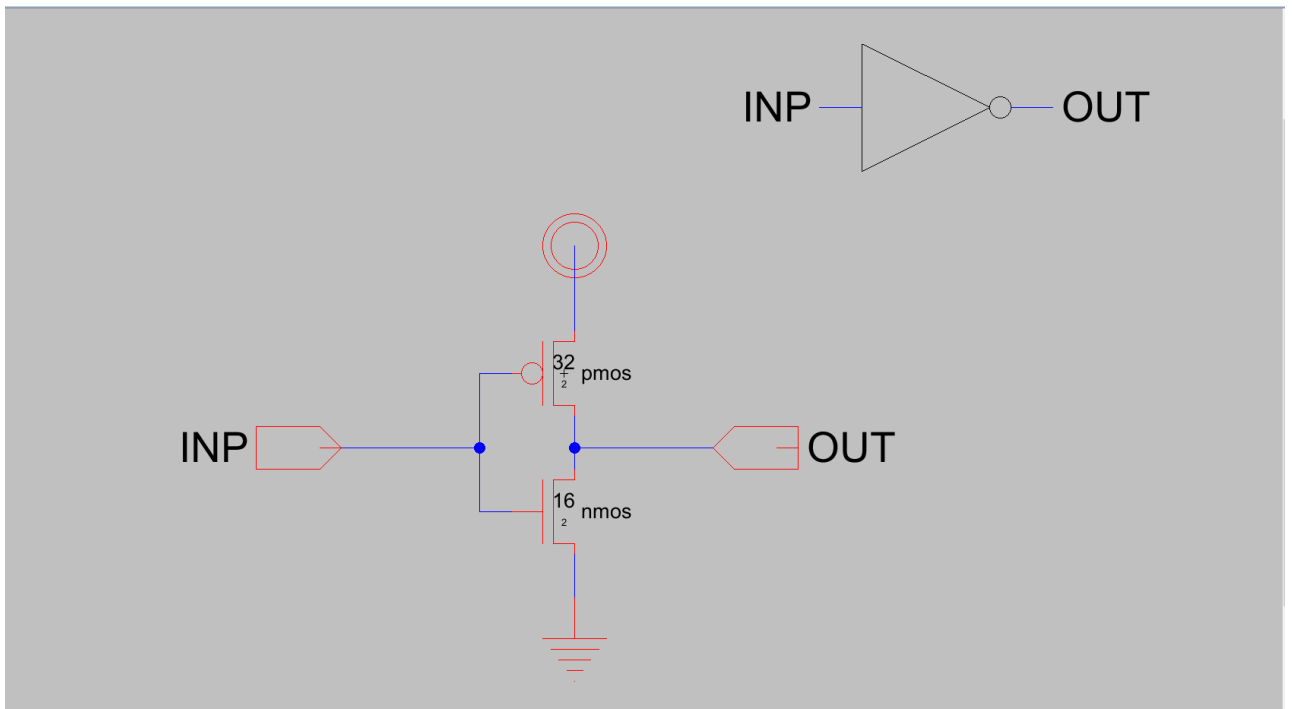
### DRC LVS Clean Screenshot



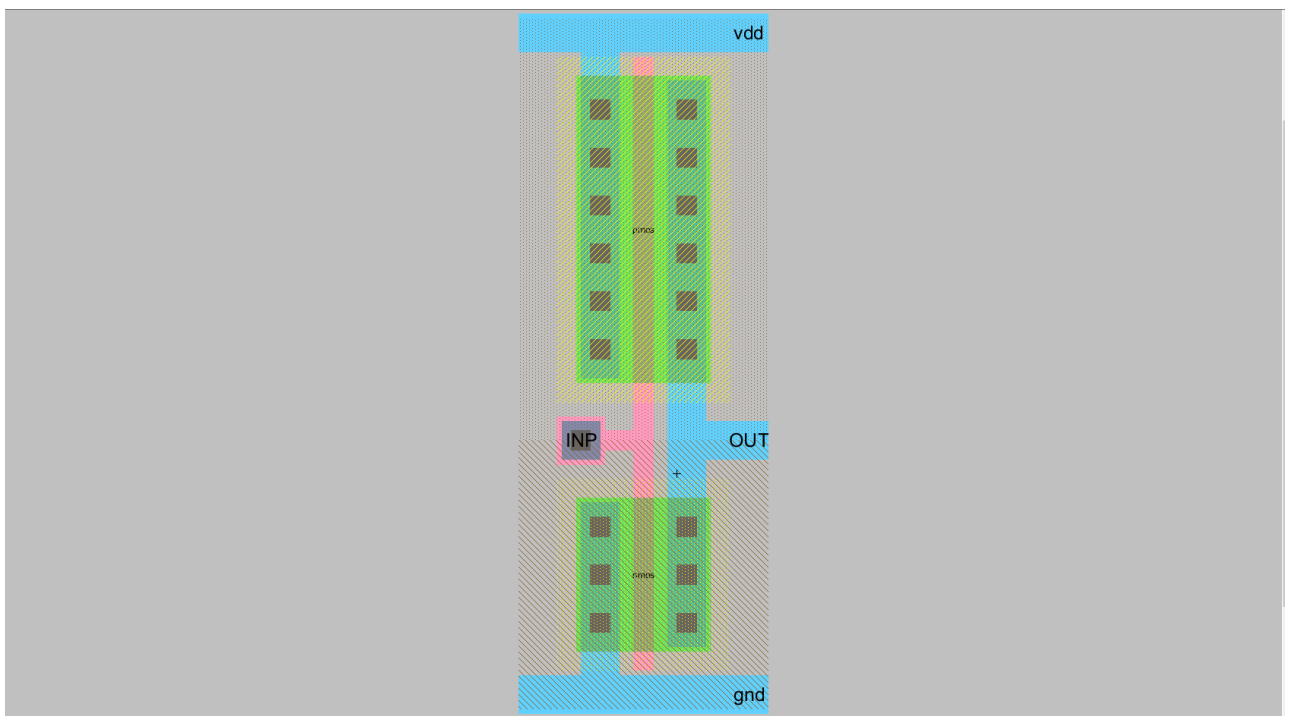
### Testbench

### Inverter 4x

Dimensions: L=2λ, Wn=16λ, Wp=32λ

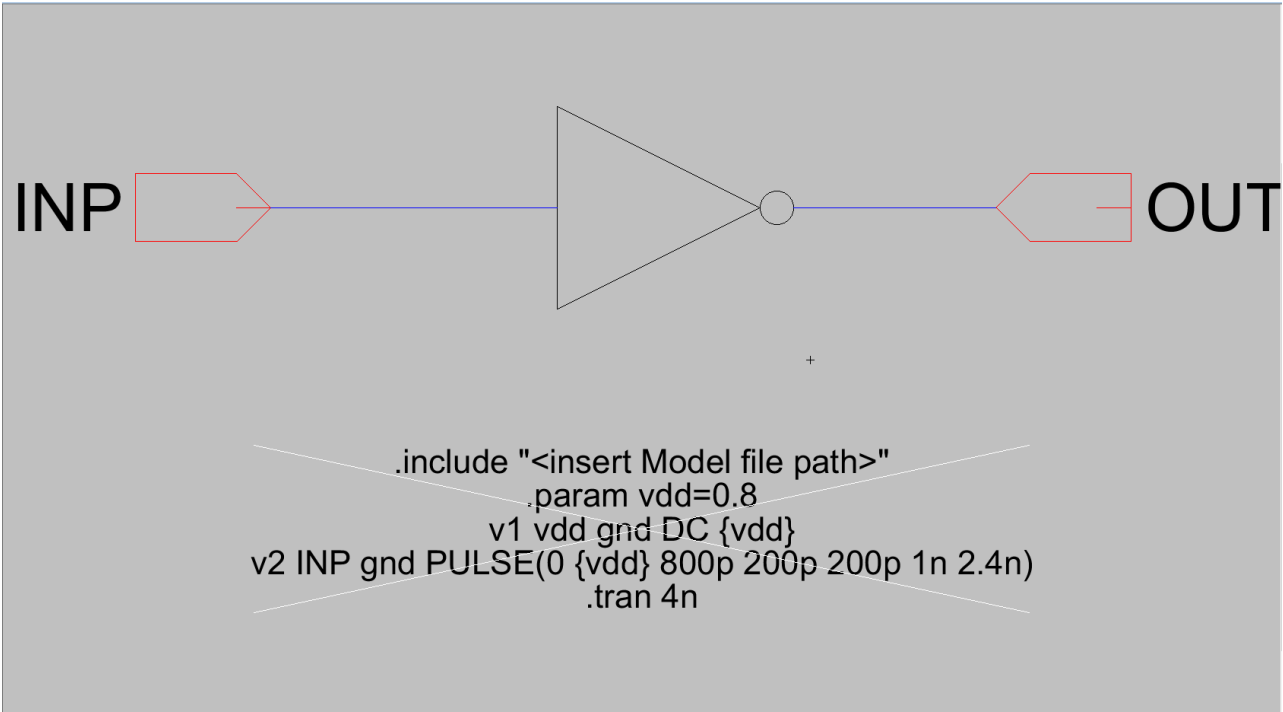


Schematic



Layout

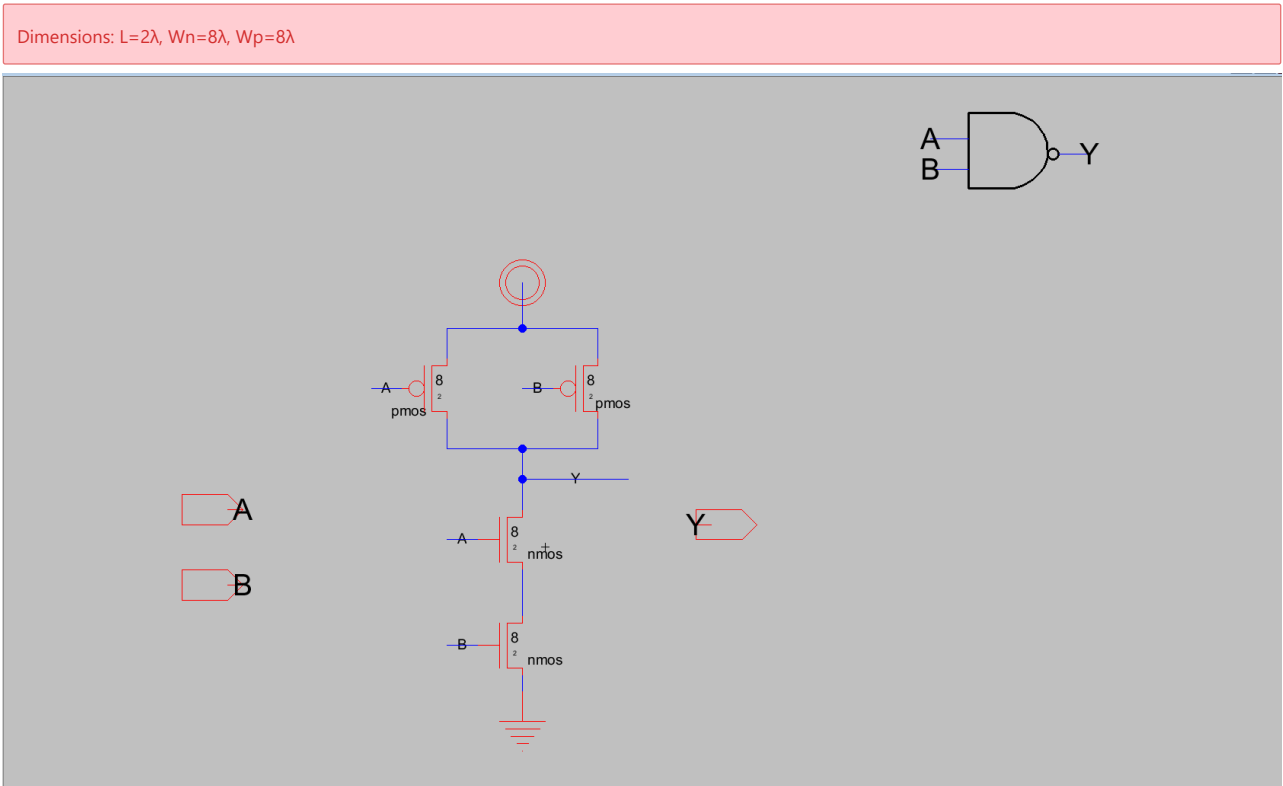
```
=====5=====
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 7 networks
Checking cell 'inv_4x_inv[lay]'
    No errors/warnings found
0 errors and 0 warnings found (took 0.035 secs)
=====6=====
Hierarchical NCC every cell in the design: cell 'inv[sch]' cell 'inv_4x_inv[lay]'
Comparing: inv_4x:inv[sch] with: inv_4x:inv_4x_inv[lay]
    exports match, topologies match, sizes match in 0.016 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.032 seconds.
```



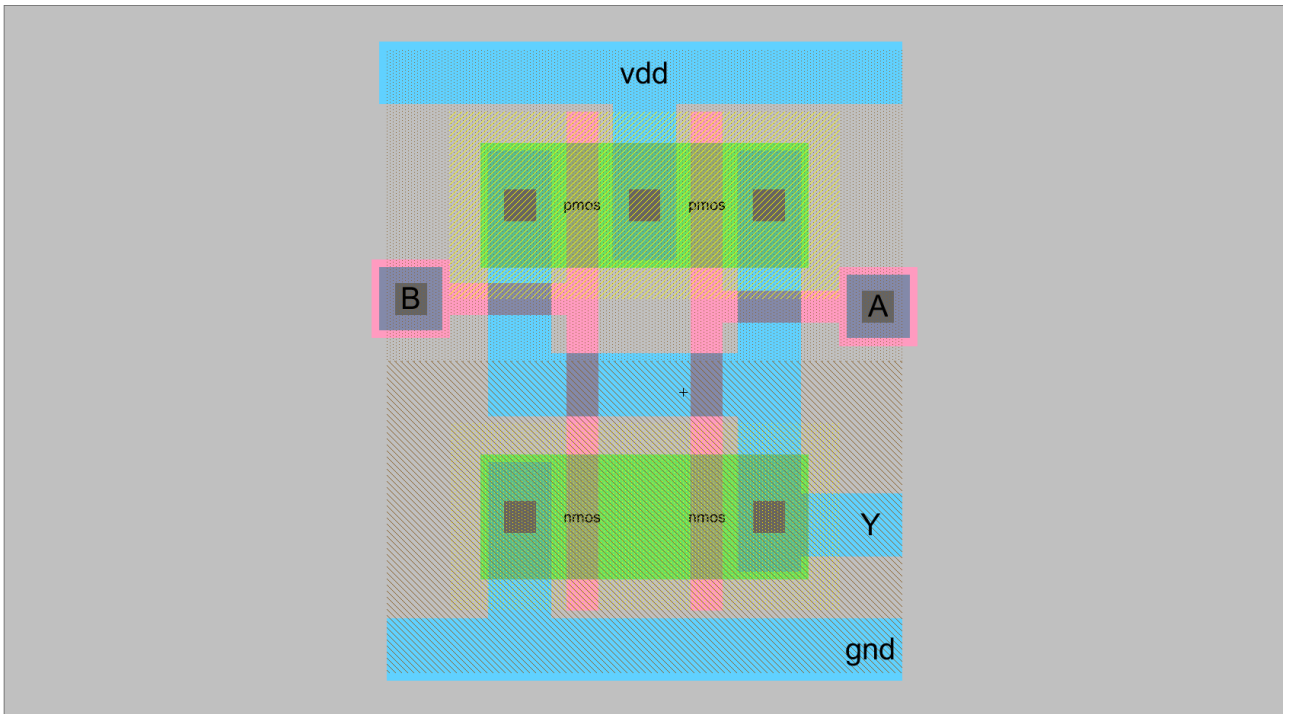
Testbench

Part B - NAND2

NAND2 1x



Schematic



Layout

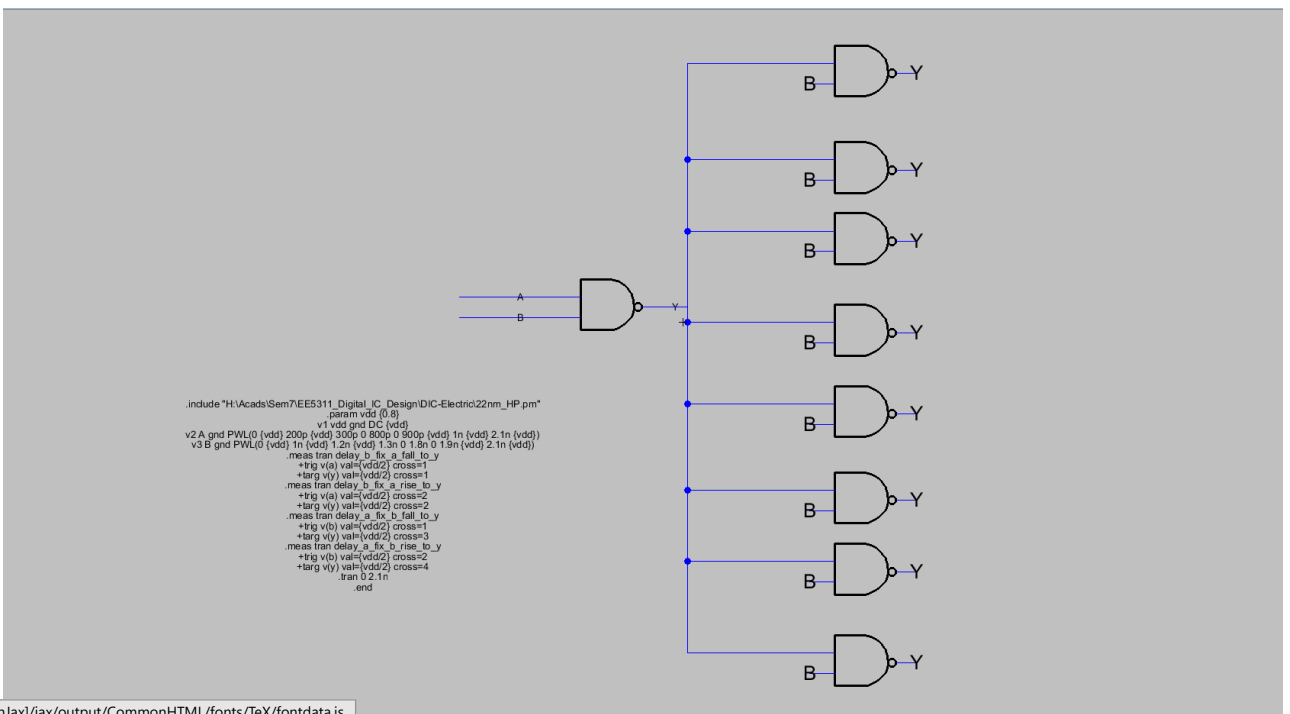
```

=====24=====
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 11 networks
0 errors and 0 warnings found (took 0.002 secs)

=====13=====
Hierarchical NCC every cell in the design: cell 'nand2{sch}' cell 'nand2-lx_nand2{lay}'
Comparing: nand2-lx:nand2{sch} with: nand2-lx:nand2-lx_nand2{lay}
  exports match, topologies match, sizes not checked in 0.028 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.037 seconds.
=====14=====

```

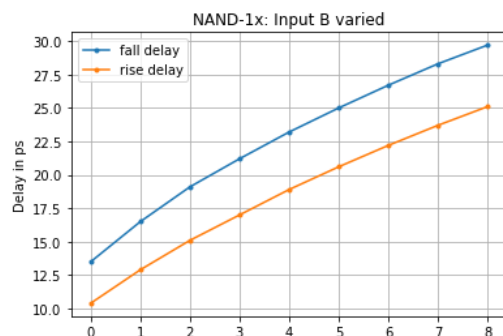
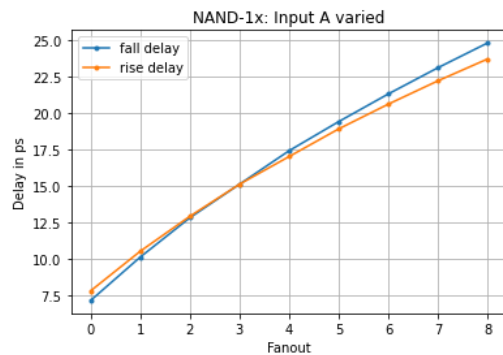
DRC LVS Clean Screenshot



## Testbench

Delay - NAND2 1x					
Fanout Count	Delay Name	Delay Type	Fixed Input(High)	Transitioning Input	Delay Value
0	delay_b_fixed_a_fall	Rise	B	A (1->0)	7.78E-12
	delay_b_fixed_a_rise	Fall	B	A(0->1)	7.12E-12
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.04E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.35E-11
1	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.05E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	1.01E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.29E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.65E-11
2	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.29E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	1.28E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.51E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.91E-11
3	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.51E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	1.51E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.70E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.12E-11
4	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.70E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	1.74E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.89E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.32E-11
5	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.89E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	1.94E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.06E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.50E-11
6	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.06E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.13E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.22E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.67E-11
7	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.22E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.31E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.37E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.83E-11
8	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.37E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.48E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.51E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.97E-11

## Delay Values

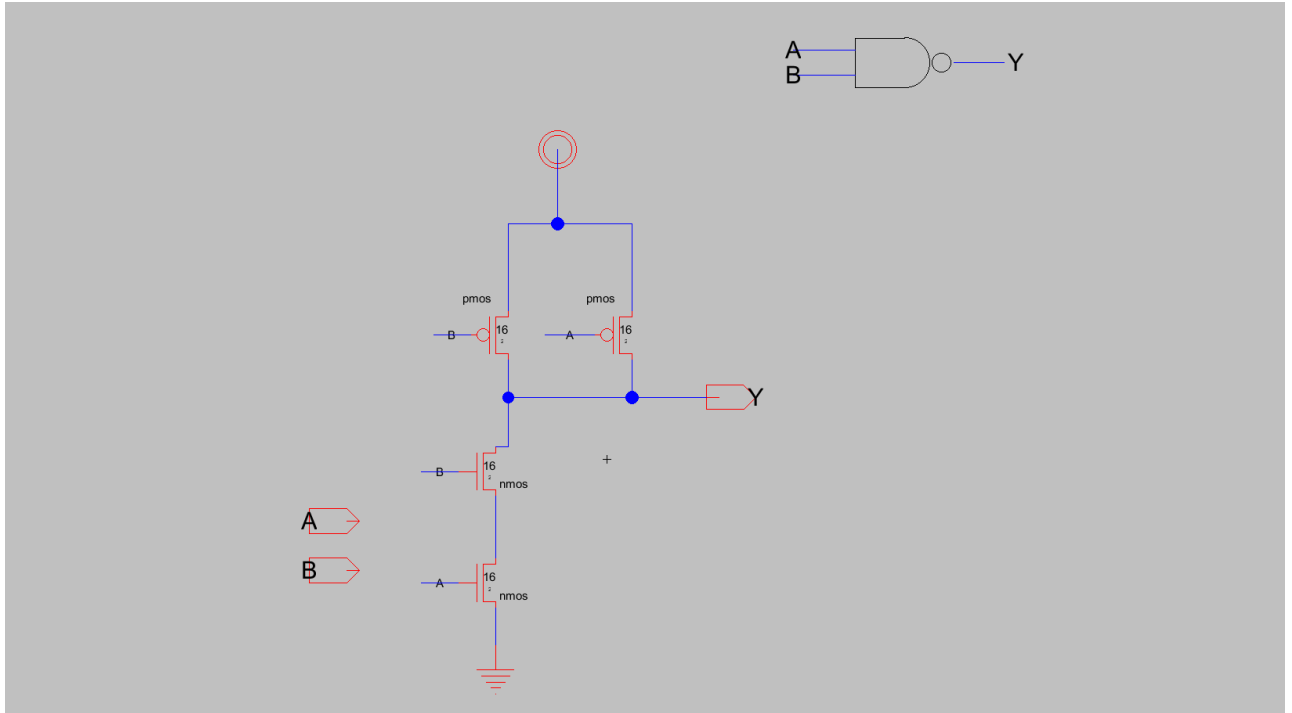




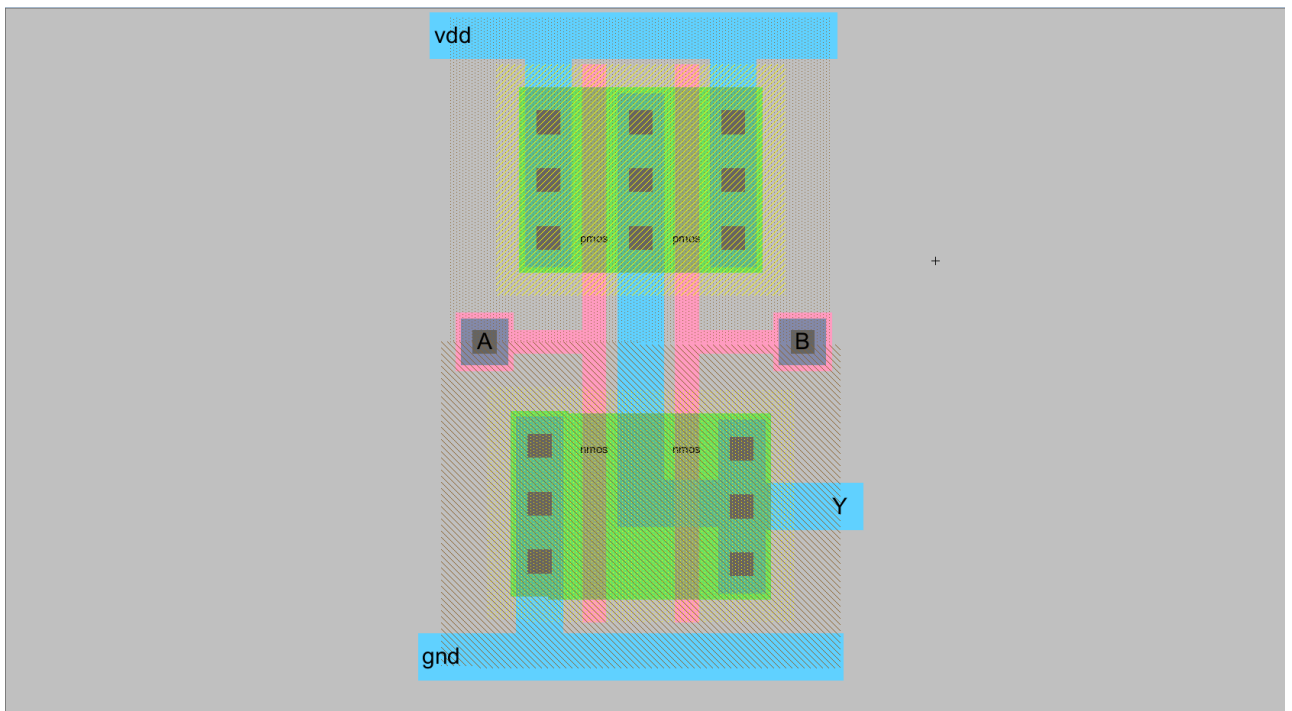
## Delay vs Fanout

### NAND2 2x

Dimensions:  $L=2\lambda$ ,  $W_n=16\lambda$ ,  $W_p=16\lambda$



### Schematic



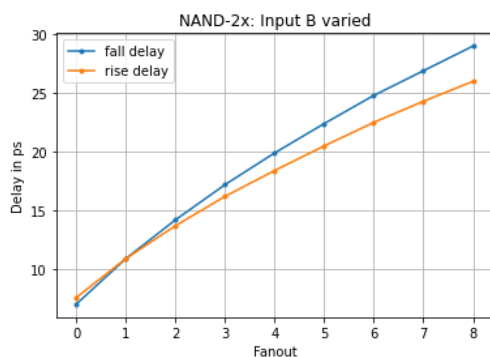
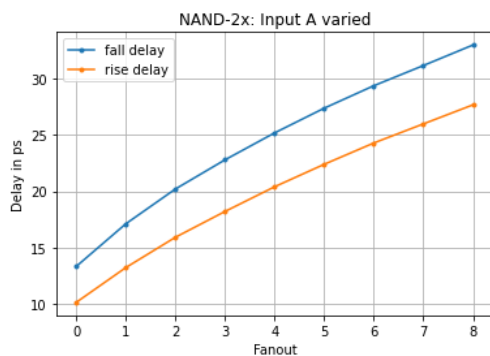
### Layout

## DRC LVS Clean Screenshot



Delay - NAND2 2x					
Fanout Count	Delay Name	Delay Type	Fixed Input(High)	Transitioning Input	Delay Value
0	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.01E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	1.33E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	7.58E-12
	delay_a_fixed_b_rise	Fall	A	B(0->1)	7.02E-12
1	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.32E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	1.71E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.09E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.09E-11
2	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.59E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.02E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.37E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.42E-11
3	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.82E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.28E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.62E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.72E-11
4	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.04E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.52E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.84E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.99E-11
5	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.24E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.74E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.05E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.24E-11
6	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.43E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.94E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.25E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.48E-11
7	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.60E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	3.12E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.43E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.69E-11
8	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.77E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	3.30E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.60E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.90E-11

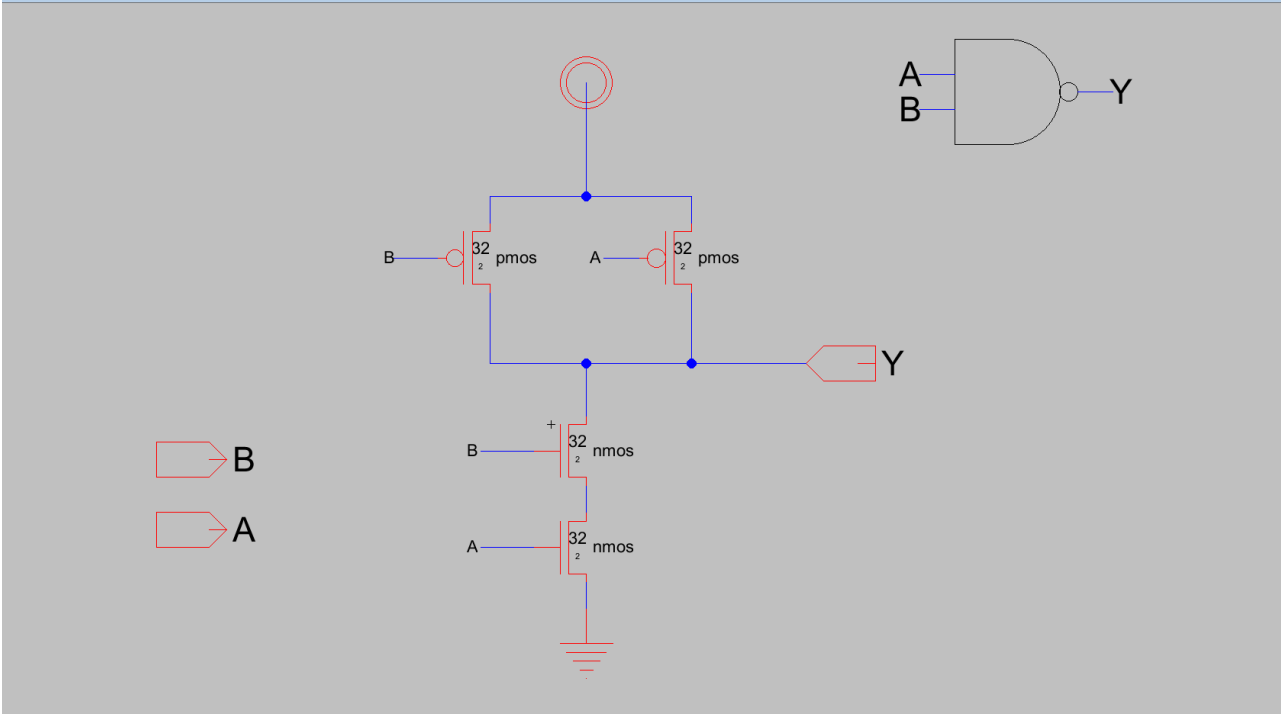
## Delay Values



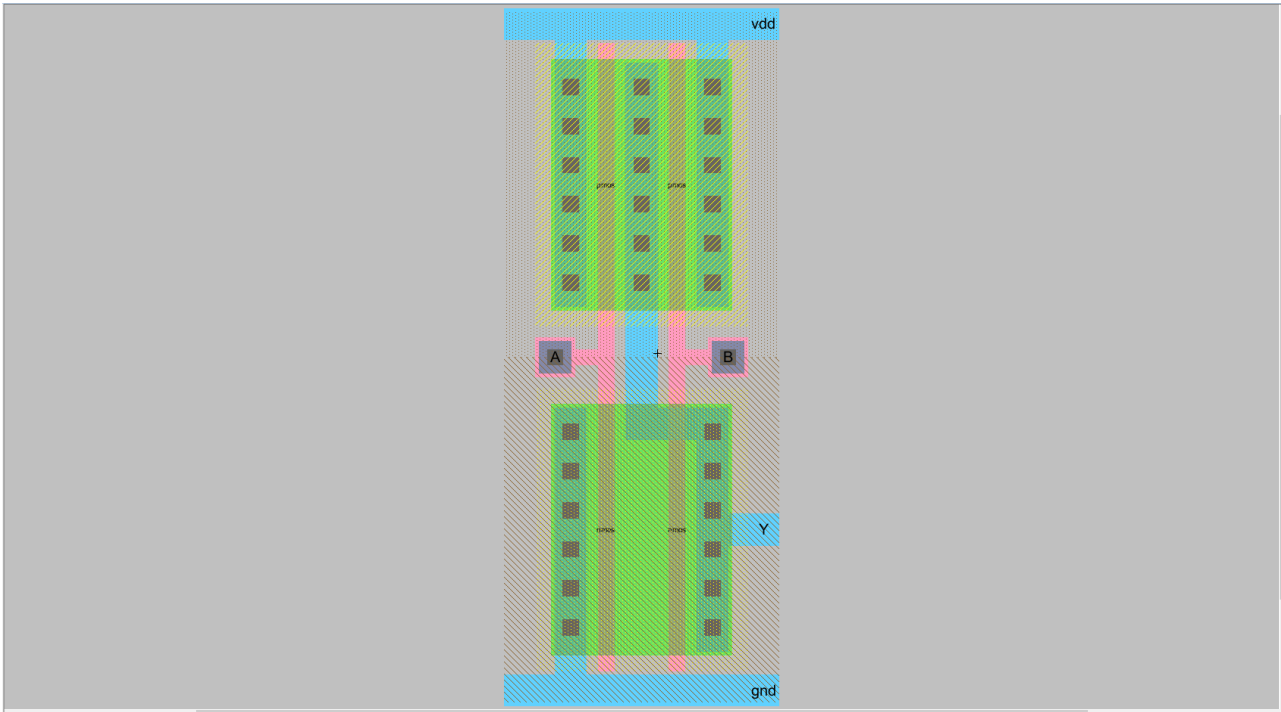
## Delay vs Fanout

NAND2 4x

Dimensions:  $L=2\lambda$ ,  $W_n=32\lambda$ ,  $W_p=32\lambda$



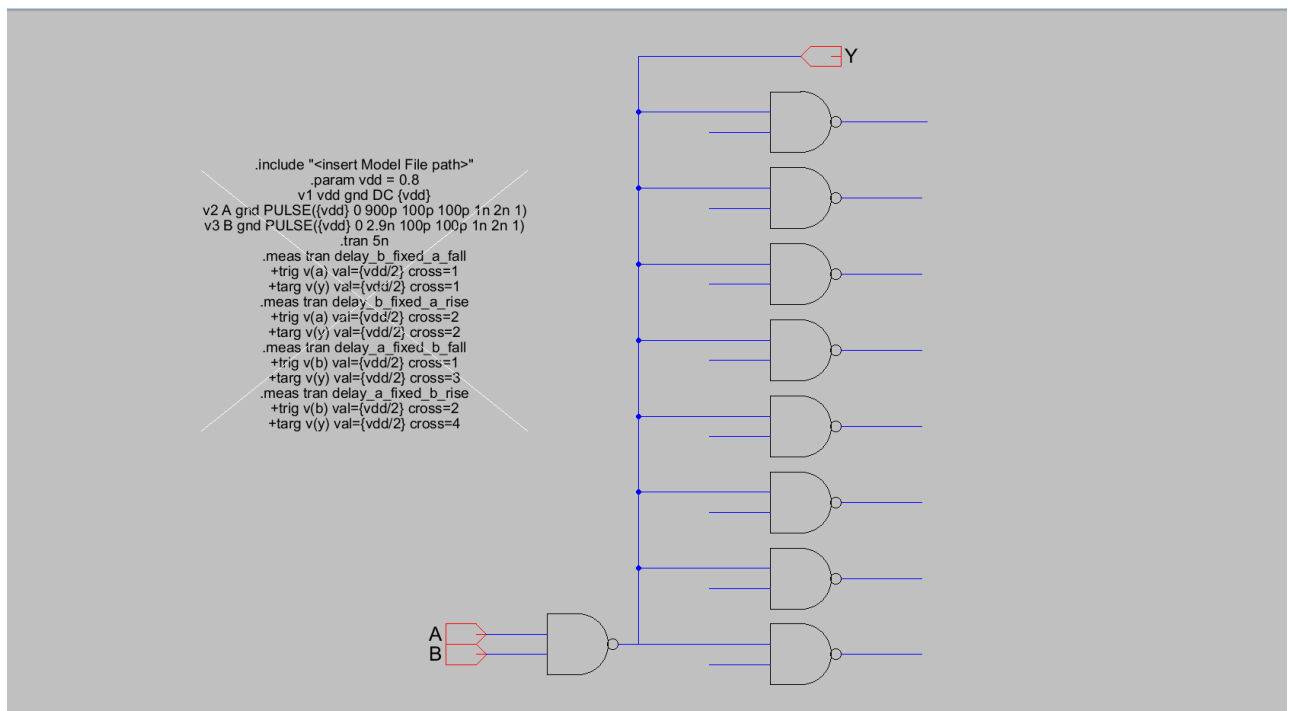
Schematic



Layout

```
Electric Messages
Electric's log file is C:\WINDOWS\system32\electric.log.
=====
Library /C:/Users/welcome/Documents/Academics/7th\20Sem/EE5311\20-220Digital\20IC\20Design/Assignments/Assignment1/Size-4x/nand2_4x.jelib read, took 0.024 secs
Checking library 'nand2_4x' for repair... library checked
No errors found
=====2=====
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.002 secs)
Found 11 networks
0 errors and 0 warnings found (took 0.017 secs)
=====3=====
Hierarchical NCC every cell in the design: cell 'nand2{sch}' cell 'nand2_4x_nand2{lay}'
Comparing: nand2_4x:nand2{sch} with: nand2_4x:nand2_4x_nand2{lay}
exports match, topologies match, sizes match in 0.025 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.032 seconds.
=====4=====
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 11 networks
0 errors and 0 warnings found (took 0.002 secs)
=====5=====
Hierarchical NCC every cell in the design: cell 'nand2{sch}' cell 'nand2_4x_nand2{lay}'
Comparing: nand2_4x:nand2{sch} with: nand2_4x:nand2_4x_nand2{lay}
exports match, topologies match, sizes match in 0.003 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.003 seconds.
```

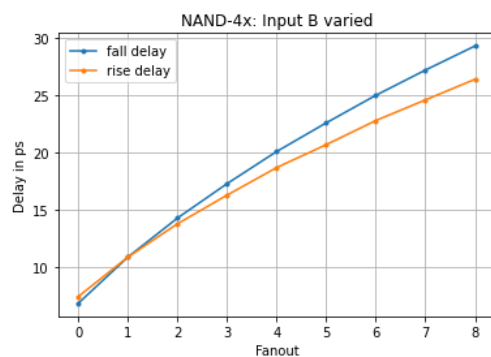
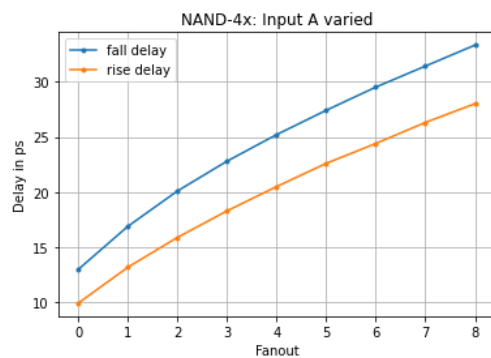
## DRC LVS Clean Screenshot



## Testbench

Delay - NAND2 4x					
Fanout Count	Delay Name	Delay Type	Fixed Input(High)	Transitioning Input	Delay Value
0	delay_b_fixed_a_fall	Rise	B	A (1->0)	9.95E-12
	delay_b_fixed_a_rise	Fall	B	A(0->1)	1.30E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	7.46E-12
	delay_a_fixed_b_rise	Fall	A	B(0->1)	6.87E-12
1	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.32E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	1.69E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.09E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.09E-11
2	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.59E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.01E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.38E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.43E-11
3	delay_b_fixed_a_fall	Rise	B	A (1->0)	1.83E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.28E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.63E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	1.73E-11
4	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.05E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.52E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	1.87E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.01E-11
5	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.26E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.74E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.07E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.26E-11
6	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.44E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	2.95E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.28E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.50E-11
7	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.63E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	3.14E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.46E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.72E-11
8	delay_b_fixed_a_fall	Rise	B	A (1->0)	2.80E-11
	delay_b_fixed_a_rise	Fall	B	A(0->1)	3.33E-11
	delay_a_fixed_b_fall	Rise	A	B(1->0)	2.64E-11
	delay_a_fixed_b_rise	Fall	A	B(0->1)	2.93E-11

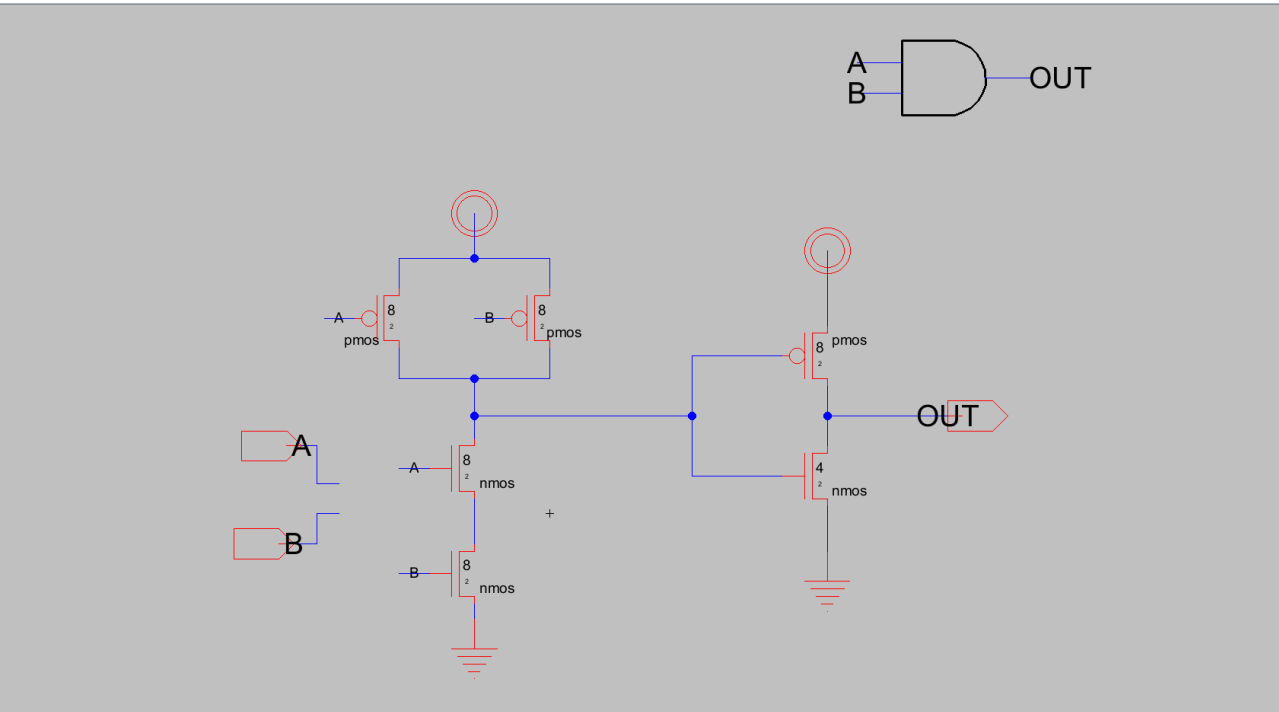
## Delay Values



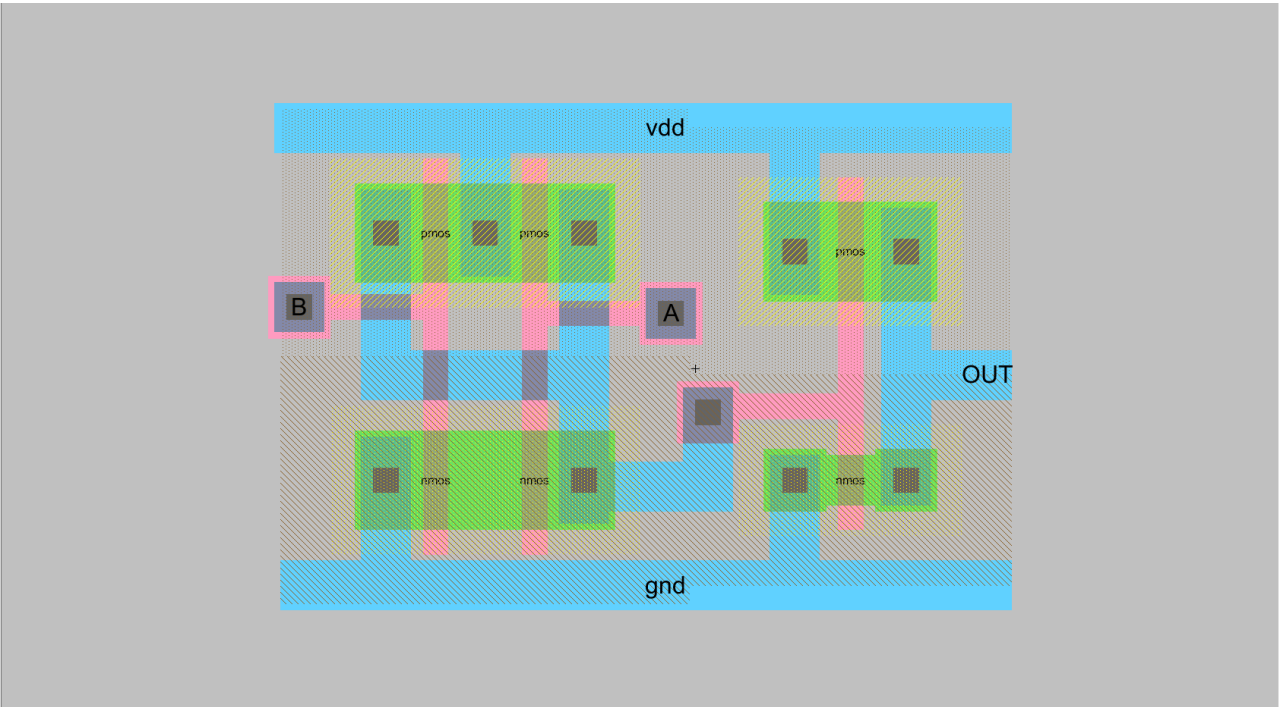
## Delay vs Fanout

Part C - AND2

AND2 1x



Schematic



Layout

```
=====21=====
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 14 networks
0 errors and 0 warnings found (took 0.002 secs)
```

```

=====1=====
Hierarchical NCC every cell in the design: cell 'and2-lx:and2{sch}' cell 'and2-lx:and2-lx_and2{lay}'
Comparing: and2-lx:and2{sch} with: and2-lx:and2-lx_and2{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.002 seconds.
=====1R=====

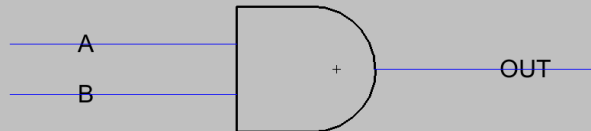
```

## DRC LVS Clean Screenshot

```

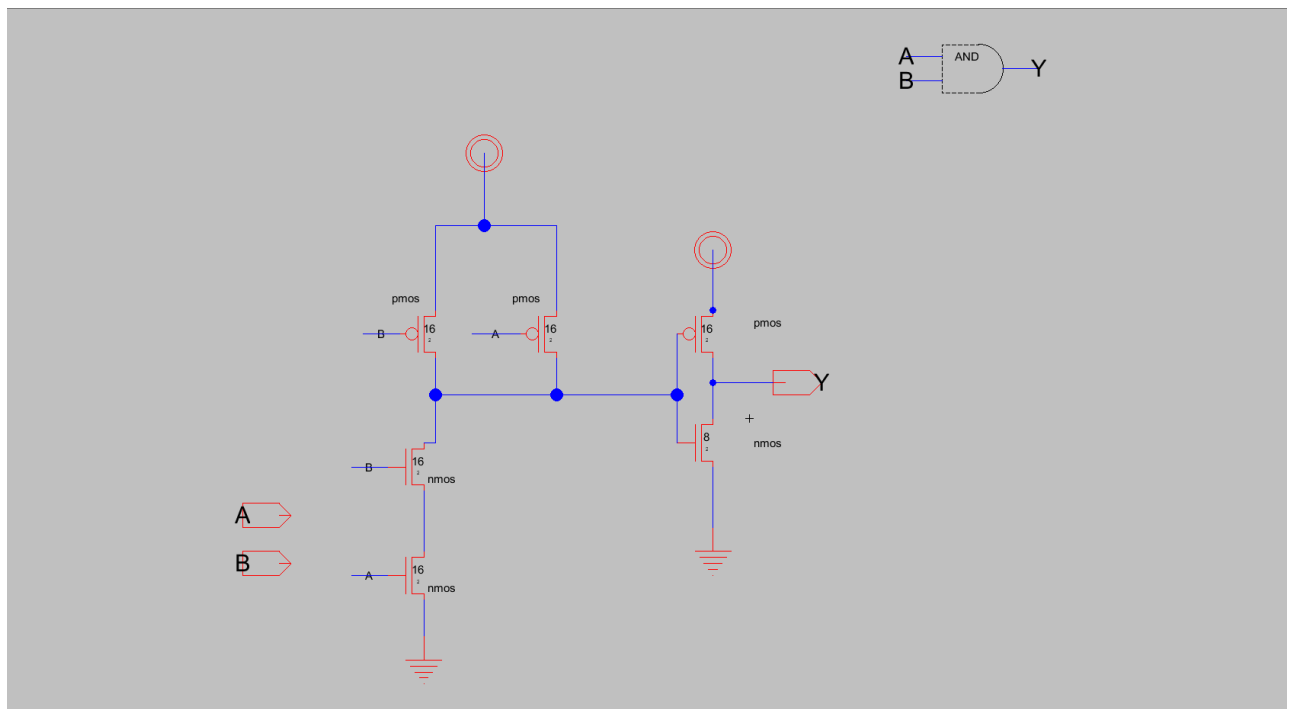
.include "H:\Acads\Sem7\EE5311_Digital_IC_Design\DIC-Electric\22nm_HP.pm"
.param vdd {0.8}
v1 vdd gnd DC {vdd}
v2 A gnd PWL(0 0 400p 0 500p {vdd} 900p {vdd} 1n 0 1.4n 0 1.5n {vdd} 1.9n {vdd} 2n 0)
v3 B gnd PWL(0 0 900p 0 1n {vdd} 1.9n {vdd} 2n 0)
.meas tran delay_a_to_out
+trig v(a) val={vdd/2} cross=3
+targ v(out) val={vdd/2} cross=1
.tran 0 2n

```



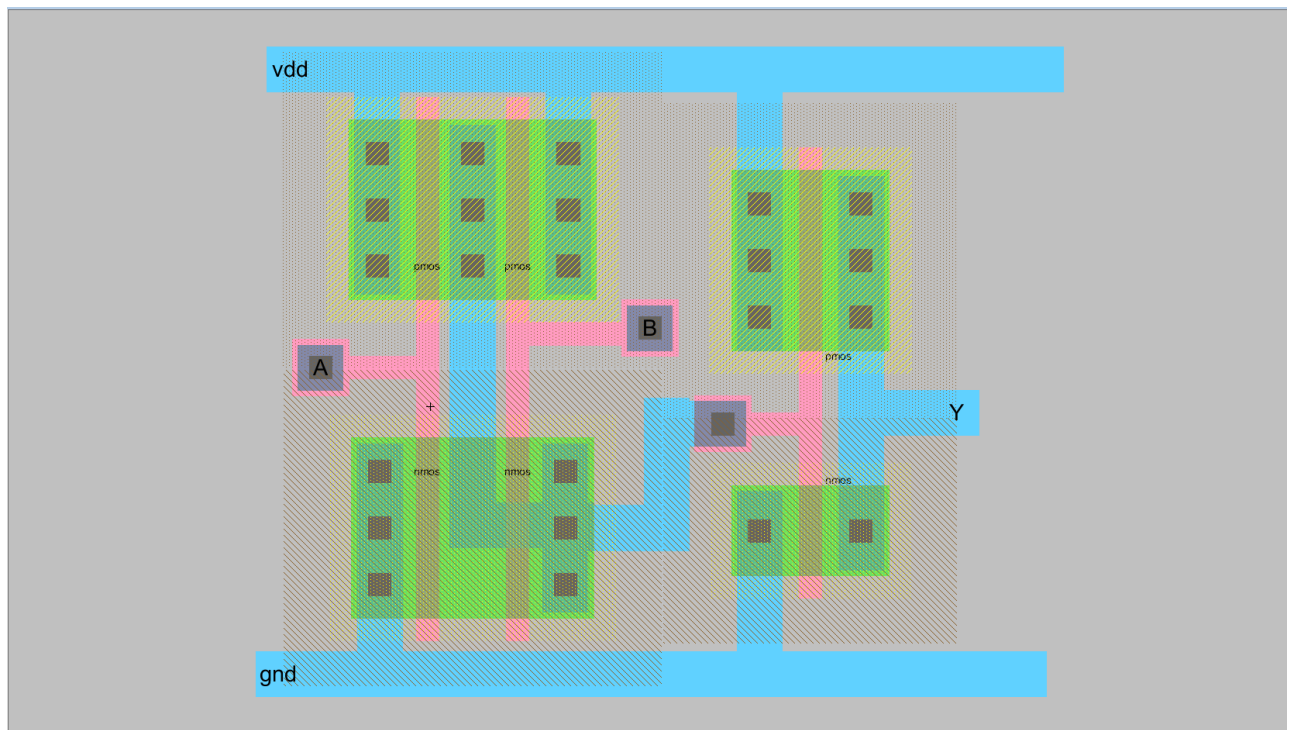
## Testbench

## AND2 2x



## Schematic





Layout

```

=====30=====
Hierarchical NCC every cell in the design: cell 'and{sch}' cell 'and_and{lay}'
Comparing: and2_2x:and{sch} with: and2_2x:and_and{lay}
  exports match, topologies match, sizes not checked in 0.003 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.003 seconds.
=====31=====
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 14 networks
0 errors and 0 warnings found (took 0.002 secs)

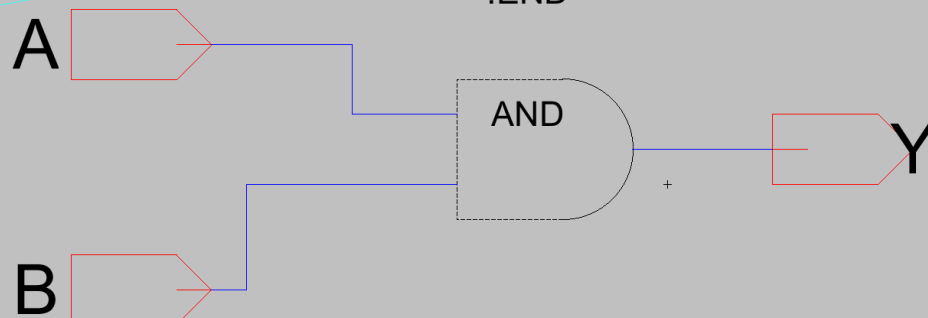
```

DRC LVS Clean Screenshot

```

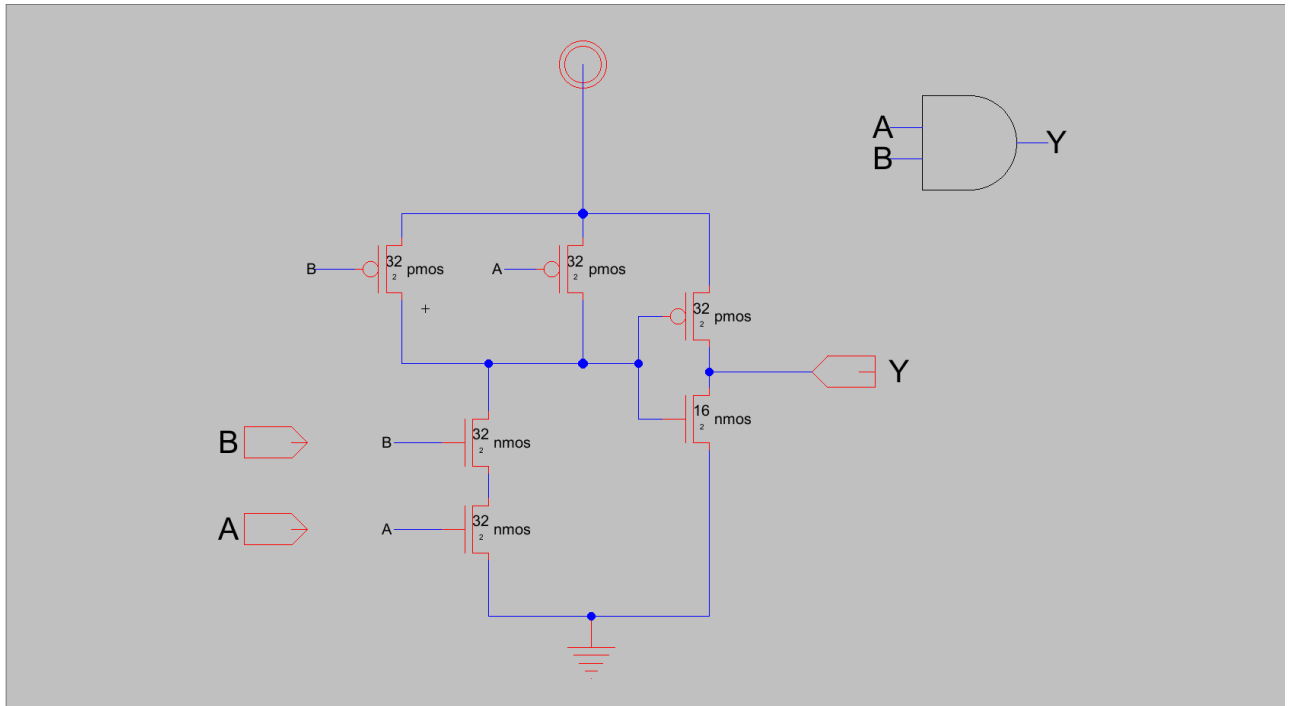
.include "C:\Users\Hemanth Ram\Desktop\sem7\ee5311\22nm_HP.pm"
v1 vdd gnd DC 0.8
v2 A gnd pulse(0 0.8 100p 100p 100p 400p 1n)
v3 B gnd pulse(0 0.8 100p 100p 100p 900p)
.trans 2.1n
.END

```

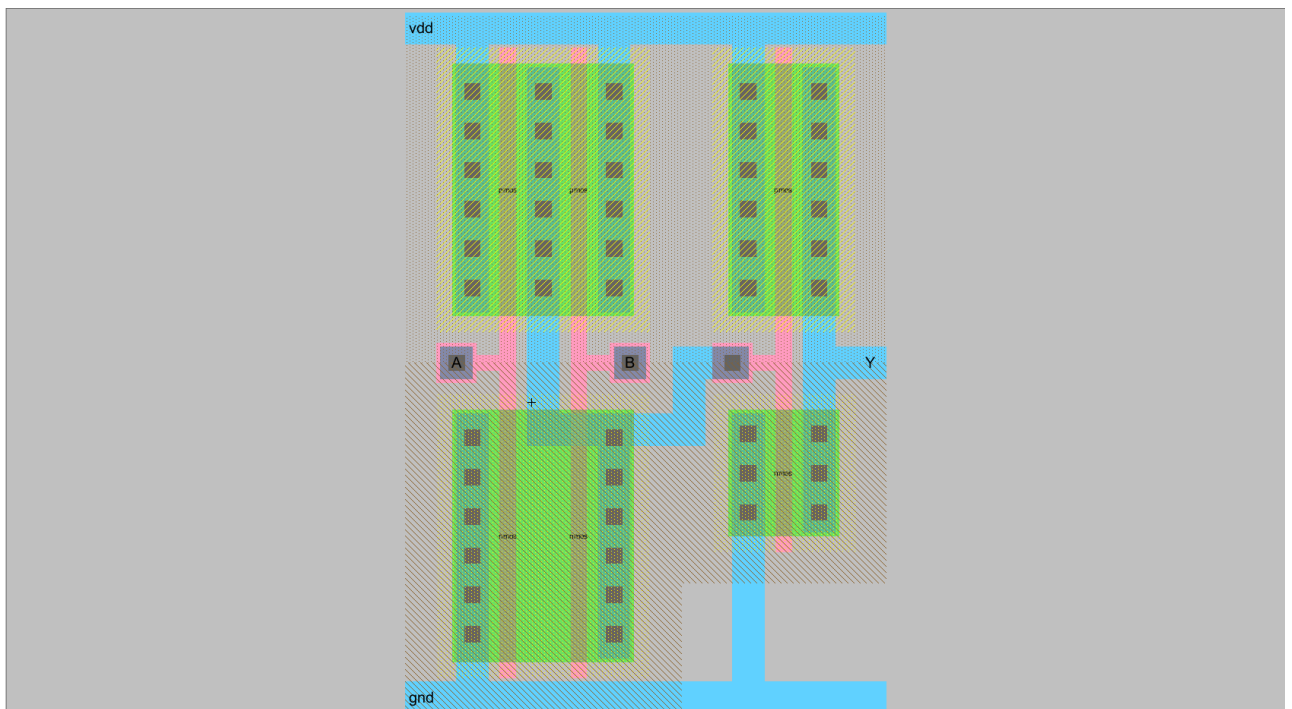


## Testbench

### AND2 4x



## Schematic



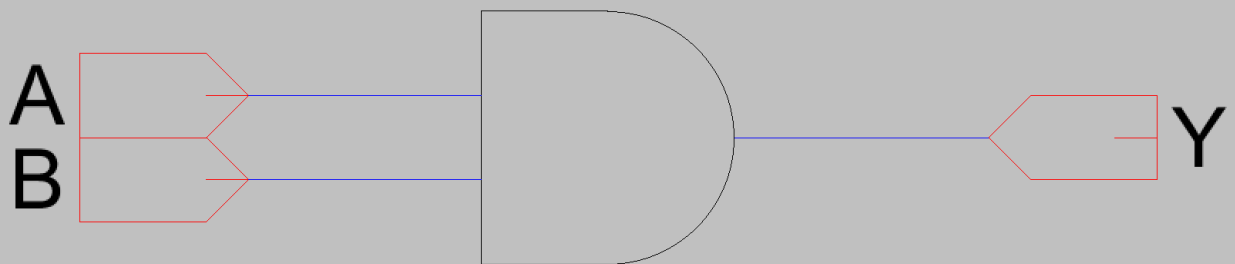
## Layout

```

Electric Messages
Electric's log file is C:\WINDOWS\system32\electric.log.
=====1=====
Library /C:/Users/welcome/Documents/Academics/7th%20Sem/EE5311%20-%20Digital%20IC%20Design/Assignments/Assignment1/Size-4x/and2_4x.jelib read, took 0.023 secs
Checking library 'and2_4x' for repair... library checked
No errors found
=====2=====
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.003 secs)
Found 14 networks
Checking cell 'and2[lay]'
No errors/warnings found
0 errors and 0 warnings found (took 0.112 secs)
=====3=====
Hierarchical NCC every cell in the design: cell 'and2[sch]' cell 'and2[lay]'
Comparing: and2_4x:and2(sch) with: and2_4x:and2[lay]
exports match, topologies match, sizes match in 0.028 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.035 seconds.

```

### DRC LVS Clean Screenshot



```

.include "<insert model file path>"
.param vdd = 0.8
v1 vdd gnd DC {vdd}
v2 A gnd PULSE(0 {vdd} 900p 100p 100p 1n 2n 2)
v3 B gnd PULSE(0 {vdd} 1.4n 100p 100p 2n 4n 1)
.tran 5n

```

### Testbench