Table 13-2: Parallel 8080 Timing Characteristics

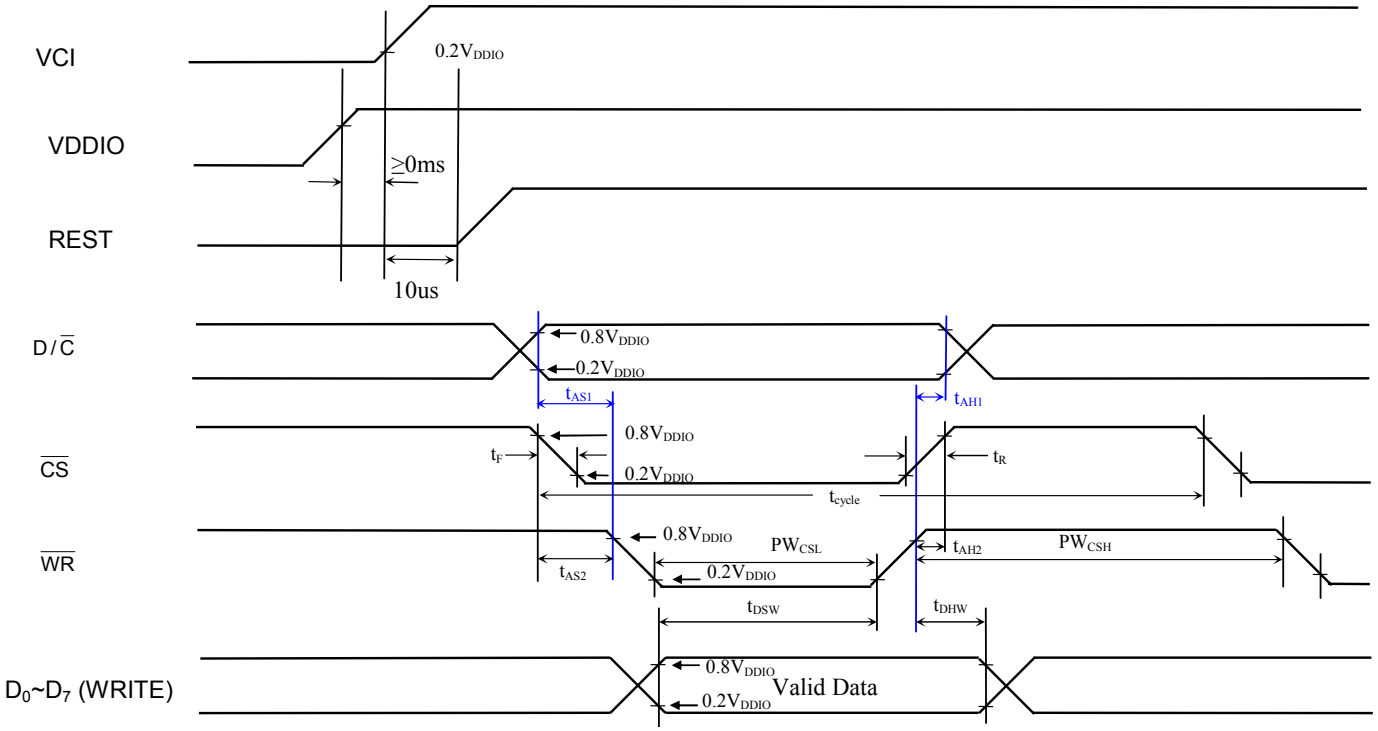
(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	75	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle) (Based on VOL/VOH = 0.3*VDDIO/0.7*VDDIO)	450	-	-	ns
t_{AS1}	Address Setup Time between ($R/\overline{W}$) and $D/\overline{C}$	0	-	-	ns
t_{AH1}	Address Hold Time between ($R/\overline{W}$) and $D/\overline{C}$	0	-	-	ns
t_{AS2}	Address Setup Time between ($R/\overline{W}$) and $\overline{CS}$	0	-	-	ns
t_{AH2}	Address Hold Time between ($R/\overline{W}$) and $\overline{CS}$	0	-	-	ns
t_{DSW}	Data Setup Time (D0~D7, WRITE)	5	-	-	ns
t_{DHW}	Data Hold Time (D0~D7, WRITE))	5	-	-	ns
t_{ACC}	Data Access Time (D0~D7, READ)	250	-	-	ns
t_{OH}	Output Hold time (D0~D7, READ)	100	-	-	ns
PW_{CSL}	Pulse width /CS low (write cycle)	40	-	-	ns
PW_{CSH}	Pulse width /CS high (write cycle)	25	-	-	ns
PW_{CSL}	Pulse width /CS low (read cycle)	500	-	-	ns
PW_{CSH}	Pulse width /CS high (read cycle)	500	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

Note: CS can be pulled low during the write cycle, only /RW is needed to be toggled

Figure 13-2: Parallel 8080-series Interface Timing Characteristics

Write Cycle



Remark: It's highly recommended that $\overline{RD}$ remains high for the whole write cycle

Read Cycle