Implementation of 8-bit Full Adder Using Hierarchical Design Flow in Synopsys ICC2

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Table of Contents

1. Introduction

In modern digital systems, arithmetic operations are fundamental building blocks, and adders are among the most critical components in arithmetic logic units (ALUs). The efficient design and implementation of adders directly influence the performance, power, and area (PPA) of larger digital systems. In this project, a hierarchical 8-bit full adder is designed using two instances of a 4-bit full adder block. This modular approach enables better scalability, reuse, and management of design complexity.

The implementation flow follows an industry-standard methodology using Synopsys tools. RTL design and synthesis are carried out using **Synopsys Design Compiler**, and the physical design process, from floorplanning to routing, is implemented in **Synopsys ICC2**. This project emphasizes understanding hierarchical digital design and applying the complete RTL-to-GDSII flow for a functional and optimized layout.

2. OBJECTIVE

- To design a hierarchical 8-bit full adder using two 4-bit full adder modules in Verilog.
- To synthesize the design using Synopsys Design Compiler, ensuring functional correctness and optimal gate-level netlist generation.
- To implement the physical design using Synopsys ICC2, covering steps such as floorplanning, power planning, placement, CTS, and routing.
- To explore hierarchical design techniques for better design reuse and integration in digital systems.
- To gain practical hands-on experience in the RTL-to-Physical Design Flow, following industry practices and tool usage.

3. Design Description

3.1 4-bit Full Adder Block

3.1.1. RTL Design Overview

RTL Code Analysis :

The 4-bit full adder module is designed in Verilog and forms the fundamental building block for constructing the 8-bit full adder through a hierarchical approach. This design performs the addition of two 4-bit binary numbers (A and B) along with a carry-in (C_in), and produces a 4-bit sum (SUM) and a carry-out (C_out).

The design utilizes three always blocks:

1. Input Sampling Block (Clocked):
   Captures the 4-bit inputs A, B, and the carry-in C_in on the rising edge of the clock. These are stored in internal registers (reg1, reg2, and c_in) for synchronous operation.

2. Output Assignment Block (Clocked):
   On the rising edge of the clock, the computed sum (sum_i) and carry-out (c_out) are assigned to the output ports SUM and C_out, respectively.

3. Combinational Logic Block:
   This block performs the actual arithmetic operation. It computes the sum and carry-out using the expression {c_out, sum_i} = reg1 + reg2 + c_in, which mimics the behavior of a standard ripple-carry adder.

The module is designed to operate synchronously with respect to the clock, ensuring predictable timing behavior. This structure is also synthesis-friendly and suitable for hierarchical integration into larger digital systems. The use of registers around the arithmetic logic also helps in pipelining and timing closure during synthesis and physical implementation.

Synthesis Of 4-BIT Full Adder Block

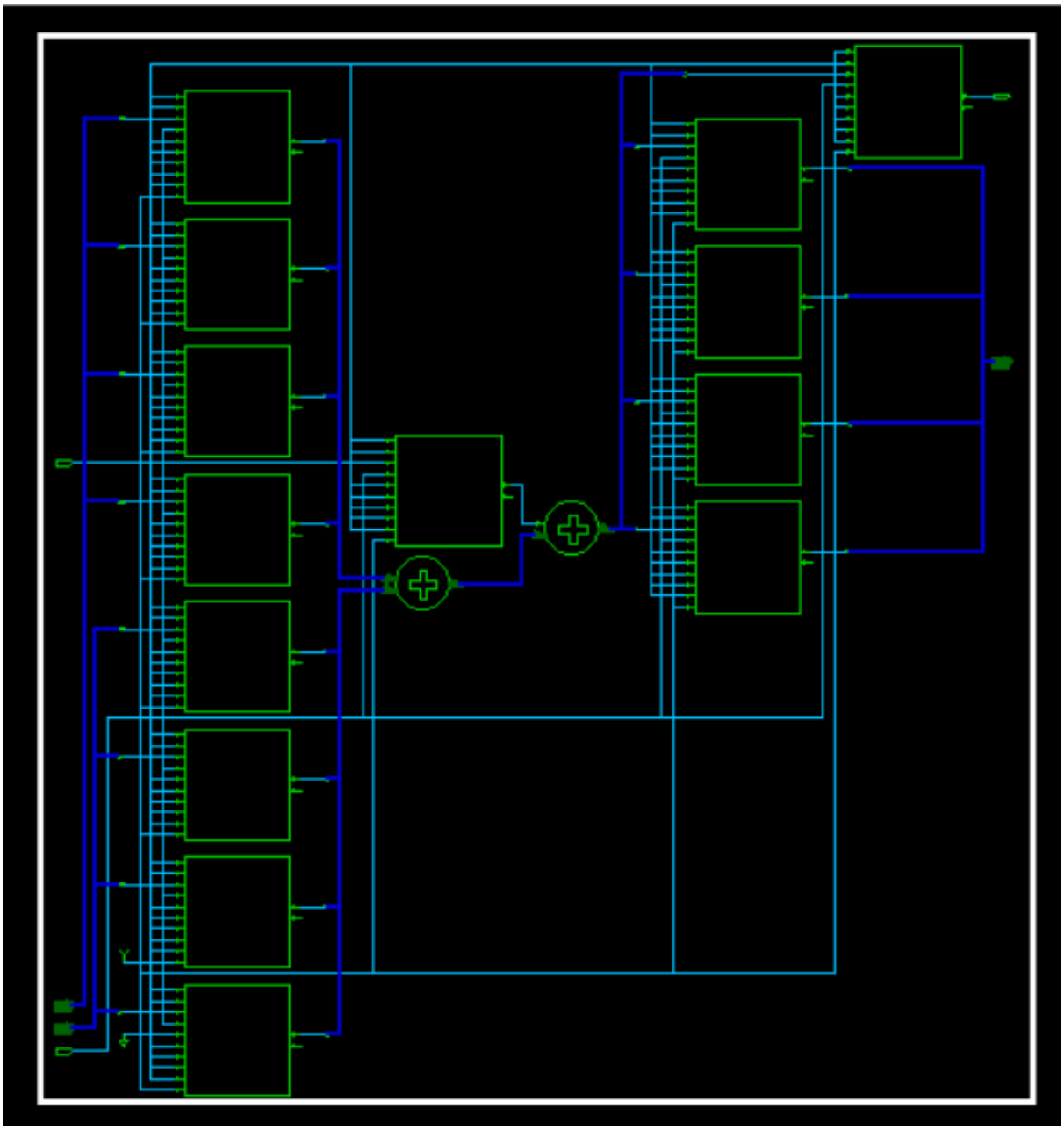
➢ Design Import

- To import the design in the design the design compiler there are some files the should be copied in our directory before proceeding to invade the dc_shell command.
- The files and directory that should be there in the directory where we are implementing synthesis of the design are : full_adder.v, rm_setup [directory] and the sdc file for full adder .
- After copying these files go to rm_setup → common_setup.tcl file and set the "DESIGN NAME " same as the name of the top module in the rtl code which is "full_adder" and set the PDK_PATH to the path where your library files are present.
- Now invoke the tool with dc_shell.

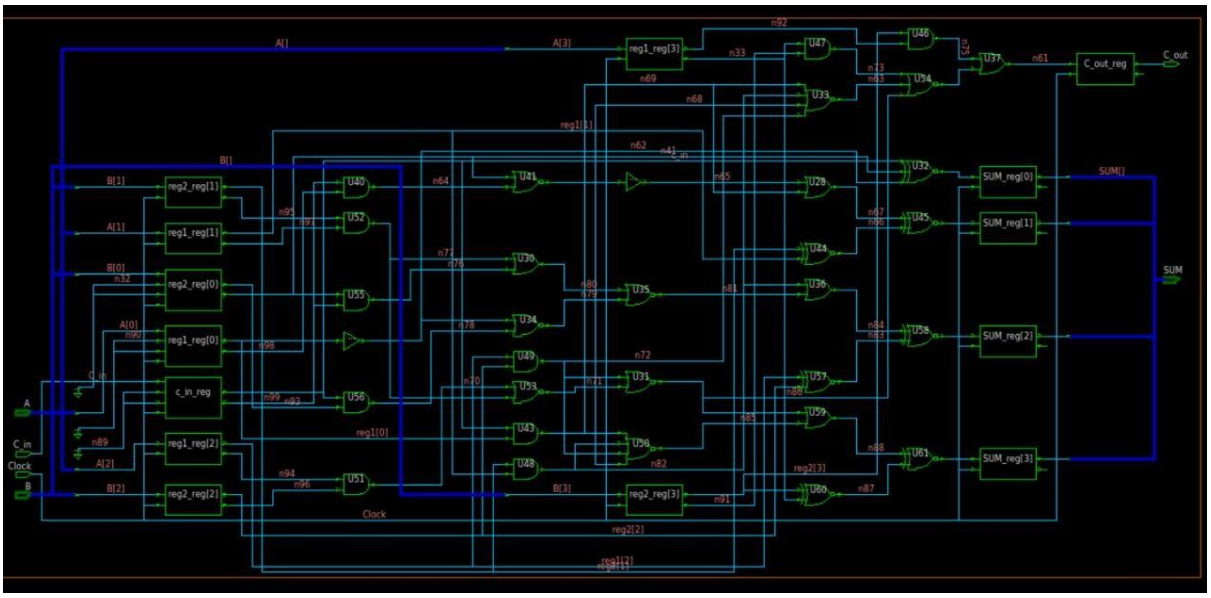
SCRIPT FOR Design Synthesis

```
set PDK_PATH /data/pdk/pdk32nm/SAED32_EDK

set RTL_SOURCE_FILES ./full_adder.v

source ./rm_setup/dc_setup.tcl

define_design_lib WORK -path ./WORK

set_app_var hdlin_enable_hier_map true

set_dont_use [get_lib_cells */FADD*]

set_dont_use [get_lib_cells */HADD*]

set_dont_use [get_lib_cells */MUX*]

set_dont_use [get_lib_cells */AO*]

set_dont_use [get_lib_cells */OA*]

set_dont_use [get_lib_cells */NAND*]

set_dont_use [get_lib_cells */XOR*]

analyze -format verilog $RTL_SOURCE_FILES
```

```
elaborate $DESIGN_NAME

current_design

set_verification_top

source ./full_adder.sdc

compile

compile_ultra

report_qor

report_timing > ./reports/timing.rpt

eport_timing

write -format verilog -hierarchy -output
 ${RESULTS_DIR}/${DCRM_FINAL_VERILOG_OUTPUT_FILE}

write_sdc    ./${RESULTS_DIR}/${DCRM_FINAL_SDC_OUTPUT_FILE}
```



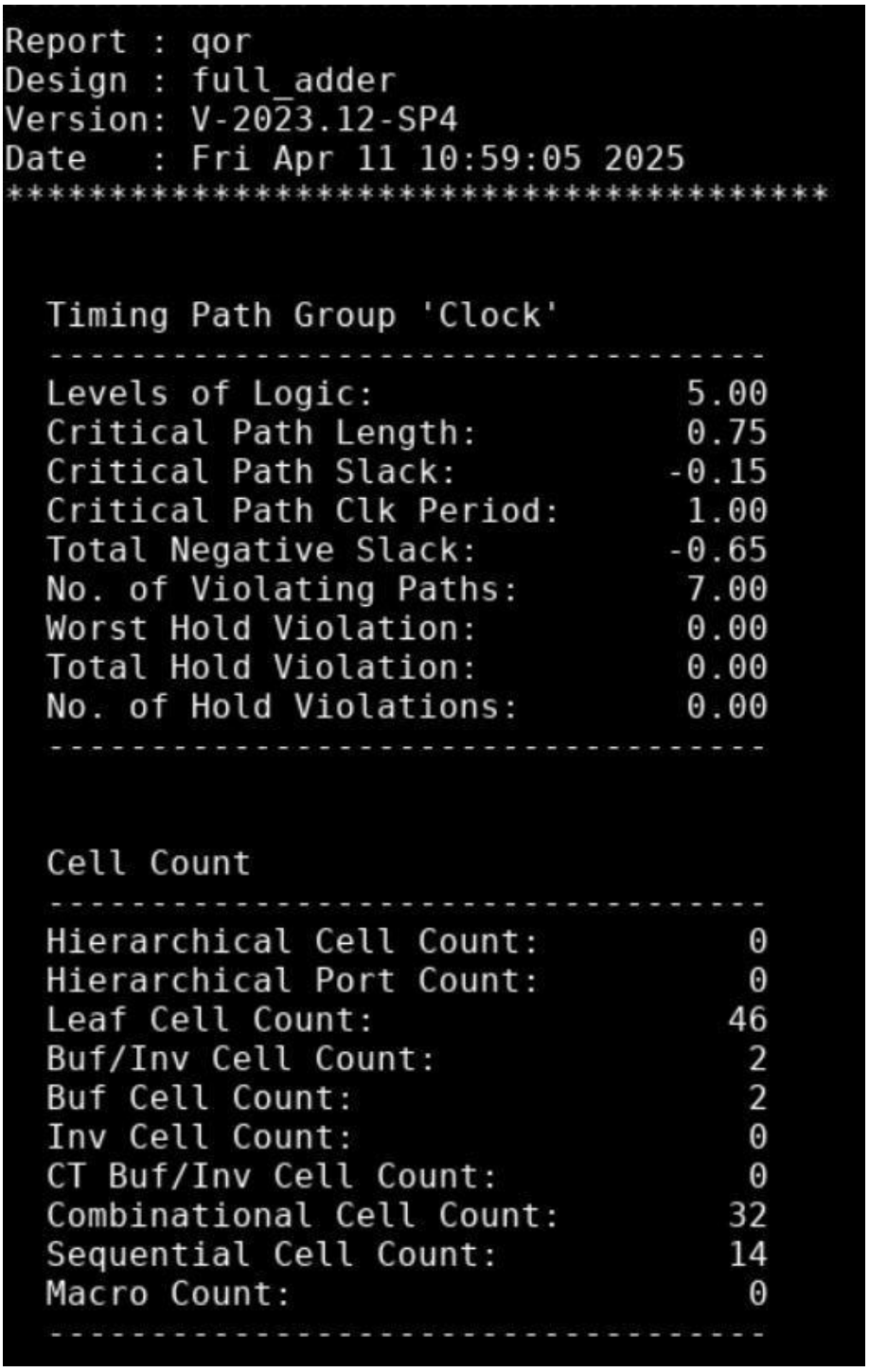
Gtech view of 8bit_full_adder



Mapped netlist of 8-bit full adder

```
Area
-----------------------------------
Combinational Area:         88.950401
Noncombinational Area:      98.607874
Buf/Inv Area:                4.066304
Total Buffer Area:               4.07
Total Inverter Area:             0.00
Macro/Black Box Area:        0.000000
Net Area:                   10.004960
-----------------------------------
Cell Area:                 187.558275
Design Area:               197.563236


Design Rules
-----------------------------------
Total Number of Nets:              68
Nets With Violations:               0
Max Trans Violations:               0
Max Cap Violations:                 0
-----------------------------------
```

report_qor


Report : qor
Design : full_adder
Version: V-2023.12-SP4
Date : Fri Apr 11 10:59:05 2025
Timing Path Group 'Clock'
Levels of Logic: 5.00
Critical Path Length: 0.75
Critical Path Slack: -0.15
Critical Path Clk Period: 1.00
Total Negative Slack: -0.65
No. of Violating Paths: 7.00
Worst Hold Violation: 0.00
Total Hold Violation: 0.00
No. of Hold Violations: 0.00
Cell Count
Hierarchical Cell Count: 0
Hierarchical Port Count: 0
Leaf Cell Count: 46
Buf/Inv Cell Count: 2
Buf Cell Count: 2
Inv Cell Count: 0
CT Buf/Inv Cell Count: 0
Combinational Cell Count: 32
Sequential Cell Count: 14
Macro Count: 0

report_qor

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : full_adder
Version: V-2023.12-SP4
Date   : Fri Apr 11 10:36:18 2025
****************************************

Operating Conditions: tt0p78vn40c   Library: saed32rvt_tt0p78vn40c
Wire Load Model Mode: enclosed

  Startpoint: c_in_reg (rising edge-triggered flip-flop clocked by Clock)
  Endpoint: SUM_reg[3] (rising edge-triggered flip-flop clocked by Clock)
  Path Group: Clock
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  full_adder         ForQA                 saed32rvt_tt0p78vn40c

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock Clock (rise edge)                  0.00       0.00
  clock network delay (ideal)              0.00       0.00
  c_in_reg/CLK (SDFFX1_RVT)                0.00       0.00 r
  c_in_reg/QN (SDFFX1_RVT)                 0.16       0.16 r
  U40/Y (AND2X1_RVT)                       0.09       0.25 r
  U41/Y (NOR2X0_RVT)                       0.11       0.36 f
  U50/Y (NOR4X1_RVT)                       0.16       0.52 r
  U59/Y (OR2X2_RVT)                        0.08       0.60 r
  U61/Y (XNOR2X2_RVT)                      0.14       0.74 f
  SUM_reg[3]/D (DFFX1_RVT)                 0.01       0.75 f
  data arrival time                                   0.75

  clock Clock (rise edge)                  1.00       1.00
  clock network delay (ideal)              0.00       1.00
  clock uncertainty                       -0.30       0.70
  SUM_reg[3]/CLK (DFFX1_RVT)               0.00       0.70 r
  library setup time                      -0.10       0.60
  data required time                                  0.60
  -----------------------------------------------------------
  data required time                                  0.60
  data arrival time                                  -0.75
  -----------------------------------------------------------
  slack (VIOLATED)                                   -0.15
```

Setup_timing report

```
Startpoint: reg1_reg[3]
            (rising edge-triggered flip-flop clocked by Clock)
Endpoint: C_out_reg (rising edge-triggered flip-flop clocked by Clock)
Path Group: Clock
Path Type: min

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
full_adder         ForQA                 saed32rvt_tt0p78vn40c

Point                                    Incr       Path
-----------------------------------------------------------
clock Clock (rise edge)                  0.00       0.00
clock network delay (ideal)              0.00       0.00
reg1_reg[3]/CLK (DFFX1_RVT)              0.00       0.00 r
reg1_reg[3]/Q (DFFX1_RVT)                0.18       0.18 r
U46/Y (AND2X1_RVT)                       0.08       0.26 r
U37/Y (OR2X1_RVT)                        0.08       0.34 r
C_out_reg/D (DFFX1_RVT)                  0.01       0.35 r
data arrival time                                   0.35

clock Clock (rise edge)                  0.00       0.00
clock network delay (ideal)              0.00       0.00
clock uncertainty                        0.10       0.10
C_out_reg/CLK (DFFX1_RVT)                0.00       0.10 r
library hold time                       -0.03       0.07
data required time                                  0.07
-----------------------------------------------------------
data required time                                  0.07
data arrival time                                  -0.35
-----------------------------------------------------------
slack (MET)                                         0.29
```

Hold_timing report

3.1.2 ICC2 Flow Of 4 Bit Full Adder

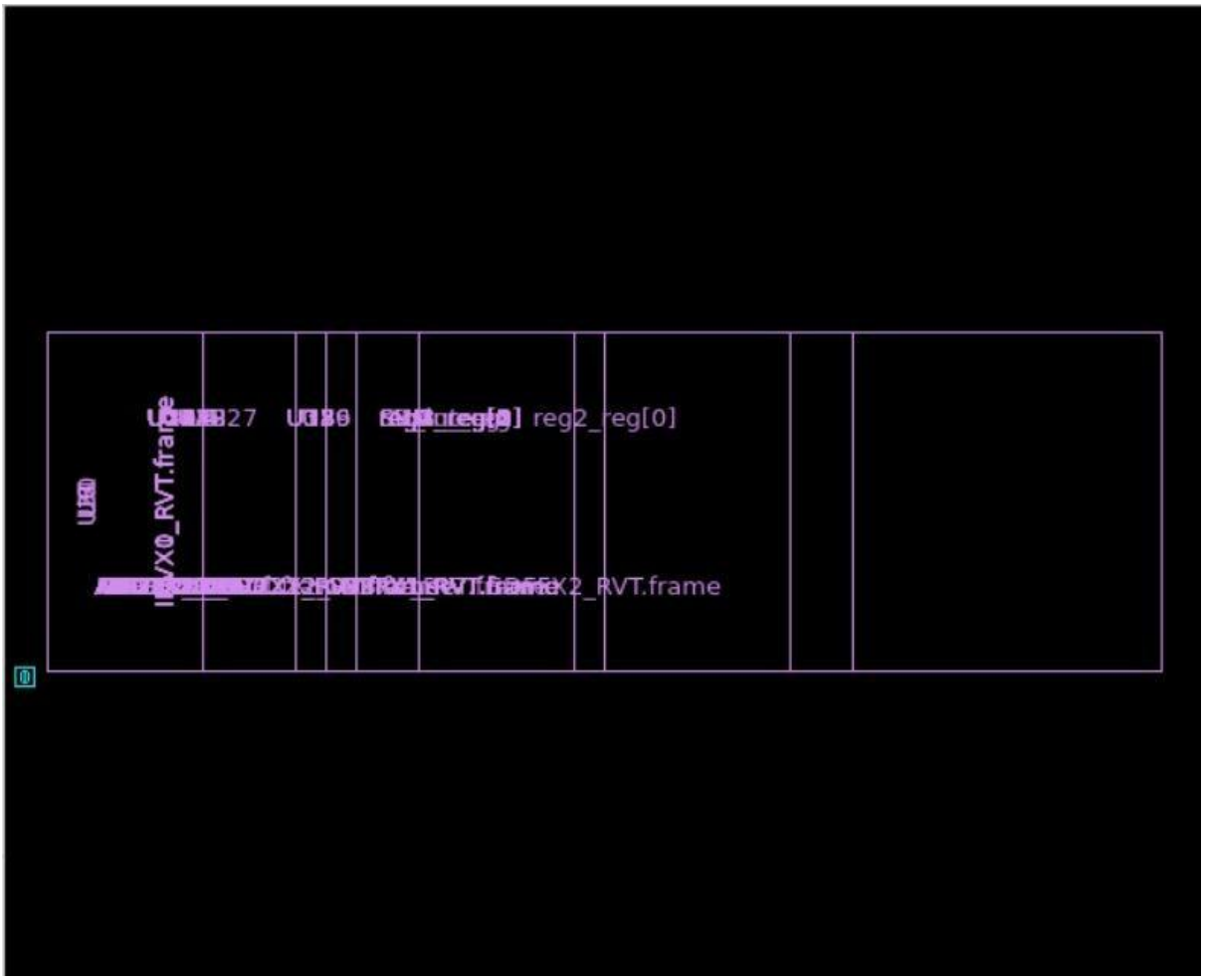
1. **Design import**

set PDK_PATH /data/pdk/pdk32nm/SAED32_EDK/

create_lib -ref_libs $PDK_PATH/lib/stdcell_rvt/ndm/saed32rvt_c.ndm FA_LIB

read_verilog {./../DC/results/full_adder.mapped.v} -library FA_LIB -design full_adder -top full_adder

Link_block

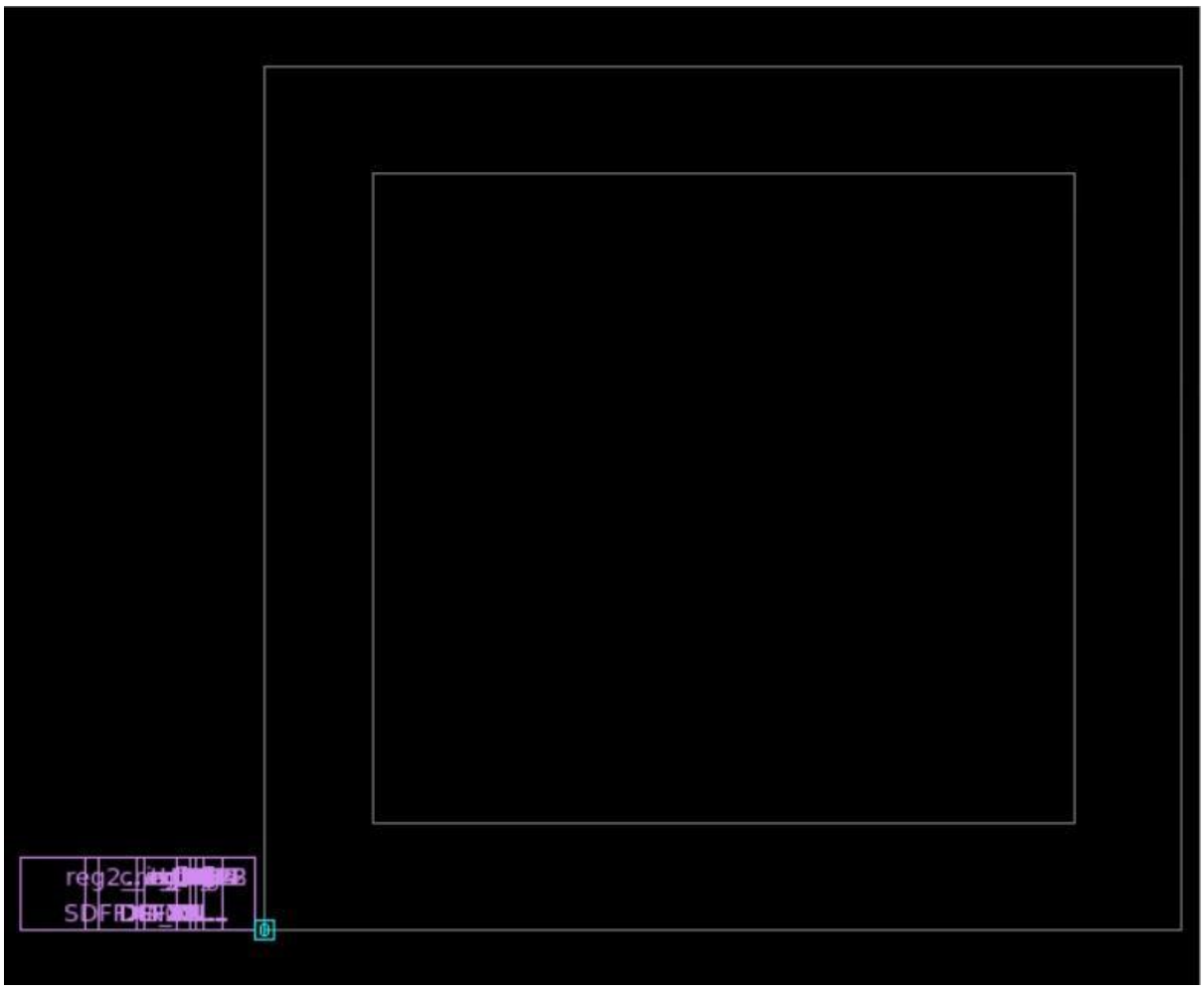


Standard Cells

2. Floorplanning

check_design -checks dp_pre_floorplan

initialize_floorplan -core_utilization 0.7 -core_offset 2.5



Floorplan Initialization

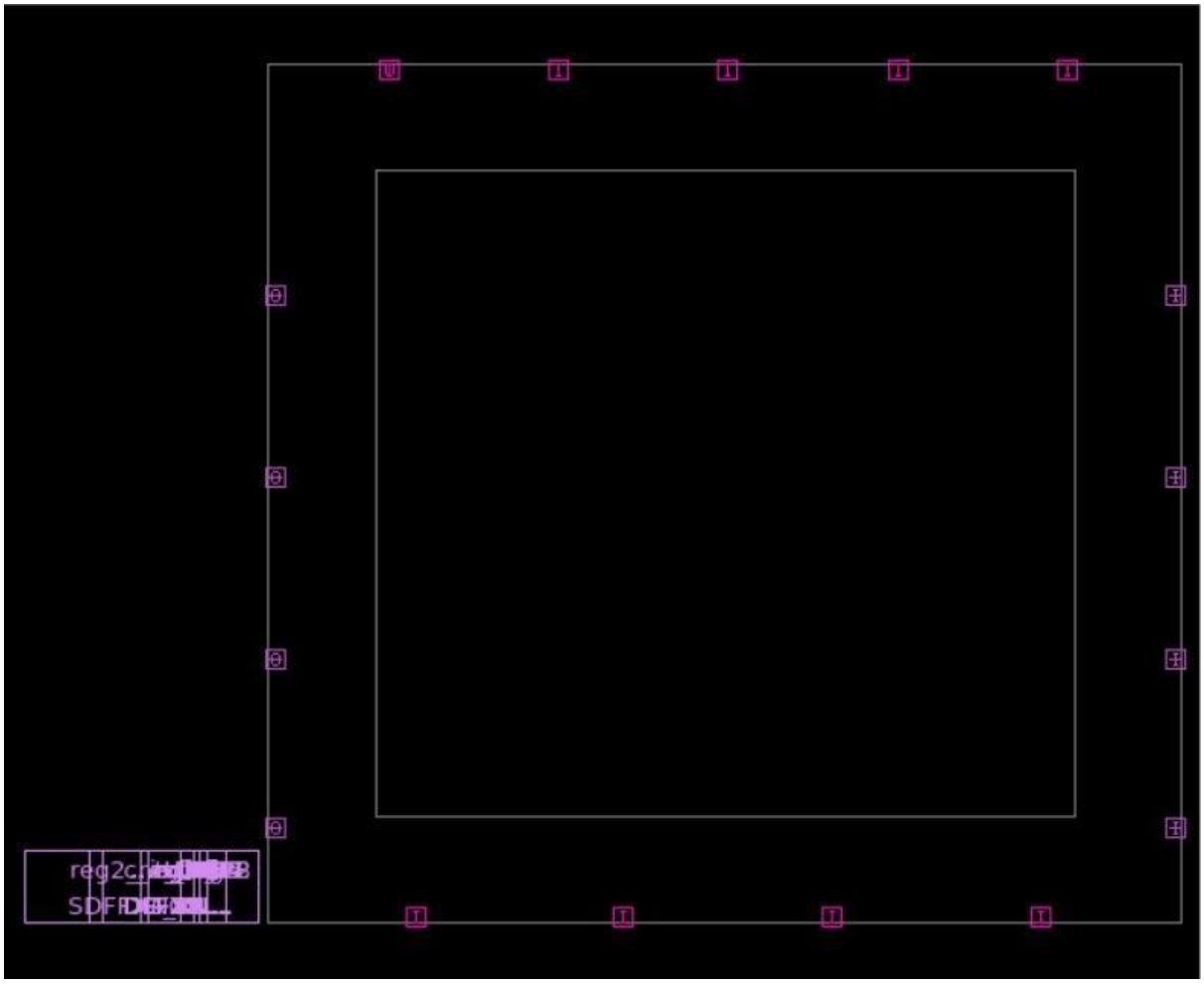
create_port -direction in VDD

create_port -direction in VSS

create_net -power VDD

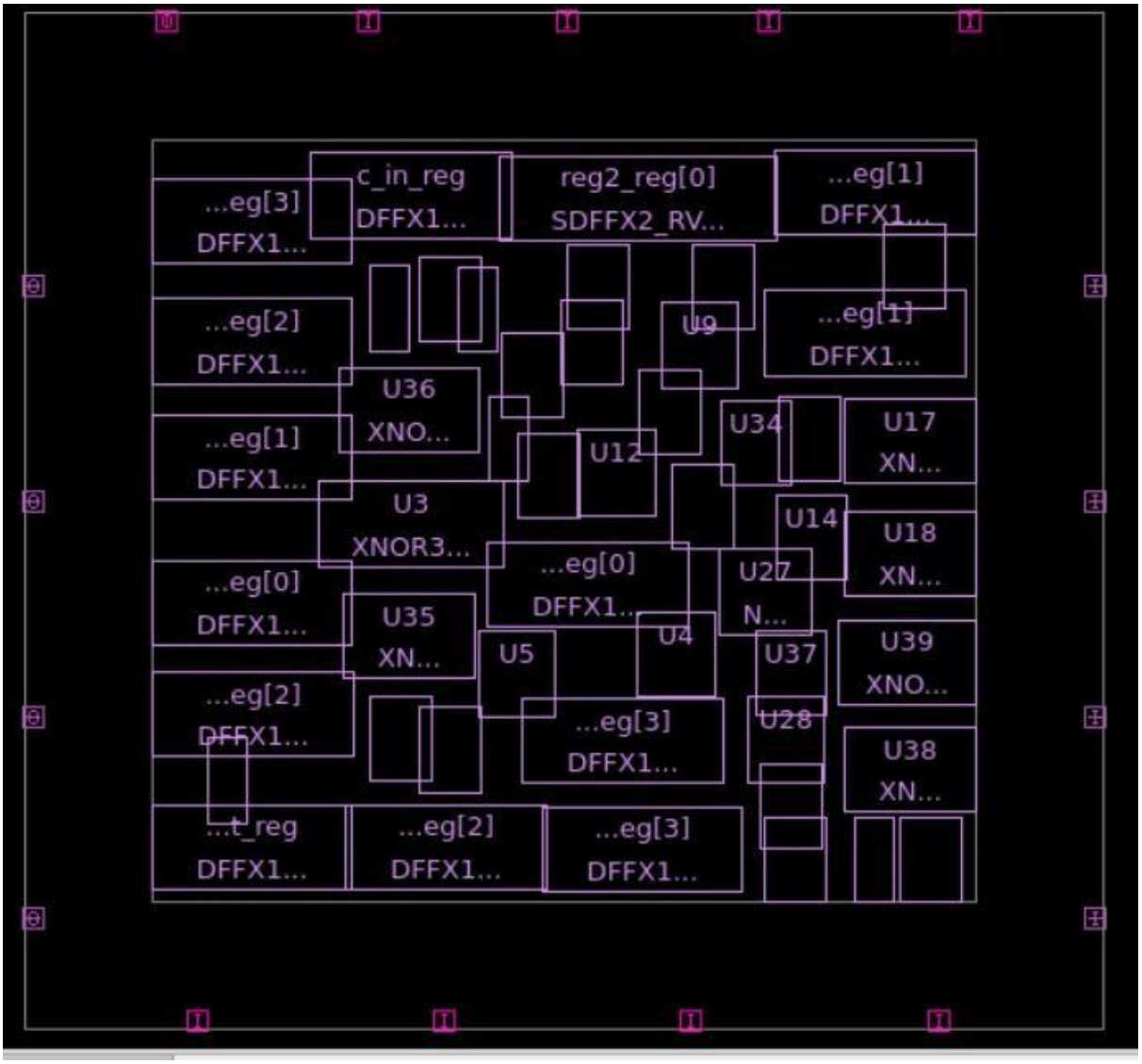
create_net -ground VSS

place_pins -self



Place I/O ports

create_palcement



Coarse placement

save_lib

save_block -as floorplan

3. Powerplanning

connect_pg_net -pg -automatic

create_shape -shape_type rect -layer M7 -boundary {{0.000 4.341} {4.003 4.924}} -port VDD

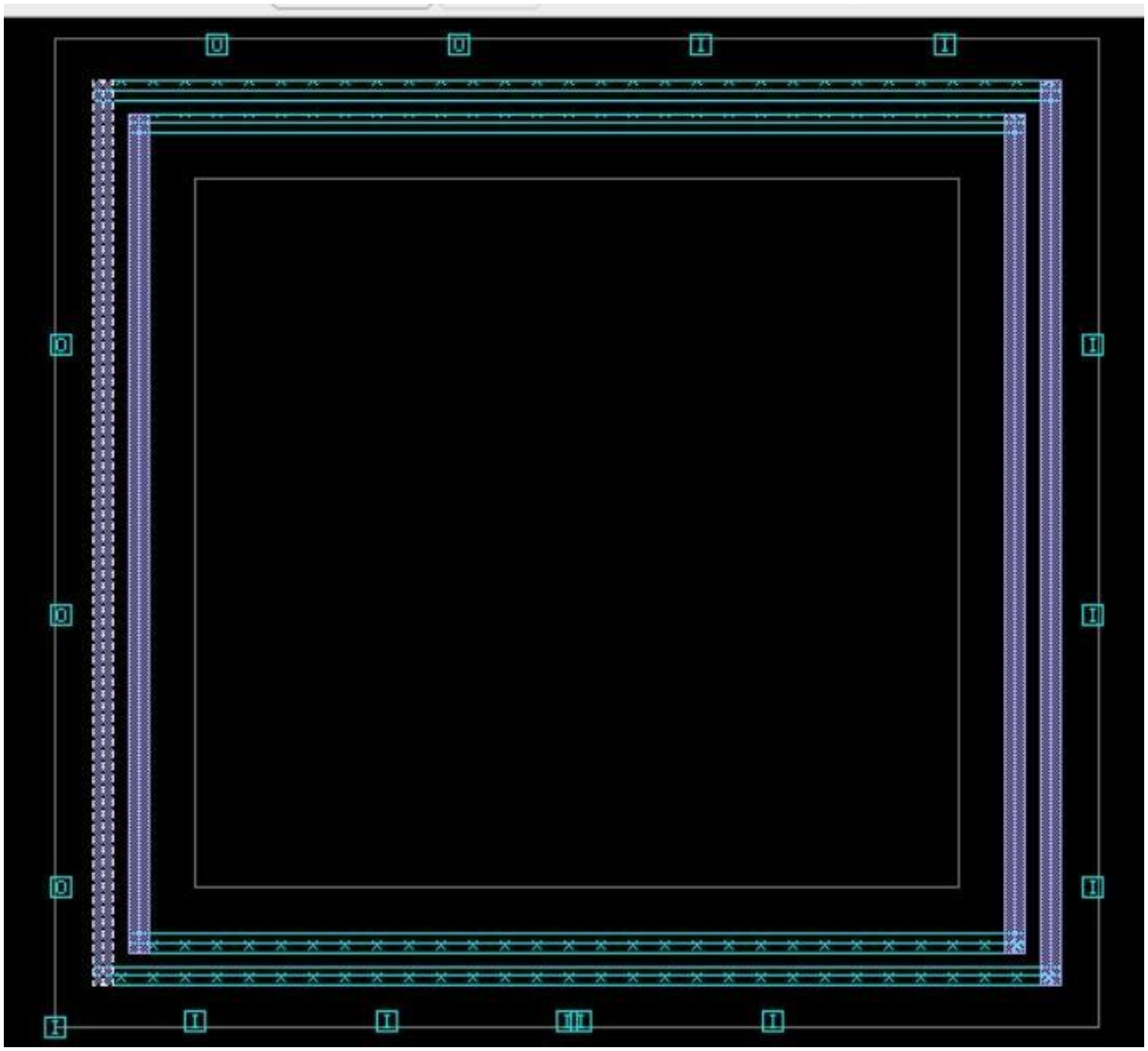
create_shape -shape_type rect -layer M7 -boundary {{0.000 12.312} {2.205 12.590}} -port VSS

#creating core power ring

create_pg_ring_pattern core_ring -horizontal_layer M7 -horizontal_width 0.4 -horizontal_spacing 0.3 -vertical_layer M8 -vertical_width 0.4 -vertical_spacing 0.36

set_pg_strategy ring_stratergy -core -pattern {{name:core_ring} {nets:{VDD VSS}} {offset:{1 1}}}

compile_pg -strategies ring_stratergy



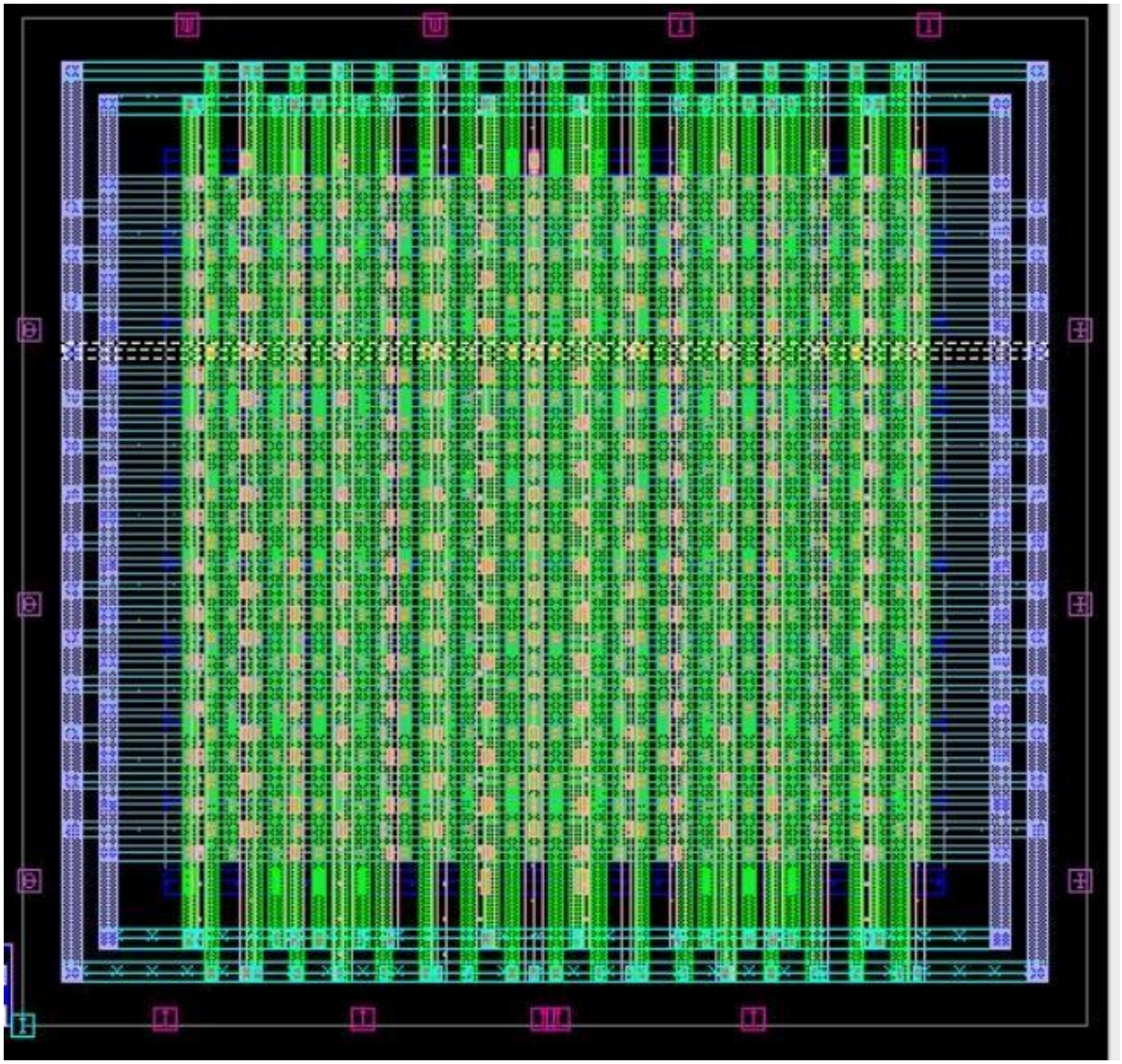
Core power ring

#creating power mesh

create_pg_mesh_pattern mesh -layers {{{vertical_layer:M6} {width:0.34} {spacing:interleaving} {pitch:2} {offset:0.7}} {{horizontal_layer:M5} {width:0.32} {spacing:interleaving} {pitch:1} {offset:0.6}} {{vertical_layer:M4} {width:0.3} {spacing:interleaving} {pitch:0.9} {offset:0.5}}}

set_pg_strategy core_mesh -pattern {{pattern:mesh} {nets:VDD VSS}} -core -extension {stop:innermost_ring}

compile_pg -strategies core_mesh



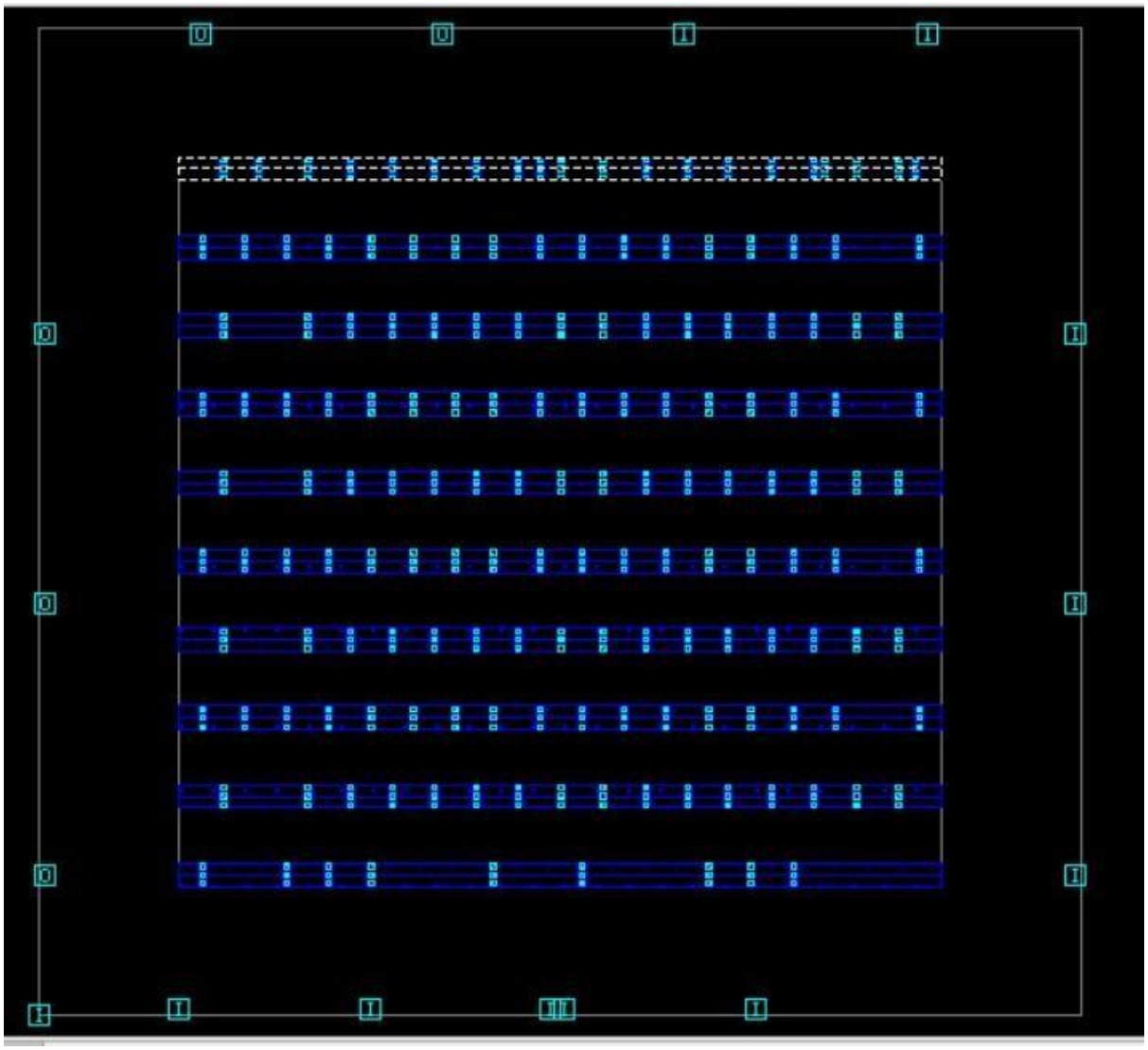
Core mesh

#std cell routes

create_pg_std_cell_conn_pattern std_cell_rail -layers M1 -rail_width 0.5

set_pg_strategy rail_stratergy -core -pattern {{name:std_cell_rail} {nets:VDD VSS}}

compile_pg -strategies rail_stratergy



Std_cells rails

check_pg_drc

```
icc2_shell> check_pg_drc
Command check_pg_drc started  at Fri Apr 11 12:25:28 2025
Command check_pg_drc finished at Fri Apr 11 12:25:28 2025
CPU usage for check_pg_drc: 0.01 seconds ( 0.00 hours)
Elapsed time for check_pg_drc: 0.01 seconds ( 0.00 hours)
No errors found.
```

check_pg_connectivity

```
icc2_shell> check_pg_connectivity
Checking secondary net through power switch is enabled.
Secondary net will be checked together from primary net. They will be treated as the same net
Primary Net : VDD    Secondary Net:
Primary Net : VSS    Secondary Net:
Loading cell instances...
Number of Standard Cells: 50
Number of Macro Cells: 0
Number of IO Pad Cells: 0
Number of Blocks: 0
Loading P/G wires and vias...
Number of VDD Wires: 50
Number of VDD Vias: 791
Number of VDD Terminals: 0
**************Verify net VDD connectivity*****************
  Number of floating wires: 0
  Number of floating vias: 0
  Number of floating std cells: 50
  Number of floating hard macros: 0
  Number of floating I/O pads: 0
  Number of floating terminals: 0
  Number of floating hierarchical blocks: 0
************************************************************
Loading cell instances...
Loading P/G wires and vias...
Number of VSS Wires: 48
Number of VSS Vias: 814
Number of VSS Terminals: 0
**************Verify net VSS connectivity*****************
  Number of floating wires: 0
  Number of floating vias: 0
  Number of floating std cells: 50
  Number of floating hard macros: 0
  Number of floating I/O pads: 0
  Number of floating terminals: 0
  Number of floating hierarchical blocks: 0
************************************************************
```

check_pg_missing_vias

```
icc2_shell> check_pg_missing_vias
Check net VDD vias...
Number of missing vias: 0
Checking net VDD vias took 0 seconds.
Check net VSS vias...
Number of missing vias: 0
Checking net VSS vias took 0 seconds.
Overall runtime: 0 seconds.
icc2_shell>
```

save_lib

save_block -as powerplan

4. **Placement**

set PDK_PATH /data/pdk/pdk32nm/SAED32_EDK

set SDC_PATH "/ve/ti_home/ti_srujan_658/Desktop/Hierarchal_eight_bit/DC/results/full_adder.sdc"

read_sdc $SDC_PATH

set_app_options -name place.coarse.continue_on_missing_scandef -value true

set_app_options -name place_opt.flow.enable_ccd -value true

set_app_options -name place_opt.flow.clock_aware_placement -value true

set_app_options -name place_opt.place.congestion_effort -value high

check_design -checks pre_placement_stage

set mode1 "func"

set corner1 "slow"

set scenario1 "${mode1}_${corner1}"

create_mode $mode1

create_corner $corner1

create_scenario -name $scenario1 -mode $mode1 -corner $corner1

set parasitic1 "p1"

set tluplus_file$parasitic1 "$PDK_PATH/tech/star_rcxt/saed32nm_1p9m_Cmax.tluplus"

set layer_map_file$parasitic1 "$PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map"

read_parasitic_tech -tlup $tluplus_filep1 -layermap $layer_map_filep1 -name p1

set_parasitic_parameters -late_spec $parasitic1 -early_spec $parasitic1

set_dont_use [get_lib_cells */FADD*]

set_dont_use [get_lib_cells */HADD*]

set_dont_use [get_lib_cells */MUX*]

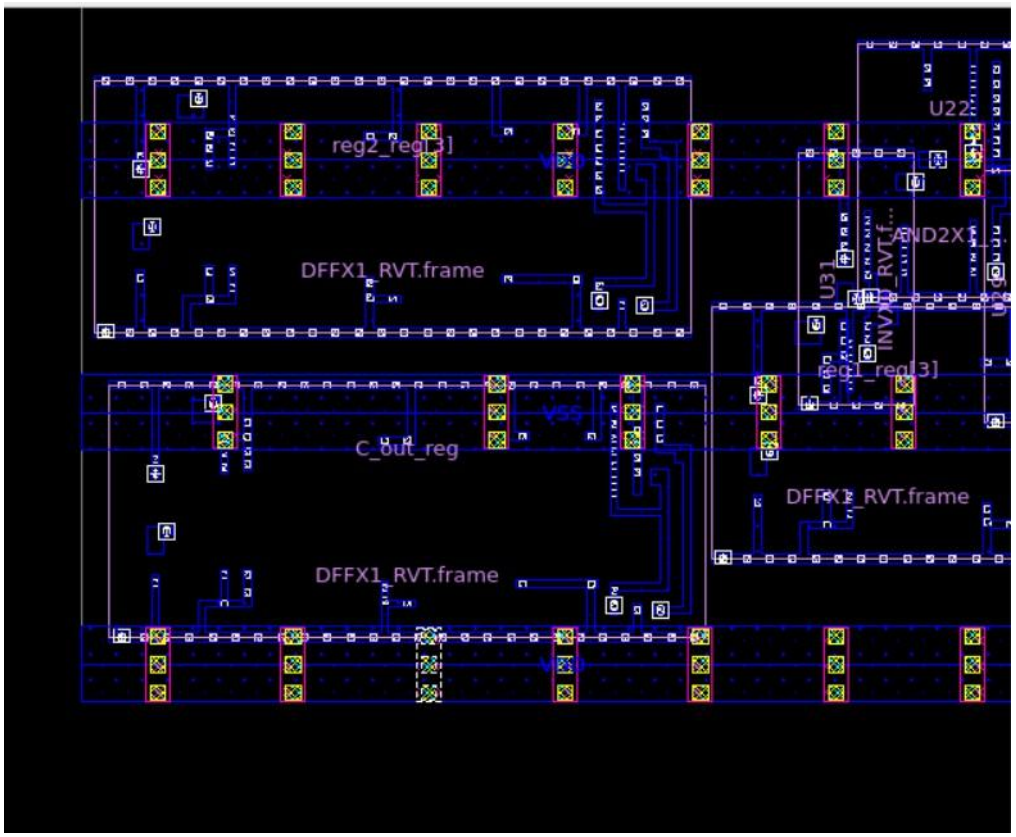
set_dont_use [get_lib_cells /*OR*]

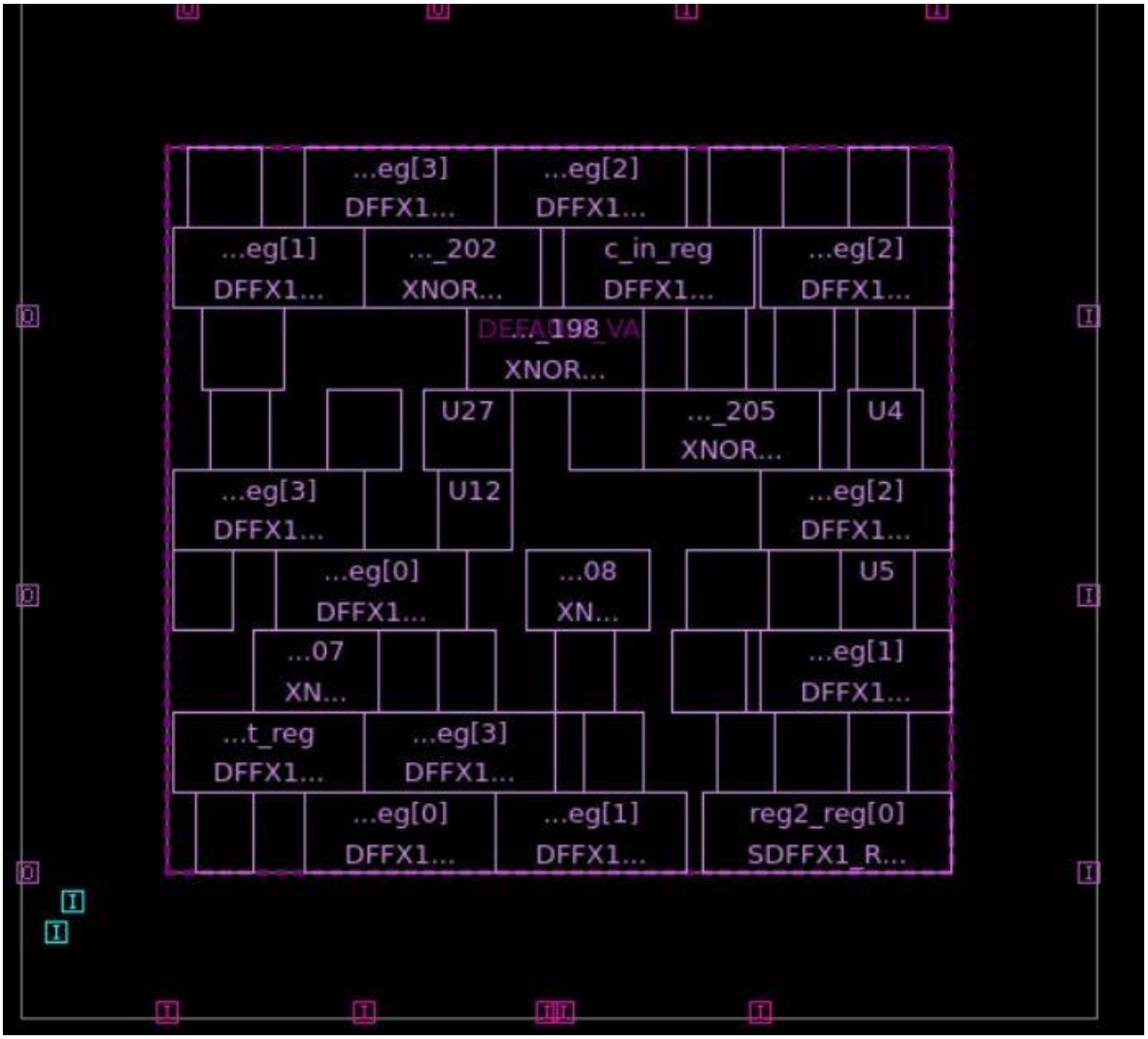
set_operating_conditions -max_library $PDK_PATH/lib/stdcell_rvt/db_ccs/saed32rvt_ss0p75v125c.db

create_clock -period 0.95 [get_ports Clock]

set_scenario_status func_slow -hold false -setup true -leakage_power true -dynamic_power true -max_capacitance true -min_capacitance false -max_transition true -active true

place_opt



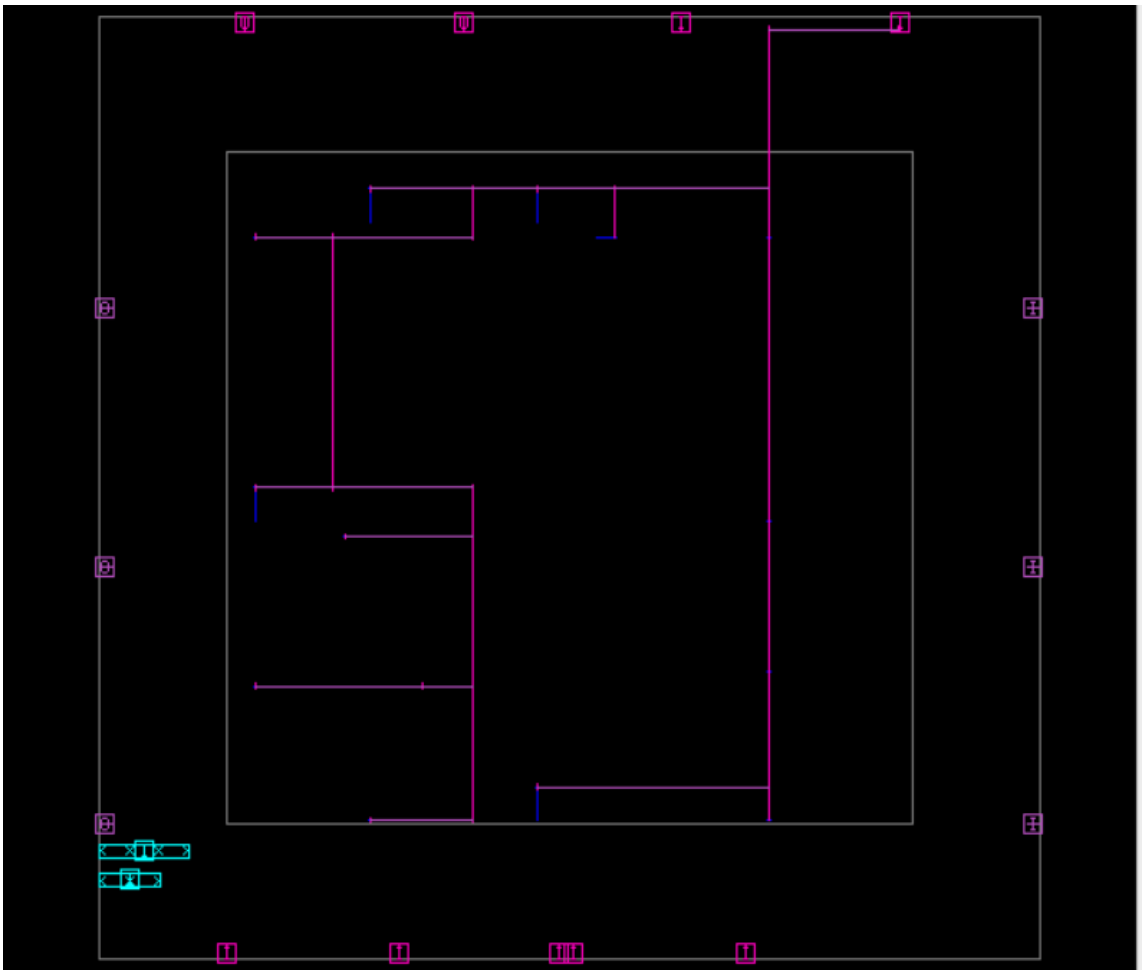


Placement of std cells

5. **CTS**

   check_design -checks pre_clock_tree_stage

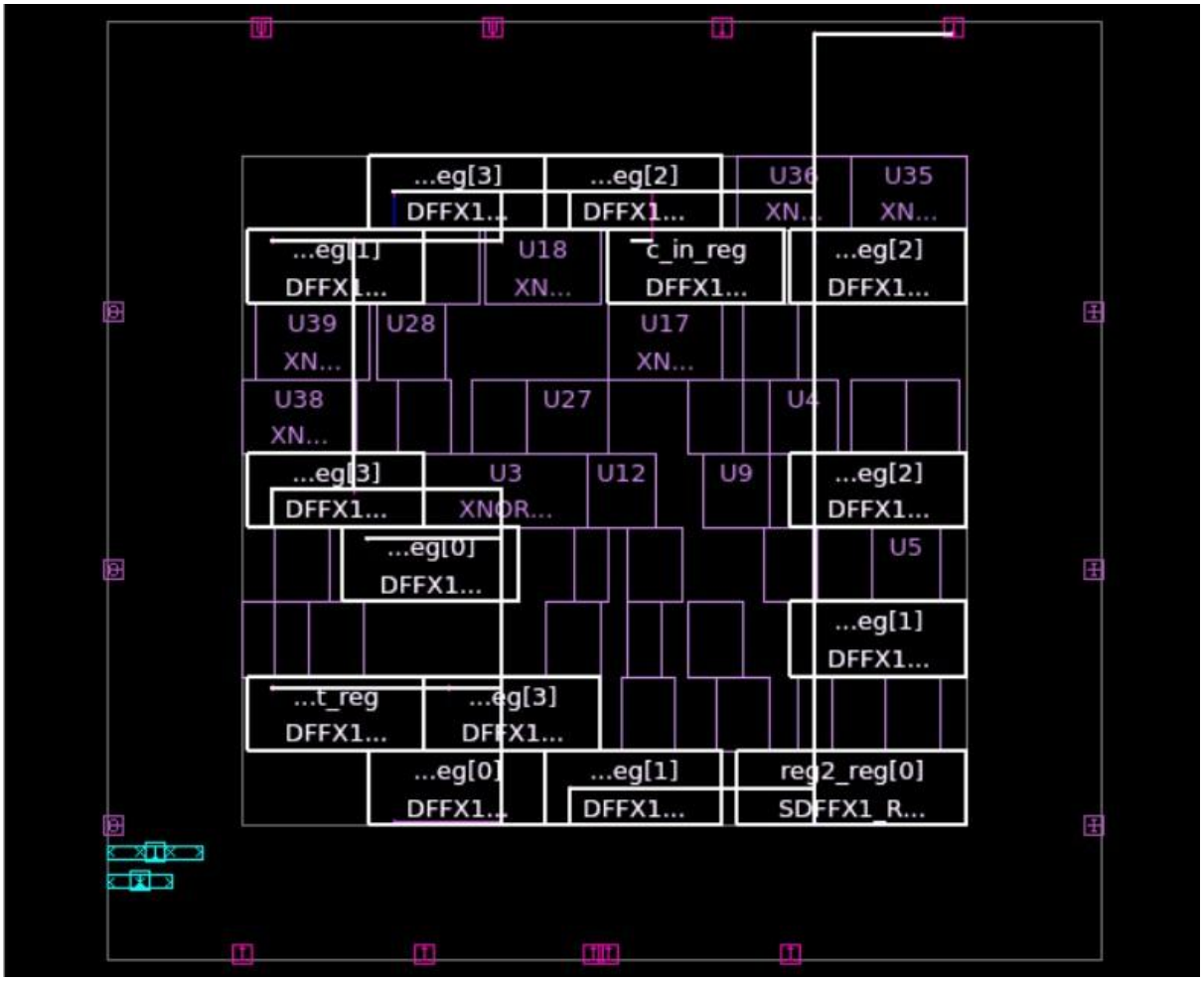
   synthesize_clock_trees



Here in the above image we can observe the clock tree is built initially before running the clock tree optimization command .

So here the clock tree is built from the clock port of the block design to the sink pins of the leaf cells .

The clock tree is built in way to balance and maintain the minimum skew so that the cells are synchronized properly.



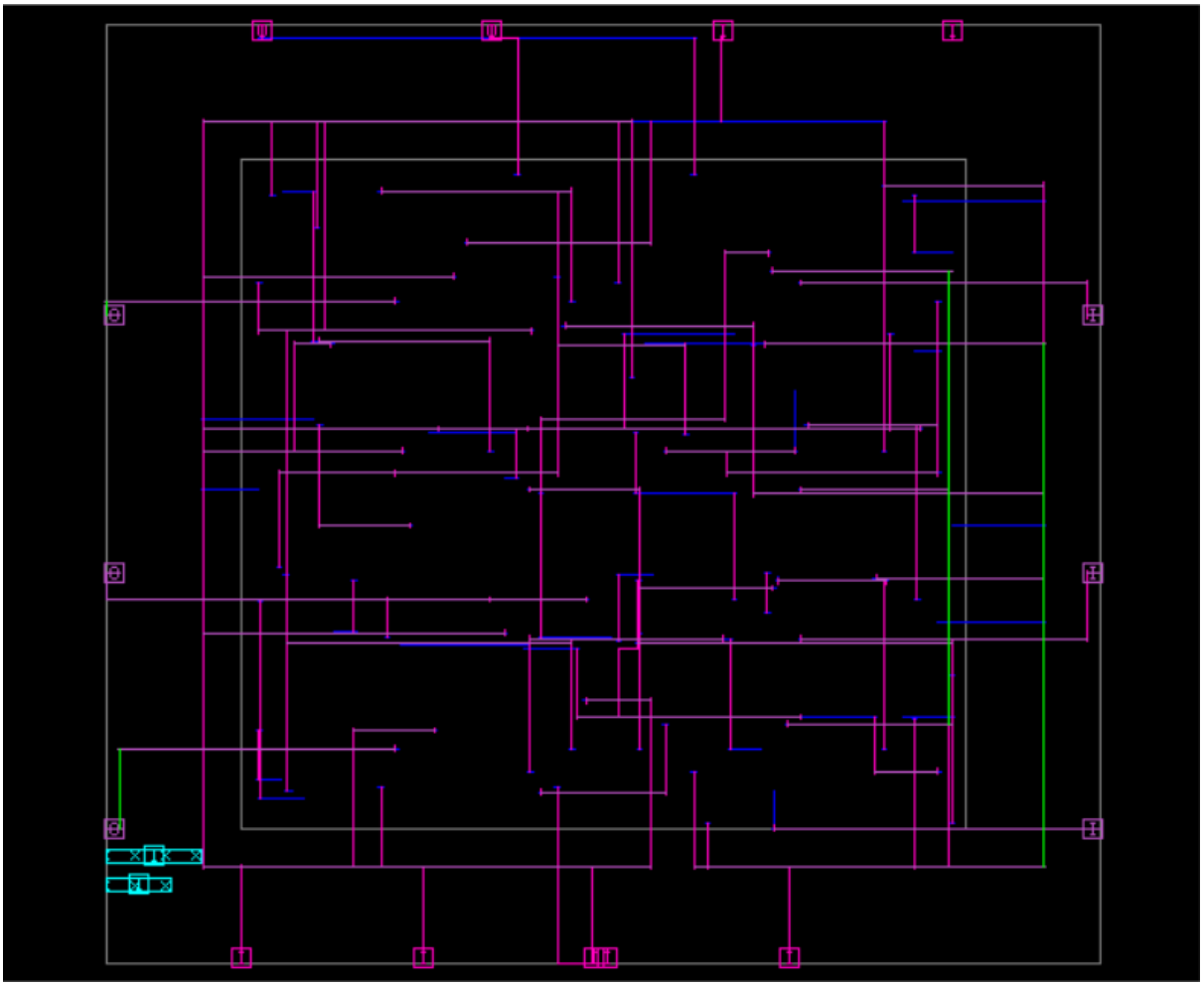
set_app_options -name cts.compile.enable_local_skew -value true

set_app_options -name cts.optimize.enable_local_skew -value true

set_app_options -name cts.compile.enable_global_route -value true

set_clock_tree_options -target_latency 0.3 -target_skew 0.02 -corner $corner1/slow

clock_opt



6. Routing

check_design -checks pre_route_stage

set_app_options -name route.global.timing_driven -value true

set_app_options -name route.global.crosstalk_driven -value true

set_app_options -name route.track.timing_driven -value true

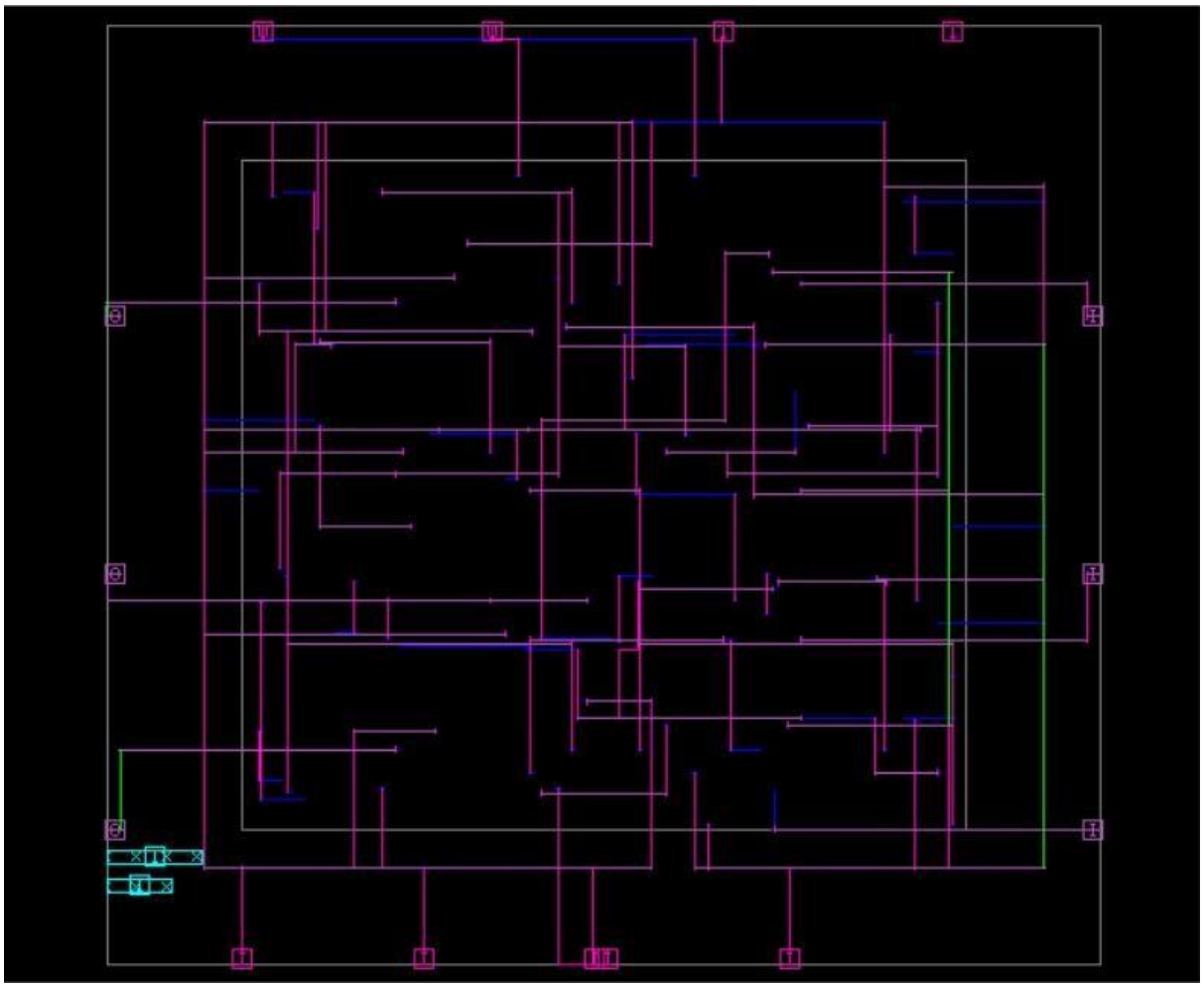
set_app_options -name route.track.crosstalk_driven -value true

set_app_options -name route.detail.timing_driven -value true

set_app_options -name route.detail.antenna -value true

set_app_options -name route.detail.antenna_fixing_preference -value use_diodes

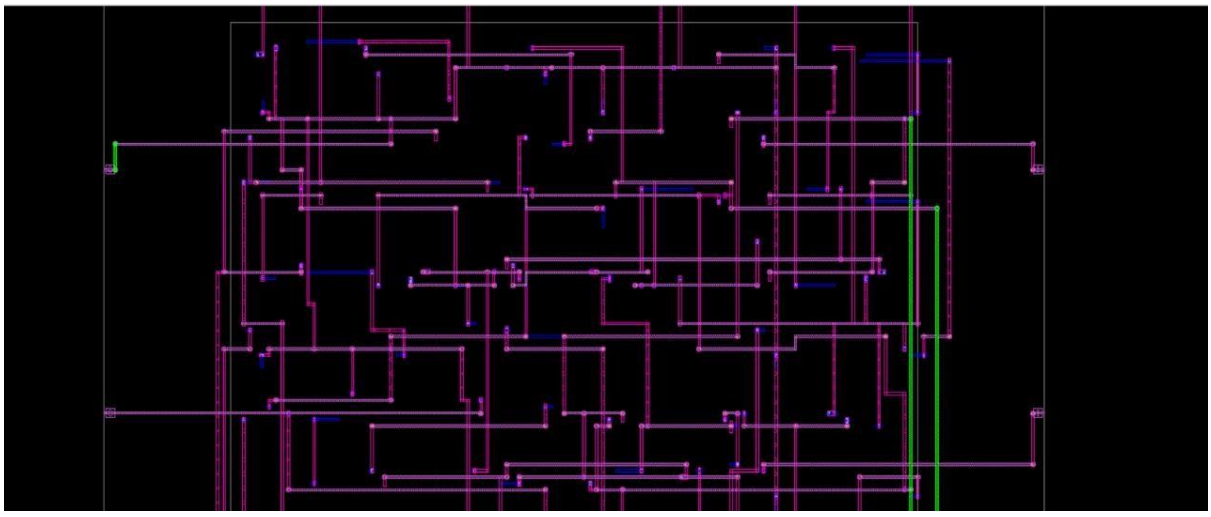
```
set_app_options -block [current_block] -name
route.detail.diode_libcell_names -value  {ANTENNA ANTENNA2}

set_app_options -block [current_block] -name
route.detail.diode_libcell_names -value {*/ANTENNA}

set_app_options -block [current_block] -name
route.detail.diode_libcell_names -value {*/ANTENNA_HVT}

set_app_options -block [current_block] -name
route.detail.diode_libcell_names -value {*/ANTENNA_RVT}

route_global

route_track
```



Track assignment

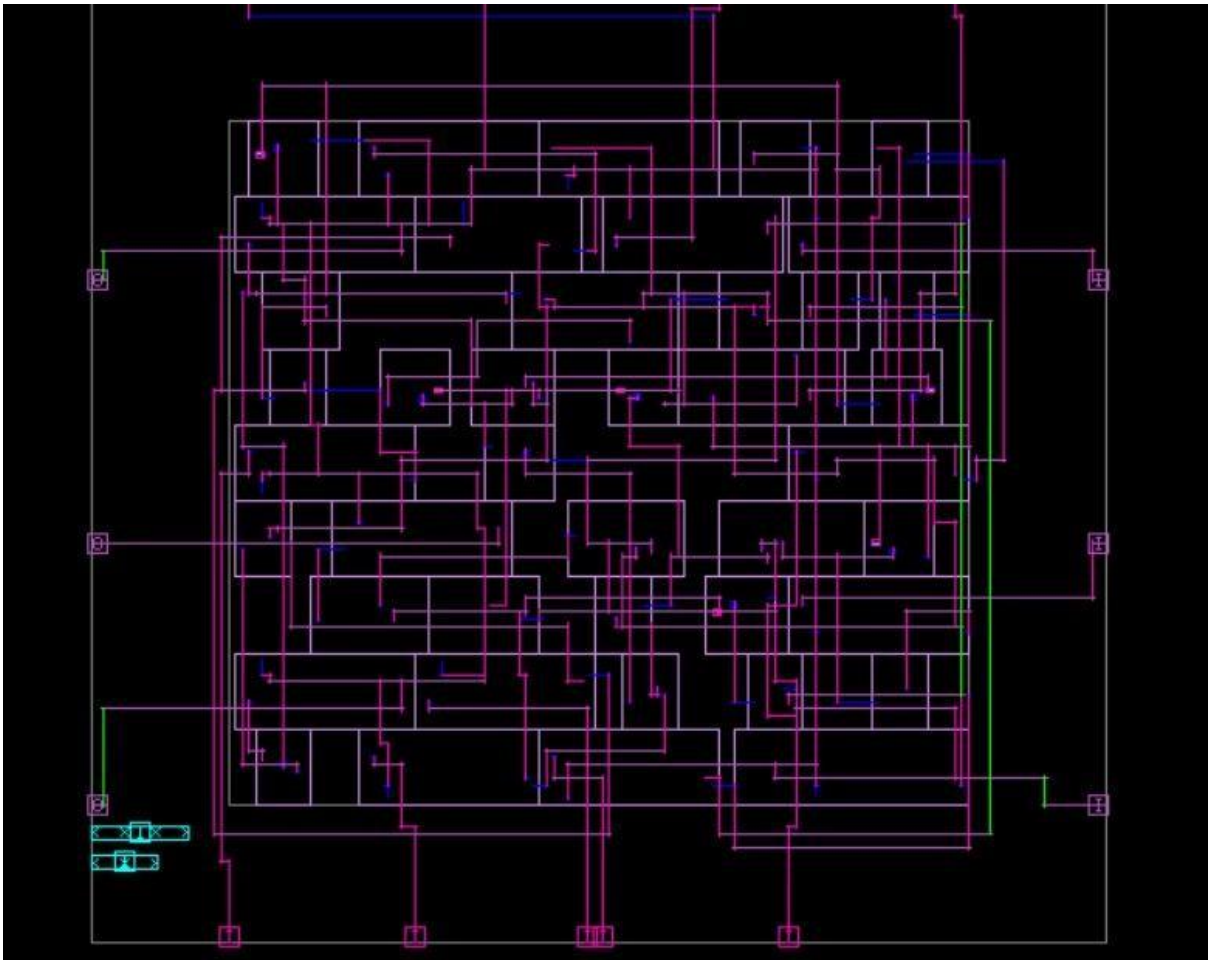
Clock network with track assignment

route_detail



Signal routing

route_opt



report_congestion

```
report_comments                    report_constraint_groups        report
icc2_shell> report_congestion
****************************************
Report : congestion
Design : full_adder
Version: V-2023.12-SP4
Date   : Fri Apr 11 14:48:28 2025
****************************************

Layer      |    overflow     |              # GRCs has
Name       |  total  |  max  | overflow (%)       | max overflow
-------------------------------------------------------------------
Both Dirs |       3 |     1 |       3  ( 0.89%) |       3
H routing |       0 |     0 |       0  ( 0.00%) |       0
V routing |       3 |     1 |       3  ( 1.78%) |       3

1
```

check_lvs

check_routes

check_routability

write_sdc FA.sdf

write_verilog routed_full_adder.route.v

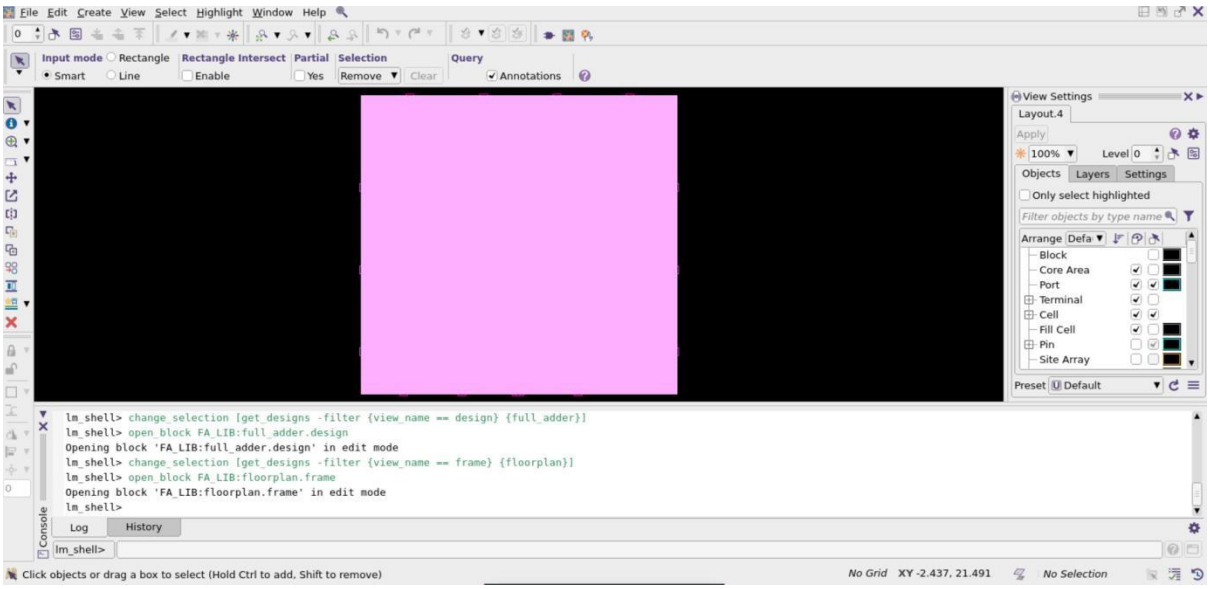
write_lef -design full_adder full_adder.lef

write_gds FA.gds

create_frame

This is the frame view of 4 bit full adder viewed in Library manager tool

{ lm_shell }



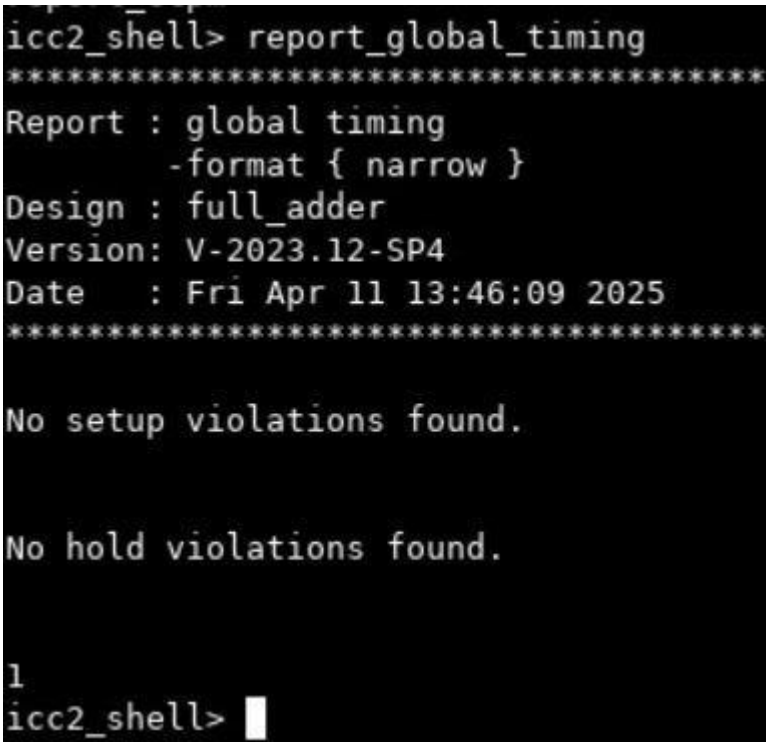
Reports:

```
Startpoint: SUM_reg[2] (rising edge-triggered flip-flop clocked by Clock)
Endpoint: SUM[2] (output port clocked by Clock)
Mode: func
Corner: slow
Scenario: func_slow
Path Group: **reg2out_default**
Path Type: max

Point                                          Incr      Path
-----------------------------------------------------------------------
clock Clock (rise edge)                        0.00      0.00
clock network delay (propagated)               0.07      0.07

SUM_reg[2]/CLK (DFFX1_RVT)                     0.00      0.07 r
SUM_reg[2]/Q (DFFX1_RVT)                       0.09      0.16 f
SUM[2] (out)                                   0.00      0.16 f
data arrival time                                        0.16

clock Clock (rise edge)                        1.00      1.00
clock network delay (propagated)               0.07      1.07
clock uncertainty                             -0.30      0.77
output external delay                         -0.50      0.27
data required time                                       0.27
-----------------------------------------------------------------------
data required time                                       0.27
data arrival time                                       -0.16
-----------------------------------------------------------------------
slack (MET)                                              0.11
```

Post CTS setup timing

```
Startpoint: reg1_reg[2] (rising edge-triggered flip-flop clocked by Clock)
Endpoint: SUM_reg[2] (rising edge-triggered flip-flop clocked by Clock)
Mode: func
Corner: slow
Scenario: func_slow
Path Group: Clock
Path Type: min

Point                                              Incr       Path
-----------------------------------------------------------------------------
clock Clock (rise edge)                           0.00       0.00
clock network delay (propagated)                  0.07       0.07

reg1_reg[2]/CLK (DFFX1_RVT)                       0.00       0.07 r
reg1_reg[2]/Q (DFFX1_RVT)                         0.08       0.15 r
ctmTdsLR_1_205/Y (XNOR3X1_RVT)                    0.03       0.18 r
SUM_reg[2]/D (DFFX1_RVT)                          0.00       0.18 r
data arrival time                                            0.18

clock Clock (rise edge)                           0.00       0.00
clock network delay (propagated)                  0.07       0.07
SUM_reg[2]/CLK (DFFX1_RVT)                        0.00       0.07 r
clock uncertainty                                 0.10       0.17
library hold time                                -0.00       0.17
data required time                                           0.17
-----------------------------------------------------------------------------
data required time                                           0.17
data arrival time                                           -0.18
-----------------------------------------------------------------------------
slack (MET)                                                  0.01
```

Post CTS hold timing



Global timing report

1. Generate .lib of 4bit FA from primetime

pt_shell

set link_path /data/pdk/pdk32nm/SAED32_EDK/lib/stdcell_rvt/db_ccs/saed32rvt_tt0p78vn40c.db

read_verilog ./../DC/full_adder_routed.v

link_design

current_design

read_sdc ./../Constraints/full_adder.sdc

read_parasitics ./../DC/full_adder_func_slow.spef.p1_125.spef

report_timing

extract_model -output full_adder -format lib

```
Startpoint: reg2_reg[0]
            (rising edge-triggered flip-flop clocked by Clock)
Endpoint: SUM_reg[3] (rising edge-triggered flip-flop clocked by Clock)
Path Group: Clock
Path Type: max

Point                                                    Incr       Path
-----------------------------------------------------------------------------
clock Clock (rise edge)                                  0.00       0.00
clock network delay (ideal)                              0.00       0.00
reg2_reg[0]/CLK (SDFFX1_RVT)                             0.00       0.00 r
reg2_reg[0]/QN (SDFFX1_RVT)                              0.18 &     0.18 r
U13/Y (AND2X1_RVT)                                       0.09 &     0.26 r
U12/Y (NOR2X0_RVT)                                       0.09 &     0.36 f
U27/Y (NOR4X1_RVT)                                       0.15 &     0.51 r
ctmTdsLR_2_203/Y (NOR2X0_RVT)                            0.10 &     0.60 f
ctmTdsLR_1_202/Y (XNOR3X1_RVT)                           0.25 &     0.85 f
SUM_reg[3]/D (DFFX1_RVT)                                 0.00 &     0.85 f
data arrival time                                                   0.85

clock Clock (rise edge)                                  1.00       1.00
clock network delay (ideal)                              0.00       1.00
SUM_reg[3]/CLK (DFFX1_RVT)                                          1.00 r
clock reconvergence pessimism                            0.00       1.00
clock uncertainty                                       -0.30       0.70
library setup time                                      -0.13       0.57
data required time                                                  0.57
-----------------------------------------------------------------------------
data required time                                                  0.57
data arrival time                                                  -0.85
-----------------------------------------------------------------------------
slack (VIOLATED)                                                   -0.28
```

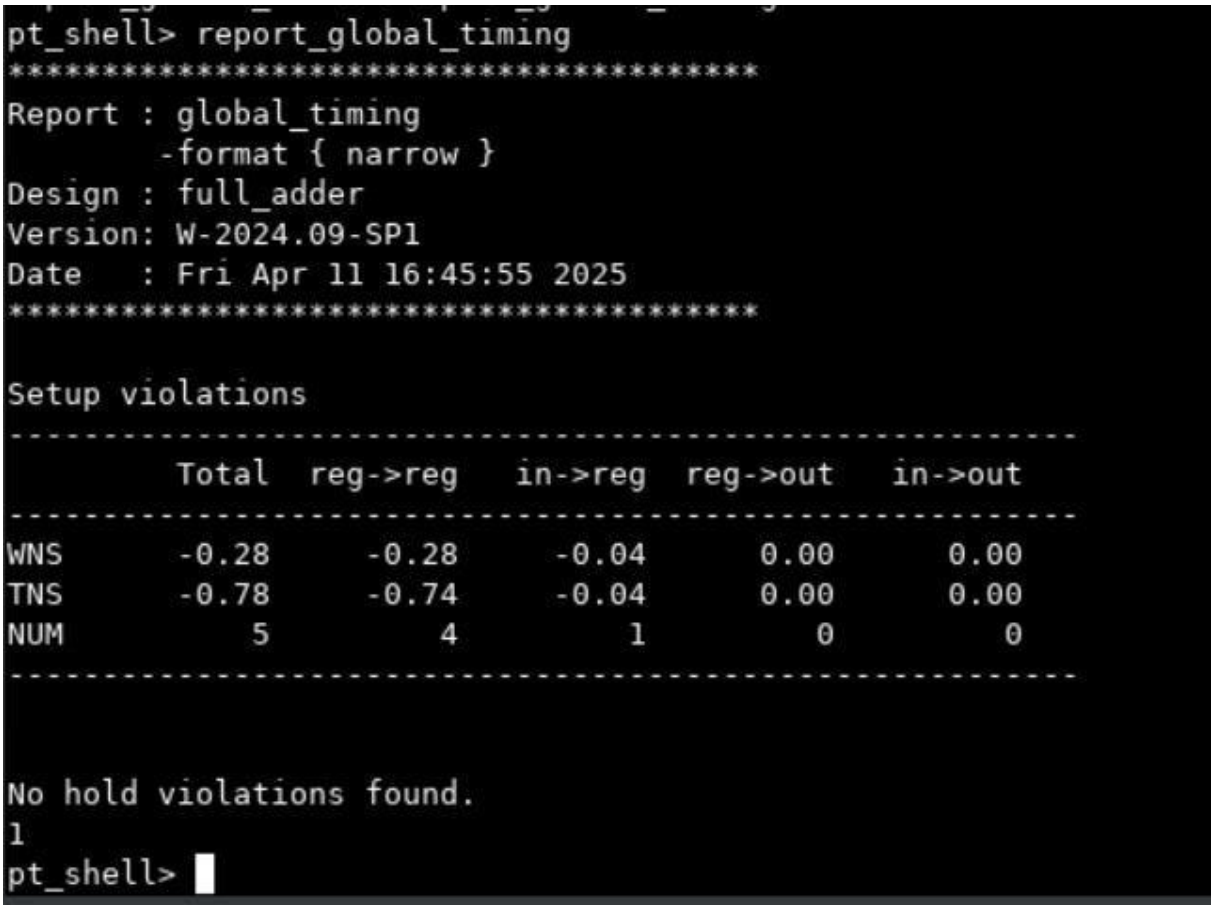
Setup report

```
pt_shell> report_analysis_coverage
****************************************
Report : analysis_coverage
Design : full_adder
Version: W-2024.09-SP1
Date   : Fri Apr 11 16:47:49 2025
****************************************

Type of Check         Total              Met         Violated         Untested
-------------------------------------------------------------------------------
setup                    16         9 ( 56%)         5 ( 31%)         2 ( 13%)
hold                     16         5 ( 31%)         0 (  0%)        11 ( 69%)
min_pulse_width          28        28 (100%)         0 (  0%)         0 (  0%)
out_setup                 5         5 (100%)         0 (  0%)         0 (  0%)
out_hold                  5         0 (  0%)         0 (  0%)         5 (100%)
-------------------------------------------------------------------------------
All Checks               70        47 ( 67%)         5 (  7%)        18 ( 26%)

1
pt_shell>
```

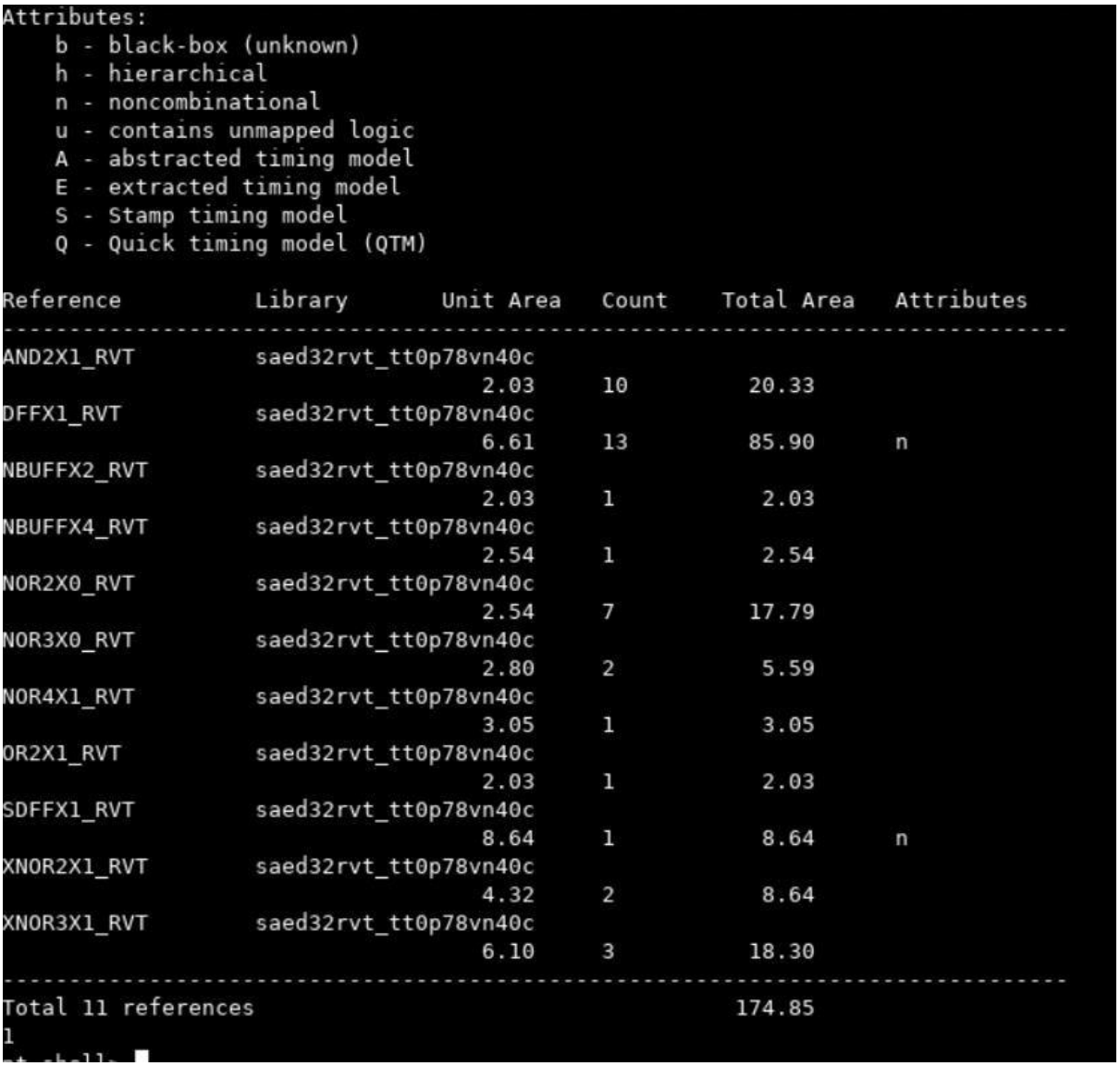
Analysis coverage report

```
Startpoint: reg1_reg[2]
            (rising edge-triggered flip-flop clocked by Clock)
Endpoint: SUM_reg[2] (rising edge-triggered flip-flop clocked by Clock)
Path Group: Clock
Path Type: min

Point                                                   Incr       Path
-----------------------------------------------------------------------------
clock Clock (rise edge)                                 0.00       0.00
clock network delay (ideal)                             0.00       0.00
reg1_reg[2]/CLK (DFFX1_RVT)                             0.00       0.00 r
reg1_reg[2]/Q (DFFX1_RVT)                               0.20 &     0.20 r
ctmTdsLR_1_205/Y (XNOR3X1_RVT)                          0.08 &     0.28 r
SUM_reg[2]/D (DFFX1_RVT)                                0.00 &     0.28 r
data arrival time                                                  0.28

clock Clock (rise edge)                                 0.00       0.00
clock network delay (ideal)                             0.00       0.00
SUM_reg[2]/CLK (DFFX1_RVT)                                         0.00 r
clock reconvergence pessimism                           0.00       0.00
clock uncertainty                                       0.10       0.10
library hold time                                      -0.04       0.06
data required time                                                 0.06
-----------------------------------------------------------------------------
data required time                                                 0.06
data arrival time                                                 -0.28
-----------------------------------------------------------------------------
slack (MET)                                                        0.21
```

Hold report



Global timing report



```
Attributes:
    b - black-box (unknown)
    h - hierarchical
    n - noncombinational
    u - contains unmapped logic
    A - abstracted timing model
    E - extracted timing model
    S - Stamp timing model
    Q - Quick timing model (QTM)

Reference          Library       Unit Area   Count    Total Area   Attributes
--------------------------------------------------------------------------------
AND2X1_RVT         saed32rvt_tt0p78vn40c
                                 2.03        10         20.33
DFFX1_RVT          saed32rvt_tt0p78vn40c
                                 6.61        13         85.90      n
NBUFFX2_RVT        saed32rvt_tt0p78vn40c
                                 2.03        1           2.03
NBUFFX4_RVT        saed32rvt_tt0p78vn40c
                                 2.54        1           2.54
NOR2X0_RVT         saed32rvt_tt0p78vn40c
                                 2.54        7          17.79
NOR3X0_RVT         saed32rvt_tt0p78vn40c
                                 2.80        2           5.59
NOR4X1_RVT         saed32rvt_tt0p78vn40c
                                 3.05        1           3.05
OR2X1_RVT          saed32rvt_tt0p78vn40c
                                 2.03        1           2.03
SDFFX1_RVT         saed32rvt_tt0p78vn40c
                                 8.64        1           8.64      n
XNOR2X1_RVT        saed32rvt_tt0p78vn40c
                                 4.32        2           8.64
XNOR3X1_RVT        saed32rvt_tt0p78vn40c
                                 6.10        3          18.30
--------------------------------------------------------------------------------
Total 11 references                                    174.85
1
```

Report_references

```
report_design          report_design_mismatch  report_design_variation
pt_shell> report_design
****************************************
Report : design
Design : full_adder
Version: W-2024.09-SP1
Date   : Fri Apr 11 16:49:39 2025
****************************************

Design Attribute                        Value
------------------------------------------------------------------------
Operating Conditions:
  analysis_type                         on_chip_variation
  operating_condition_min_name          tt0p78vn40c
  process_min                           1
  temperature_min                       -40
  voltage_min                           0.78
  tree_type_min                         balanced_case

  operating_condition_max_name          tt0p78vn40c
  process_max                           1
  temperature_max                       -40
  voltage_max                           0.78
  tree_type_max                         balanced_case

Wire Load:                              (use report_wire_load for more information)
  wire_load_mode                        enclosed
  wire_load_model_max                   ForQA
  wire_load_model_library_max           saed32rvt_tt0p78vn40c
  wire_load_selection_type_max          automatic-by-area
  wire_load_model_min                   ForQA
  wire_load_model_library_min           saed32rvt_tt0p78vn40c
  wire_load_selection_type_min          automatic-by-area
  wire_load_selection_group_max         predcaps
  wire_load_selection_group_min         predcaps
  wire_load_min_block_size              0
```

report_design

```
Timing Path Group 'Clock' (max_delay/setup)
-------------------------------------------
Levels of Logic:                         6
Critical Path Length:                 0.85
Critical Path Slack:                 -0.28
Total Negative Slack:                -0.78
No. of Violating Paths:                  5
-------------------------------------------

Timing Path Group 'Clock' (min_delay/hold)
-------------------------------------------
Levels of Logic:                         2
Critical Path Length:                 0.28
Critical Path Slack:                  0.21
Total Negative Slack:                 0.00
No. of Violating Paths:                  0
-------------------------------------------

Area
-------------------------------------------
Net Interconnect area:                9.10
Total cell area:                    174.85
Design Area:                        183.95
-------------------------------------------


Cell & Pin Count
-------------------------------------------
Pin Count:                             147
Hierarchical Cell Count:                 0
Hierarchical Port Count:                 0
Leaf Cell Count:                        42
-------------------------------------------
```

Report_qor

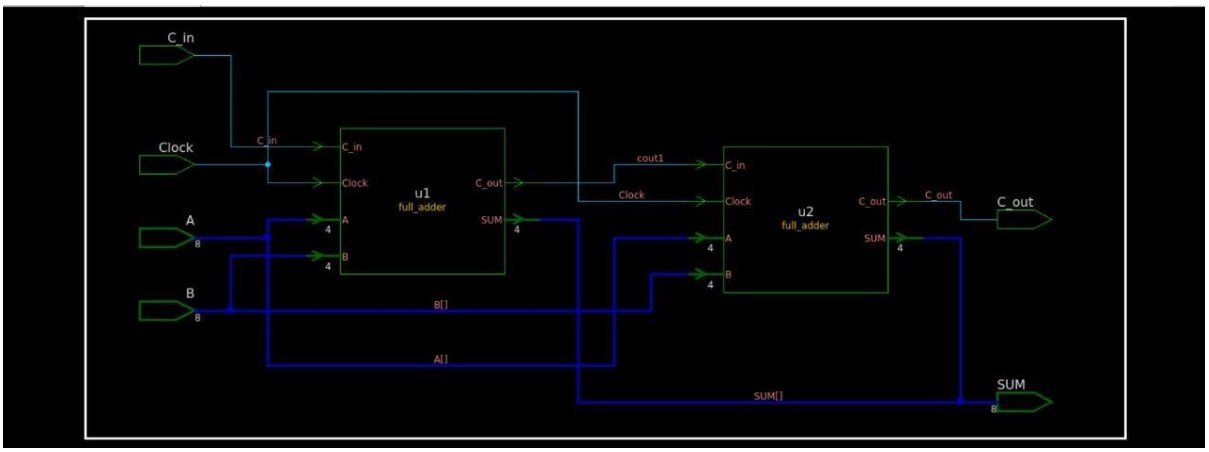
3.2 8 Bit Full Adder Hierarchal Design

3.2.1 Hierarchal Synthesis Of 8 Bit Full Adder

Extract the .lib file in

Primetime

```
# Set the standard cell library path
set link_path /data/pdk/pdk32nm/SAED32_EDK/lib/stdcell_rvt/db_ccs/saed32rvt_tt0p78vn40c.db

# Read the synthesized and routed Verilog netlist
read_verilog ./../ICC2/data/final_full_adder_routed_netlist.v

# Link the design (required after reading netlist)
link_design

# Optional: Confirm current design name
current_design

# Read the timing constraints (SDC)
read_sdc ./../Constraints/full_adder.sdc

# Read the parasitics (post-layout)
read_parasitics ./../ICC2/data/full_adder_func_slow.spef.p1_125.spef

# Generate timing report (for verification)
report_timing

# Extract Liberty model with parasitics and constraints applied
extract_model -output final_full_adder -format lib

# Switch to Library Compiler Shell (LC Shell) to work with Liberty files

# Run this from LC shell environment (optional header for clarity)
 # FA lc_shell

# Read the Liberty model generated from extract_model
read_lib ./../PT/full_adder.lib

# Write the library in .db format for later use in PT or DC
write_lib full_adder -output full_adder.db -format db
```



Gtech view of 8-bit FA

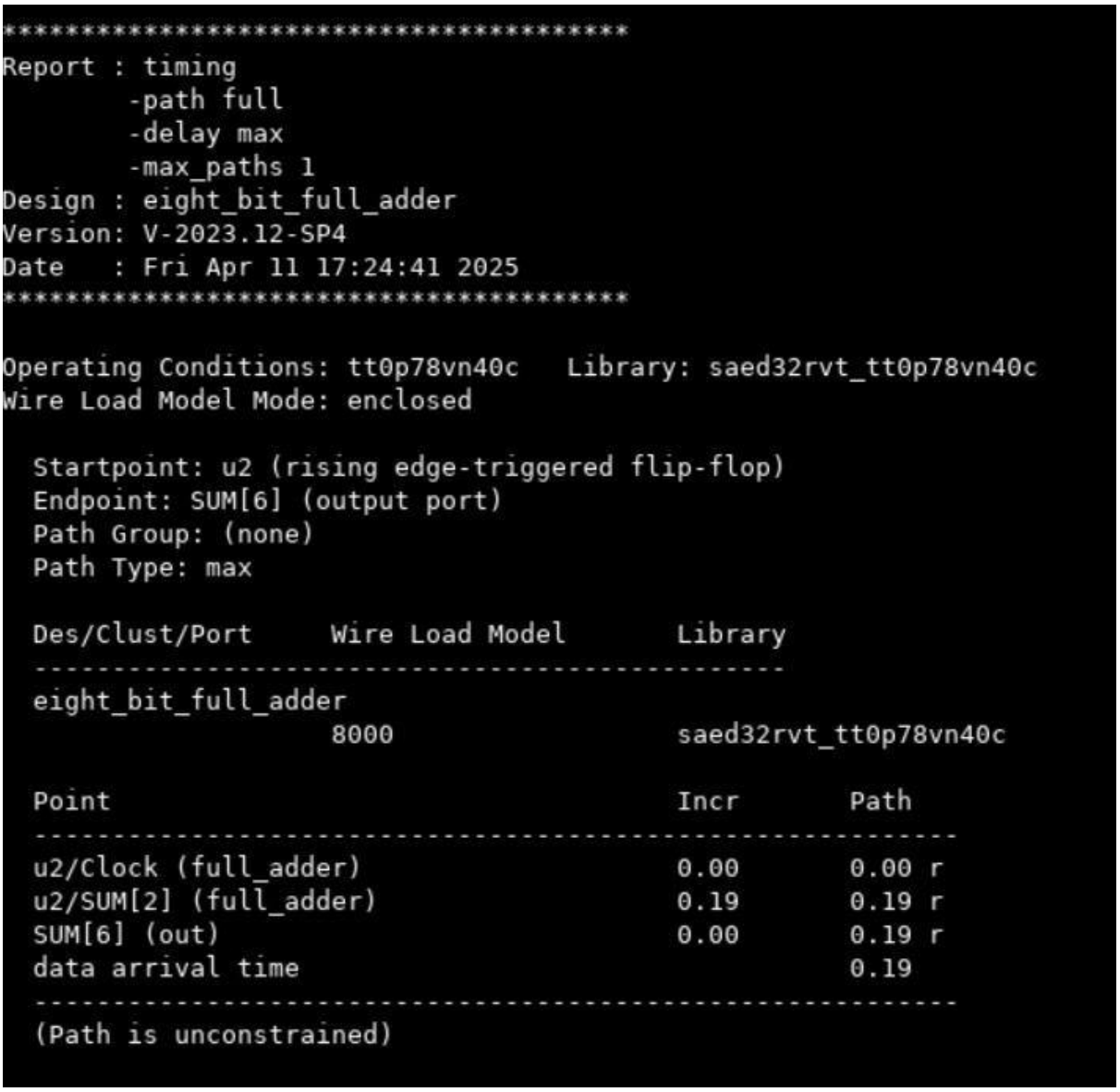
```
****************************************
Report : cell
Design : eight_bit_full_adder
Version: V-2023.12-SP4
Date   : Fri Apr 11 17:20:20 2025
****************************************

Attributes:
    b - black box (unknown)
    d - dont_touch
    h - hierarchical
    n - noncombinational
    r - removable
    u - contains unmapped logic

Cell                    Reference       Library            Area  Attributes
--------------------------------------------------------------------------------
u1                      full_adder      full_adder      183.948364
                                                                  b, d
u2                      full_adder      full_adder      183.948364
                                                                  b, d
--------------------------------------------------------------------------------
Total 2 cells                                           367.896729
1
```

report_cell

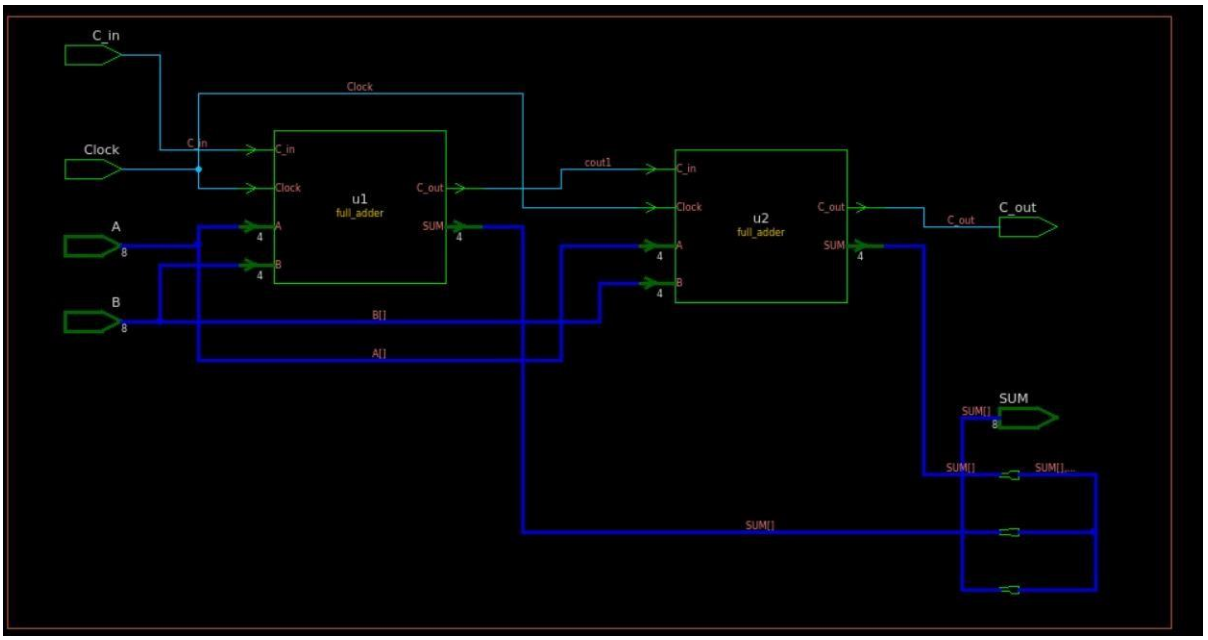
```
Connections for cell 'u1':
    Reference:          full_adder
    Library:            full_adder

    Input Pins          Net
    ----------------    ------------
    A[0]                A[0]
    A[1]                A[1]
    A[2]                A[2]
    A[3]                A[3]
    B[0]                B[0]
    B[1]                B[1]
    B[2]                B[2]
    B[3]                B[3]
    C_in                C_in
    Clock               Clock

    Output Pins         Net
    ----------------    ------------
    C_out               cout1
    SUM[0]              SUM[0]
    SUM[1]              SUM[1]
    SUM[2]              SUM[2]
    SUM[3]              SUM[3]
```

```
    Output Pins          Net
    ----------------     ------------
    C_out                cout1
    SUM[0]               SUM[0]
    SUM[1]               SUM[1]
    SUM[2]               SUM[2]
    SUM[3]               SUM[3]

Connections for cell 'u2':
    Reference:           full_adder
    Library:             full_adder

    Input Pins           Net
    ----------------     ------------
    A[0]                 A[4]
    A[1]                 A[5]
    A[2]                 A[6]
    A[3]                 A[7]
    B[0]                 B[4]
    B[1]                 B[5]
    B[2]                 B[6]
    B[3]                 B[7]
    C_in                 cout1
    Clock                Clock

    Output Pins          Net
    ----------------     ------------
    C_out                C_out
    SUM[0]               SUM[4]
    SUM[1]               SUM[5]
    SUM[2]               SUM[6]
    SUM[3]               SUM[7]
```

Report_connections



Timing report before sdc



Mapped netlist

3.2.2 ICC2_FLOW OF EIGHT BIT FULL ADDER:

FLOORPLAN:

set PDK_PATH /data/pdk/pdk32nm/SAED32_EDK/

create_lib -ref_libs "$PDK_PATH/lib/stdcell_rvt/ndm/saed32rvt_c.ndm ./FA_LIB1/lib.ndm" EIGHT_BIT_FULL_ADDER_LIB3

read_verilog {./../DC/results/eight_bit_full_adder.mapped.v} -library EIGHT_BIT_FULL_ADDER_LIB1 -design eight_bit_full_adder -top eight_bit_full_adder

link_block

read_tech_lef ./full_adders.lef

initialize_floorplan -core_offset 5 -side_length {60 70}

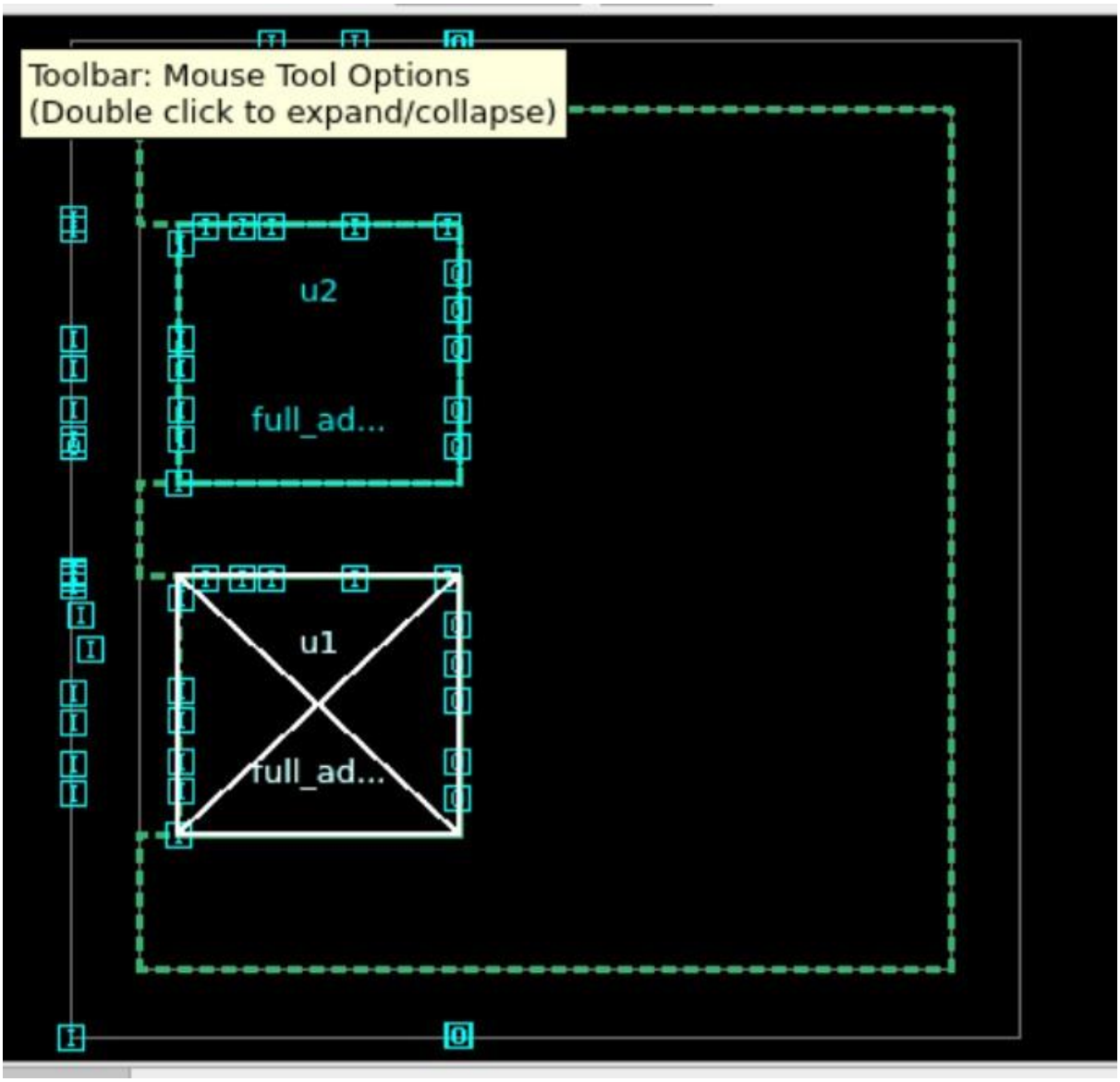
set_attribute -objects [get_cells u1] -name origin -value {8 8}

set_attribute -objects [get_cells u2] -name origin -value {8 32}

set_attribute -objects [get_cells "u1 u2"] -name physical_status fixed -value placed

set_fixed_objects [get_cells -filter "is_soft_macro"]

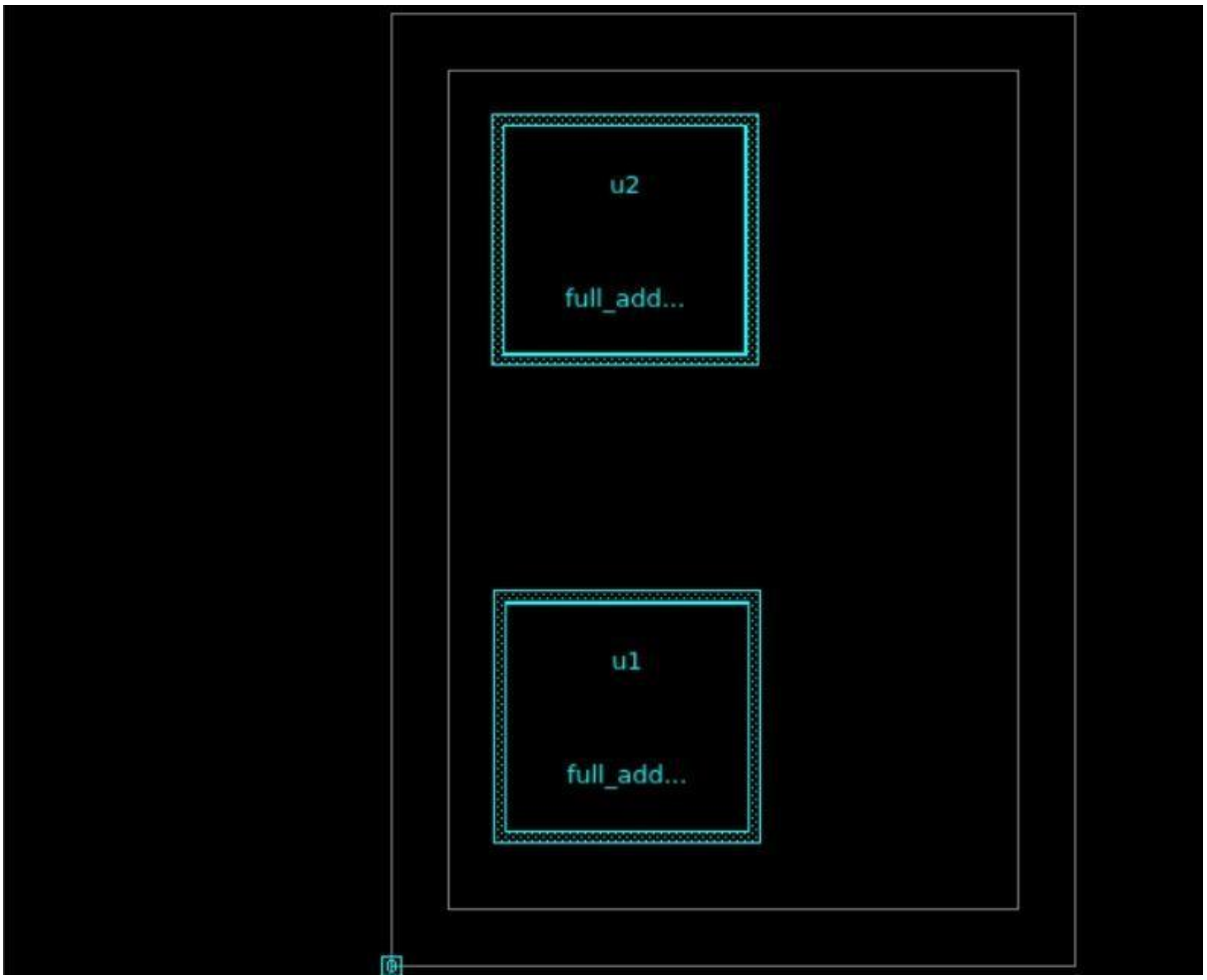
get_attribute [get_cells *] is_fixed



Soft_macros placement

create_keepout_margin u1 -outer {1 1 1 1} -type hard

create_keepout_margin u2 -outer {1 1 1 1} -type hardf



Keep_out margins

create_port -direction in VDD

create_port -direction in VSS

create_net -power VDD

create_net -ground VSS

place_pins -self

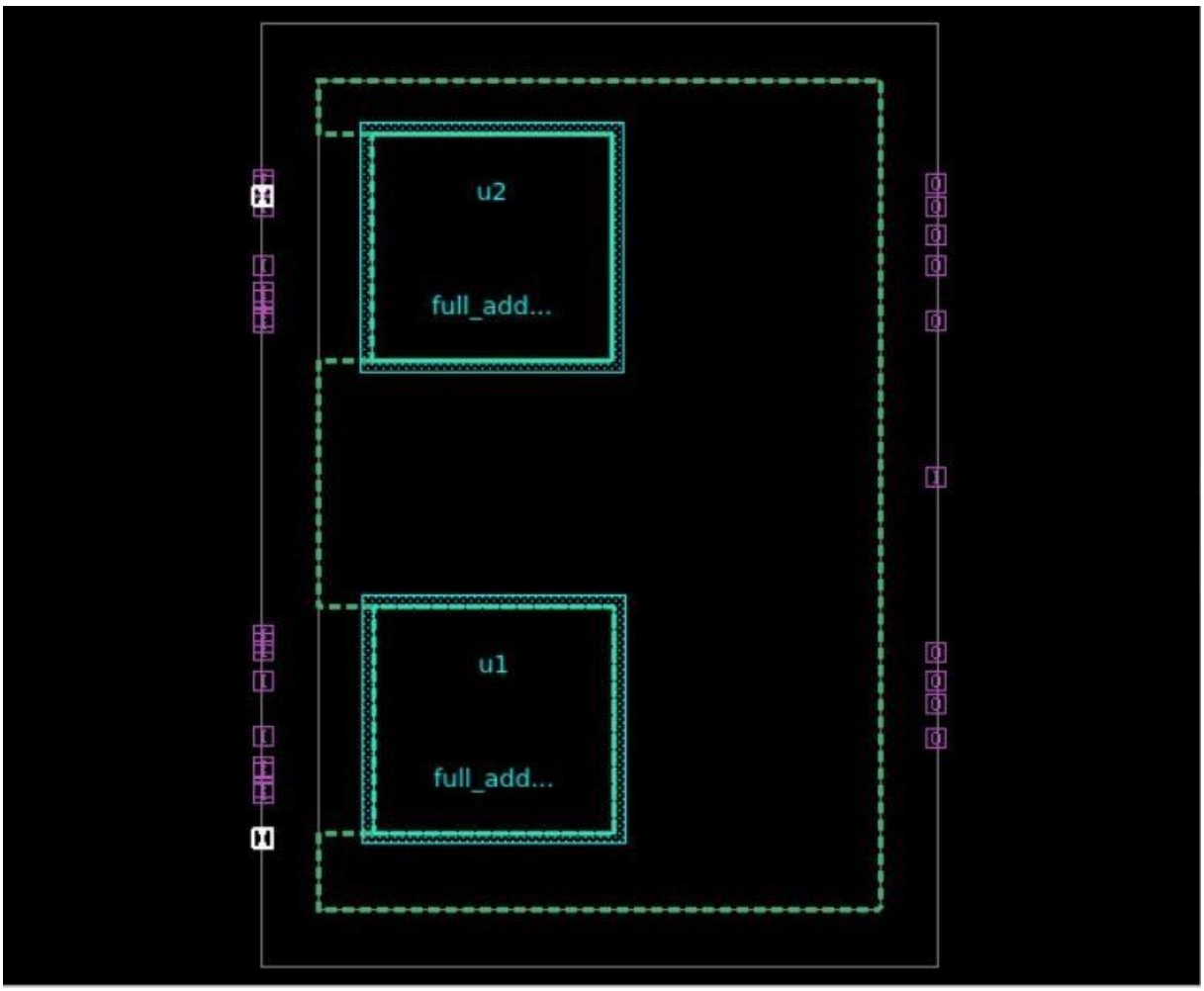
save_lib

save_block -as floorplan

create_pg_region pg_0 -block u1

create_pg_region pg_1 -block u2

create_pg_region C1 -core -exclude_regions "pg_0 pg_1"



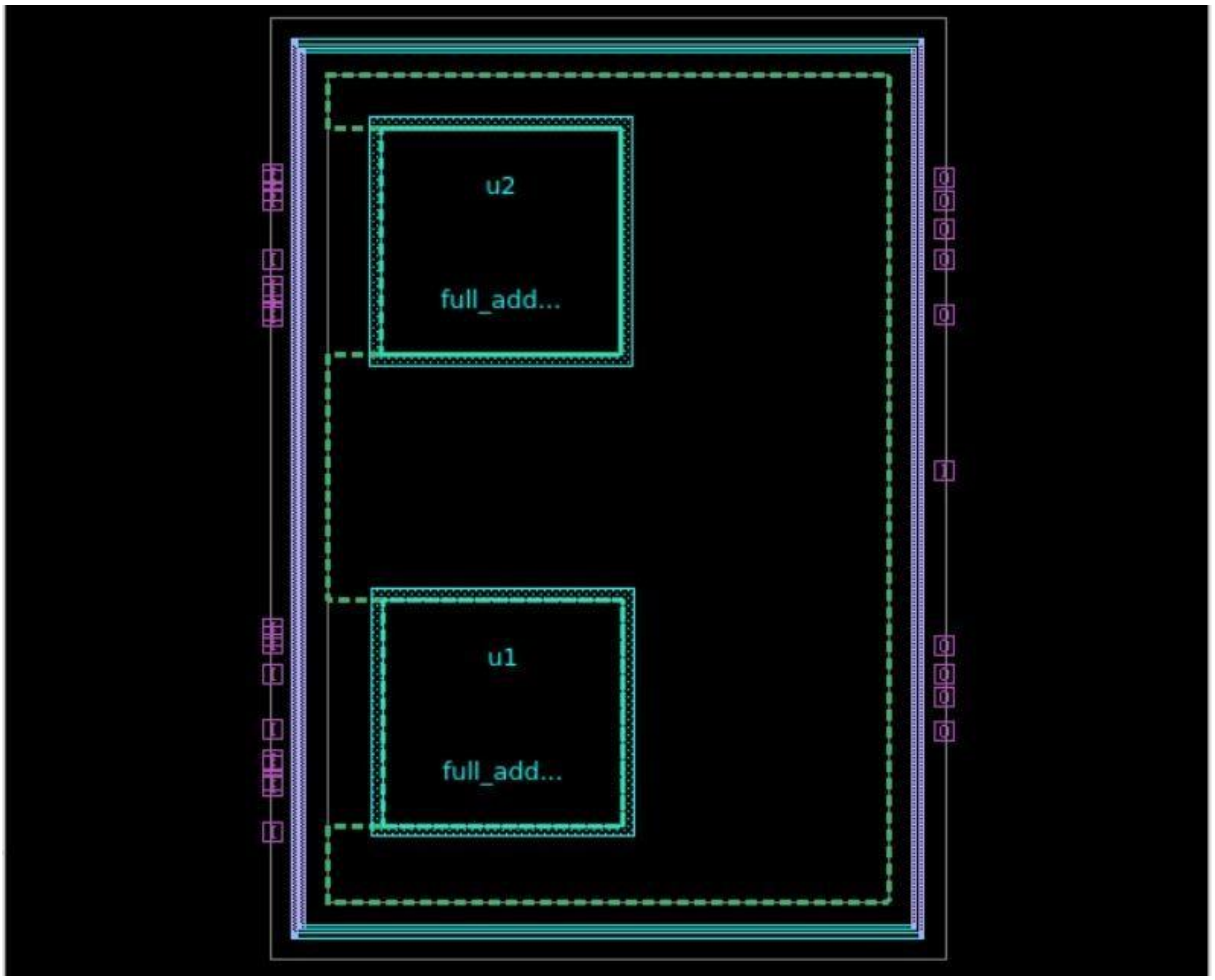
connect_pg_net -automatic -pg -all_blocks

create_pg_ring_pattern core_ring_pattern -horizontal_layer M9 -horizontal_width 0.4 -horizontal_spacing 0.7 -vertical_layer M8 -vertical_width 0.4 -vertical_spacing 0.7

set_pg_strategy core_power_ring -core -pattern {{name:core_ring_pattern} {nets:{VDD VSS}} {offset: {1.5 1.5}}}

compile_pg -strategies core_power_ring

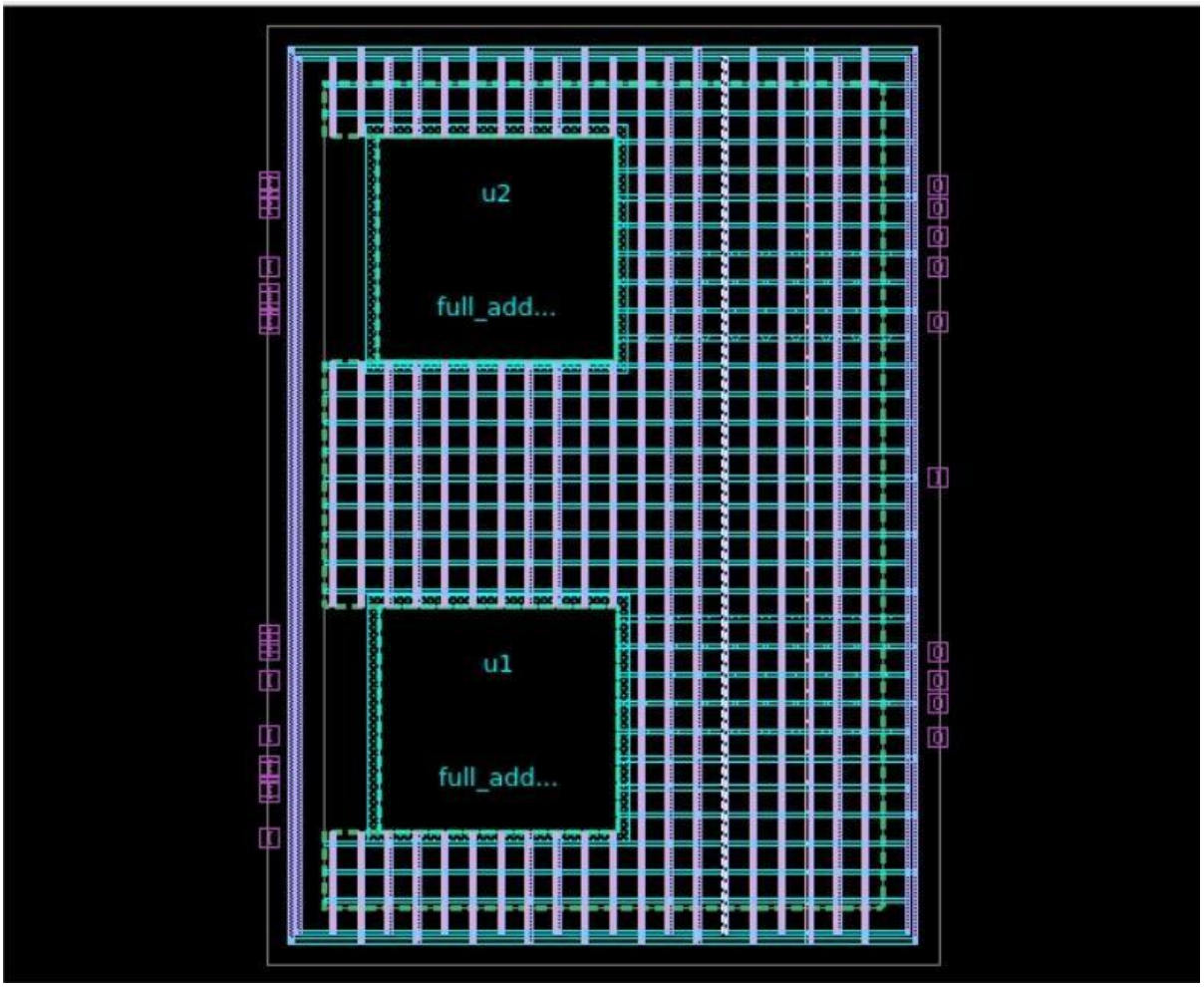
POWERPLAN :



create_pg_mesh_pattern mesh -layers {{{vertical_layer: M6} {width: 0.4} {spacing: interleaving} {pitch: 2} {offset: 1}} {{horizontal_layer: M7} {width: 0.4} {spacing: interleaving} {pitch: 2} {offset: 1}}}

set_pg_strategy core_mesh -pattern {{name: mesh} {nets: VDD VSS}} -pg_regions C1 -pattern { {pattern:mesh} {nets: VDD VSS}} -extension {{{side: 234} {direction: T B R}{stop: innermost_ring}}}

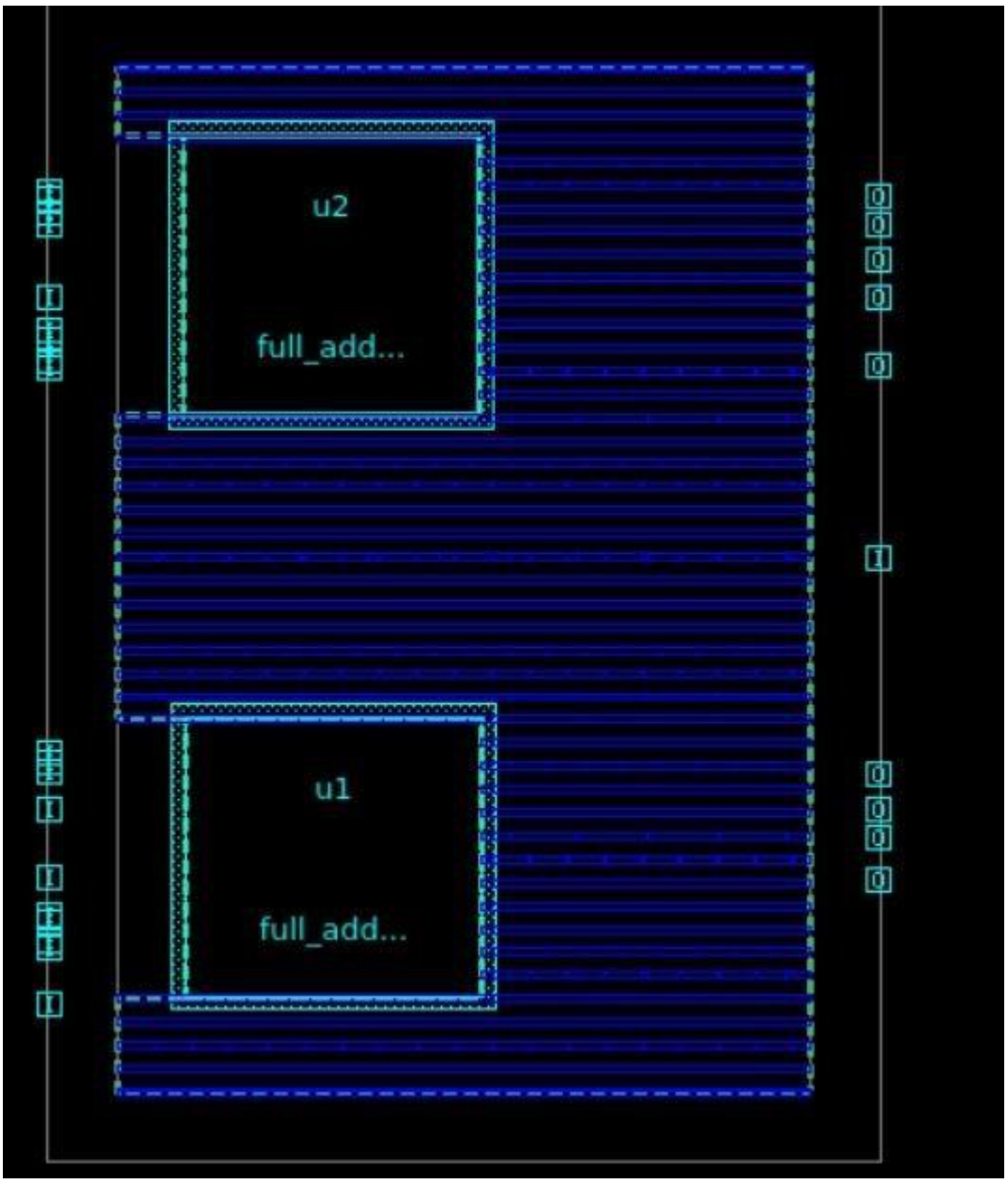
compile_pg -strategies core_mesh



create_pg_std_cell_conn_pattern std_cell_rail -layers M1 -rail_width 0.5

set_pg_strategy rail_strategy -pg_regions C1 -pattern {{name: std_cell_rail} {nets: VDD VSS}}

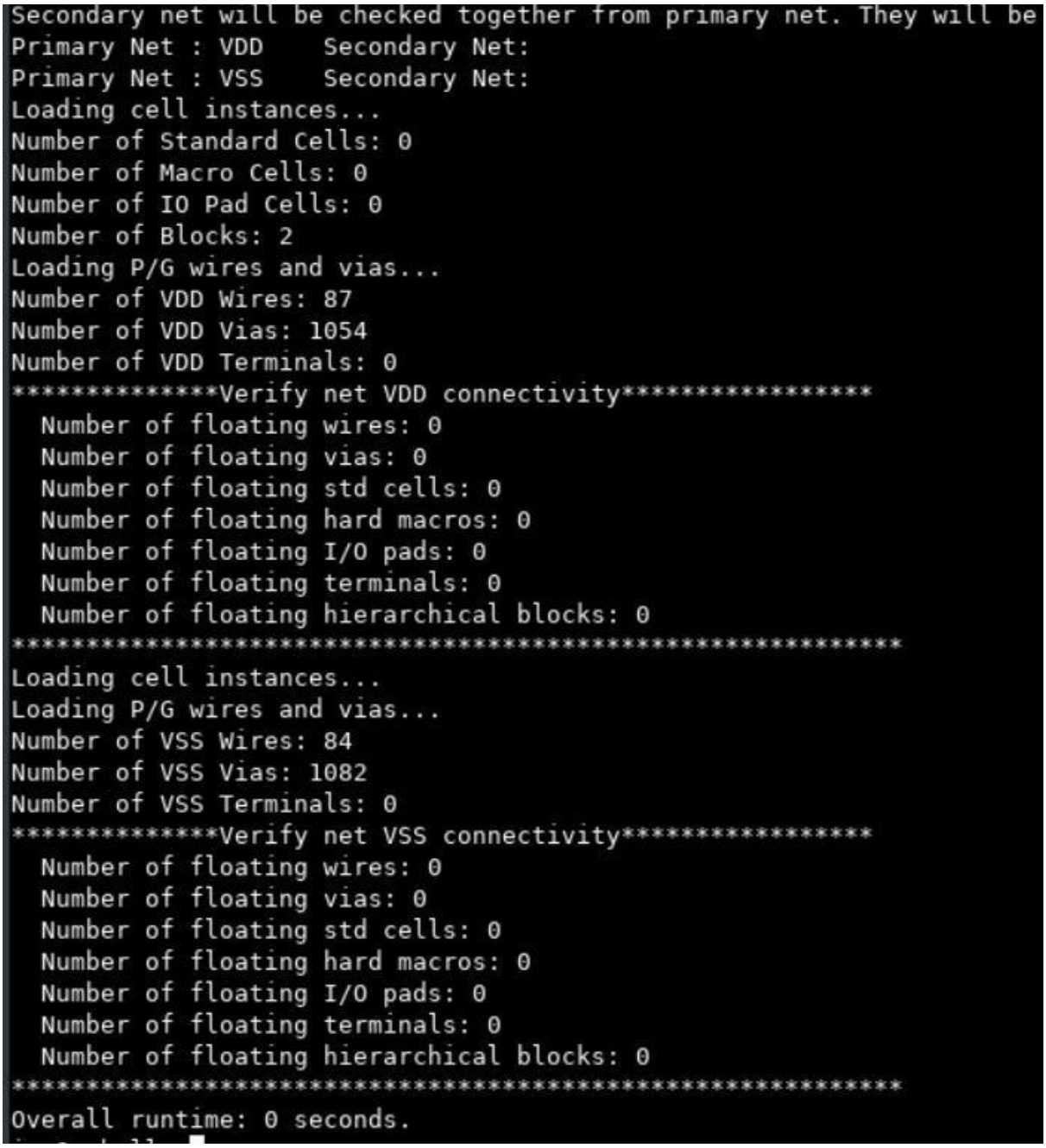
compile_pg -strategies rail_strategy



check_pg_drc

```
icc2_shell> check_pg_drc
Command check_pg_drc started  at Fri Apr 11 18:44:17 2025
Command check_pg_drc finished at Fri Apr 11 18:44:17 2025
CPU usage for check_pg_drc: 0.07 seconds ( 0.00 hours)
Elapsed time for check_pg_drc: 0.07 seconds ( 0.00 hours)
No errors found.
```

Check_pg_connectivity



PLACEMENT :

set PDK_PATH /data/pdk/pdk32nm/SAED32_EDK

read_sdc ./../Constraints/full_adder.sdc

set_app_options -name place.coarse.continue_on_missing_scandef -value true

set_app_options -name place_opt.flow.enable_ccd -value true

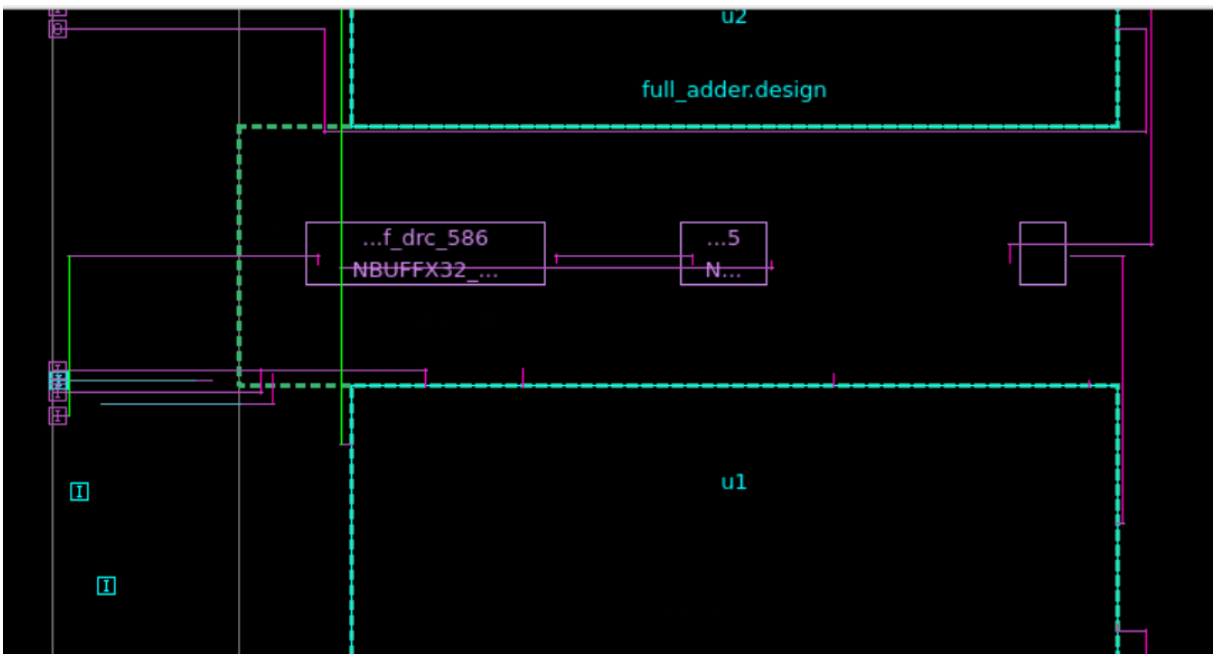
set_app_options -name place_opt.flow.clock_aware_placement -value true

```
set_app_options -name place_opt.place.congestion_effort -value high

set mode1 "func"

set corner1 "slow"

set scenario1 "${mode1}_${corner1}"

create_mode $mode1

create_corner $corner1

create_scenario -name $scenario1 -mode $mode1 -corner $corner1

set parasitics "p1"

read_parasitic_tech -tlup
"/data/pdk/pdk32nm/SAED32_EDK/tech/star_rcxt/saed32nm_1p9m_Cmax.tlu
plus" -layermap
"/data/pdk/pdk32nm/SAED32_EDK/tech/star_rcxt/saed32nm_tf_itf_tluplus.ma
p" -name p1

set_eary_data_check_policy -checks hier.block.missing_frame_view -policy
tolerate

create_placement -effort high

set_parasitic_parameters -late_spec $parasitics -early_spec $parasitics

set_dont_use [get_lib_cells /*FADD*]

set_dont_use [get_lib_cells /*HADD*]

set_dont_use [get_lib_cells /*NAND*]

set_dont_use [get_lib_cells /*OR*]

set_scenario_status func_slow -hold true -setup true -leakage_power true -
max_capacitance true -min_capacitance true -dynamic_power true -
max_transition true -active true

place_opt
```

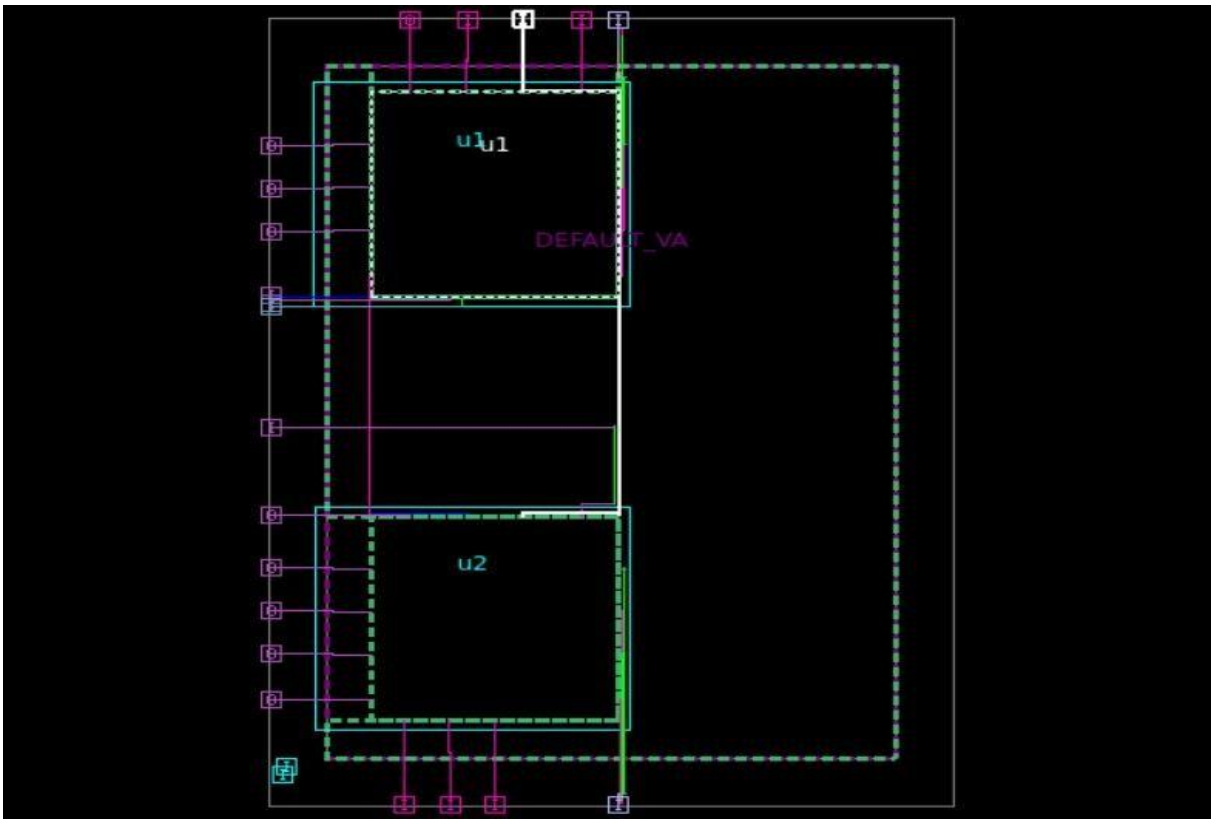
CTS :

synthesize_clock_trees

clock_opt

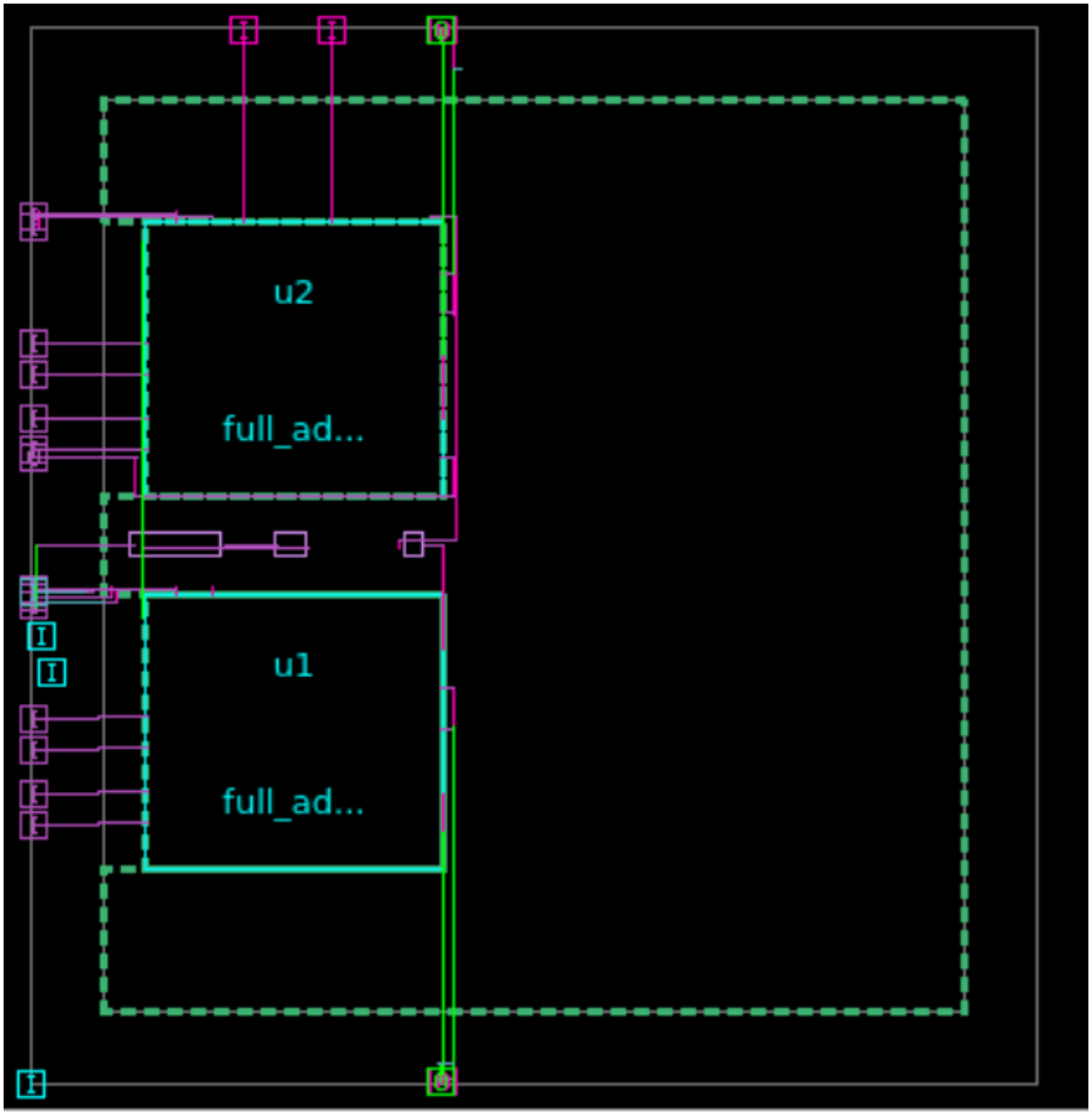


Clock buffers are added in cts



Signal route(virtual and clock buffers are not visible because I switched off standard cells in gui mode)

ROUTING:



All port nets connected to respective pins

```
Information: The command 'report_congestion' cleared the undo his
****************************************
Report : congestion
Design : eight_bit_full_adder
Version: V-2023.12-SP4
Date   : Fri Apr 11 19:37:47 2025
****************************************

Layer      |    overflow     |              # GRCs has
Name       |  total  |  max  | overflow (%)       | max overflow
-------------------------------------------------------------------
Both Dirs |       0 |     0 |       0  ( 0.00%) |       0
H routing |       0 |     0 |       0  ( 0.00%) |       0
V routing |       0 |     0 |       0  ( 0.00%) |       0

1
```

Congestion report

```
Startpoint: u2/SUM_reg[0] (rising edge-triggered flip-flop clocked by Clock)
Endpoint: SUM[4] (output port clocked by Clock)
Mode: func
Corner: slow
Scenario: func_slow
Path Group: **reg2out_default**
Path Type: max

Point                                              Incr      Path
-----------------------------------------------------------------------
clock Clock (rise edge)                           0.00      0.00
clock network delay (propagated)                  0.09      0.09

u2/SUM_reg[0]/CLK (DFFX1_RVT)                     0.00      0.09 r
u2/SUM_reg[0]/Q (DFFX1_RVT)                       0.10      0.18 f
SUM[4] (out)                                      0.00      0.18 f
data arrival time                                           0.18

clock Clock (rise edge)                           1.00      1.00
clock network delay (propagated)                  0.00      1.00
clock uncertainty                                -0.30      0.70
output external delay                            -0.50      0.20
data required time                                          0.20
-----------------------------------------------------------------------
data required time                                          0.20
data arrival time                                          -0.18
-----------------------------------------------------------------------
slack (MET)                                                 0.02
```

Final setup

```
Endpoint: u1/SUM_reg[0] (rising edge-triggered flip-flop clocked by Clock)
Mode: func
Corner: slow
Scenario: func_slow
Path Group: Clock
Path Type: min

Point                                          Incr      Path
-----------------------------------------------------------------------
clock Clock (rise edge)                        0.00      0.00
clock network delay (propagated)               0.08      0.08

u1/c_in_reg/CLK (DFFX1_RVT)                    0.00      0.08 r
u1/c_in_reg/QN (DFFX1_RVT)                     0.07      0.16 f
u1/U38/Y (XNOR3X1_RVT)                         0.03      0.19 f
u1/SUM_reg[0]/D (DFFX1_RVT)                    0.00      0.19 f
data arrival time                                        0.19

clock Clock (rise edge)                        0.00      0.00
clock network delay (propagated)               0.09      0.09
u1/SUM_reg[0]/CLK (DFFX1_RVT)                  0.00      0.09 r
clock uncertainty                              0.10      0.19
library hold time                             -0.00      0.18
data required time                                       0.18
-----------------------------------------------------------------------
data required time                                       0.18
data arrival time                                       -0.19
-----------------------------------------------------------------------
slack (MET)                                              0.01
```

Final hold slack

4 Report and Analysis :

In this project, a hierarchical physical design and synthesis flow was implemented for an 8-bit full adder using two 4-bit full adders. The process began with RTL synthesis of the 4-bit full adder in **Design Compiler (DC)**. The design was synthesized using a 32nm SAED standard cell library (`saed32rvt_tt_1p0v_25c.lib`), targeting a clock period of **1ns** with input and output delays set to **50% of the clock period**. The synthesized netlist revealed **46 total leaf cells**, including **32 combinational cells**, **14 sequential cells**, and **2 buffer cells**. The mapped design achieved a **maximum setup slack of 0.11ns** and a **hold slack of 0.01ns**, indicating good timing closure. The area report showed a **total cell area of 187.61 µm²**, with **combinational area** of **88.95 µm²**, **non-combinational area** of **98.6 µm²**, and **buffer area** of **4.06 µm²**. No violations were found in max transition or max capacitance, and the total number of nets was **68**. The technology-mapped netlist and the SDC constraints were then exported for further physical implementation.

Using **ICC2**, the mapped 4-bit full adder netlist was imported for floorplanning and physical design. The flow began by defining library paths and creating a block and library (`FA_LIB`). The design was floorplanned with a core offset of 2.5 units. Power and ground ports (VDD, VSS) were created and connected using rings, mesh, and rail-based power strategies. A combination of **M4, M6, M7, and M8 layers** were used for PG routing with carefully defined patterns. After creating the power grid and running DRC and connectivity checks, the floorplanned design was saved. Placement was optimized with **clock-aware and congestion-driven placement options**, and a scenario (`func_slow`) was created using the slow corner and parasitic extraction (`tluplus`) models for SAED 32nm technology. Post-placement timing was validated using the same SDC constraints from DC. Clock tree synthesis was performed, followed by optimization and post-CTS hold timing analysis. The design was then routed with timing- and crosstalk-driven options enabled, along with antenna rule compliance using diode insertion. Post-route reports including **timing, congestion, and DRC** confirmed a successful layout. The design outputs included a **routed netlist**, **LEF**, and **SPEF** file.

For library modeling, **PrimeTime** was used to load the routed netlist and extracted parasitics (SPEF), followed by timing report generation and **library extraction** in `.lib` format. This `.lib` file was then converted to a `.db` using **Library Compiler**, enabling its inclusion in downstream synthesis flows as a macro cell. This `.db` of the 4-bit full adder was later linked in the **common.tcl** of the RM flow.

The final stage involved performing **RTL-to-GDSII flow for the 8-bit full adder**, using the previously generated `.db` file as a hierarchical block. RTL synthesis was conducted in DC with the 8-bit adder Verilog code using hierarchical mapping enabled. Specific cells like `FADD`, `HADD`, `INV`, `NAND`, and `OR` gates were set as `dont_use` to force reuse of the hierarchical macro. Post-synthesis netlist and SDC were passed to ICC2 for floorplanning, placement, clock tree synthesis, and routing. The `.ndm` file for the full adder macro was included in the ICC2 database to support macro-aware physical design.

Overall, the hierarchical design methodology resulted in efficient area utilization, clean timing closure, and successful integration of custom IP blocks using Synopsys tools, showcasing an end-to-end digital implementation of an 8-bit full adder using industry-standard flows.

4 Challenges Faced :

Physical Design Debugging Experience – 8-bit and 4-bit Full Adder

1. **Short Violations**
   - Faced short violations during physical design.
   - Couldn't clear all, but minimized them significantly through optimization and refinement in routing stages.
2. **Metal1 (M1) Spacing Issues**
   - Encountered minimum spacing violations in M1 layer.
   - Resolved by adjusting routing constraints and ensuring minimum design rules were met.
3. **M6 Via Drop Issue in Power Mesh**
   - In the power mesh, vias were not dropping properly on the M6 layer.
   - Resolved by increasing the width of the M6 layer in the power mesh to meet via enclosure rules.
4. **M8 Via Missing in Core Power Ring**
   - A via was not getting dropped in the core power ring on M8.
   - Fixed the issue by increasing the M8 layer width to meet DRC and enclosure constraints.
5. **Floating Straps in M7**
   - Observed some floating nets on M7 straps during power planning.
   - Resolved by maintaining proper pitch and connectivity across straps to eliminate floating segments.
6. **Clock Tree Synthesis Failure in Hierarchical 8-bit Full Adder**
   - Clock tree synthesis (CTS) couldn't proceed due to a max transition violation on the clock path at the top level.
   - Solved by relaxing the max transition constraint, allowing CTS to complete successfully.
7. **Clock Routing Rule and NDR Handling**
   - Faced difficulty with clock net routing due to undefined NDR rules.
   - Set clock routing rules to follow **default NDR**, which enabled successful clock tree build and clean routing.
8. **Routing Completion Post-CTS**
   - After resolving CTS and clock routing issues, proceeded with signal routing for the complete design.
   - Ensured DRC clean routing with optimized wirelength and minimal congestion.

6 . Conclusion :

Through this project, I developed problem-solving and debugging skills by analyzing reports, identifying physical design issues, and applying effective solutions. I gained hands-on experience in resolving short violations, spacing issues, via drops, floating nets, congestion, and clock tree synthesis challenges.

This helped me build a solid understanding of the full physical design flow, enhanced my ability to read and interpret tool reports, and strengthened my practical knowledge of optimization in different design scenarios.