

RTL-GDS II IMPLEMENTATION OF HIERARCHAL Mini -ALU DESIGN

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1. Introduction

This project focuses on the **complete RTL-to-GDSII implementation** of a **hierarchical ALU (Arithmetic Logic Unit)** design using Synopsys industry tools. The ALU performs a combination of arithmetic and logic operations and is implemented using hierarchical design principles.

The flow follows the ASIC implementation cycle:

- RTL Design using **Verilog**.
- Functional Simulation using **VCS & Verdi**
- Logic Synthesis via **Design Compiler**
- Physical Design through **ICC2**
- Final layout and **GDSII generation**

This work was conducted under the guidance of “VLSI Expert Institute”, where extensive hands-on experience was gained in tool flows and digital design implementation.

2. RTL Design

2.1 Hierarchical Architecture

The ALU is designed using a hierarchical approach. The top module `hybrid_alu` instantiates a reusable `full_adder` block for implementing arithmetic operations such as addition, subtraction, increment, and decrement.

2.2 Functional Blocks

- **Arithmetic Unit:** Performs $A+B$, $A-B$, $A+1$, $A-1$ using instances of `full_adder`.
- **Logic Unit:** Computes $A \text{ AND } B$, $A \text{ OR } B$, $A \text{ XOR } B$, $\text{NOT } A$, shift operations.
- **Control Unit:** Selects output based on 3-bit `ALU_Sel` signal.
- **Clocked Design:** All outputs are clock-synchronized, making it synthesis-friendly.

2.3 RTL CODE :

Top_module :

```
module hybrid_alu (
    input [3:0] A, B,
    input Clock,
    input [2:0] ALU_Sel, // Selects which output to drive
    output reg [3:0] Result,
    output reg C_out
);
```

```
wire [3:0] sum_add, sum_sub, sum_inc, sum_dec;
wire c_add, c_sub, c_inc, c_dec;
```

// Soft macro: A + B

```
full_adder FA_add (
    .A(A),
    .B(B),
    .Clock(Clock),
    .C_in(1'b0),
    .SUM(sum_add),
    .C_out(c_add)
);
```

// Soft macro: A - B = A + (\sim B + 1)

```
full_adder FA_sub (
    .A(A),
    .B( $\sim$ B),
    .Clock(Clock),
    .C_in(1'b1),
    .SUM(sum_sub),
    .C_out(c_sub)
);
```

// Soft macro: A + 1

```
full_adder FA_inc (
    .A(A),
    .B(4'b0000),
    .Clock(Clock),
    .C_in(1'b1),
    .SUM(sum_inc),
    .C_out(c_inc)
);
```

```

// Soft macro: A - 1
full_adder FA_dec (
    .A(A),
    .B(4'b1111), // -1 in 2's comp
    .Clock(Clock),
    .C_in(1'b0),
    .SUM(sum_dec),
    .C_out(c_dec)
);

// Standard cell-based logic
wire [3:0] and_op = A & B;
wire [3:0] or_op = A | B;
wire [3:0] xor_op = A ^ B;
wire [3:0] not_a = ~A;
wire [3:0] shl = A << 1; // Shift left
wire [3:0] shr = A >> 1; // Shift right

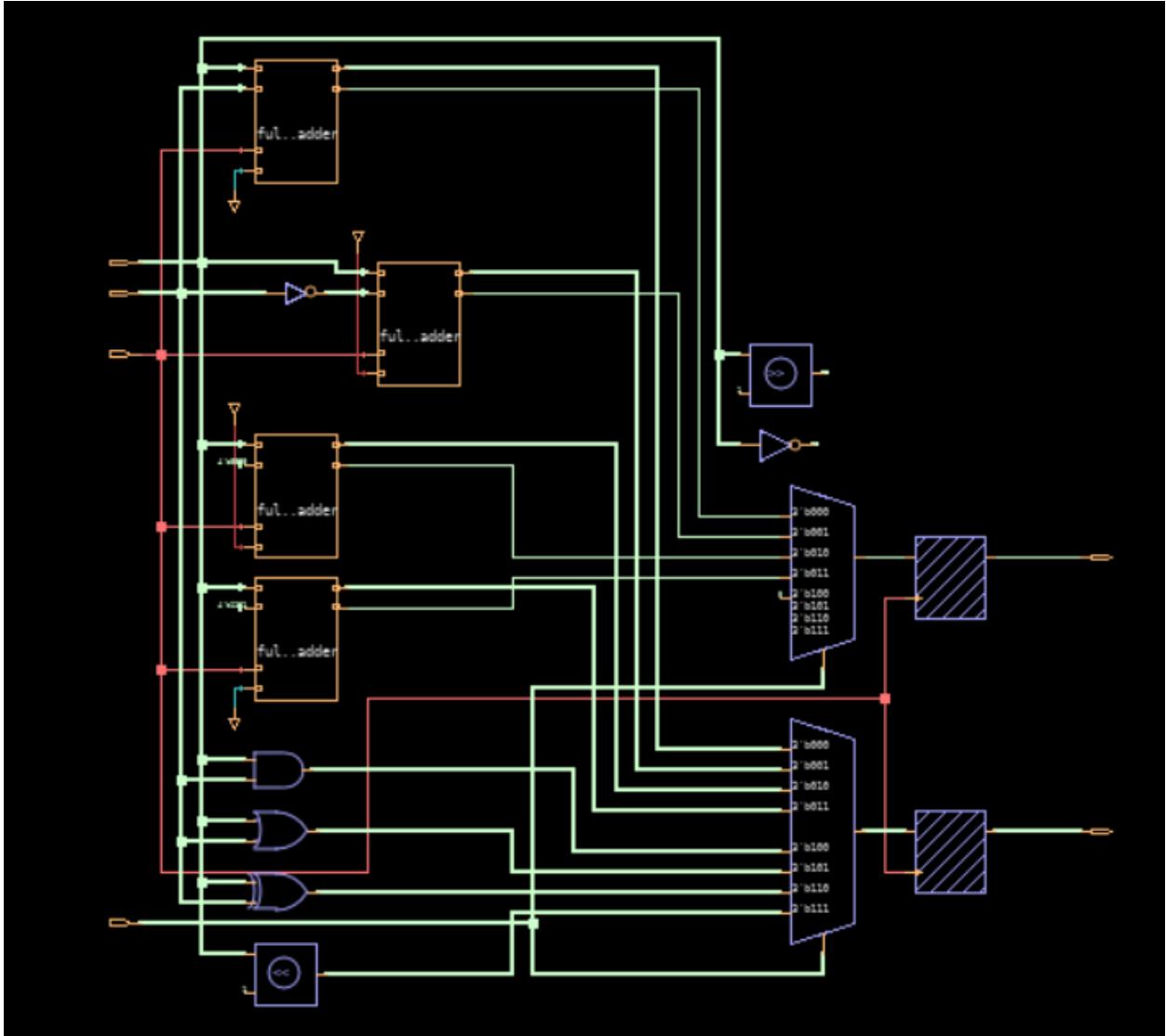
// Output selection
always @ (posedge Clock) begin
    case (ALU_Sel)
        3'b000: begin Result <= sum_add; C_out <= c_add; end // A + B
        3'b001: begin Result <= sum_sub; C_out <= c_sub; end // A - B
        3'b010: begin Result <= sum_inc; C_out <= c_inc; end // A + 1
        3'b011: begin Result <= sum_dec; C_out <= c_dec; end // A - 1
        3'b100: begin Result <= and_op; C_out <= 0; end // A AND B
        3'b101: begin Result <= or_op; C_out <= 0; end // A OR B
        3'b110: begin Result <= xor_op; C_out <= 0; end // A XOR B
        3'b111: begin Result <= shl; C_out <= 0; end // Shift A left
        // You can add more like NOT A or SHR if needed
    endcase
end

endmodule

```

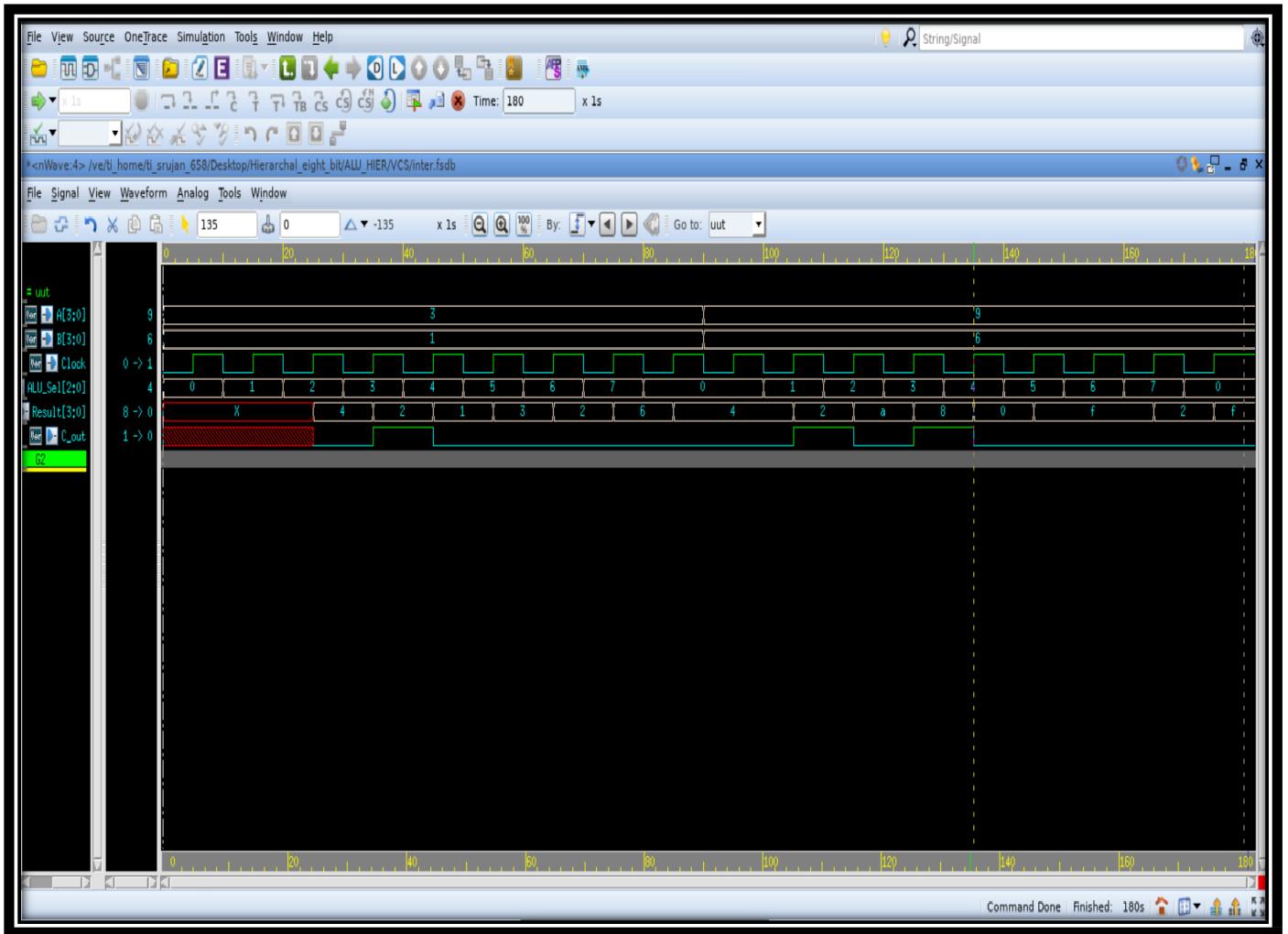
2.4 Simulation Using VCS and VERDI

Schematic :

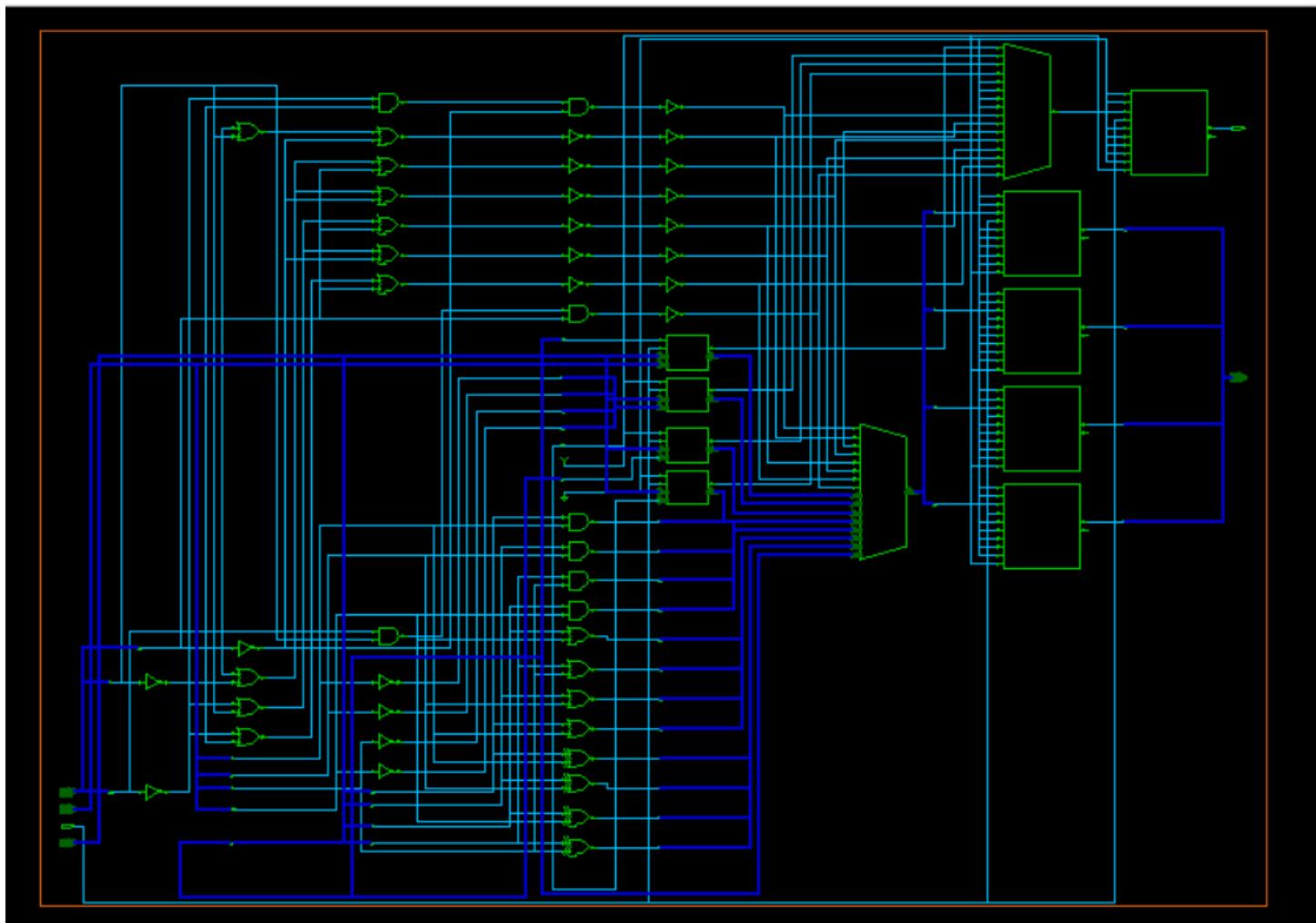


Schematic of Top module `hybrid_alu`

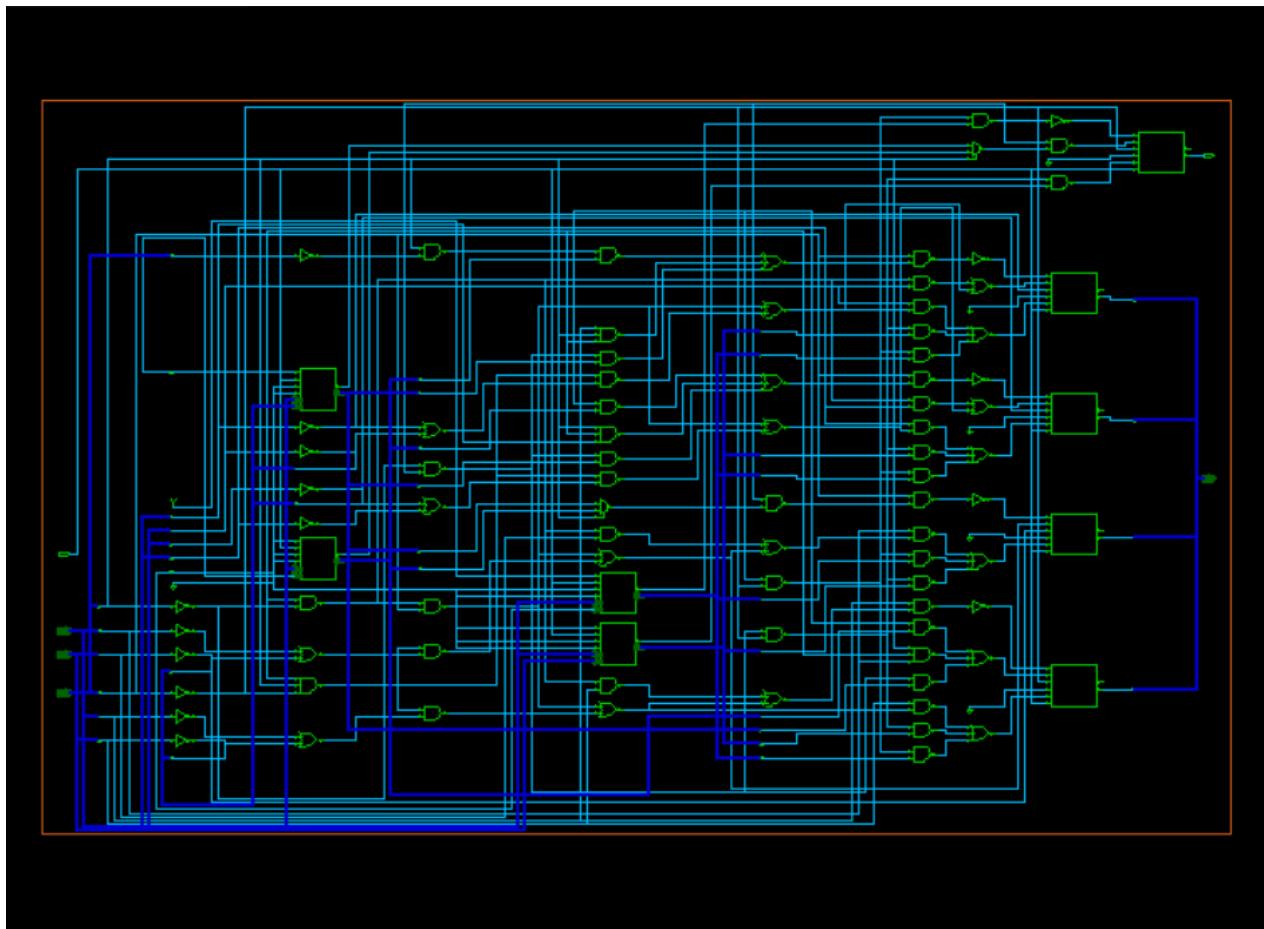
Waveform Of Simulation :



3. Synthesis :



Gtech Mapping



Actual technology mapping happens here after compile ultra

The below is the qor report of synthesis:

Timing Path Group 'clk'

Levels of Logic:	7.00
Critical Path Length:	0.64
Critical Path Slack:	1.13
Critical Path Clk Period:	3.40
Total Negative Slack:	0.00
No. of Violating Paths:	0.00
Worst Hold Violation:	0.00
Total Hold Violation:	0.00
No. of Hold Violations:	0.00

Cell Count

Hierarchical Cell Count:	0
Hierarchical Port Count:	0
Leaf Cell Count:	90
Buf/Inv Cell Count:	16
Buf Cell Count:	0
Inv Cell Count:	16
CT Buf/Inv Cell Count:	0
Combinational Cell Count:	81
Sequential Cell Count:	9
Macro Count:	4

Area

Combinational Area:	159.602438
Noncombinational Area:	44.475198
Buf/Inv Area:	20.331520
Total Buffer Area:	0.00
Total Inverter Area:	20.33
Macro/Black Box Area:	822.841919
Net Area:	42.980249

Cell Area:	1026.919555
Design Area:	1069.899804

Design Rules

Total Number of Nets:	125
Nets With Violations:	0
Max Trans Violations:	0
Max Cap Violations:	0

4. Physical Design Flow Documentation for Hierarchical Mini ALU

Objective

The purpose of this physical design script is to implement a hierarchical **Hybrid ALU** by integrating pre-placed full adders (FA_add, FA_sub, FA_inc, FA_dec) using Synopsys ICC2 tool. The script defines power planning, placement, clock tree synthesis (CTS), routing, and timing analysis.

1. Library and Design Initialization :

Commands :

```
create_lib -ref_libs "/data/pdk/pdk32nm/SAED32_EDK/lib/stdcell_rvt/ndm/saed32rvt_c.ndm  
..../FULL_ADDER/icc2/FA_LIB/lib.ndm" ALU_LIB
```

```
read_verilog ..//DC/MAPPED_HYBRID_ALU.v
```

```
link_block
```

```
start_gui
```

- The **standard cell libraries** (SAED32nm and custom FA_LIB) are loaded to form the basis of design cells.
- The **synthesized Verilog netlist** (MAPPED_HYBRID_ALU.v) is read and linked to create the initial database.

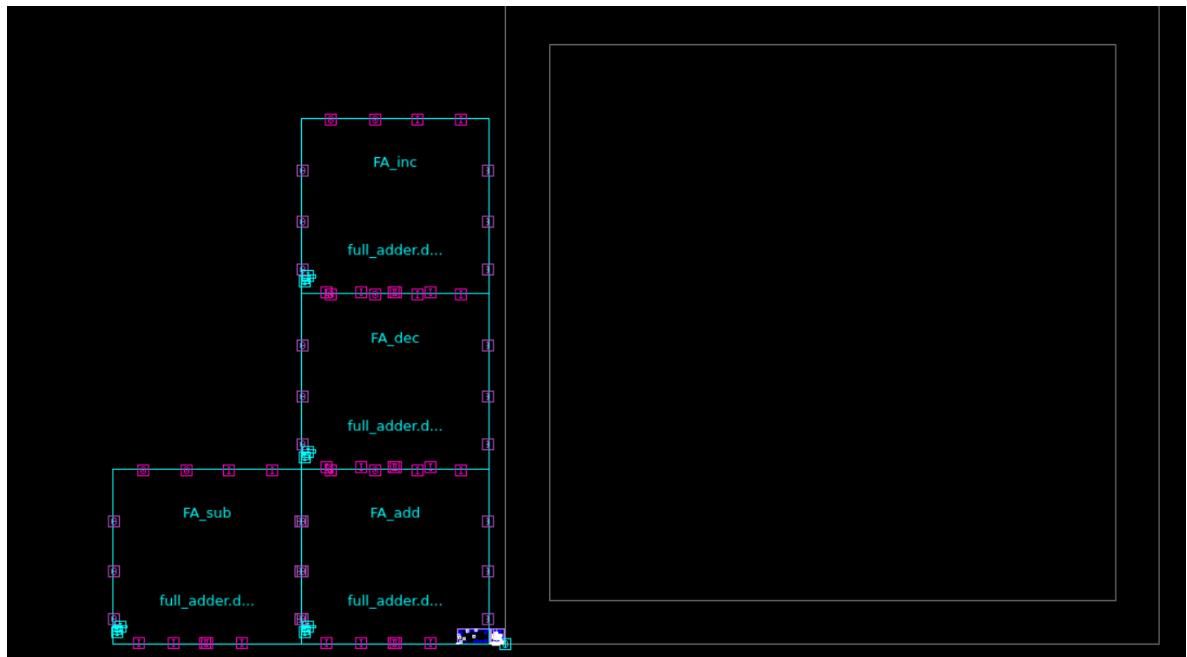
2. Floorplan and Soft Macro Placement :

```
read_tech_lef ../../FULL_ADDER/icc2/full_adder.lef
```

```
initialize_floorplan -side_length {65 65 } -core_offset 5
```

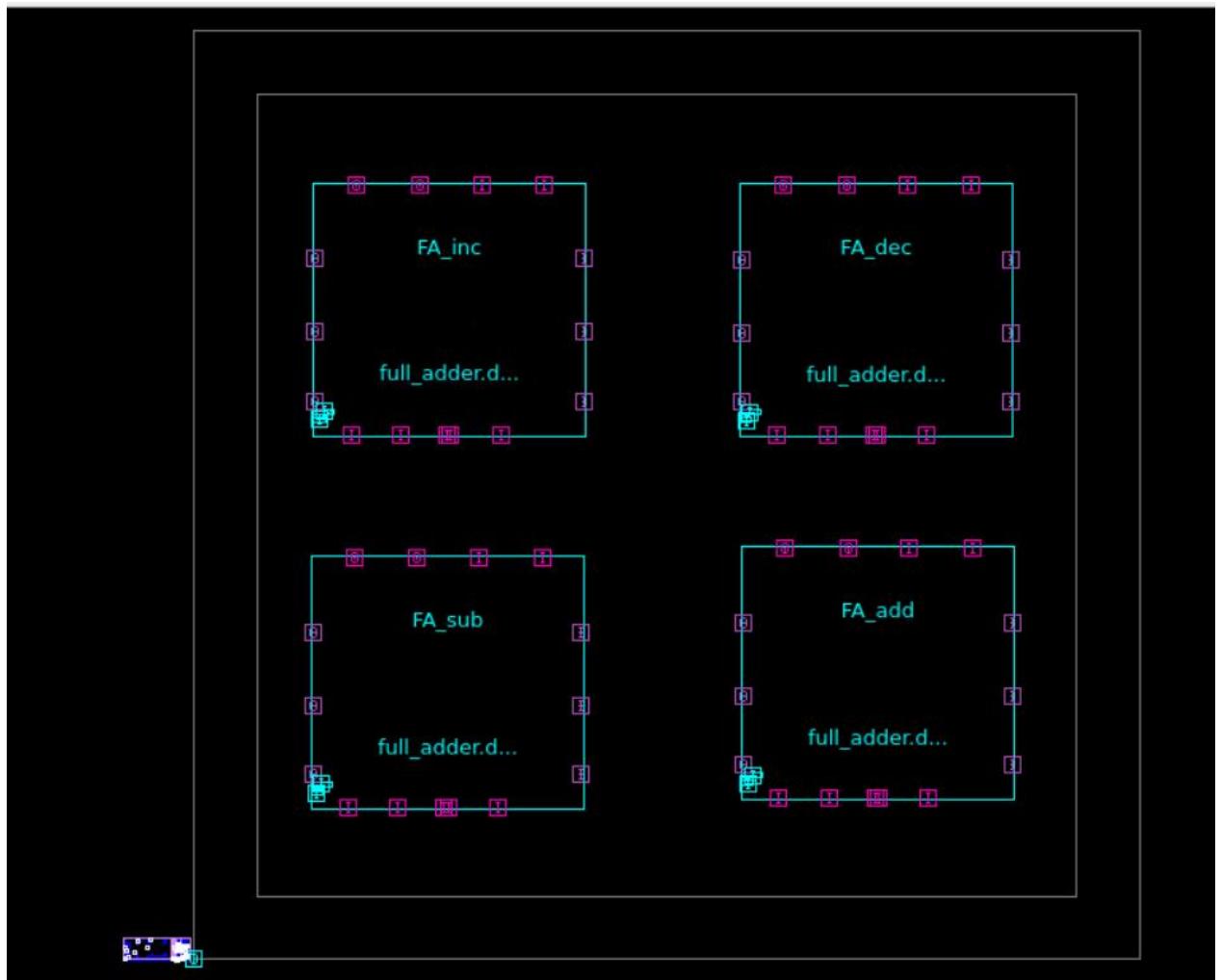
- Reads the **technology LEF** to understand cell geometries.
- The **floorplan** is initialized with core and boundary dimensions. Soft macros are manually placed , by analyzing the **flylines** and assigned **keepout margins** to prevent cell overlaps and routing congestion.

Floorplan initialization



// place four soft macros manually by carefully analyzing the flylines of macros to ports .

MACRO placement



3. Power Planning :

Commands :

```
create_keepout_margin -outer {1 1 1 1} -type hard FA_dec
create_keepout_margin -outer {1 1 1 1} -type hard FA_sub
create_keepout_margin -outer {1 1 1 1} -type hard FA_inc
create_keepout_margin -outer {1 1 1 1} -type hard FA_add
```



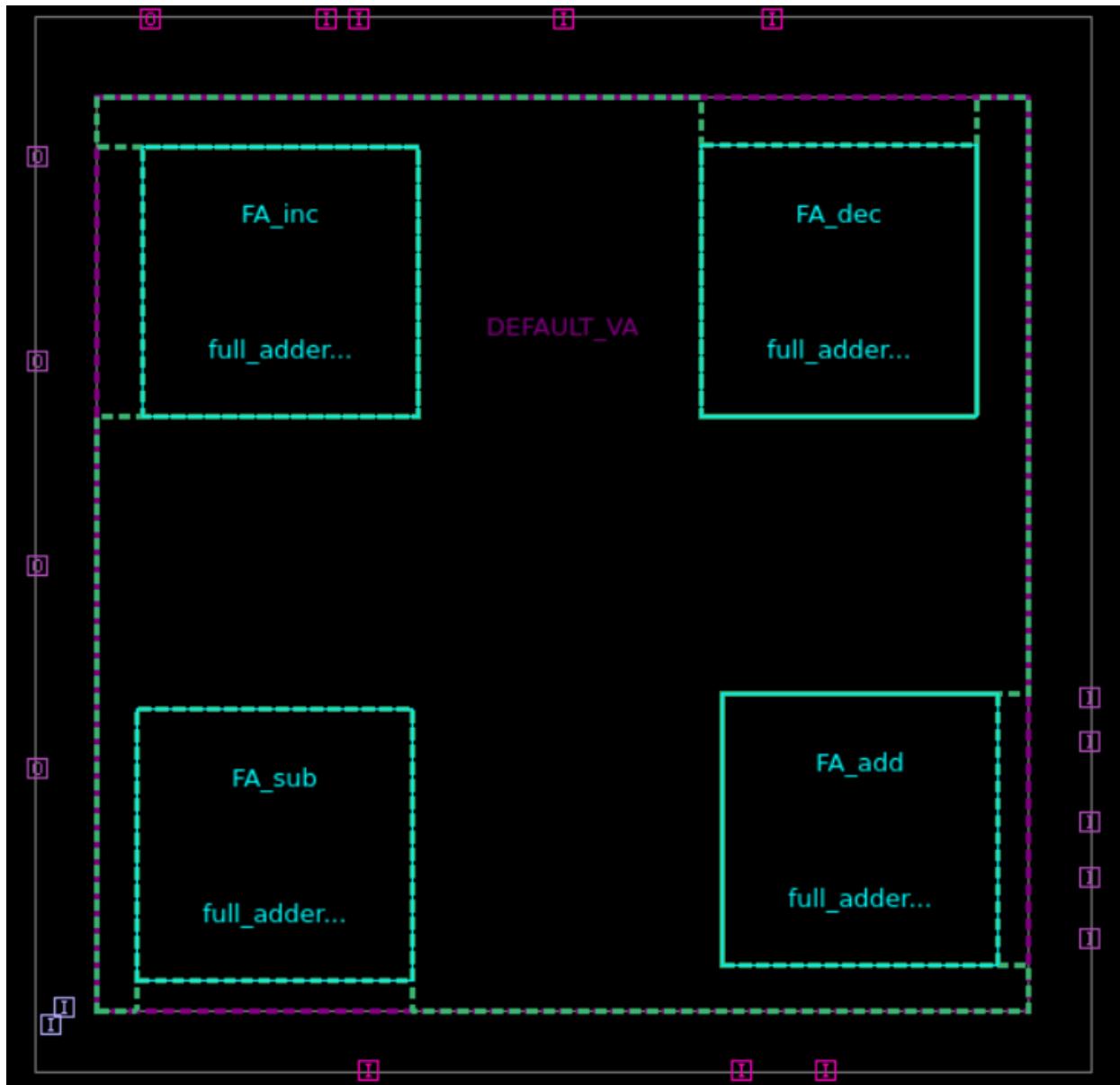
Keep-out Margin Creation around the Soft Macro

```
set_attribute -objects [get_cells "FA_add FA_sub FA_dec FA_inc"] -name physical_status -value placed
```

```

create_port -direction in VDD
create_port -direction in VSS
create_net -power VDD
create_net -ground VSS
create_pg_region pg_dec -block FA_dec
create_pg_region pg_add -block FA_add
create_pg_region pg_sub -block FA_sub
create_pg_region pg_inc -block FA_inc
create_pg_region -core ALU_CORE -exclude_regions "pg_add pg_dec pg_sub pg_inc "
place_pins -self

```

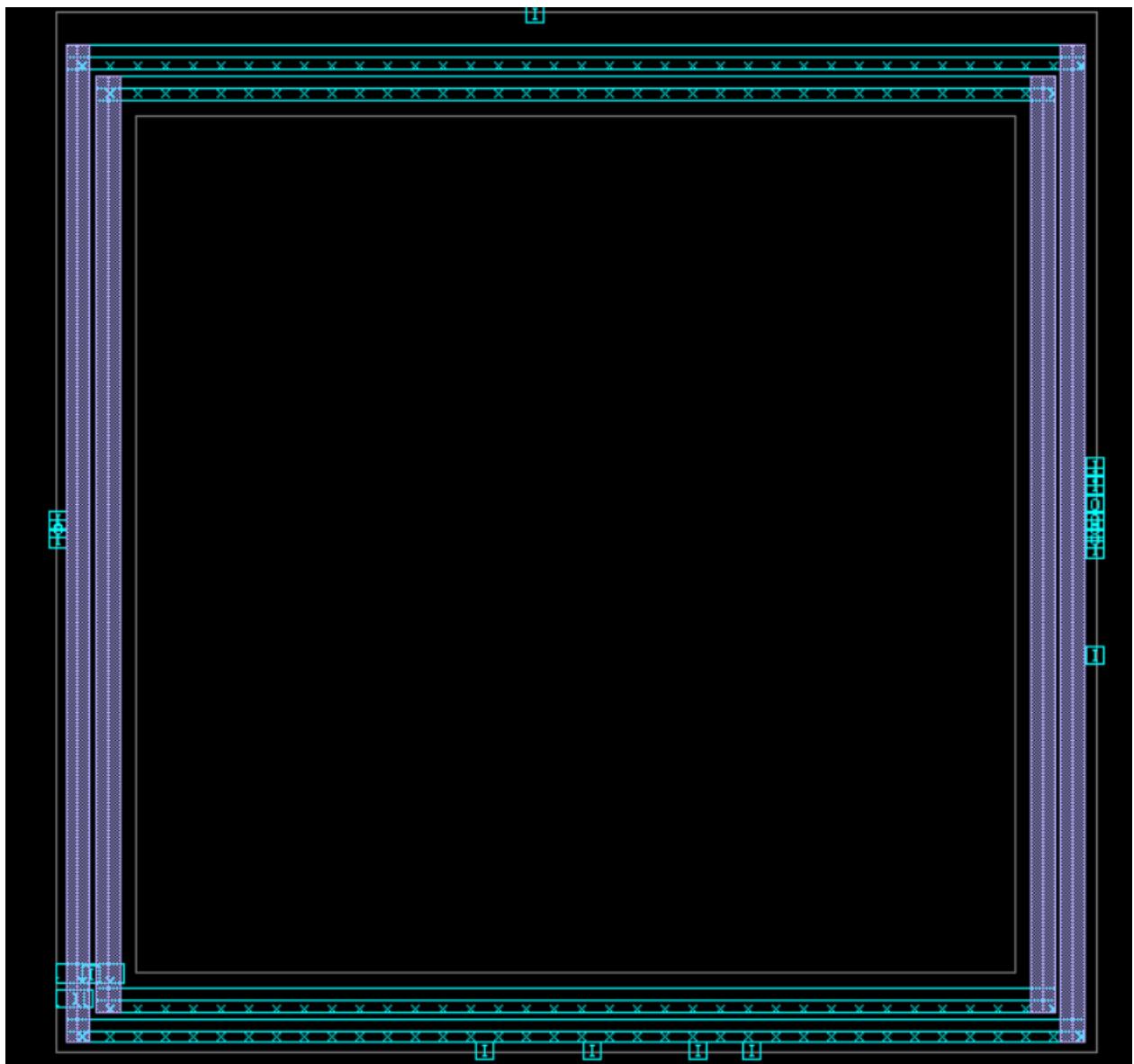


PG-Region Creation and pin-placement

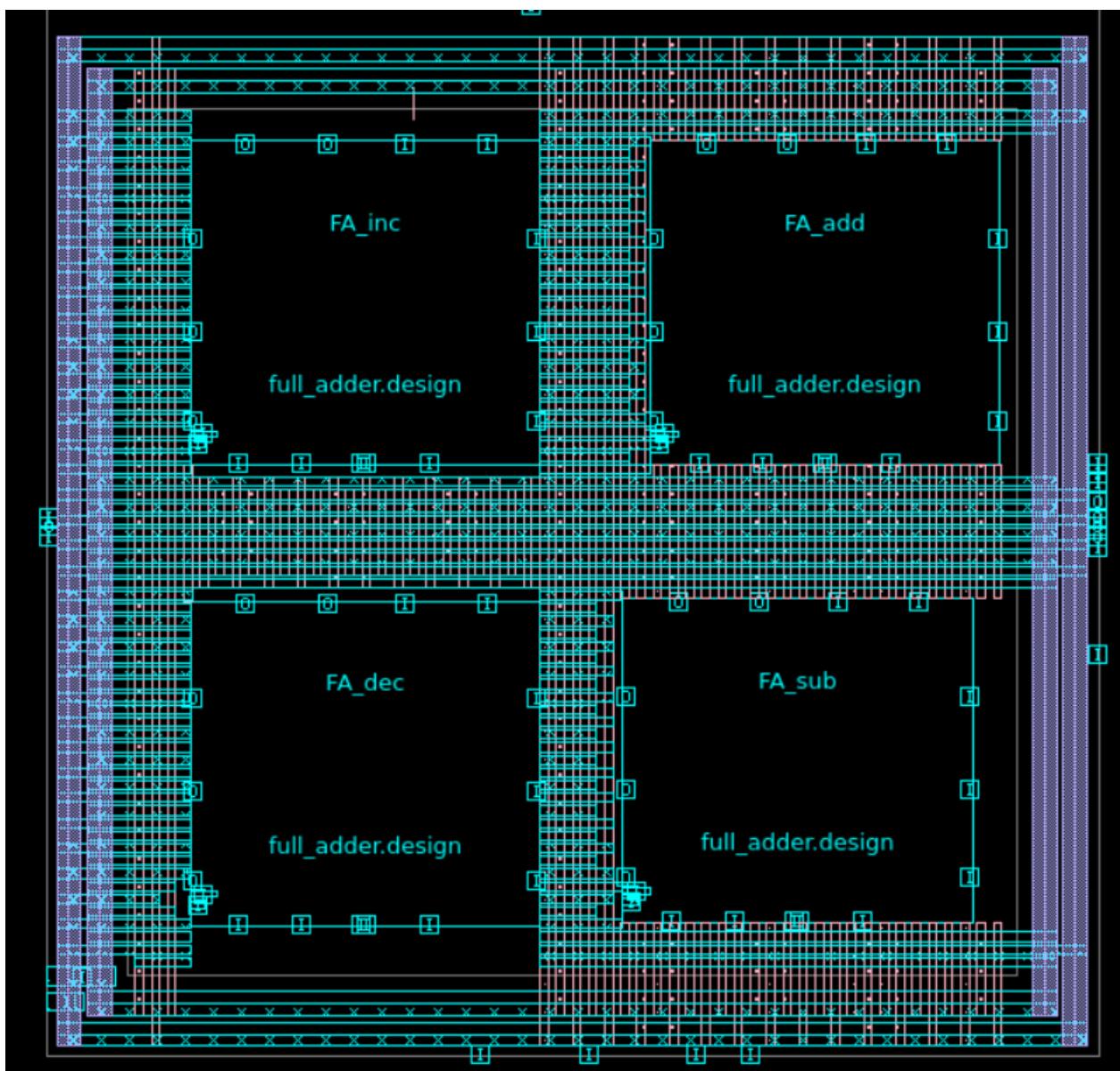
```
connect_pg_net -create_nets_only
```

```
create_pg_ring_pattern core_ring_pattern -horizontal_layer M7 -horizontal_width 1.5 -  
horizontal_spacing 0.7 -vertical_layer M8 -vertical_width 1.5 -vertical_spacing 0.7
```

```
set_pg_strategy core_power_ring -core -pattern { {name:core_ring_pattern} {nets:{VDD VSS}} }  
{offset: {0.65 0.65}}}  
compile_pg -strategies core_power_ring
```



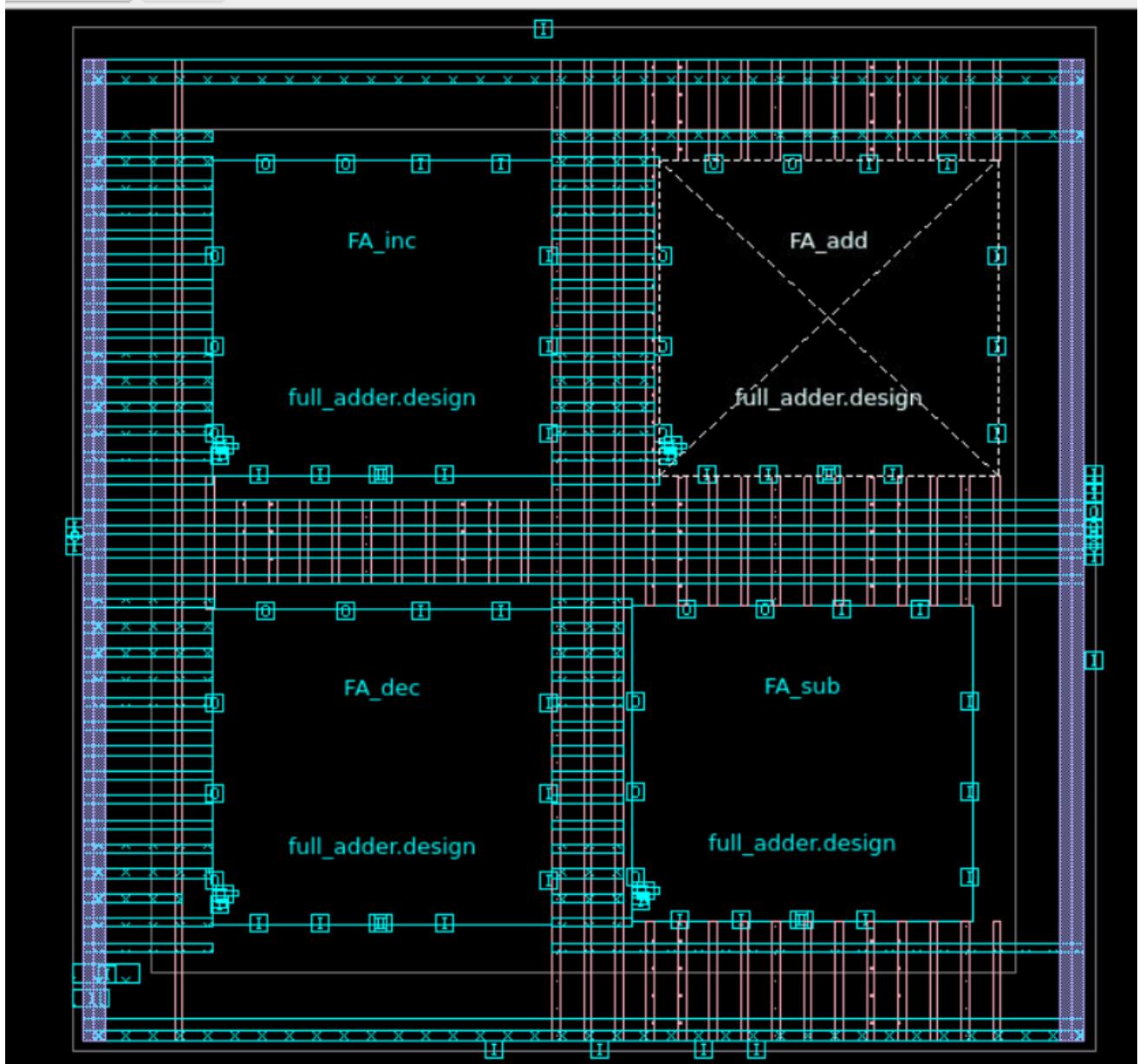
Core power ring



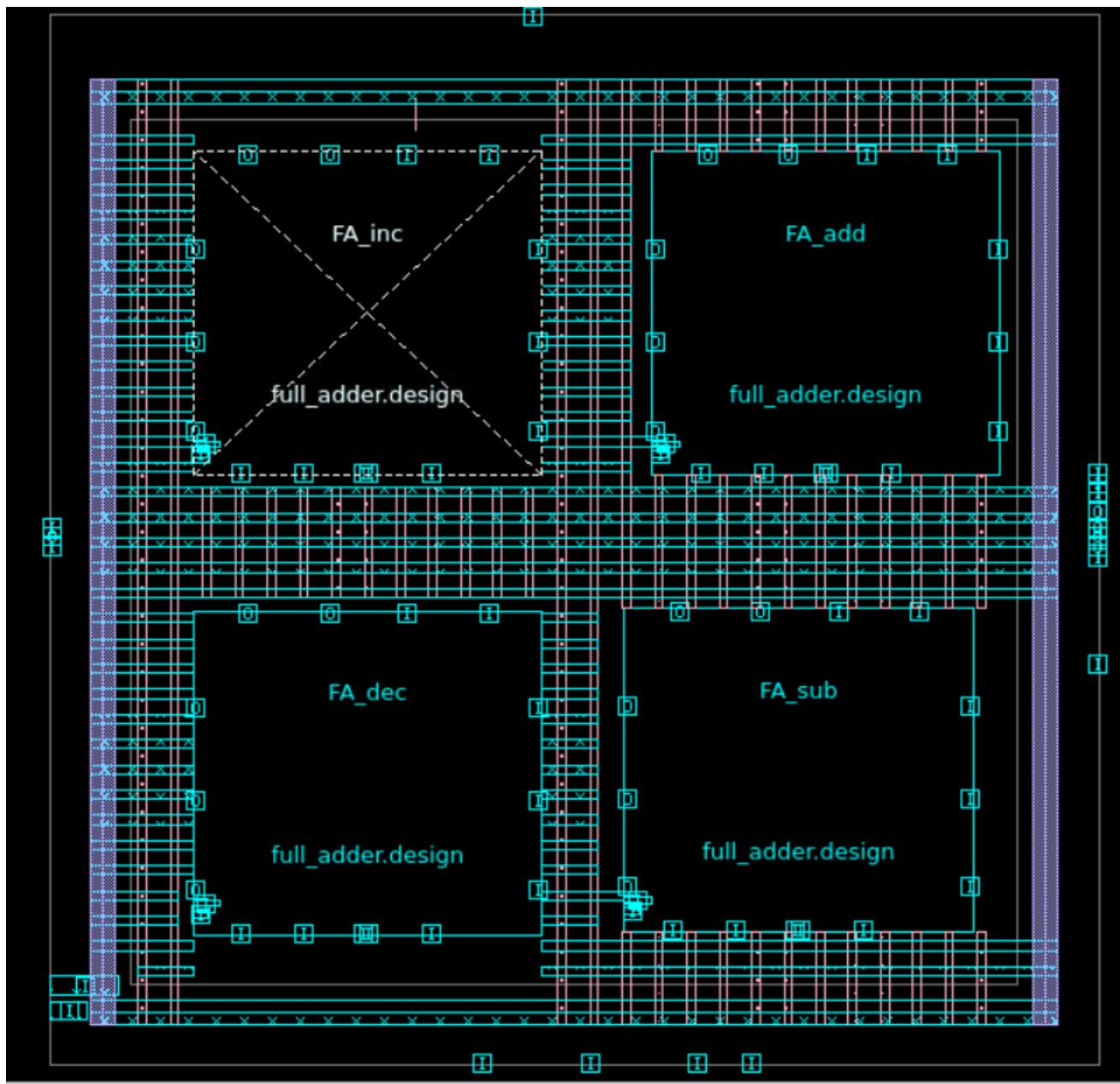
CORE_MESH

Individual meshes of VDD and VSS :

```
create_pg_mesh_pattern mesh -layers {{{vertical_layer: M6} {width: 0.4} {spacing: interleaving} {pitch: 2} {offset: 1}} {{horizontal_layer: M7} {width: 0.4} {spacing: interleaving} {pitch: 2} {offset: 1}}}
set_pg_strategy core_mesh -pattern {{name: mesh} {nets: VDD VSS}} -pg_regions ALU_CORE -pattern { {pattern:mesh} {nets: VDD VSS}} -extension {{ {side: 1234} {direction: T B R L} {stop: innermost_ring}}}
compile_pg -strategies core_mesh
```

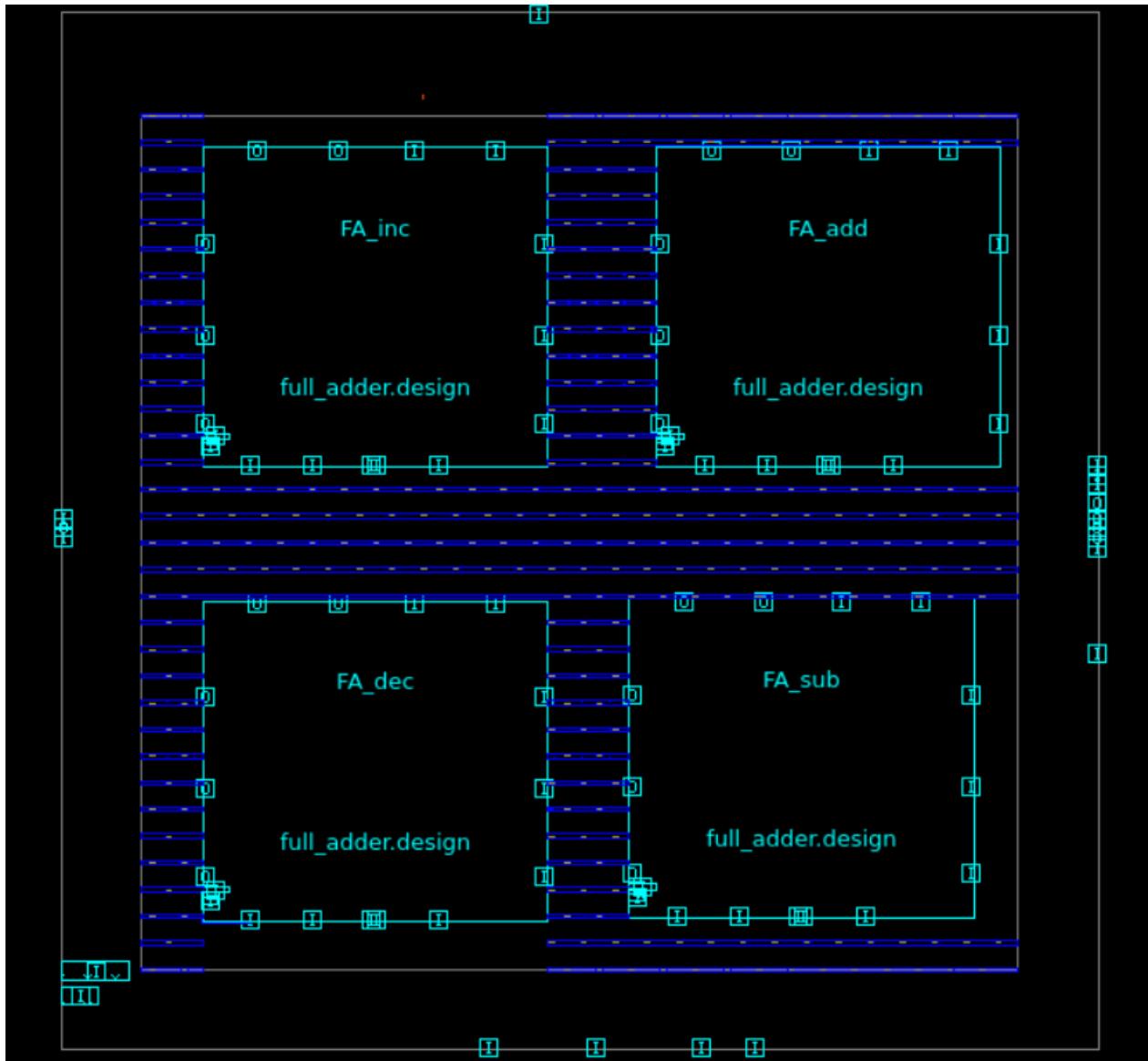


VSS MESH

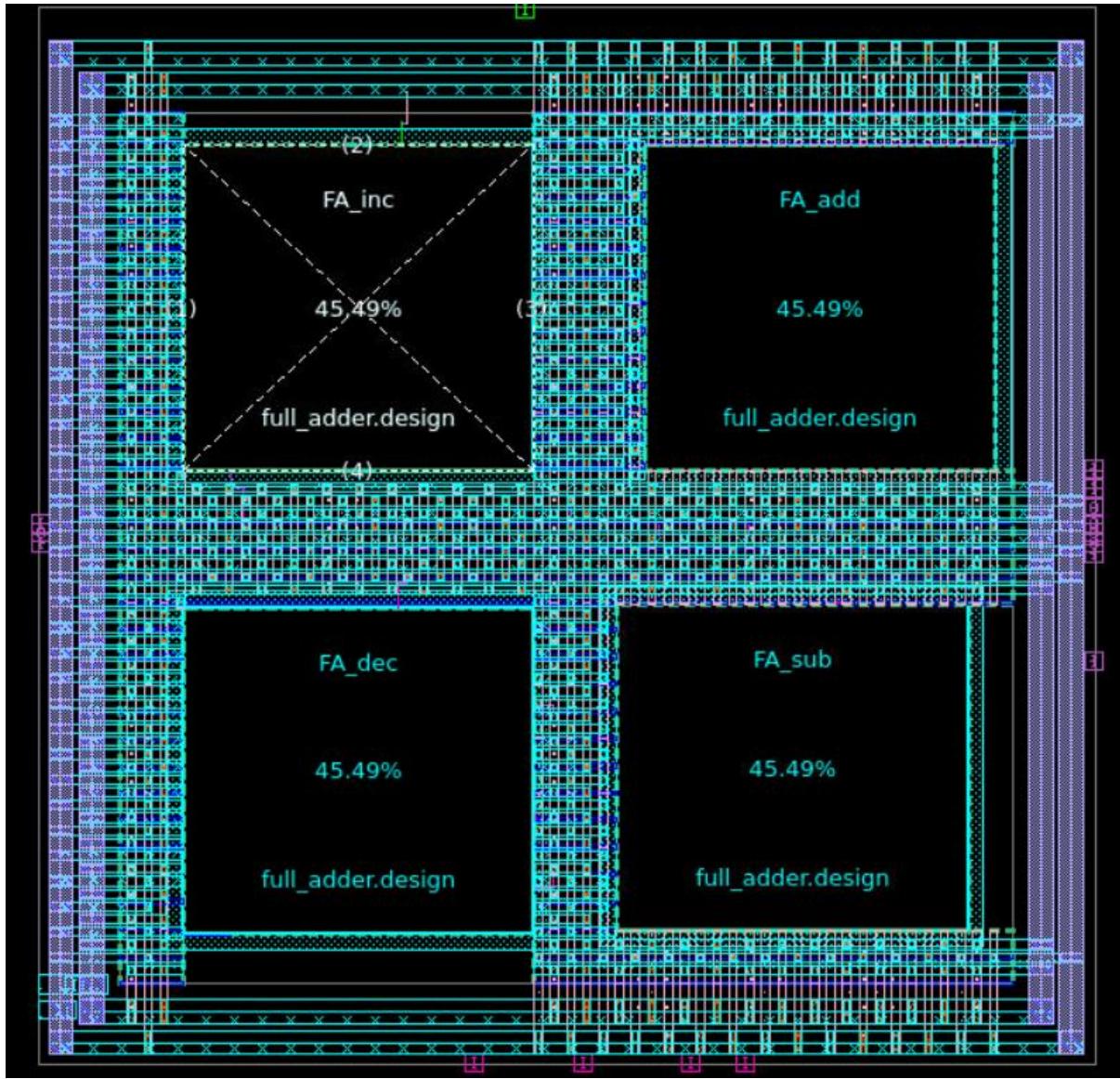


VDD MESH

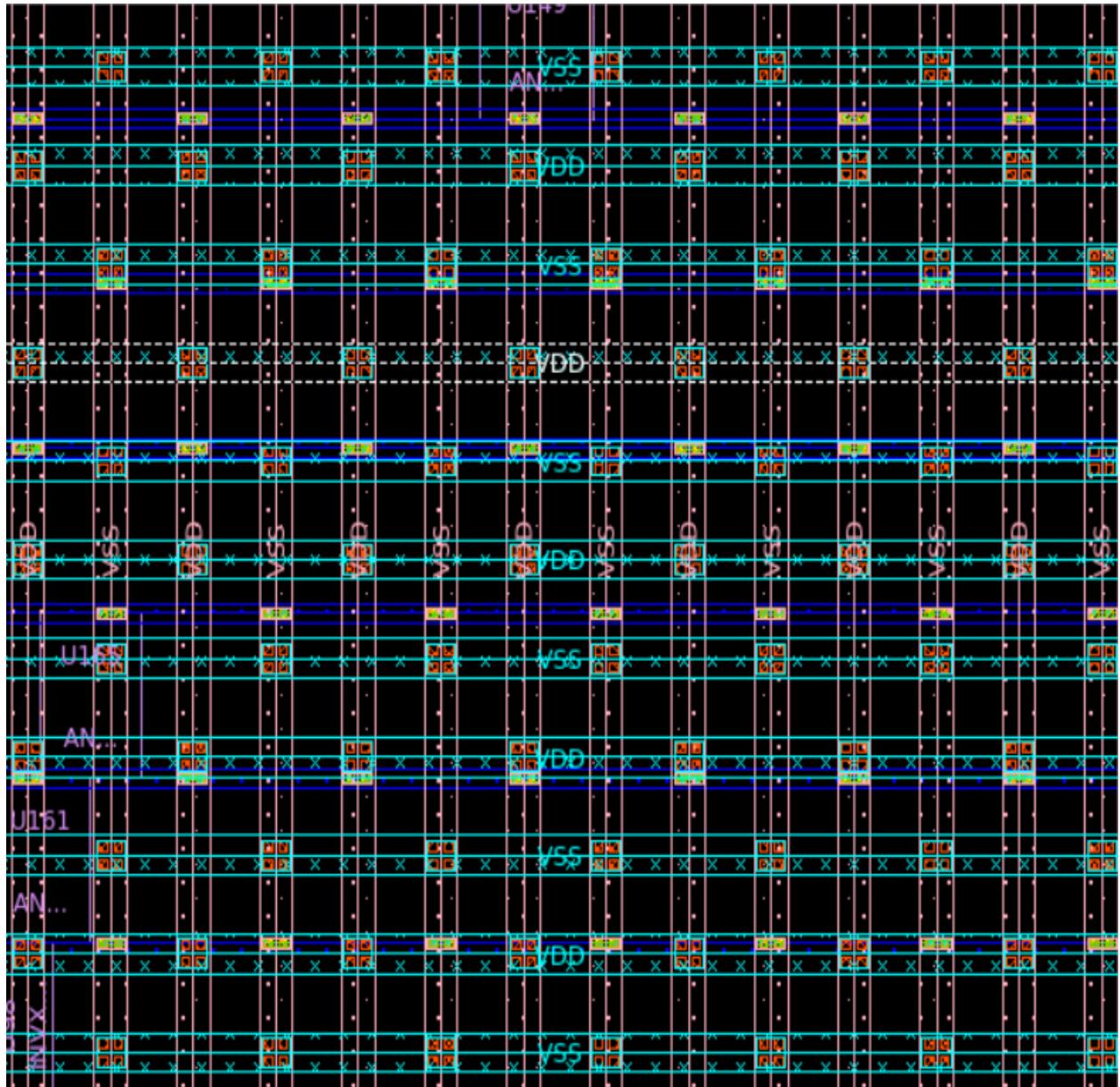
```
create_pg_std_cell_conn_pattern std_cell_rail -layers M1 -rail_width 0.19
set_pg_strategy rail_strategy -pg_regions ALU_CORE -pattern { {name: std_cell_rail} {nets:
VDD VSS} }
compile_pg -strategies rail_strategy
```



Standartd cell rails



Final Power Grid



All the vias of mesh and standard cell rails are dropped

- Power (**VDD**) and Ground (**VSS**) ports and nets are created.
- Defines **power grid (PG) regions** for individual soft macros and the ALU core.
- A **ring-based power grid** is created around the core and compiled.
- A **mesh** pattern is applied over the ALU core for consistent power distribution.
- Standard cell rails are defined using metal layer M1 and compiled.

4. Power Grid Checks :

check_pg_connectivity

```
icc2_shell> check_pg_connectivity
Checking secondary net through power switch is enabled.
Secondary net will be checked together from primary net. They will be treated as the same net
Primary Net : VDD Secondary Net:
Primary Net : VSS Secondary Net:
Loading cell instances...
Number of Standard Cells: 86
Number of Macro Cells: 0
Number of IO Pad Cells: 0
Number of Blocks: 0
Loading P/G wires and vias...
Number of VDD Wires: 167
Number of VDD Vias: 3596
Number of VDD Terminals: 0
*****Verify net VDD connectivity*****
Number of floating wires: 0
Number of floating vias: 0
Number of floating std cells: 0
Number of floating hard macros: 0
Number of floating I/O pads: 0
Number of floating terminals: 0
Number of floating hierarchical blocks: 0
*****
Loading cell instances...
Loading P/G wires and vias...
Number of VSS Wires: 164
Number of VSS Vias: 3343
Number of VSS Terminals: 0
*****Verify net VSS connectivity*****
Number of floating wires: 0
Number of floating vias: 0
Number of floating std cells: 0
Number of floating hard macros: 0
Number of floating I/O pads: 0
Number of floating terminals: 0
Number of floating hierarchical blocks: 0
*****
Overall runtime: 0 seconds
```

As we can see there are no floating standard cells , no floating hierachal blocks , no floating terminals of VDD and VSS and no floating vias of VDD and VSS .

```
check_pg_missing_vias
icc2_shell> check_pg_missing_vias
Check net VDD vias...
Number of missing vias: 0
Checking net VDD vias took 1 seconds.
Check net VSS vias...
Number of missing vias: 0
Checking net VSS vias took 0 seconds.
Overall runtime: 1 seconds.
icc2_shell> █
```

check_pg_drc

```
icc2_shell> check_pg_drc -ignore_std_cells
Command check_pg_drc started at Thu Apr 24 11:30:27 2025
Command check_pg_drc finished at Thu Apr 24 11:30:27 2025
CPU usage for check_pg_drc: 0.05 seconds ( 0.00 hours)
Elapsed time for check_pg_drc: 0.05 seconds ( 0.00 hours)
No errors found.
icc2_shell> █
```

As we can see the design is free from design rule violations and there are no missing vias in the power-plan stage.

- Ensures **power connectivity**, absence of **missing vias**, and no **design rule violations** in the PG network.
- Reports generated help validate proper power distribution.

5. Constraints and Scenario Setup

- Reads **timing constraints** from the `.sdc` file.
- Defines a **functional mode** and a **slow process corner** to simulate worst-case timing.
- Creates a **timing scenario** and links it with parasitic information (`.tluplus`) for accurate delay estimation.

```

check_design -checks pre_placement_stage
check_design -checks design_mismatch
read_sdc ../../ALU_HIER/DC/Hybrid_alu.sdc

set_app_options -name place.coarse.continue_on_missing_scandef -value true

set mode1 "func"

set corner1 "slow"

set scenario1 "${mode1}_${corner1}"

create_mode $mode1

create_corner $corner1

create_scenario -name $scenario1 -mode $mode1 -corner $corner1

set parasitics "p1"

read_parasitic_tech -tlup
"/data/pdk/pdk32nm/SAED32_EDK/tech/star_rcxt/saed32nm_1p9m_Cmax.tlupplus" -layermap
"/data/pdk/pdk32nm/SAED32_EDK/tech/star_rcxt/saed32nm_tf_itf_tlupplus.map" -name p1

set_parasitic_parameters -late_spec $parasitics -early_spec $parasitics

```

6. Placement and Optimization

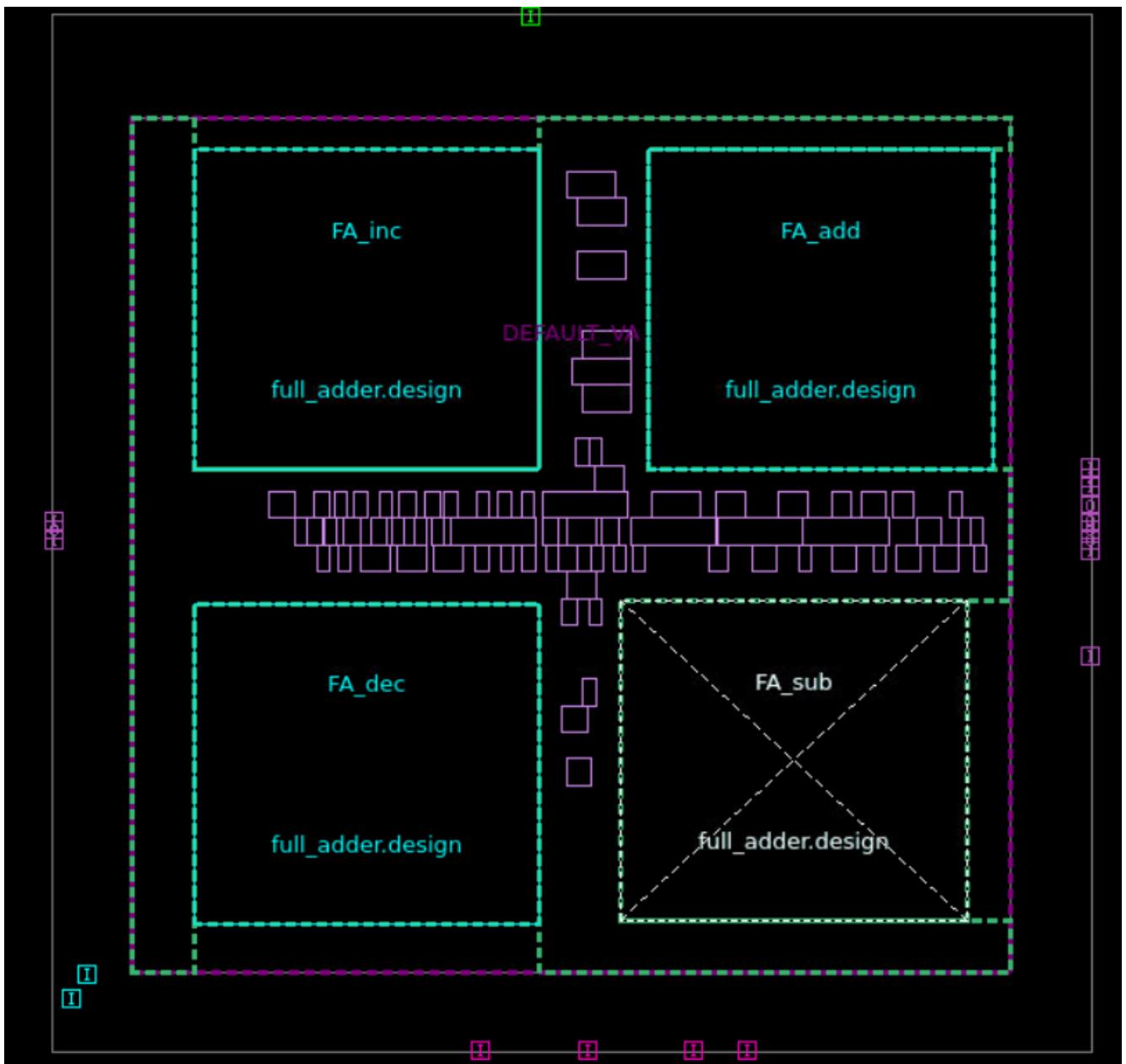
create_placement -effort high

set_scenario_status func_slow -hold true -setup true -leakage_power true -max_capacitance true – min_capacitance true -dynamic_power true -max_transition true -active true

place_opt

legalize_placement

- The initial placement is done with high effort, followed by **placement optimization** to reduce congestion and timing violations.
- **Legalization** ensures all cells are aligned to placement rows and not overlapping.



Placement Report:

```
icc2_shell> report_placement
*****
Report : report_placement
Design : hybrid_alu
Version: V-2023.12-SP4
Date   : Wed May 14 19:15:29 2025
*****
=====
Note: Including violations of fixed cells or between fixed pairs of cells.
      To ignore violations of / between fixed cells, enable -ignore_fixed.
=====

Wire length report (all)
=====
wire length in design good_powerplan: 1711.973 microns.
wire length in design good_powerplan (see through blk pins): 1846.276 microns.

Physical hierarchy violations report
=====
Violations in design good_powerplan:
    0 cells have placement violation.

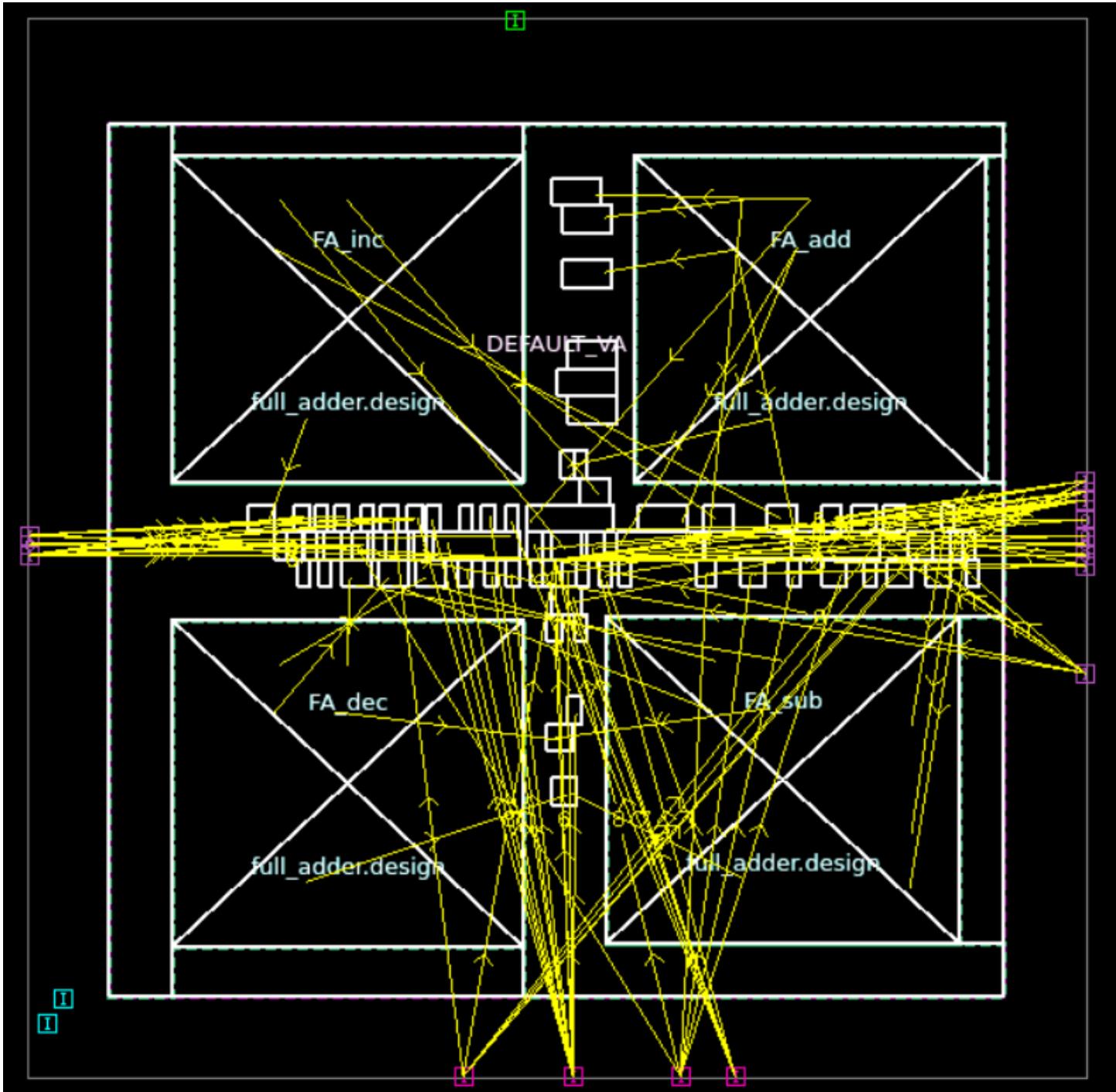
Voltage area violations report
=====
Voltage area placement violations in design good_powerplan:
    0 cells placed outside the voltage area which they belong to.

Information: Default error view good_powerplan_dpplace.err is created in GUI error browser. (DPP-054)
1
```

Utilization Report:

```
Report : report_utilization
Design : hybrid_alu
Version: V-2023.12-SP4
Date   : Wed May 14 19:16:28 2025
*****
Utilization Ratio:          0.2712
Utilization options:
- Area calculation based on: site_row of block good_powerplan
- Categories of objects excluded: hard_macros macro_keepouts soft_macros io_cells hard_blockages
Total Area:                2935.8715
Total Capacity Area:        716.8026
Total Area of cells:        194.4202
Area of excluded objects:
- hard_macros      :       0.0000
- macro_keepouts   :       487.9565
- soft_macros      :       1732.2455
- io_cells         :       0.0000
- hard_blockages  :       0.0000
Total Area of excluded objects: 2220.2020
Ratio of excluded objects:     0.7562

Utilization of site-rows with:
- Site 'unit':           0.2712
0.2712
```

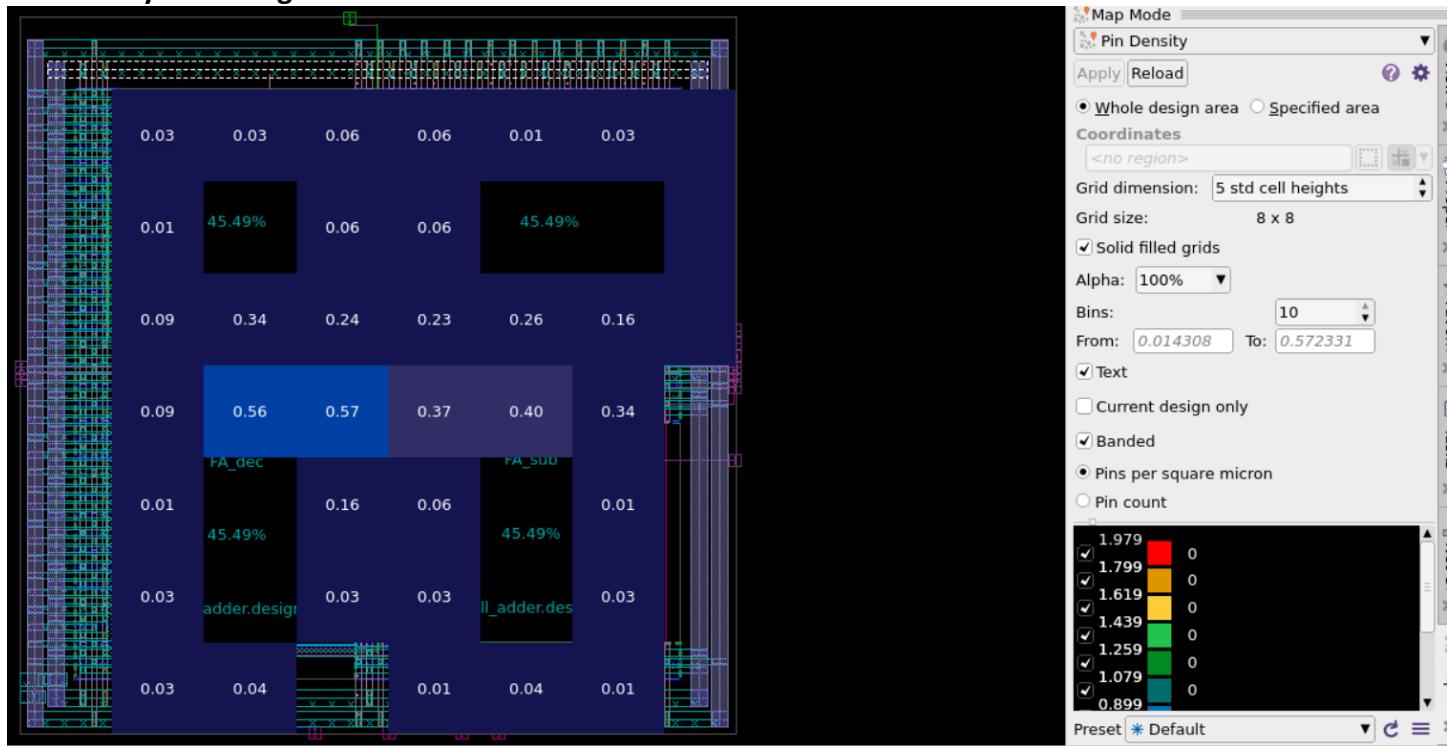


Fly Lines representing connections between ports , soft macros and standard cells

Cell Density View in gui :



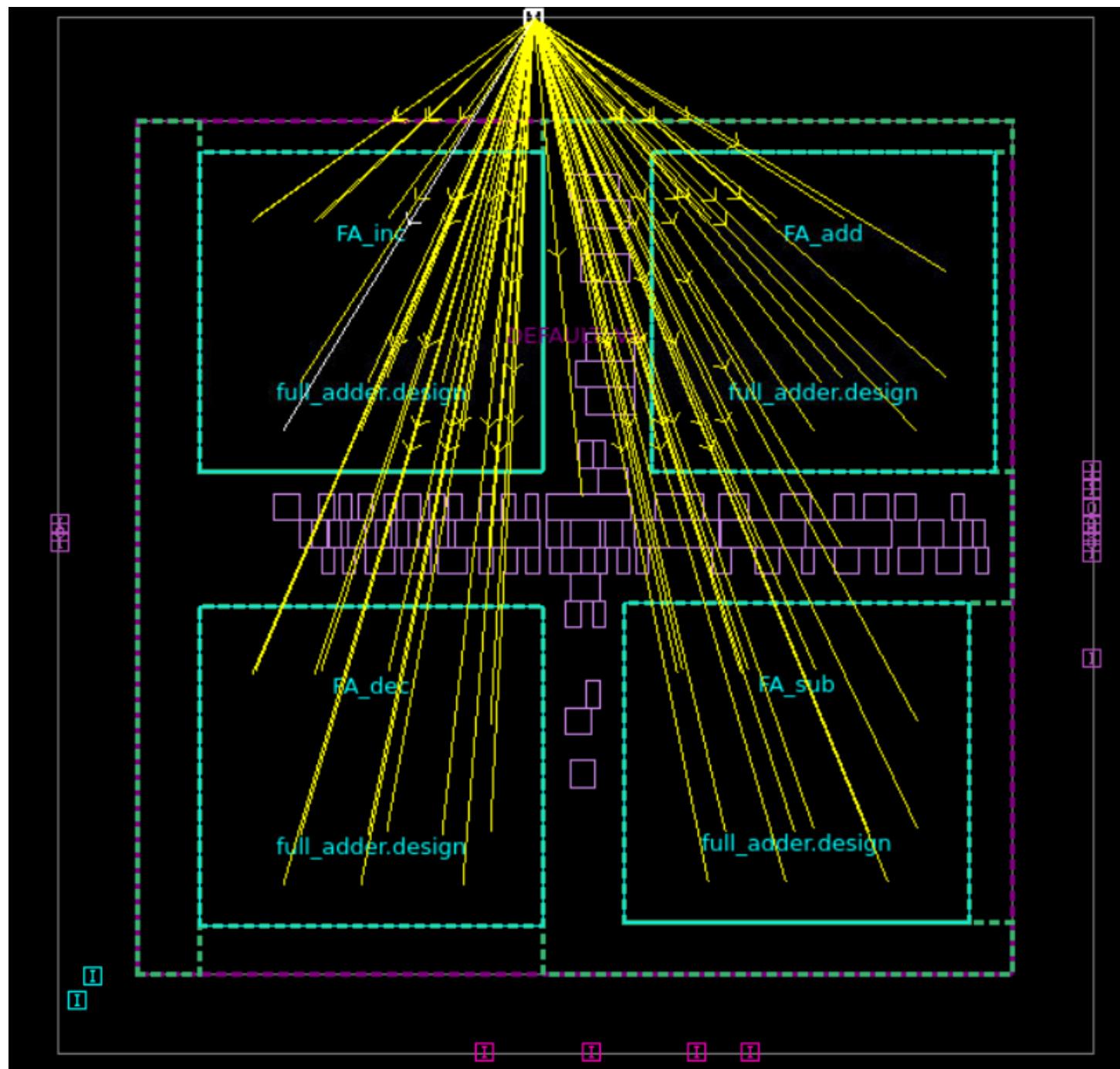
Pin Density View in gui :



Clock Tree Synthesis (CTS)

- Synthesizes the **clock tree** for the design, balancing delays and minimizing skew.
- Optimizes the tree to meet **timing, power, and noise constraints**.

Fly lines of Clock port :

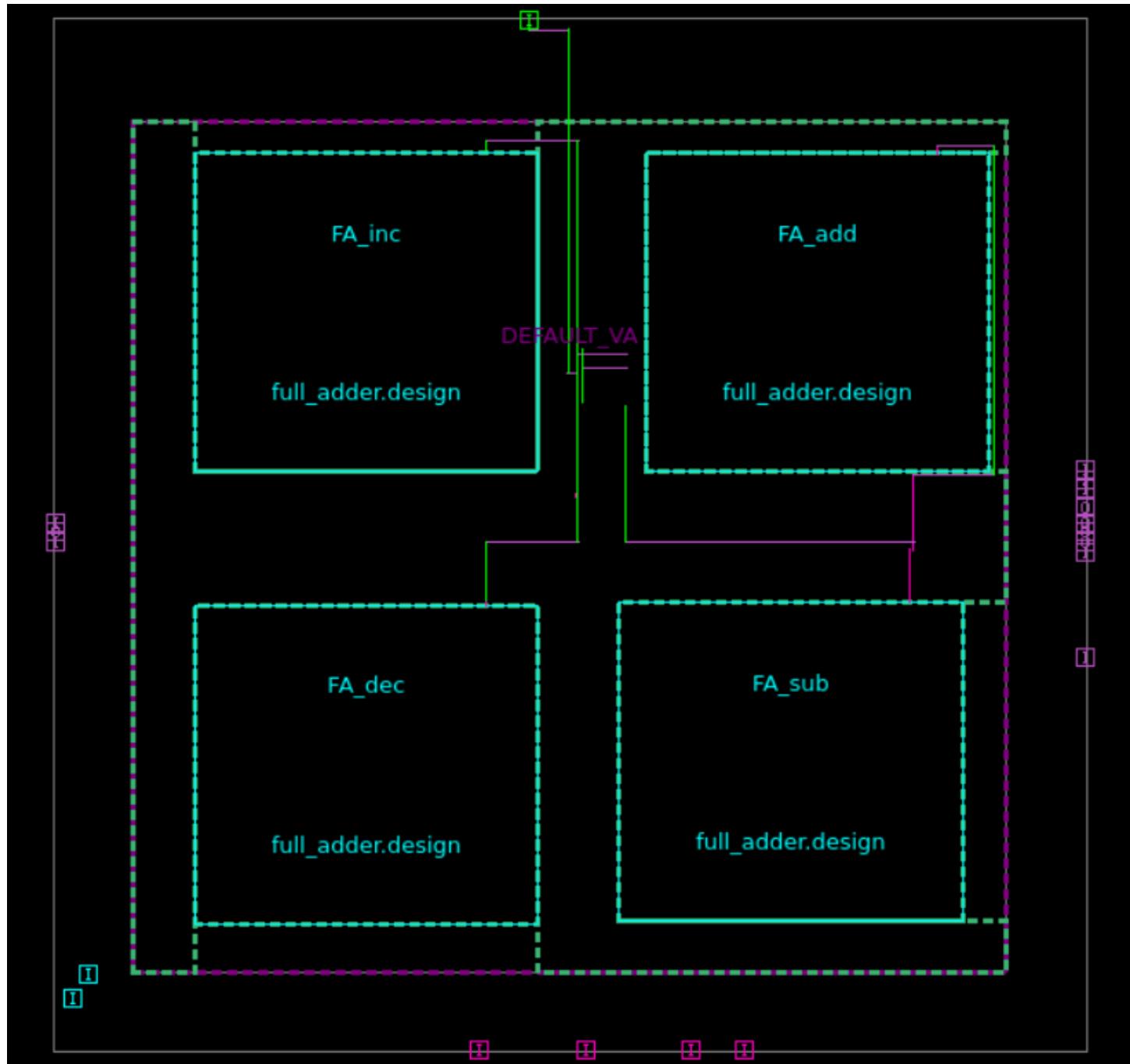


```
set_clock_routing_rules -default_ndr -clock Clocks -min_layer M3 -max_layer M4
```

```
set_scenario_status func_slow -hold true -setup true -leakage_power true -max_capacitance true -min_capacitance true -dynamic_power true -max_transition true -active true
```

```
synthesize_clock_trees
```

```
clock_opt
```



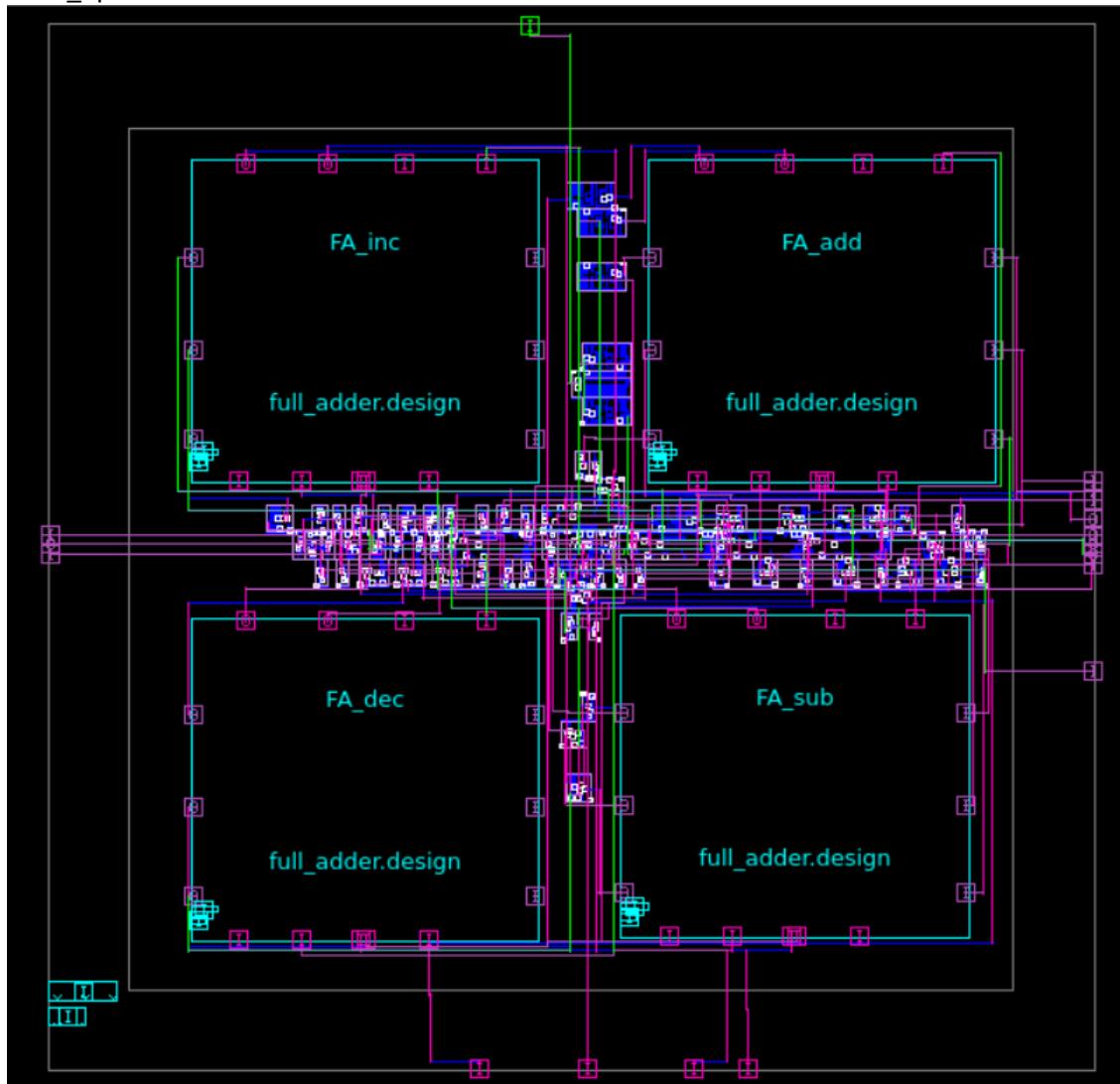
Clock Tree Synthesis

Routing

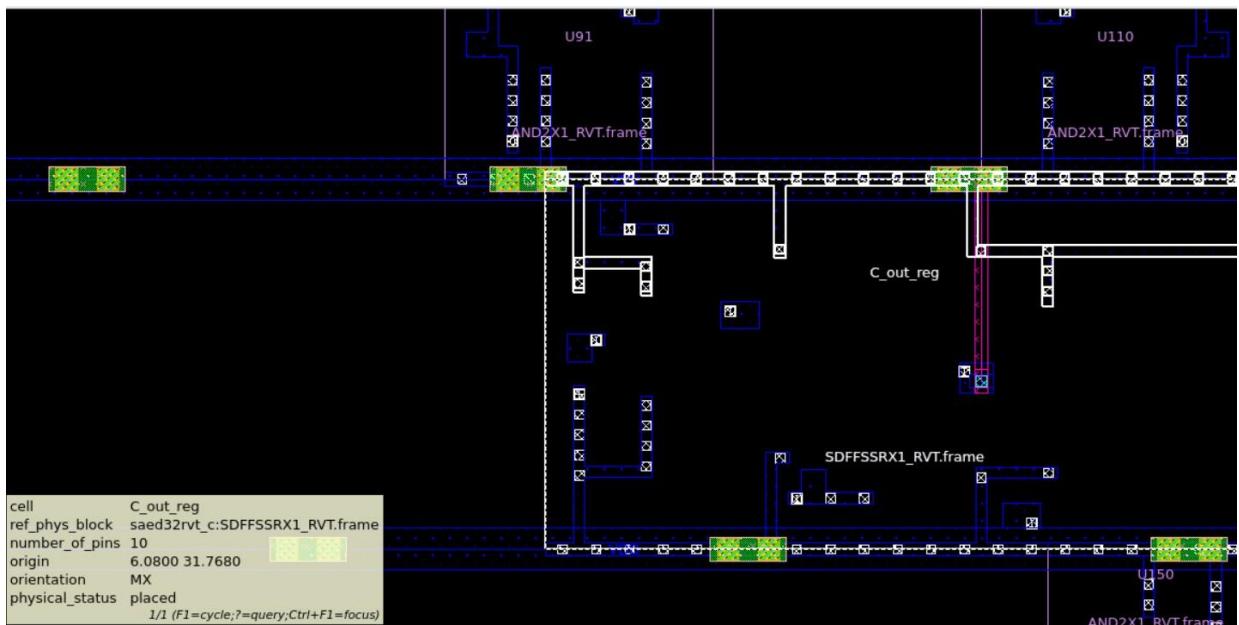
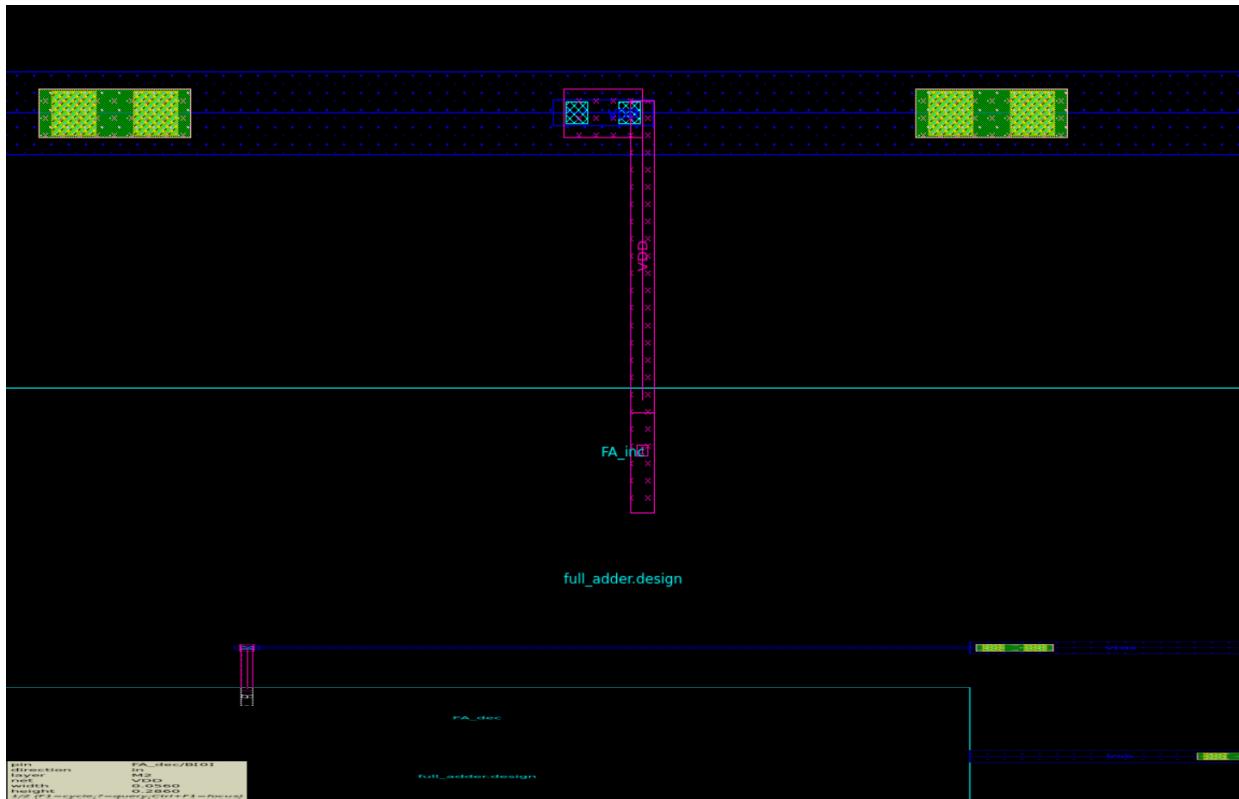
- Performs **global**, **track**, and **detailed routing** while being **timing- and crosstalk-driven**.
- Applies **antenna fixing** and uses **diodes** where required.

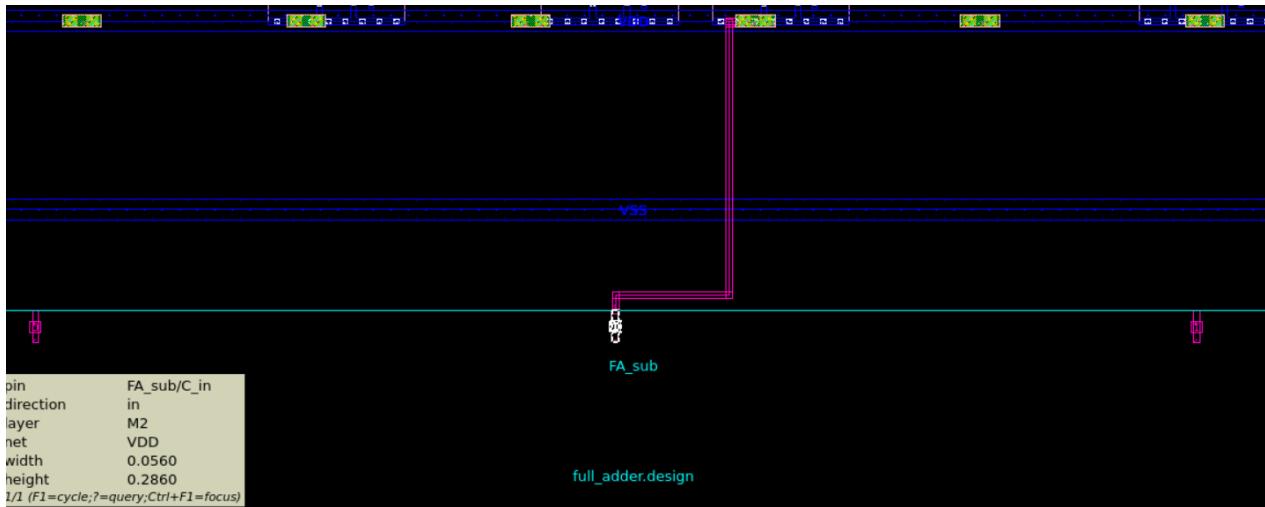
Commands:

```
check_design -checks pre_route_stage  
set_app_options -name route.global.timing_driven -value true  
set_app_options -name route.global.crosstalk_driven -value true  
set_app_options -name route.track.timing_driven -value true  
set_app_options -name route.track.crosstalk_driven -value true  
set_app_options -name route.detail.timing_driven -value true  
set_app_options -name route.detail.antenna -value true  
set_app_options -name route.detail.antenna_fixing_preference -value use_diodes  
set_app_options -block [current_design] -name route.detail.diode_libcell_names -value  
{*/ANTENNA_RVT}  
route_global  
route_track  
route_detail  
set_app_options -name route_opt.flow.enable_ccd -value true  
route_opt
```



Signal and clock routing





As we can see the VDD and VSS pins of all the macros and standard cells are being connected to the standad cell rail for power.

7. Post-Route Analysis

- Generates **timing reports** (both setup and hold) post-routing.
- Saves the design database, outputs **final netlist** and **LEF**, useful for backend integration or chip assembly.

Congestion Report

```

: report_congestion          report_constraint_groups
icc2_shell> report_congestion
*****
Report : congestion
Design : hybrid_alu
Version: V-2023.12-SP4
Date   : Wed May 14 19:53:44 2025
*****


Layer      |      overflow      |      # GRCs has
Name       | total | max |      overflow (%) |      max overflow
-----
Both Dirs |      5 | 3 |      2 ( 0.07%) |      1
H routing |      5 | 3 |      2 ( 0.13%) |      1
V routing |      0 | 0 |      0 ( 0.00%) |      0

```

• 1

Setup Report:

```
Startpoint: ALU_Sel[2] (input port clocked by Clock)
Endpoint: Result_reg[2] (rising edge-triggered flip-flop clocked by Clock)
Mode: func
Corner: slow
Scenario: func_slow
Path Group: **in2reg_default**
Path Type: max
```

Point	Incr	Path
clock Clock (rise edge)	0.00	0.00
clock network delay (propagated)	0.08	0.08
input external delay	1.00	1.08 f
ALU_Sel[2] (in)	0.00	1.08 f
ctmTdsLR_2_943/Y (NAND2X0_RVT)	0.06	1.14 r
ctmTdsLR_1_942/Y (INVX0_RVT)	0.05	1.19 f
ctmTdsLR_2_951/Y (NAND2X0_RVT)	0.05	1.24 r
ctmTdsLR_1_950/Y (INVX0_RVT)	0.05	1.29 f
ctmTdsLR_1_958/Y (OA22X1_RVT)	0.06	1.35 f
ctmTdsLR_1_936/Y (A0221X1_RVT)	0.04	1.39 f
Result_reg[2]/SE (SDFFSSRX1_RVT)	0.00	1.39 f
data arrival time		1.39
clock Clock (rise edge)	2.00	2.00
clock network delay (propagated)	0.15	2.15
Result_reg[2]/CLK (SDFFSSRX1_RVT)	0.00	2.15 r
clock uncertainty	-0.07	2.08
library setup time	-0.07	2.01
data required time		2.01

data required time	2.01	
data arrival time	-1.39	

slack (MET)		0.63

Hold Report:

```
Report : timing
  -path_type full
  -delay_type min
  -max_paths 1
  -report_by design
Design : hybrid_alu
Version: V-2023.12-SP4
Date   : Thu Apr 24 12:26:48 2025
*****
Startpoint: Result_reg[0] (rising edge-triggered flip-flop clocked by clk)
Endpoint: Result[0] (output port clocked by clk)
Mode: func
Corner: slow
Scenario: func_slow
Path Group: **reg2out_default**
Path Type: min

Point                      Incr    Path
-----
clock clk (rise edge)      0.00    0.00
clock network delay (propagated) 0.10    0.10
                                         0.00    0.10 r
Result_reg[0]/CLK (SDFFSSRX1_RVT) 0.06    0.16 f
Result_reg[0]/QN (SDFFSSRX1_RVT) 0.00    0.16 f
                                         0.16
Result[0] (out)             0.00    0.16 f
data arrival time          0.16

clock clk (rise edge)      0.00    0.00
clock network delay (propagated) 0.18    0.18
clock uncertainty           0.20    0.38
output external delay       -1.20   -0.82
data required time          -0.82
data arrival time           -0.16
-----
data required time          -0.82
data arrival time           -0.16
-----
slack (MET)                 0.99
```

```

Report : clock timing
    -type summary
Design : hybrid_alu
Version: V-2023.12-SP4
Date   : Thu Apr 24 13:05:03 2025
*****  

Mode: func
Clock: clk
                                         Corner
-----  

Maximum setup launch latency:
  C_out_reg/CLK                         0.10    rp-+    slow  

Minimum setup capture latency:
  Result_reg[2]/CLK                      0.10    rp-+    slow  

Minimum hold launch latency:
  Result_reg[2]/CLK                      0.10    rp-+    slow  

Maximum hold capture latency:
  C_out_reg/CLK                         0.10    rp-+    slow  

Maximum active transition:
  C_out_reg/CLK                         0.00    rp-+    slow  

Minimum active transition:
  Result_reg[2]/CLK                      0.00    rp-+    slow  

Maximum setup skew:
  --                                     --  

Maximum hold skew:
  --                                     --

```

```

icc2_shell> report_clock_routing_rules
*****
Report : clock routing rules
Design : hybrid_alu
Date   : Thu Apr 24 12:48:06 2025
*****
Clock: clk (mode func); Net Type: all;      Rule: default rule; Min Layer: M3; Max Layer: M4
icc2_shell> █

```

Clock routing rules

Pg_Strategies that I used in this design :

```
icc2_shell> report_pg_strategies
#-----
#-----#
name: ring_strategy
region:
    Region: core area
    Coordinate: {{5.0000 5.0000} {5.0000 58.5040} {59.8720 58.5040} {59.8720 5.0000} }

Pattern Expression :
    pattern: core_ring
    nets: VDD VSS
    parameters:
        offset: 1.0000 1.0000
        offset start: boundary
        skip_sides:
        side_offset:
        merge: undefined undefined
        fill_gap: undefined

Instantiated Pattern :
Pattern Name: core_ring
Type: Ring Pattern
Symbolic Nets: VDD VSS
Ring Width:
    {side: horizontal}{width: 1.5}
    {side: vertical}{width: 1.5}
Ring Layer:
    {side: horizontal}{layer: M7}
    {side: vertical}{layer: M8}
Ring Spacing:
    {side: horizontal}{spacing: 0.4}
    {side: vertical}{spacing: 0.4}
Corner Bridge: false
Via Rules:
    {intersection: all} {via_master : {default}}
Track Alignment: no alignment
Parameters:
```

```
#-----#
name: core_mesh
region:
    Region: PG region ALU_CORE
    Coordinate: {{5.0000 5.0000} {5.0000 58.5040} {8.8530 58.5040} {8.8530 36.4560} {30.4210 36.4560} {30.4210 58.5040} {59.8720 58.5040} {59.8720 5.0040} {37.3040 56.5040} {37.3040 36.4560} {59.8720 36.4560} {59.8720 28.2500} {35.5780 28.2500} {35.5780 8.2020} {59.8720 8.2020} {59.8720 5.0000} {30.4210 5.0000} {30.4210 28.0790} {8.8530 28.0790} {8.8530 5.0000} }

Pattern Expression :
pattern: mesh
nets: VDD VSS
parameters:
offset: undefined undefined
offset start: boundary
pitch: undefined undefined
repeat: undefined undefined

Instantiated Pattern :
Pattern Name: mesh
Type: Mesh Pattern
Parameters:
Layers:
{ {vertical_layer : M6} {width : {0.5 }} {spacing : interleaving} {trim : true} {track_alignment : none} {pitch : 2} {offset : 0.7} }
{ {horizontal_layer : M7} {width : {0.567 }} {spacing : interleaving} {trim : true} {track_alignment : none} {pitch : 1.56} {offset : 0.8} }
Via Rules:
{intersection: all} {via_master : {default}}
```

Extension:

- Nets:
- Layers:
- Sides:
- Direction: LRTB
- Stop: inner-most ring

```

name: rail_strategy
region:
  Region: PG region ALU CORE
  Coordinate: {{5.0000 5.0000} {5.0000 58.5040} {8.8530 58.5040} {8.8530 36.4560} {30.4210 36.4560} {30.4210 58.5040} {59.8720 58.5040} {59.8720 5.0000} {30.4210 5.0000} {30.4210 28.0790} {8.8530 28.0790} {8.8530 5.0000} }

Pattern Expression :
  pattern: std_cell_rail
  nets: VDD VSS
  parameters:
    offset: undefined
    offset start: boundary

Instantiated Pattern :
  Pattern Name: std_cell_rail
  Type: Standard Cell Rail Pattern
  Rail Width: 0.2700 0.2700
  Rail Layers: M1
  Rail Shift: undefined undefined
  Rail Masks: no_mask no_mask
  Rail pin DRC option: false
  Mark as follow pin option: false
  Parameters:

  Extension:
  Blockage:
#-----#

```

Files to be written post route :

write_gds ALU.gdsii

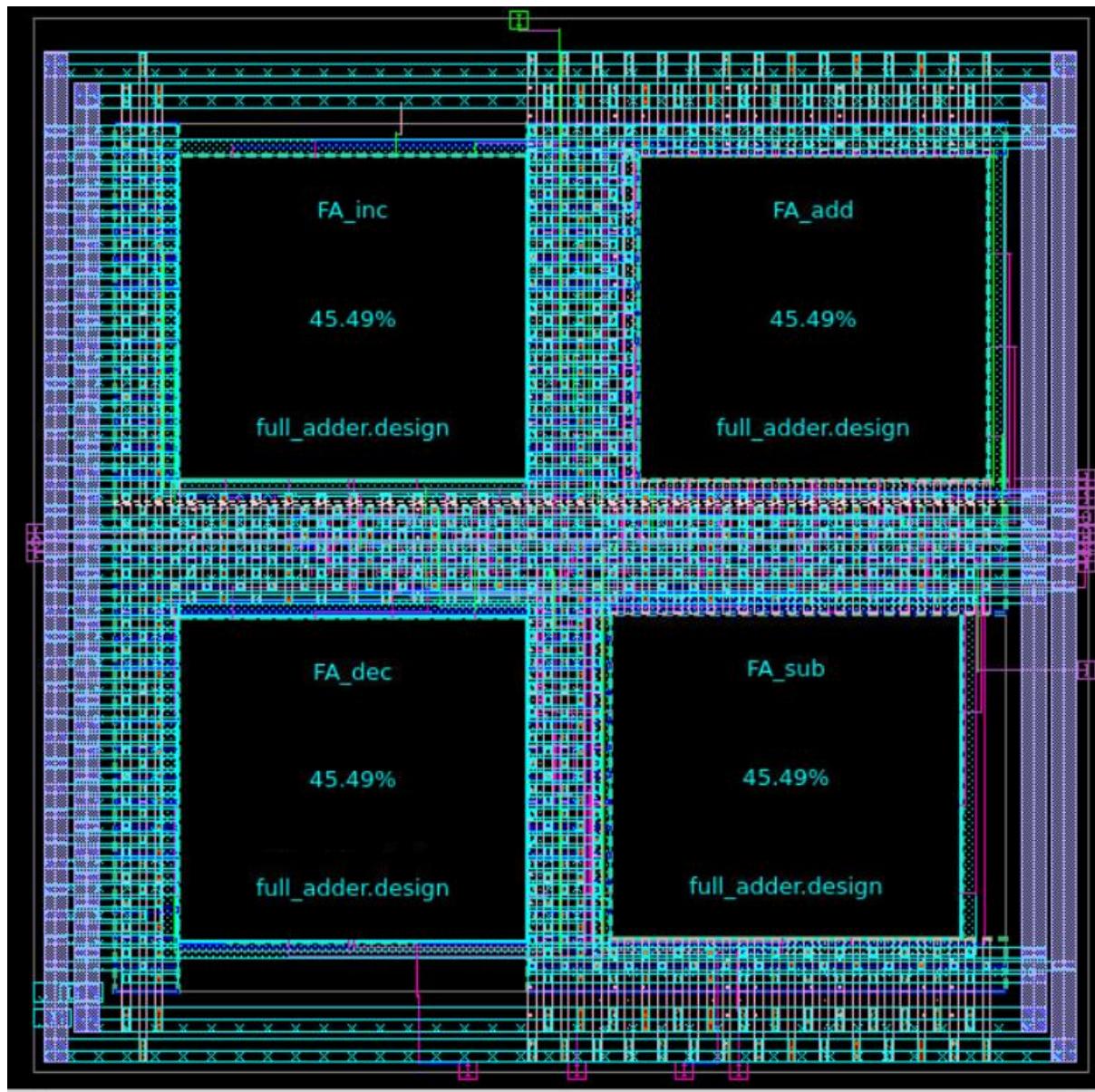
write_verilog ALU.routed.v

write_parasitics –format spef –output ALU

create_frame

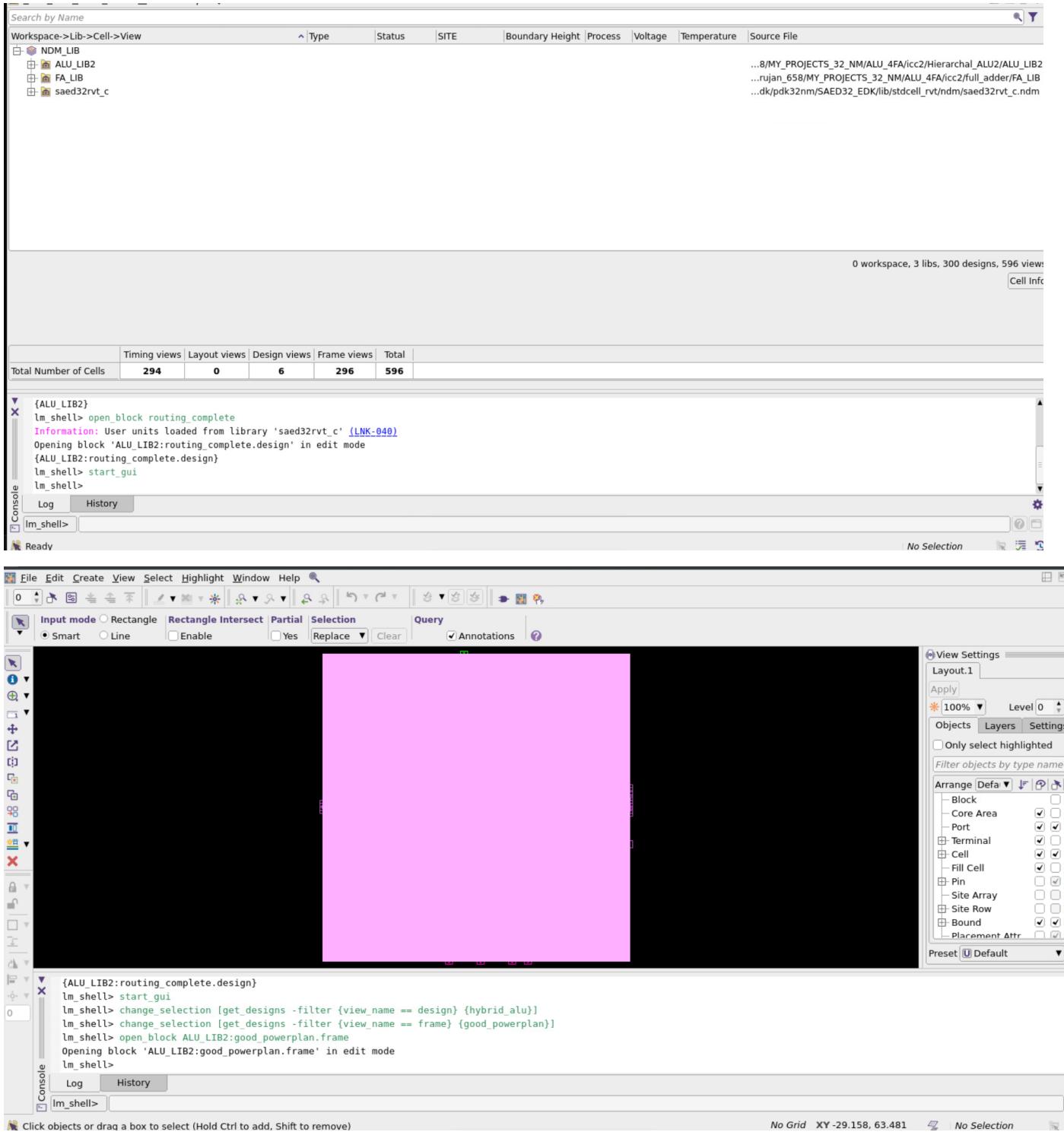
write_lef ALU.lef

Final Layout of the design :

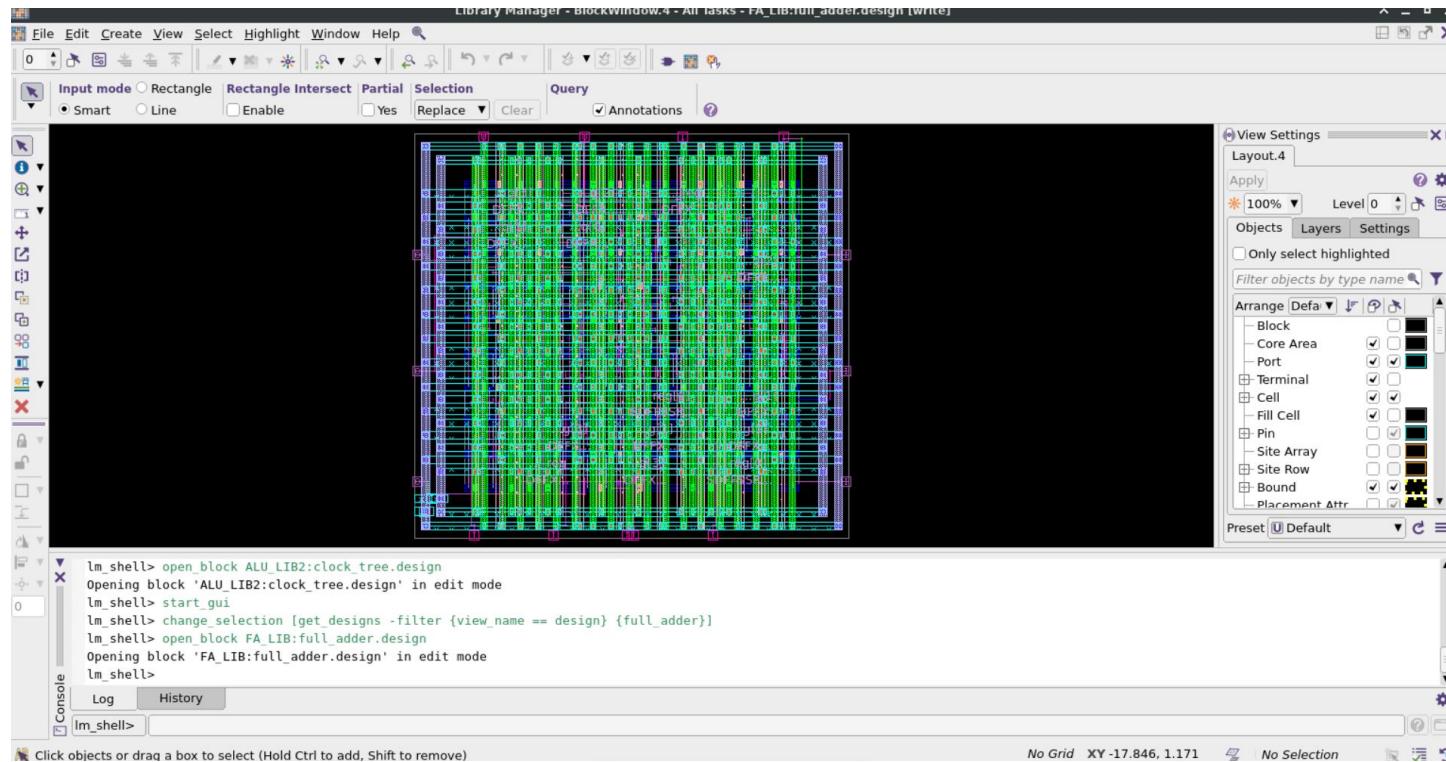


View in Library Manager Tool :

Top design View [hybrid_alu]:



Layout View Of Soft Macro Full Adder Used in this Design :



Summary and Conclusion

In this project, a hierarchical **Hybrid ALU** design was successfully implemented using the Synopsys ICC2 physical design flow. Standard cell libraries and technology files were integrated to initialize the floorplan, and soft macros representing full adders were placed manually to create a modular ALU layout. Power planning was meticulously handled using ring, mesh, and rail strategies, ensuring proper power delivery across all modules.

Clock tree synthesis and optimization were performed to ensure uniform clock distribution with minimal skew. The routing stage was completed using a timing-driven approach to enhance signal integrity and reduce crosstalk effects. Post-route checks, including DRC, LVS, and connectivity verification, were passed successfully.

Final post-route timing analysis yielded the following results:

- **Setup Slack:** +0.63 ns
- **Hold Slack:** +0.99 ns

These results indicate that the design meets all critical timing constraints with sufficient margin, proving the effectiveness of floorplanning, placement, CTS, and routing strategies applied throughout the flow.

This implementation demonstrates strong understanding and practical application of VLSI physical design principles, with successful sign-off metrics validating the design's robustness and manufacturability.