

# **Pico-RV Report (Scenario setup , Place and Route)**

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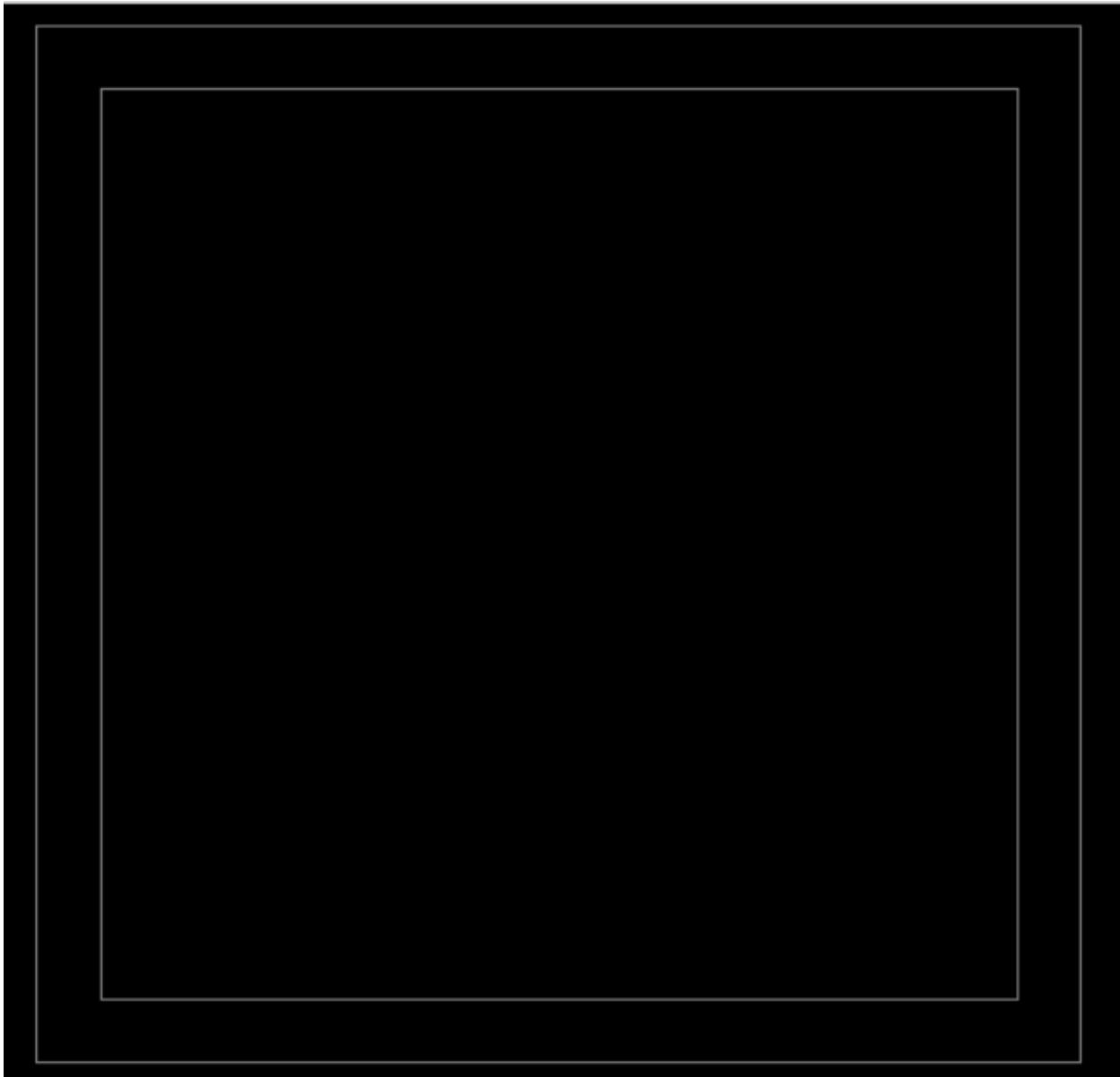
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# 1 Parasitic Scenario and Analysis Setup

## FLOORPLAN [Common For all Tasks]

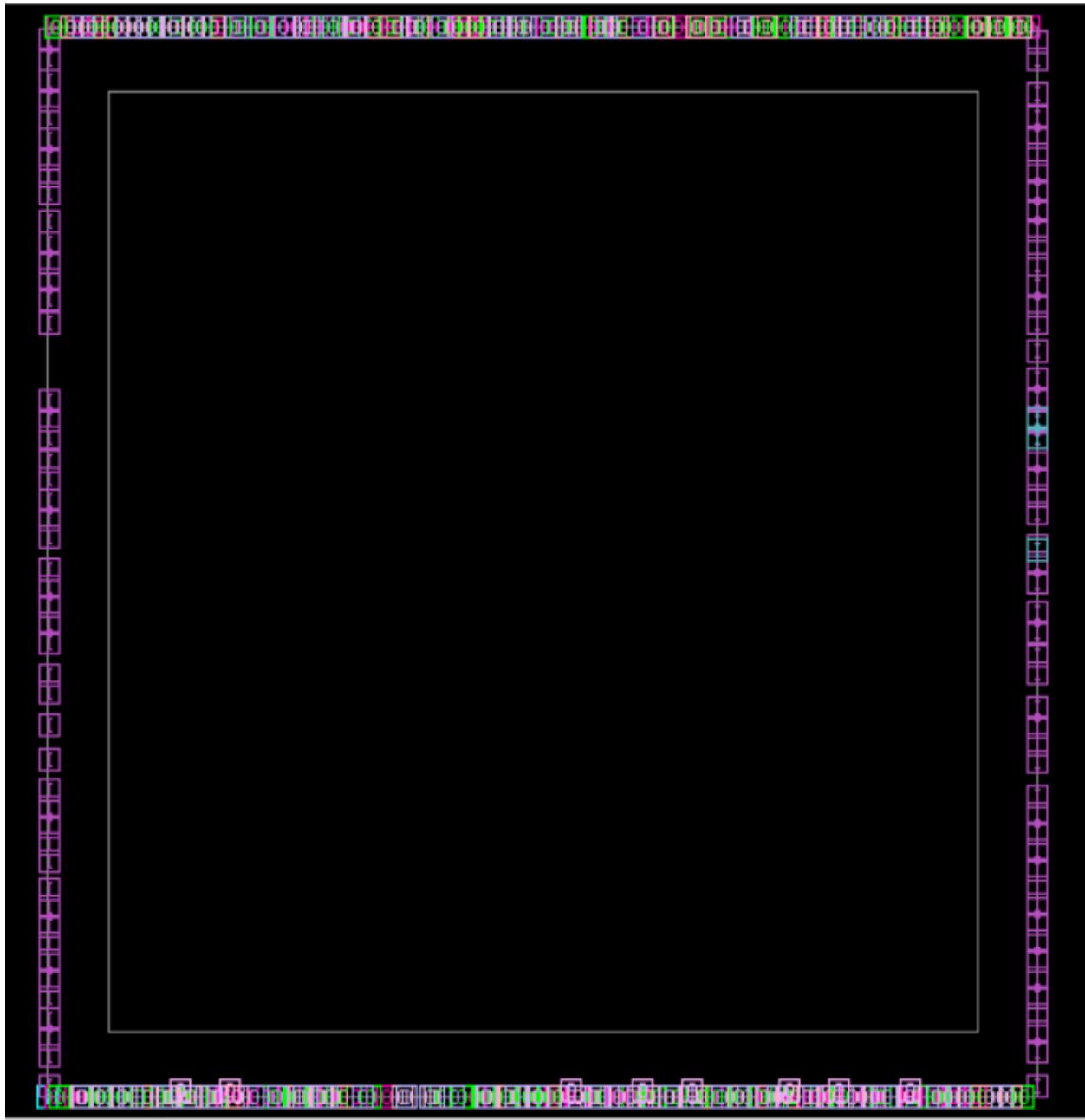


```
initialize_floorplan -coincident_boundary true -core_utilization 0.8 -  
core_offset 12
```

- `initialize_floorplan` : Sets up the initial floorplan of the design.
- `-coincident_boundary true` : Makes the floorplan boundary coincide with the core boundary.

- `-core_utilization 0.8` : Specifies 80% core utilization (i.e., 80% of core area will be used for standard cells).
  - `-core_offset 12` : Places a 12-unit margin between core and die boundaries (core offset on all four sides).
- 

## PIN PLACEMENT



```
set_individual_pin_constraints -ports [remove_from_collection [all_inputs] clk] -sides {6 7 8}
```

- Applies side constraints for **all input ports except clk**.
- **-sides {6 7 8}**: These are the **south (6), east (7), and north (8)** sides of the die.

```
set_individual_pin_constraints -ports [all_outputs] -sides {6 7 8}
```

- Constrains **all output pins** to sides 6, 7, and 8.

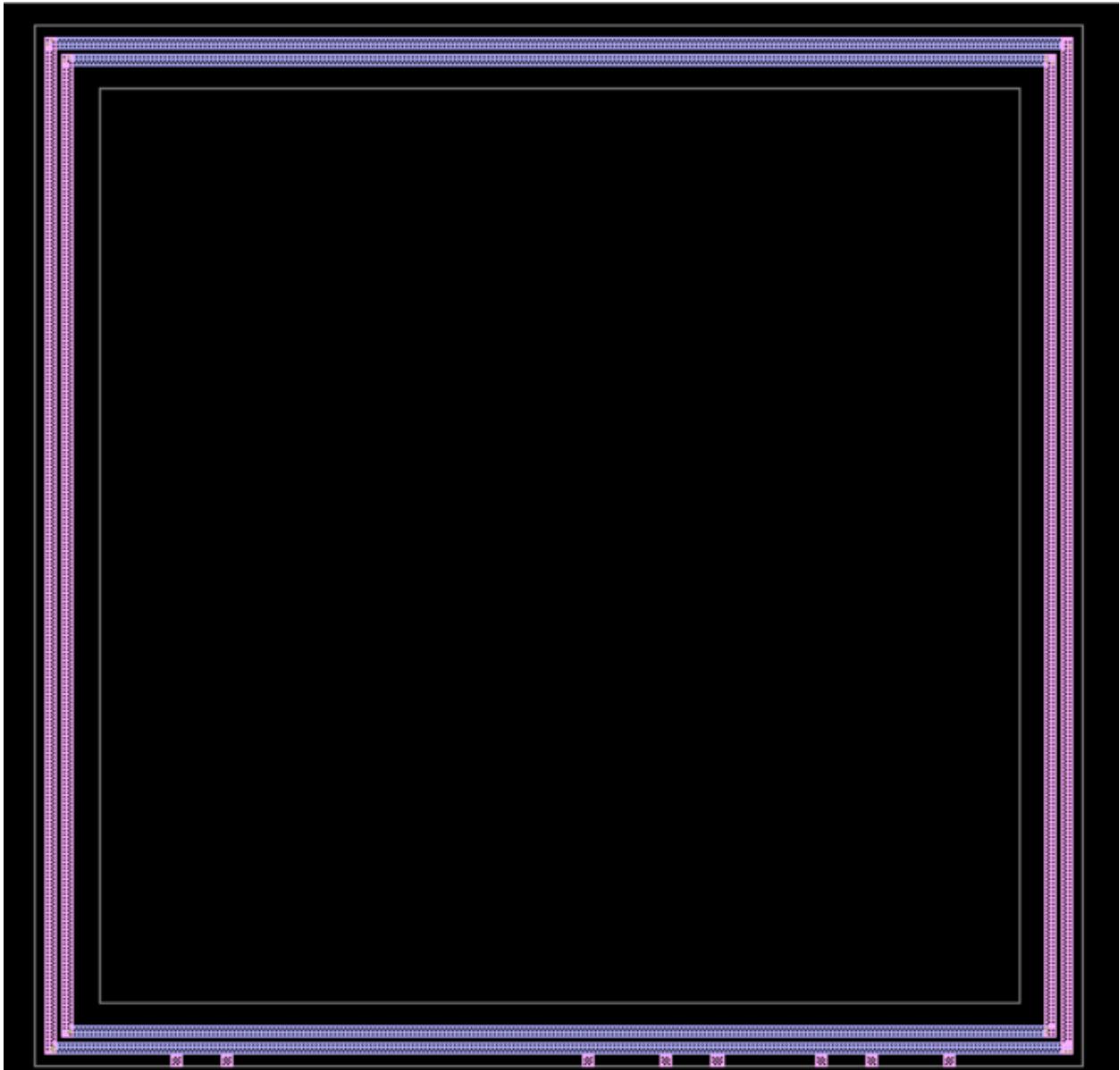
```
set_individual_pin_constraints -ports clk -sides {5}
```

- Constrains **clk pin only** to side 5, which is the **west side** of the die.

```
place_pins -ports [all_outputs]  
place_pins -ports [remove_from_collection [all_inputs] clk]  
place_pins -ports [get_ports clk]
```

- Places the constrained pins onto their designated sides:
    - Outputs first,
    - Then all inputs except `clk`,
    - Then the `clk` pin.
-

## POWER PLAN – CORE RING



```
create_pg_ring_pattern core_ring \
    -horizontal_layer M8 -horizontal_width 2 -horizontal_spacing 1. \
    -vertical_layer M9 -vertical_width 2 -vertical_spacing 1.2
```

- Defines a **core ring pattern** named `core_ring` for power/ground (PG).
- Horizontal rings:
  - Layer: M8
  - Width: 2  $\mu\text{m}$
  - Spacing: 1  $\mu\text{m}$
- Vertical rings:

- Layer: M9
- Width: 2  $\mu\text{m}$
- Spacing: 1.2  $\mu\text{m}$

```
set_pg_strategy ring_strategy -core -pattern {{name:core_ring} {nets:{VDD VSS}} {offset:{5 4.5}}}
```

- Sets a **power strategy** named `ring_strategy` using the `core_ring` pattern for the **core**.
- Targets the **VDD and VSS** nets.
- Offset the ring from core boundary: 5  $\mu\text{m}$  horizontal, 4.5  $\mu\text{m}$  vertical.

---

```
compile_pg -strategies ring_strategy
```

- Compiles and applies the `ring_strategy` power ring to the floorplan.
- 

## POWER PLAN – CORE MESH

```
create_pg_mesh_pattern mesh \
    -layers    {{vertical_layer:M7}      {width:0.78}      {spacing:interleaving} \
{pitch:2.1} {offset:0.7}} \
        {{horizontal_layer:M8}       {width:0.8}       {spacing:interleaving} \
{pitch:2.5} {offset:0.8}}}
```

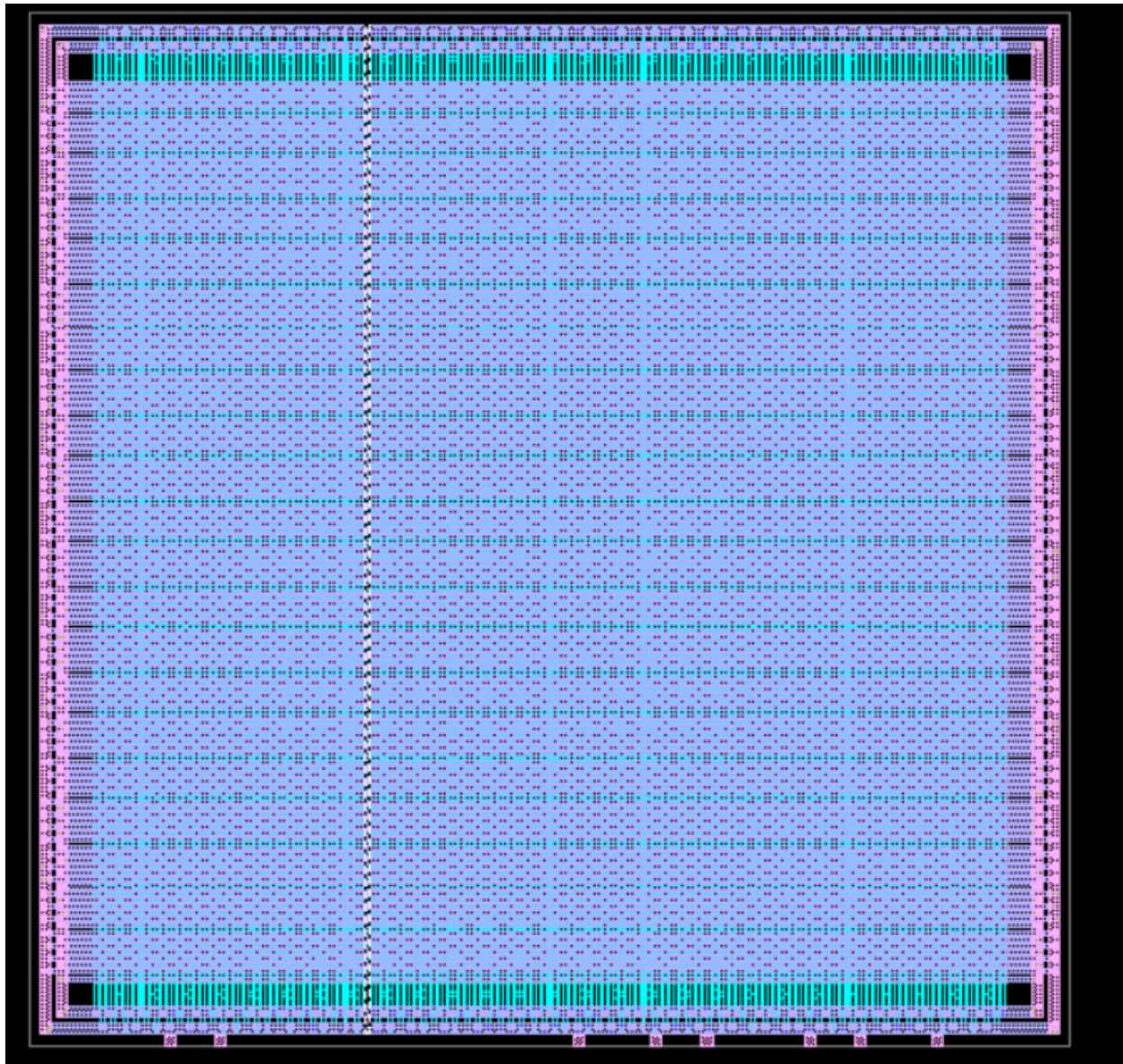
- Creates a **mesh pattern** named `mesh`:
  - Vertical lines:
    - Layer: M7
    - Width: 0.78  $\mu\text{m}$
    - Interleaving spacing
    - Pitch: 2.1  $\mu\text{m}$
    - Offset: 0.7  $\mu\text{m}$
  - Horizontal lines:
    - Layer: M8
    - Width: 0.8  $\mu\text{m}$
    - Interleaving spacing
    - Pitch: 2.5  $\mu\text{m}$
    - Offset: 0.8  $\mu\text{m}$

```
set_pg_strategy core_mesh -pattern {{pattern:mesh} {nets:VDD VSS}} \
-extension {{direction: T L R B} {stop:innermost_ring}} -core
```

- Creates a PG strategy called `core_mesh` using the mesh pattern for VDD/VSS.
- The mesh extends in **all directions (Top, Left, Right, Bottom)** and **stops at the innermost ring**.

```
compile_pg -strategies core_mesh
```

- Applies and compiles the `core_mesh` power mesh into the floorplan.



---

## POWER PLAN – STANDARD CELL RAILS

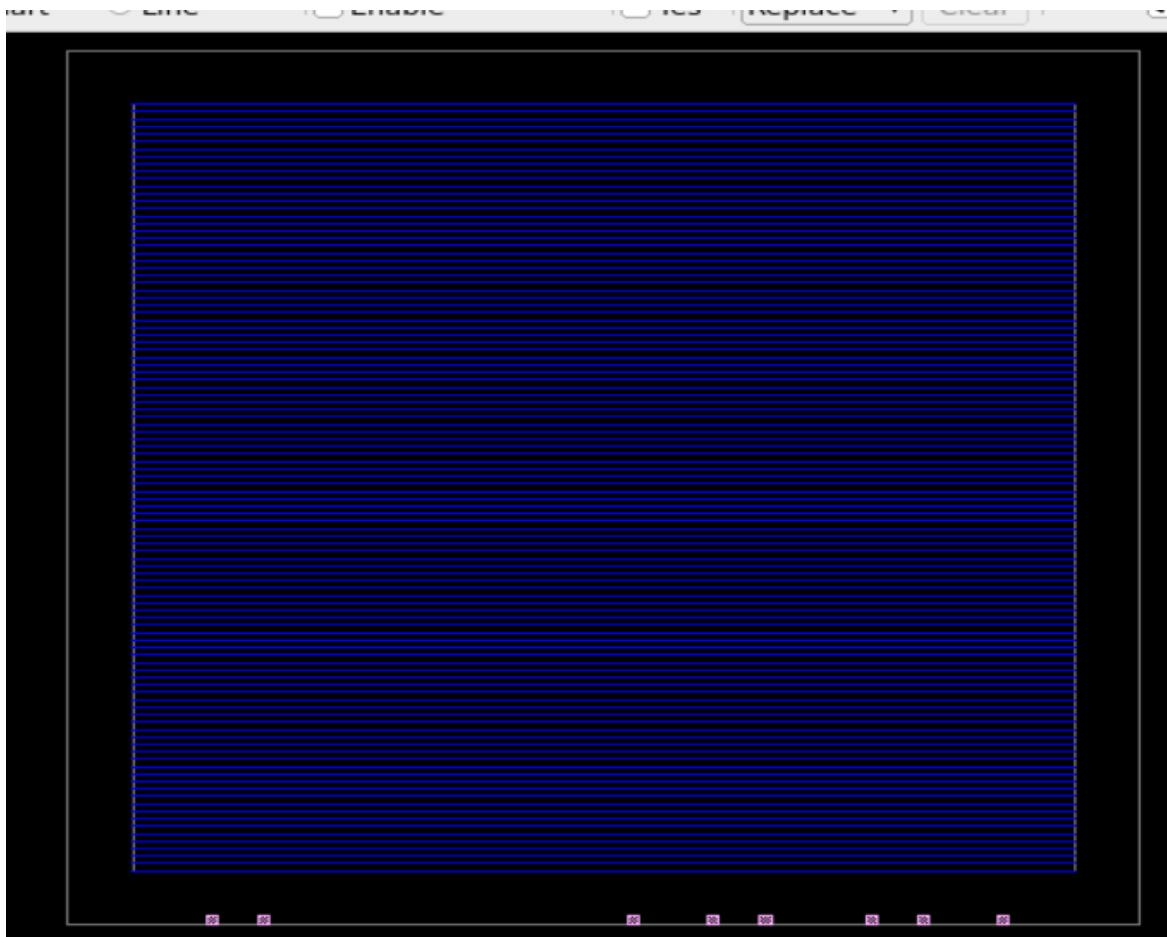
```
create_pg_std_cell_conn_pattern std_cell_rail -layers {M1} -rail_width 0.27
```

- Creates a **standard cell rail pattern** named `std_cell_rail`:
  - Uses **Metal1 (M1)** for rails.
  - Rail width: 0.27  $\mu\text{m}$  (typically matching the standard cell row power rails).

```
set_pg_strategy rail_strategy -core -pattern {{name:std_cell_rail} {nets:VDD VSS}}
```

- Defines a **power strategy** named `rail_strategy` using `std_cell_rail` for VDD/VSS connections to **standard cells** in the core.

```
compile_pg -strategies rail_strategy
```



# Parasitic Scenario and Analysis Setup

## Task 1.1 : Worst-Case Analysis Setup

### 1. Create a Scenario for Worst-Case Analysis:

```
# Define the mode and corner for the worst-case analysis
set mode1 "func"
set corner1 "slow" # Slow corner corresponds to the worst-case scenario
(slowest performance)

# Create the functional mode and the slow corner
create_mode $mode1
create_corner $corner1

# Create a scenario that combines the mode and corner
set scenario1 "${mode1}_${corner1}"
create_scenario -name $scenario1 -mode $mode1 -corner $corner1
```

Explanation:

- Here, you define a "functional" mode (`mode1`) and the "slow" corner (`corner1`), which simulates the worst-case scenario in terms of performance (slowest process corner).
  - Then, you create the scenario (`scenario1`) by combining the mode and corner.
- 

### 2. Set Parasitic Scenario for Max Capacitance Calculation:

```
# Set the parasitic scenario for maximum capacitance calculation
set parasitics "p1"
```

Explanation:

- This sets the parasitic model (`p1`) that will be used for the worst-case analysis, specifically targeting the maximum capacitance (`Cmax`).
- 

### 3. Read One or More Parasitic Model Files (Max Capacitance) in TLUPlus Format:

```
# Read the parasitic model for maximum capacitance (Cmax) in TLUPlus format
read_parasitic_tech -tlup
"/data/pdk/pdk32nm/SAED32_EDK/tech/star_rcxt/saed32nm_1p9m_Cmax.tlupplus" -
layermap
"/data/pdk/pdk32nm/SAED32_EDK/tech/star_rcxt/saed32nm_tf_itf_tlupplus.map" -
name p1
```

Explanation:

- The parasitic model file (in TLUPlus format) is read here. This file contains information about the maximum capacitance ( $C_{max}$ ), and it's crucial for simulating the worst-case scenario in terms of parasitic effects on the design.
- 

#### 4. Set Parasitic Parameters for the Slow Corner:

```
# Set the parasitic parameters for the slow corner (worst-case scenario)
set_parasitic_parameters -late_spec $parasitics -early_spec $parasitics
```

Explanation:

- This sets the parasitic parameters for both the **early** and **late** timing specifications, which will be used during the slow corner analysis. These specifications account for variations in the slowest process corner.
- 

#### 5. Set the Operating Conditions to Check for Worst-Case Analysis:

```
# Set the operating conditions to simulate worst-case analysis
# (e.g., voltage, temperature, process corner settings)
# This might be dependent on the tool and specific conditions you want to
simulate.
set_operating_conditions -max_library
/data/pdk/pdk32nm/SAED32_EDK/lib/stdcell_rvt/db_ccs/saed32rvt_ss0p75v125c.db
```

Explanation:

- In this step, the operating conditions like voltage, temperature, and process corner are set to simulate the worst-case scenario (slow corner, high temperature, etc.). These conditions affect the performance of the design, and adjusting them ensures that the worst-case timing analysis takes them into account.
-

## 6. Set the Analysis Configuration for Worst-Case Scenario:

```
# Configure the analysis tool for the worst-case scenario
set_scenario_status func_slow -hold true -setup true -leakage_power true -
max_capacitance true -min_capacitance true -dynamic_power true -
max_transition true -active true
icc2 shell> report scenarios
*****
Report : scenario
Design : picorv32
Version: V-2023.12-SP4
Date   : Thu May 1 12:34:00 2025
*****
Name      Mode       Corner      Active  Setup  Hold  Leakage Power  Dynamic Power  Max_tran  Max_cap  Min_cap  Cell    Signal
-----  -----  -----  -----  -----  -----  -----  -----  -----  -----  -----  -----  -----  -----  -----
func_slow *  func      slow     true    true   true   true    true   true    true   true   true   false   false
1
icc2 shell>
```

```
Top-Level PVT Settings:
early process label          (none)
early process number          1.01
early voltage                 0.85
  source                      default
  file/line                   --
early temperature              125.00
  source                      default
  file/line                   --
late process label            (none)
late process number           1.01
late voltage                  0.85
  source                      default
  file/line                   --
late temperature               125.00
  source                      default
  file/line                   --
0 objects with explicit PVT settings.

Top-level cell timing derates:
data_cell derate early: rise: 1.00    fall: 1.00
clk_cell derate early:  rise: 1.00    fall: 1.00
cell_check derate early:  rise: 1.00    fall: 1.00
data_cell derate late:   rise: 1.00    fall: 1.00
clk_cell derate late:   rise: 1.00    fall: 1.00
cell_check derate late:  rise: 1.00    fall: 1.00

Global net timing derates:
net_data, early:  rise: 1.00    fall: 1.00
net_data, late:   rise: 1.00    fall: 1.00
net_clock, early: rise: 1.00    fall: 1.00
net_clock, late:  rise: 1.00    fall: 1.00
```

```
*****
Report : mode
Design : picorv32
Version: V-2023.12-SP4
Date  : Thu May 1 12:39:26 2025
*****


-----Mode default-----
-----


Current: false Default: true Empty: false
No scenarios associated with this mode!


-----Mode func-----
-----


Current: true Default: false Empty: false
Scenarios associated with this mode:


Scenario      Corner      Active  Setup   Hold   Leakage Power   Dynamic
                                                               Power
-----func_slow    slow       true    true    true    true    true    true
                                                               true
                                                               true
                                                               true
                                                               false
                                                               false
```

PIN : U5479/Y

8.00

8.01

-----Number of max\_capacitance violation(s): 586

Mode: func Corner: slow  
 Scenario: func\_slow

-----Number of min\_capacitance violation(s): 0

Mode: func  
 Corner: slow  
 Scenario: func\_slow

-----Number of min\_pulse\_width violation(s): 0  
 Total number of violation(s): 1151

Explanation:

- This command configures the analysis tool with the appropriate scenario, parasitics model, and corner (slow corner) to ensure that all the parameters are correctly defined for the worst-case analysis.
- 

## 7. Save as place\_task1:

```
# Save the configuration as place_task1
save_design -name place_task1
```

Explanation:

- Finally, all the configurations, settings, and parameters that have been defined in the previous steps are saved as `place_task1`. This file will be used for the physical design placement step in your flow.
- 

## Summary of Commands in the Script:

1. **Create a scenario for worst-case analysis:** Defined using mode and corner for slowest process corner.
2. **Set parasitic scenario for max capacitance calculation:** Assigned a parasitic model (maximum capacitance).
3. **Read parasitic model files:** Loaded the parasitic data for maximum capacitance in TLUPPlus format.
4. **Set parasitic parameters for the slow corner:** Applied parasitic parameters for the worst-case timing scenario.
5. **Set the operating conditions:** Configured the voltage, temperature, and corner for worst-case performance.
6. **Set the analysis configuration:** Configured the analysis tool to work with the worst-case scenario.
7. **Save as place\_task1:** Saved all the configurations as a task file for placement.

## 1.2 Task 2: Best-Case Scenario Setup (Fast Corner, Minimum Capacitance)

This task configures the design for **best-case timing analysis**, where delays are minimized due to fast transistor behavior and minimum parasitic effects.

### 1. Mode and Corner Creation for Best-Case Analysis

```
set mode2 "func"
```

- Sets a variable `mode2` to "func" which represents the functional mode of the chip (as opposed to test or scan modes).

```
set corner2 "fast"
```

- Defines the process corner as "fast" (best-case scenario where transistors are at their fastest).

```
set scenario2 "${mode2}_${corner2}"
```

- Combines the mode and corner into a scenario name like "func\_fast".

```
create_mode $mode2
```

- Creates the functional mode for the scenario.

```
create_corner $corner2
```

- Creates the fast process corner for best-case timing analysis.

```
create_scenario -name $scenario2 -mode $mode2 -corner $corner2
```

- Combines the created mode and corner into a scenario named "func\_fast".
-

## 2. Set Parasitic Scenario for Minimum Capacitance

```
set parasitics "p2"
```

- Sets a name (p2) for this parasitic extraction environment (for min cap).
- 

## 3. Read TLUPlus Model for Min Capacitance

```
read_parasitic_tech -tlup
"/data/pdk/pdk32nm/SAED32_EDK/tech/star_rcxt/saed32nm_1p9m_Cmin.tlupplus" \
    -layermap
"/data/pdk/pdk32nm/SAED32_EDK/tech/star_rcxt/saed32nm_tf_itf_tlupplus.map" \
    -name $parasitics
```

- Loads the **Cmin TLU+** file (minimum parasitic model) for best-case delay simulation.
  - Also provides the **layer map file**, which maps layers in the layout to the names used in the TLU+ file.
  - Associates this data with the name p2.
- 

## 4. Set Parasitic Parameters

```
set_parasitic_parameters -late_spec $parasitics -early_spec $parasitics
```

- Assigns the same parasitic data (p2) for both **early** (min delay) and **late** (max delay) analysis for this scenario.
  - For best-case, delay is primarily influenced by min parasitic conditions.
- 

## 5. Set Operating Conditions

```
set_operating_conditions -min_library
"/data/pdk/pdk32nm/SAED32_EDK/lib/stdcell_rvt/db_ccs/saed32rvt_ff0p85v125c.db"
"
```

- Specifies the **standard cell library** to use for fast corner simulation.

- `ff0p85v125C` refers to Fast-Fast process at 0.85V and 125°C — typical best-case timing conditions.
- 

## 6. Configure Analysis

```
set_scenario_status $scenario2 -hold true -setup true -leakage_power true \
                     -max_capacitance false -min_capacitance true \
                     -dynamic_power true -max_transition true -active true
```

- Configures what kinds of analyses will be run for the "`func_fast`" scenario:
  - `-hold true` → Perform hold time checks.
  - `-setup true` → Perform setup time checks.
  - `-leakage_power true` → Enable leakage power analysis.
  - `-max_capacitance false` → Do **not** check for max capacitance violations (only min cap).
  - `-min_capacitance true` → Enable min capacitance checks (important in best-case).
  - `-dynamic_power true` → Enable switching (dynamic) power analysis.
  - `-max_transition true` → Check max transition time.
  - `-active true` → Activate this scenario so that it is considered in optimization.

```
icc2_shell> report_scenarios
*****
Report : scenario
Design : picorv32
Version: V-2023.12-SP4
Date   : Thu May 1 15:40:46 2025
*****  
  

          Leakage  Dynamic
Cell  Signal           Mode       Corner     Active  Setup  Hold  Power    Power   Max_tran  Max_cap  Min_cap
Name  Name
EM    EM
-----  

func_fast *    func        fast      true    true  true  true    true   true    false   true  

1
icc2_shell> ■
```

```

-----
Number of max_transition violation(s): 290

Mode: func Corner: fast
Scenario: func_fast
-----
Number of min_capacitance violation(s): 0

Mode: func
Corner: fast
Scenario: func_fast
-----
Number of min_pulse_width violation(s): 0
Total number of violation(s): 290
1
icc2 shell>

```

Group (min_delay/hold)	Cost	Weight	Cost	Scenario
**default**	0.00	1.00	0.00	func_fast
**async_default**	0.00	1.00	0.00	func_fast
**clock_gating_default**	0.00	1.00	0.00	func_fast
**in2reg_default**	0.00	0.10	0.00	func_fast
**reg2out_default**	0.00	0.10	0.00	func_fast
**in2out_default**	0.00	0.10	0.00	func_fast
min_delay/hold			0.00	

Group (max_delay/setup)	Cost	Weight	Cost	Scenario
**default**	0.00	1.00	0.00	func_fast
**async_default**	0.00	1.00	0.00	func_fast
**clock_gating_default**	0.00	1.00	0.00	func_fast
**in2reg_default**	0.00	0.10	0.00	func_fast
**reg2out_default**	0.00	0.10	0.00	func_fast
**in2out_default**	0.00	0.10	0.00	func_fast
max_delay/setup			0.00	

Constraint	Cost
min_delay/hold	0.00 (MET)
max_delay/setup	0.00 (MET)
max_transition	7.27 (VIOLATED)
max_capacitance	0.00 (MET)
min_capacitance	0.00 (MET)

## 7. Save the Design Setup

```
save design -name place task2
```

- Saves the entire scenario configuration and design state with the name `place_task2`.
  - This can later be loaded for placement or further steps like CTS and routing.

### 1.3 Task 3: MCMM Scenario Creation and Analysis

In this task, **Multi-Corner Multi-Mode (MCMM)** analysis is performed. The goal is to validate the design across both **worst-case (slow corner)** and **best-case (fast corner)** scenarios by analyzing timing, power, and transition metrics comprehensively. Here's a breakdown of what this task includes:

- 1. Create MCMM Scenarios for WCS and BCS**
    - Combines both slow and fast corner scenarios in one environment to ensure the design meets constraints under all operating conditions.
    - Typical modes: `func_slow`, `func_fast` (as created in Task 1 and Task 2).
  - 2. Analyze the Design for:**
    - Minimum/Maximum Capacitance:** Ensures the design handles parasitic variation extremes.
    - Setup and Hold Timing Checks:** Verifies correct data arrival time at flip-flops under all conditions.
    - Power Analysis:** Measures dynamic and leakage power under different corners.
    - Transition Checks:** Ensures signal transition times remain within allowed thresholds.
  - 3. Save the Analysis as `place_task3`:**
    - This database saves the results and configuration of MCMM setup and analysis after placement.

```

icc2_shell> report_scenarios
*****
Report : scenario
Design : picorv32
Version: V-2023.12-SP4
Date   : Thu May 1 16:00:59 2025
*****

```

Name	Mode	Corner	Active	Setup	Hold	Leakage Power	Dynamic Power	Max_tran	Max_cap	Min_cap	Cell EM	Signal EM
func_fast *	func	fast	true	true	true	true	true	false	true	false	func	false
func_slow *	func	slow	true	true	true	true	true	true	true	true	func	false

	8.00	8.05	-0
n7039	8.00	8.01	-0
PIN : U5479/Y	8.00	8.01	-0

---

Number of max\_capacitance violation(s): 586

Mode: func Corner: fast  
Scenario: func\_fast

---

Number of min\_capacitance violation(s): 0

Mode: func Corner: slow  
Scenario: func\_slow

---

Number of min\_capacitance violation(s): 0

Mode: func  
Corner: fast  
Scenario: func\_fast

---

Number of min\_pulse\_width violation(s): 0

Mode: func  
Corner: slow  
Scenario: func\_slow

---

Number of min\_pulse\_width violation(s): 0

Total number of violation(s): 1978

### Setup Timing report in func\_fast

Startpoint: cpu\_state\_reg[7] (rising edge-triggered flip-flop clocked by clk)  
 Endpoint: cpuregs\_reg[17][4] (rising edge-triggered flip-flop clocked by clk)  
 Mode: func  
 Corner: fast  
 Scenario: func\_fast  
 Path Group: clk  
 Path Type: max

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
cpu_state_reg[7]/CLK (DFFX1_RVT)	0.00	0.00 r
cpu_state_reg[7]/QN (DFFX1_RVT)	0.07	0.07 r
U4599/Y (NAND3X0_RVT)	0.04	0.12 f
U4600/Y (NOR3X0_RVT)	0.05	0.17 r
U4601/Y (NAND3X0_RVT)	0.09	0.25 f
U4530/Y (INVX1_RVT)	0.04	0.29 r
U4256/Y (AND2X1_RVT)	0.19	0.48 r
U5412/Y (AND2X1_RVT)	0.01	0.49 r
U5414/Y (AND2X1_RVT)	0.05	0.54 r
U5415/Y (AND3X1_RVT)	0.04	0.58 r
U4464/Y (NAND3X0_RVT)	0.70	1.29 f
U4465/Y (INVX1_RVT)	0.66	1.95 r
U8456/Y (A022X1_RVT)	0.06	2.01 r
cpuregs_reg[17][4]/D (DFFX1_RVT)	0.00	2.01 r
data arrival time		2.01
clock clk (rise edge)	2.00	2.00
clock network delay (ideal)	0.00	2.00
cpuregs_reg[17][4]/CLK (DFFX1_RVT)	0.00	2.00 r
library setup time	-0.03	1.97
data required time		1.97
data required time		1.97
data arrival time		-2.01
slack (VIOLATED)		-0.05

## Setup Timing report in func\_slow

Startpoint:	resetn (input port clocked by clk)	
Endpoint:	cpuregs_reg[17][4] (rising edge-triggered flip-flop clocked by clk)	
Mode:	func	
Corner:	slow	
Scenario:	func_slow	
Path Group:	**in2reg_default**	
Path Type:	max	
Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
input external delay	0.50	0.50 r
resetn (in)	0.00	0.50 r
U4256/Y (AND2X1_RVT)	0.23	0.73 r
U5412/Y (AND2X1_RVT)	0.01	0.74 r
U5414/Y (AND2X1_RVT)	0.05	0.79 r
U5415/Y (AND3X1_RVT)	0.05	0.83 r
U4464/Y (NAND3X0_RVT)	0.77	1.60 f
U4465/Y (INVX1_RVT)	0.75	2.34 r
U8456/Y (A022X1_RVT)	0.06	2.41 r
cpuregs_reg[17][4]/D (DFFX1_RVT)	0.00	2.41 r
data arrival time		2.41
clock clk (rise edge)	2.00	2.00
clock network delay (ideal)	0.00	2.00
cpuregs_reg[17][4]/CLK (DFFX1_RVT)	0.00	2.00 r
clock uncertainty	-0.30	1.70
library setup time	-0.03	1.67
data required time		1.67
data required time		1.67
data arrival time		-2.41
slack (VIOLATED)		-0.74

### Hold Timg report in func slow

Startpoint: count_cycle_reg[0] (rising edge-triggered flip-flop clocked by clk)		
Endpoint: count_cycle_reg[0] (rising edge-triggered flip-flop clocked by clk)		
Mode: func		
Corner: slow		
Scenario: func_slow		
Path Group: clk		
Path Type: min		
Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
count_cycle_reg[0]/CLK (DFFX1_RVT)	0.00	0.00 r
count_cycle_reg[0]/QN (DFFX1_RVT)	0.07	0.07 r
U7871/Y (AND2X1_RVT)	0.03	0.09 r
count_cycle_reg[0]/D (DFFX1_RVT)	0.00	0.09 r
data arrival time		0.09
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
count_cycle_reg[0]/CLK (DFFX1_RVT)	0.00	0.00 r
clock uncertainty	0.10	0.10
library hold time	-0.00	0.10
data required time		0.10
-----		
data required time		0.10
data arrival time		-0.09
-----		
slack (VIOLATED)		-0.00

### Hold Time report in func\_fast

Startpoint: count_cycle_reg[0] (rising edge-triggered flip-flop clocked by clk)		
Endpoint: count_cycle_reg[0] (rising edge-triggered flip-flop clocked by clk)		
Mode: func		
Corner: fast		
Scenario: func_fast		
Path Group: clk		
Path Type: min		
Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
count_cycle_reg[0]/CLK (DFFX1_RVT)	0.00	0.00 r
count_cycle_reg[0]/QN (DFFX1_RVT)	0.06	0.06 f
U7871/Y (AND2X1_RVT)	0.03	0.09 f
count_cycle_reg[0]/D (DFFX1_RVT)	0.00	0.09 f
data arrival time		0.09
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
count_cycle_reg[0]/CLK (DFFX1_RVT)	0.00	0.00 r
library hold time	-0.01	-0.01
data required time		-0.01
-----		
data required time		-0.01
data arrival time		-0.09
-----		
slack (MET)		0.10

### 3 COMPARATIVE ANALYSIS

#### ANALYSIS OF DESIGN IN FUNC\_FAST SCENARIO

Startpoint: cpu\_state\_reg[7] (rising edge-triggered flip-flop clocked by clk)  
Endpoint: cpuregs\_reg[17][4] (rising edge-triggered flip-flop clocked by clk)  
Mode: func  
Corner: fast  
Scenario: func\_fast  
Path Group: clk  
Path Type: max

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
cpu_state_reg[7]/CLK (DFFX1_RVT)	0.00	0.00 r
cpu_state_reg[7]/QN (DFFX1_RVT)	0.07	0.07 r
U4599/Y (NAND3X0_RVT)	0.04	0.12 f
U4600/Y (NOR3X0_RVT)	0.05	0.17 r
U4601/Y (NAND3X0_RVT)	0.09	0.25 f
U4530/Y (INVX1_RVT)	0.04	0.29 r
U4256/Y (AND2X1_RVT)	0.19	0.48 r
U5412/Y (AND2X1_RVT)	0.01	0.49 r
U5414/Y (AND2X1_RVT)	0.05	0.54 r
U5415/Y (AND3X1_RVT)	0.04	0.58 r
U4464/Y (NAND3X0_RVT)	0.70	1.29 f
U4465/Y (INVX1_RVT)	0.66	1.95 r
U8456/Y (A022X1_RVT)	0.06	2.01 r
cpuregs_reg[17][4]/D (DFFX1_RVT)	0.00	2.01 r
data arrival time		2.01
clock clk (rise edge)	2.00	2.00
clock network delay (ideal)	0.00	2.00
cpuregs_reg[17][4]/CLK (DFFX1_RVT)	0.00	2.00 r
library setup time	-0.03	1.97
data required time		1.97
data required time		1.97
data arrival time		-2.01
slack (VIOLATED)		-0.05

#### early\_timing

#### o paths.

max_transition	82.69	(VIOLATED)
max_capacitance	12226.93	(VIOLATED)
min_capacitance	0.00	(MET)

## ANALYSIS OF DESIGN IN FUNC\_SLOW SCENARIO

Startpoint: count\_cycle\_reg[0] (rising edge-triggered flip-flop clocked by clk)  
 Endpoint: count\_cycle\_reg[0] (rising edge-triggered flip-flop clocked by clk)  
 Mode: func  
 Corner: slow  
 Scenario: func\_slow  
 Path Group: clk  
 Path Type: min

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
count_cycle_reg[0]/CLK (DFFX1_RVT)	0.00	0.00 r
count_cycle_reg[0]/QN (DFFX1_RVT)	0.07	0.07 r
U7871/Y (AND2X1_RVT)	0.03	0.09 r
count_cycle_reg[0]/D (DFFX1_RVT)	0.00	0.09 r
data arrival time		0.09
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
count_cycle_reg[0]/CLK (DFFX1_RVT)	0.00	0.00 r
clock uncertainty	0.10	0.10
library hold time	-0.00	0.10
data required time		0.10
data required time		0.10
data arrival time		-0.09
slack (VIOLATED)		-0.00
max_transition	82.69	(VIOLATED)
max_capacitance	12226.93	(VIOLATED)
min_capacitance	0.00	(MET)

Congestion Report before placement :

```
*****
Report : congestion
Design : picorv32
Version: V-2023.12-SP4
Date   : Thu May  1 17:22:16 2025
*****
```

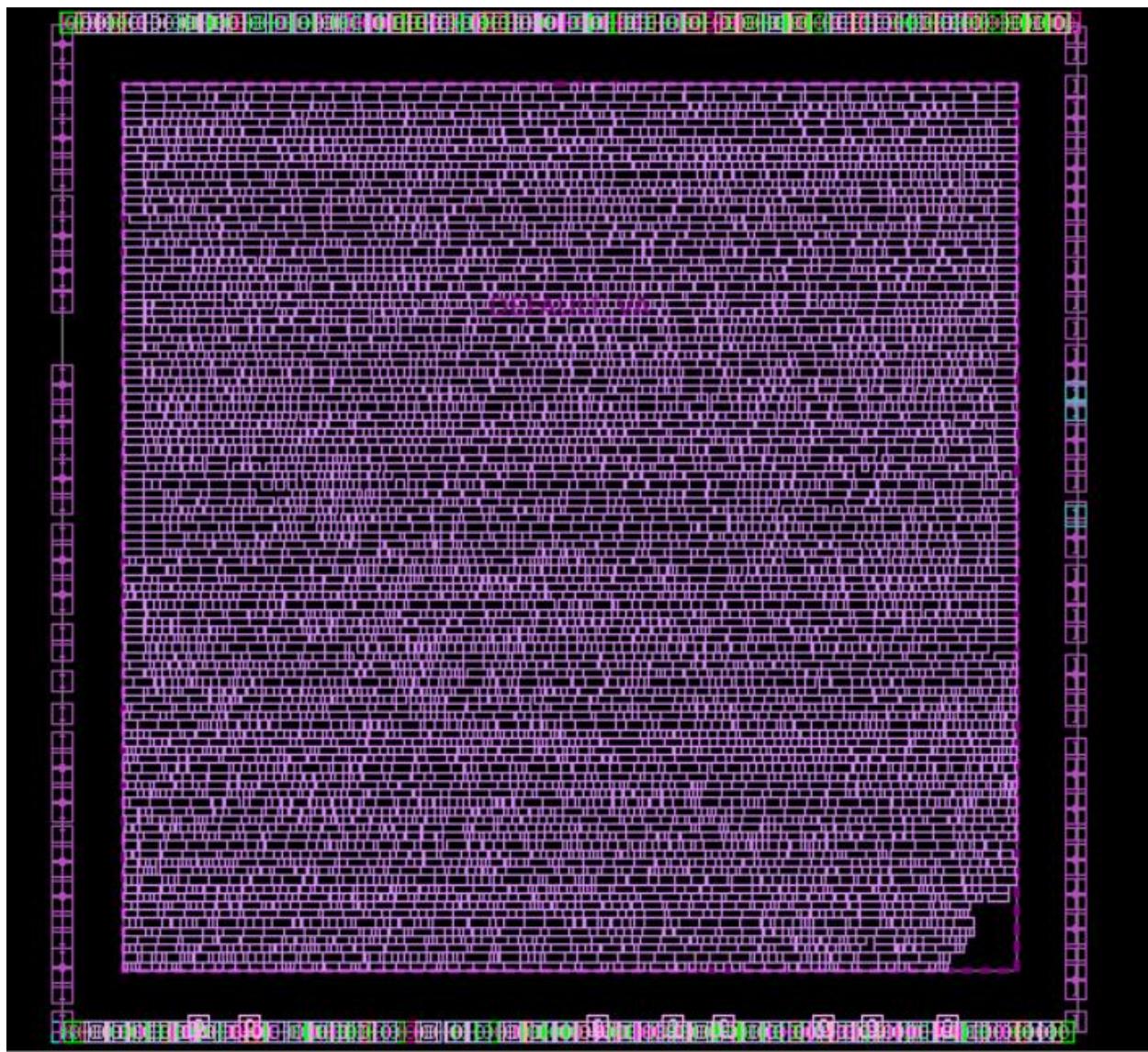
Layer	overflow		# GRCs has		
Name	total	max	overflow (%)		max overflow
Both Dirs	4833	3	4376	(15.85%)	27
H routing	2978	3	2814	(20.38%)	1
V routing	1855	3	1562	(11.31%)	26

1

After placement :

```
*****
Report : congestion
Design : picorv32
Version: V-2023.12-SP4
Date   : Thu May  1 17:41:11 2025
*****
```

Layer	overflow		# GRCs has		
Name	total	max	overflow (%)		max overflow
Both Dirs	6193	5	4894	(17.72%)	3
H routing	4077	4	3393	(24.58%)	3
V routing	2116	5	1501	(10.87%)	3



## Utilization Report :

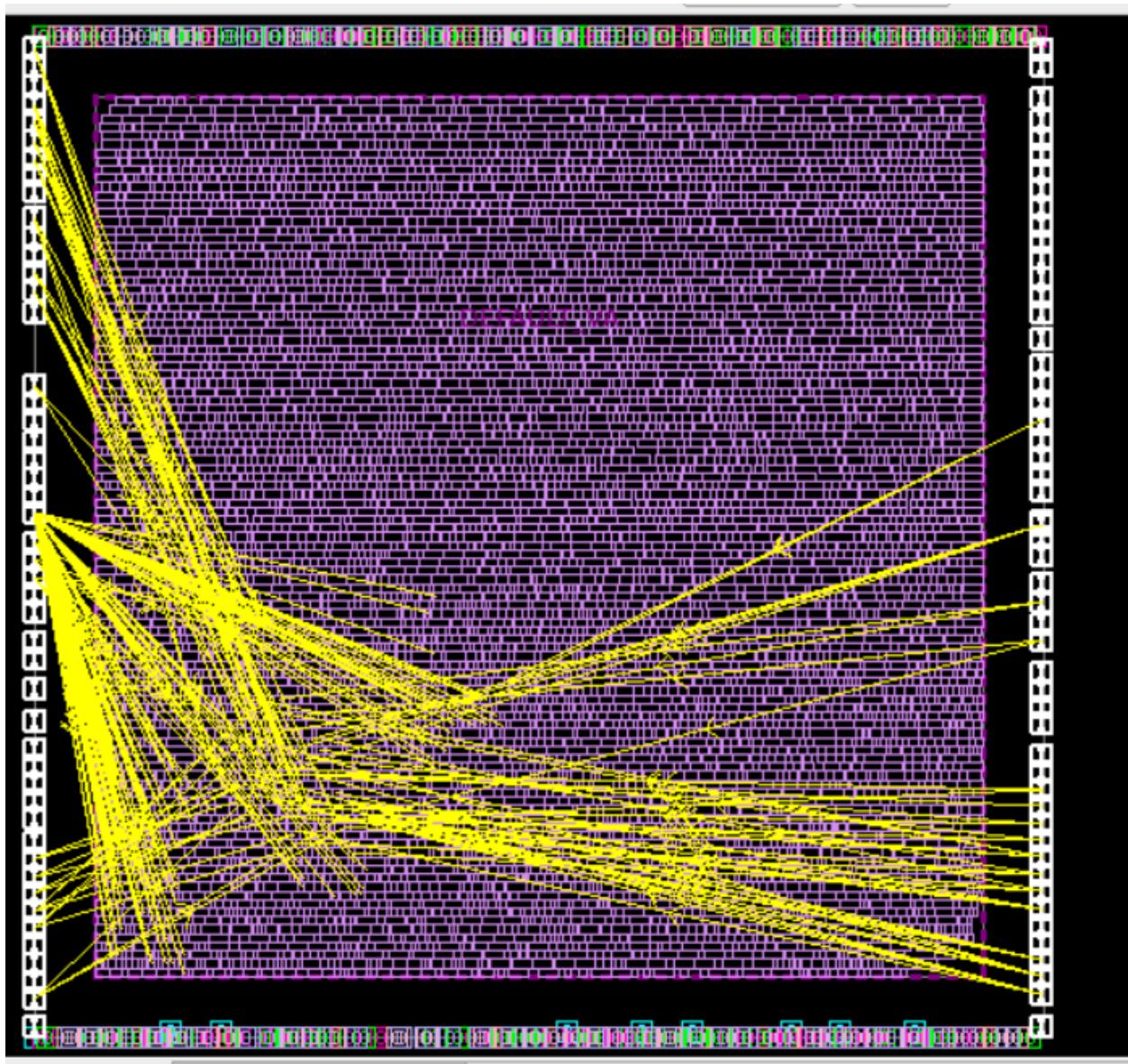
```
*****
Report : report_utilization
Design : picorv32
Version: V-2023.12-SP4
Date   : Thu May  1 17:28:34 2025
*****
Utilization Ratio:          0.8312
Utilization options:
- Area calculation based on:      site_row of block upto_u_blockage
- Categories of objects excluded: hard_macros macro_keepouts soft_macros io_cells hard_blockages
Total Area:                  29920.1190
Total Capacity Area:         29920.1190
Total Area of cells:         24868.7528
Area of excluded objects:
- hard_macros      :      0.0000
- macro_keepouts   :      0.0000
- soft_macros      :      0.0000
- io_cells          :      0.0000
- hard_blockages   :      0.0000
Total Area of excluded objects: 0.0000
Ratio of excluded objects:    0.0000

Utilization of site-rows with:
- Site 'unit':           0.8312
0.8312
```

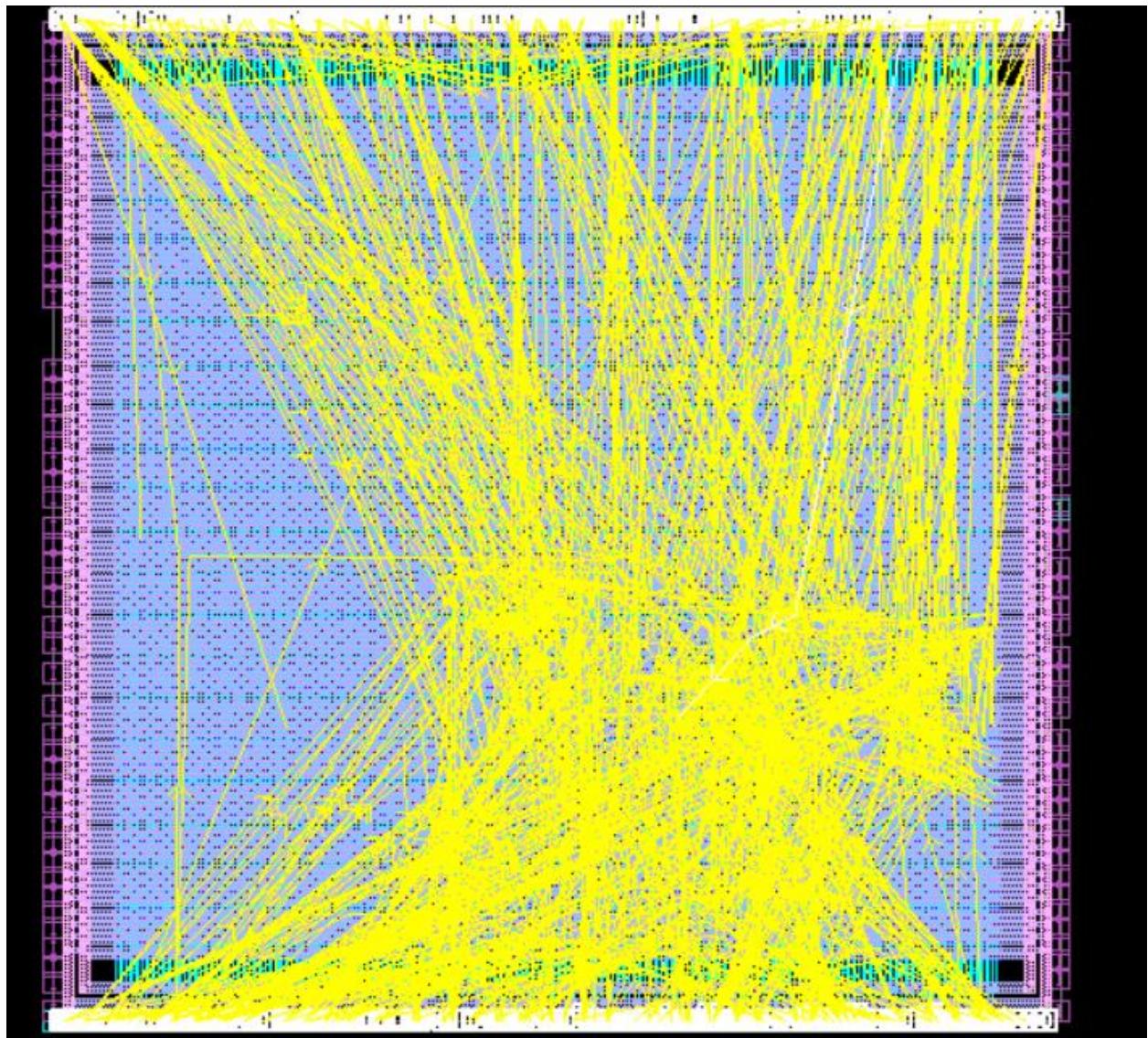
## Number of cells Cells after placement :

reg_pc_reg[25]	DFFX1_RVT	saed32rvt_c	n, S
reg_pc_reg[26]	DFFX1_RVT	saed32rvt_c	n, S
reg_pc_reg[27]	DFFX1_RVT	saed32rvt_c	n, S
reg_pc_reg[28]	DFFX1_RVT	saed32rvt_c	n, S
reg_pc_reg[29]	DFFX1_RVT	saed32rvt_c	n, S
reg_pc_reg[2]	DFFX1_RVT	saed32rvt_c	n, S
reg_pc_reg[30]	DFFX1_RVT	saed32rvt_c	n, S
reg_pc_reg[31]	DFFX1_RVT	saed32rvt_c	n, S
reg_pc_reg[3]	DFFX1_RVT	saed32rvt_c	n, S
reg_pc_reg[4]	DFFX2_RVT	saed32rvt_c	n, S
reg_pc_reg[5]	DFFX1_RVT	saed32rvt_c	n, S
reg_pc_reg[6]	DFFX1_RVT	saed32rvt_c	n, S
reg_pc_reg[7]	DFFX1_RVT	saed32rvt_c	n, S
reg_pc_reg[8]	DFFX1_RVT	saed32rvt_c	n, S
reg_pc_reg[9]	DFFX1_RVT	saed32rvt_c	n, S
reg_sh_reg[0]	DFFX1_RVT	saed32rvt_c	n, S
reg_sh_reg[1]	DFFX1_RVT	saed32rvt_c	n, S
reg_sh_reg[2]	DFFX1_RVT	saed32rvt_c	n, S
reg_sh_reg[3]	DFFX1_RVT	saed32rvt_c	n, S
reg_sh_reg[4]	DFFX1_RVT	saed32rvt_c	n, S
trap_reg	DFFX1_RVT	saed32rvt_c	n, S
-----			
Total 7033 cells			
1			

**Fly-line connections of all inputs to standard cells:**



Fly – line connections of outputs :



Power Report after placement:

Warning: Power table extrapolation (extrapolation mode) for port QN on cell count\_cycle\_reg[59] for parameter linp. Lowest table value = 0.00000 (POW-046)

Note - message 'POW-046' limit (10) exceeded. Remainder will be suppressed.

Warning: Fall toggles on pin count\_cycle\_reg[58]/QN are impossible given input states; converted to rise toggles. (POW-069)

Warning: Fall toggles on pin count\_cycle\_reg[57]/QN are impossible given input states; converted to rise toggles. (POW-069)

Warning: Fall toggles on pin count\_cycle\_reg[56]/QN are impossible given input states; converted to rise toggles. (POW-069)

Warning: Fall toggles on pin count\_cycle\_reg[55]/QN are impossible given input states; converted to rise toggles. (POW-069)

Warning: Fall toggles on pin count\_cycle\_reg[54]/QN are impossible given input states; converted to rise toggles. (POW-069)

Note - message 'POW-069' limit (10) exceeded. Remainder will be suppressed.

Cell Internal Power = 3.14e+09 pW ( 99.0%)

Net Switching Power = 3.02e+07 pW ( 1.0%)

Total Dynamic Power = 3.17e+09 pW (100.0%)

Cell Leakage Power = 5.54e+10 pW

Attributes

u - User defined power group

i - Includes clock pin internal power

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	( % )	Attrs
io_pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00	( 0.0%)	
memory	0.00e+00	0.00e+00	0.00e+00	0.00e+00	( 0.0%)	
black_box	0.00e+00	0.00e+00	0.00e+00	0.00e+00	( 0.0%)	
clock_network	3.19e+09	0.00e+00	0.00e+00	3.19e+09	( 5.4%)	i
register	-3.08e+07	3.00e+06	2.94e+10	2.94e+10	( 50.2%)	
sequential	-3.48e+07	5.51e+05	1.17e+09	1.14e+09	( 1.9%)	
combinational	2.04e+07	2.67e+07	2.48e+10	2.48e+10	( 42.4%)	
Total	3.14e+09 pW	3.02e+07 pW	5.54e+10 pW	5.86e+10 pW		

## Constraints after placement

```

Report : constraint
Design : picorv32
Version: V-2023.12-SP4
Date   : Thu May 1 18:28:28 2025
xxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

                                         Weighted
Group (min_delay/hold)      Cost    Weight    Cost    Scenario
-----
**default**                  0.00    1.00    0.00    func_slow
**async_default**            0.00    1.00    0.00    func_slow
**clock_gating_default**    0.00    1.00    0.00    func_slow
**in2reg_default**          0.00    0.10    0.00    func_slow
**reg2out_default**         0.00    0.10    0.00    func_slow
**in2out_default**          0.00    0.10    0.00    func_slow
clk                          0.09    1.00    0.09    func_slow
**default**                  0.00    1.00    0.00    func_fast
**async_default**            0.00    1.00    0.00    func_fast
**clock_gating_default**    0.00    1.00    0.00    func_fast
**in2reg_default**          0.00    0.10    0.00    func_fast
**reg2out_default**         0.00    0.10    0.00    func_fast
**in2out_default**          0.00    0.10    0.00    func_fast
clk                          0.00    1.00    0.00    func_fast
-----
min_delay/hold                0.09

                                         Weighted
Group (max_delay/setup)      Cost    Weight    Cost    Scenario
-----
**default**                  0.00    1.00    0.00    func_slow
**async_default**            0.00    1.00    0.00    func_slow
**clock_gating_default**    0.00    1.00    0.00    func_slow
**in2reg_default**          0.00    0.10    0.00    func_slow
**reg2out_default**         0.00    0.10    0.00    func_slow
**in2out_default**          0.00    0.10    0.00    func_slow
clk                          0.00    1.00    0.00    func_slow
**default**                  0.00    1.00    0.00    func_fast
**async_default**            0.00    1.00    0.00    func_fast
**clock_gating_default**    0.00    1.00    0.00    func_fast
**in2reg_default**          0.00    0.10    0.00    func_fast
**reg2out_default**         0.00    0.10    0.00    func_fast
**in2out_default**          0.00    0.10    0.00    func_fast
clk                          0.00    1.00    0.00    func_fast
-----
max_delay/setup                0.00

                                         Cost
Constraint
-----
min_delay/hold                  0.09 (VIOLATED)
max_delay/setup                 0.00 (MET)
max_transition                  0.00 (MET)
max_capacitance                 0.00 (MET)
min_capacitance                  0.00 (MET)

```

## 4 CLOCK TREE SYNTHESIS

### 4.1 TASK 1 :

#### FLOORPLAN & PIN PLACEMENT

```
initialize_floorplan -side_length {300 150} -control_type die -core_offset 15
```

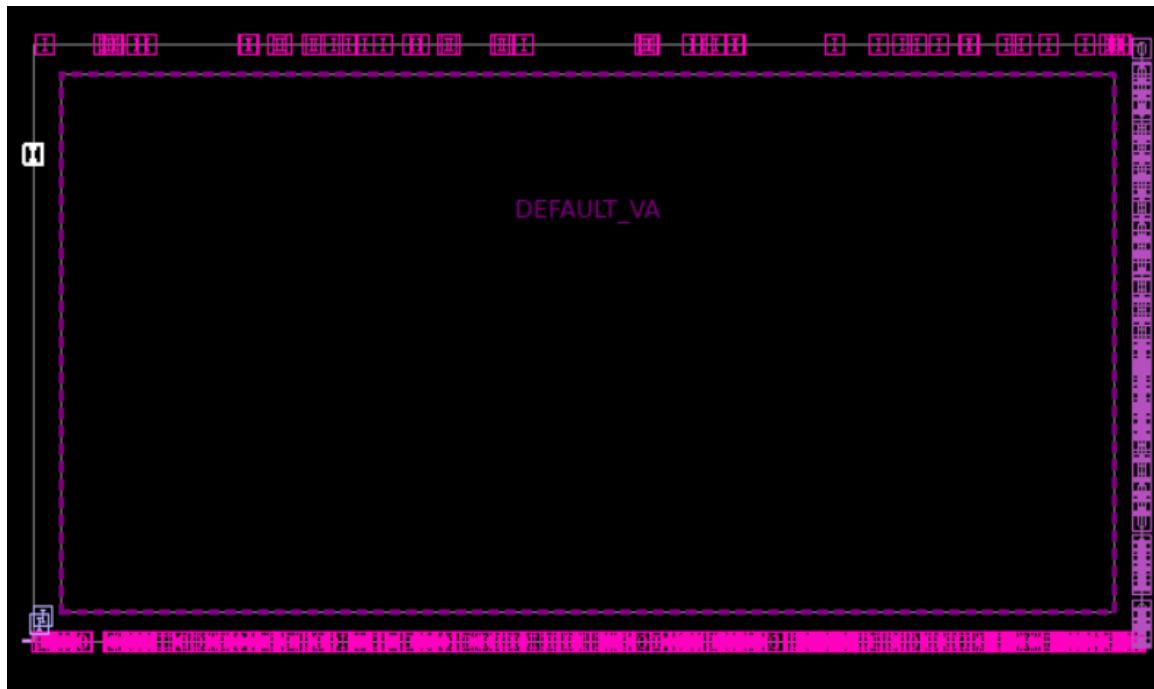
- Creates a **2:1 aspect ratio die** with core offset of 15 units on all sides.

```
set_individual_pin_constraints -ports clk -sides {1}  
set_individual_pin_constraints -ports [remove_from_collection [all_inputs] clk] -sides {2 4}  
set_individual_pin_constraints -ports [all_outputs] -sides {3 4}
```

- clk is placed on side 1 (shorter side).
- Inputs (excluding clk) are placed on sides 2 and 4.
- Outputs on sides 3 and 4.

```
place_pins -ports [all_outputs]  
place_pins -ports [remove_from_collection [all_inputs] clk]  
place_pins -ports clk
```

- Places the pins accordingly.



---

## POWER PLANNING

```
connect_pg_net -automatic -pg
```

- Connects power (VDD) and ground (VSS) nets automatically.

```
create_shape -shape_type rect -layer M8 -boundary {{0 8.299} {7.433 10.04}} -port VSS  
create_shape -shape_type rect -layer M8 -boundary {{0 12.299} {10.89 14.089}} -port VDD
```

- Creates **manual power stripes** on M8 for VSS and VDD.

② Rings

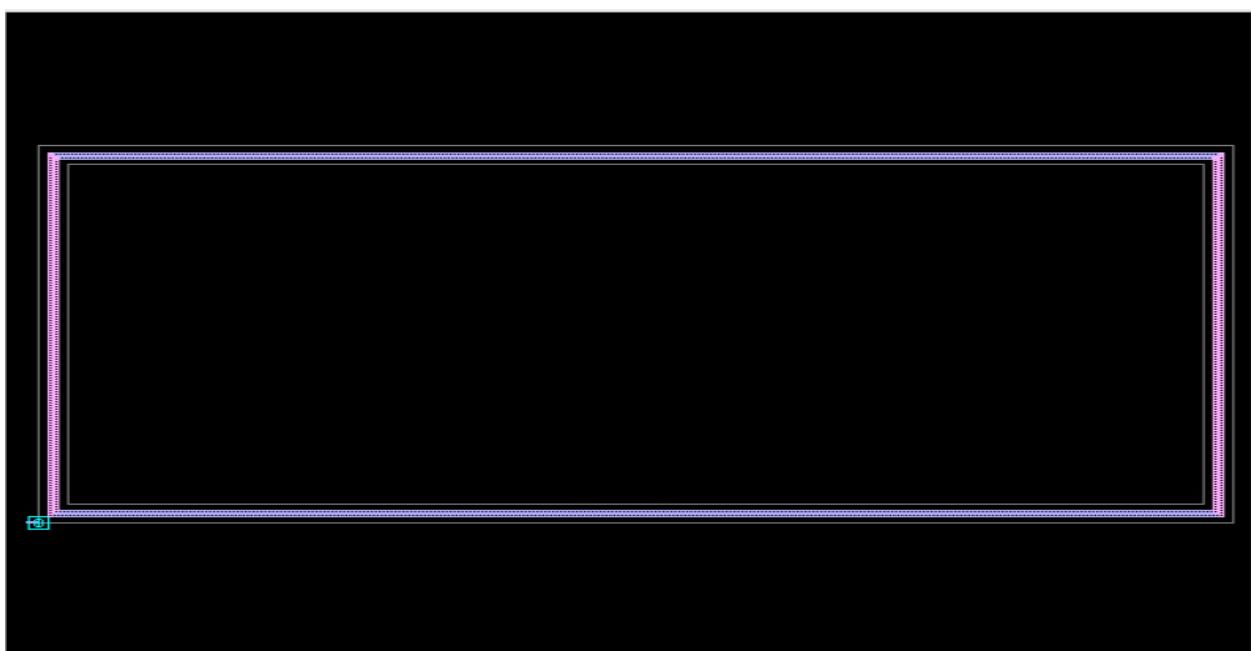
```
create_pg_ring_pattern core_ring -horizontal_layer M8 -horizontal_width 2 -horizontal_spacing 1.
```

```
-vertical_layer M9 -vertical_width 2 -vertical_spacing 1.2
```

```
set_pg_strategy ring_strategy -core -pattern {{name:core_ring} {nets:{VDD VSS}} {offset:{5 4.5}}}
```

```
compile_pg -strategies ring_strategy
```

- Creates and applies a **core ring** with M8/M9 layers.



\

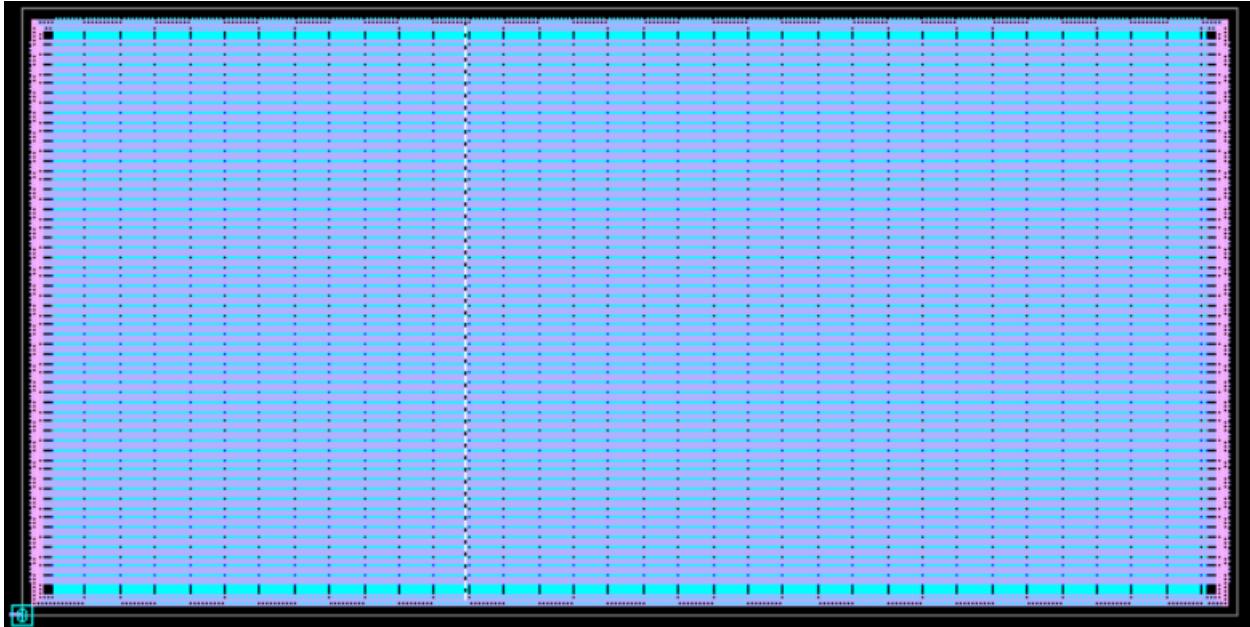
## Mesh

```
create_pg_mesh_pattern mesh -layers {{vertical_layer:M7} {width:0.78} {spacing:interleaving} {pitch:2.1} {offset:0.7}} {{horizontal_layer:M8} {width:0.8} {spacing:interleaving} {pitch:2.5} {offset:0.8}}
```

```
set_pg_strategy core_mesh -pattern {{pattern:mesh} {nets:VDD VSS}} -extension {{direction: T L R B} {stop:innermost_ring}} -core
```

```
compile_pg -strategies core_mesh
```

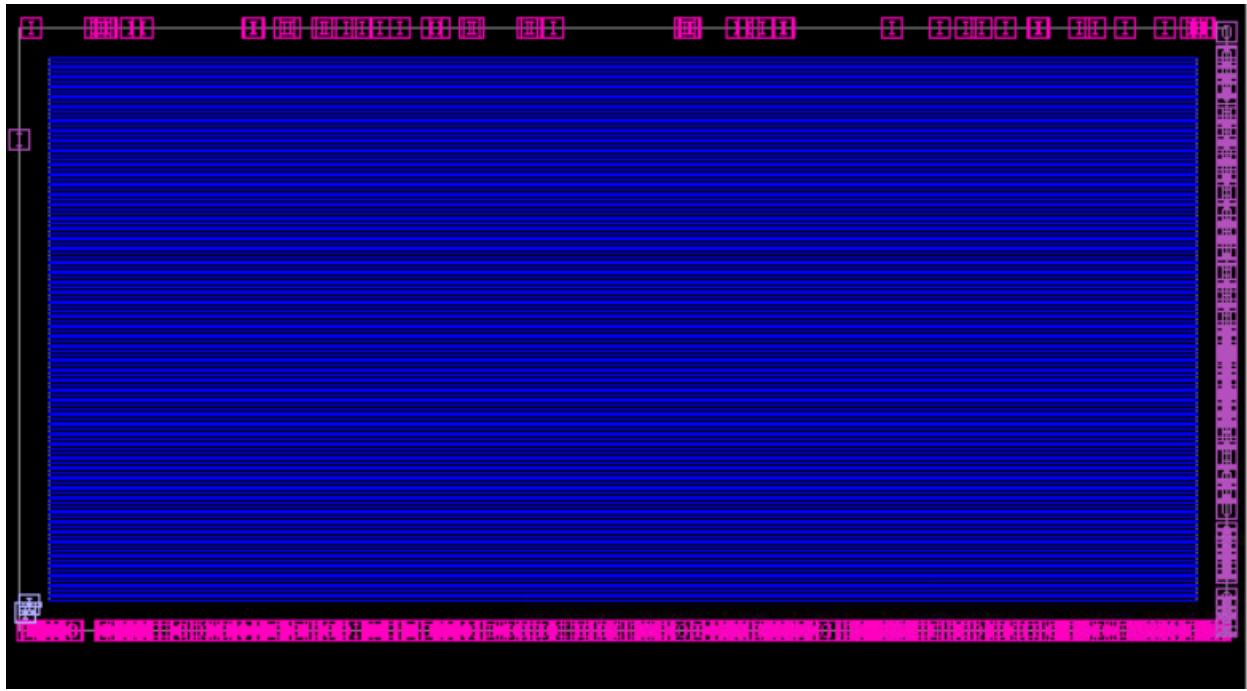
- Adds a **power mesh** using M7 and M8 for robustness.



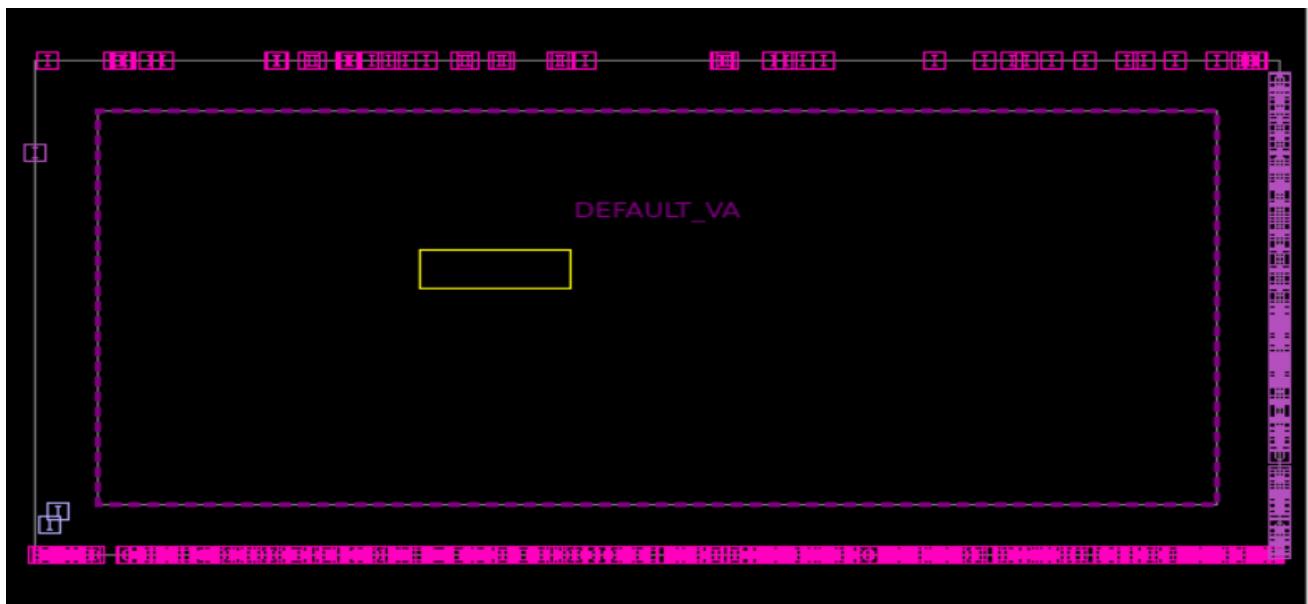
## Rail

```
create_pg_std_cell_conn_pattern std_cell_rail -layers {M1} -rail_width 0.27  
set_pg_strategy rail_strategy ...  
compile_pg -strategies rail_strategy
```

- Ensures **power rail connectivity** at the standard cell level using M1.



Hard Blockage:



```

Number of Macro Cells: 0
Number of IO Pad Cells: 0
Number of Blocks: 0
Loading P/G wires and vias...
Number of VDD Wires: 221
Number of VDD Vias: 34415
Number of VDD Terminals: 1
*****Verify net VDD connectivity*****
  Number of floating wires: 0
  Number of floating vias: 0
  Number of floating std cells: 0
  Number of floating hard macros: 0
  Number of floating I/O pads: 0
  Number of floating terminals: 0
  Number of floating hierarchical blocks: 0
*****
Loading cell instances...
Loading P/G wires and vias...
Number of VSS Wires: 446
Number of VSS Vias: 34158
Number of VSS Terminals: 107
*****Verify net VSS connectivity*****
  Number of floating wires: 0
  Number of floating vias: 0
  Number of floating std cells: 0
  Number of floating hard macros: 0
  Number of floating I/O pads: 0
  Number of floating terminals: 0
  Number of floating hierarchical blocks: 0
*****
Overall runtime: 0 seconds.
soc2 shell> 

```

## PLACEMENT OPT OPTIONS

```

read_sdc ./PICO_RV/pico.sdc
set_app_options -name place.coarse.continue_on_missing_scandef -value true
...
set_app_options -name place_opt.place.congestion_effort -value high

```

- Reads timing constraints.
- Enables clock-aware placement and congestion-driven options.

## SCENARIO SETUP (WC + BC)

WC - slow corner

```
set mode1 "func"
set corner1 "slow"
create_mode $mode1
create_corner $corner1
create_scenario -name ${mode1}_${corner1} ...
read_parasitic_tech -tlup ...Cmax...
set_parasitic_parameters ...
set_scenario_status func_slow ...
```

BC - fast corner

```
set mode2 "func"
set corner2 "fast"
create_mode $mode2
create_corner $corner2
create_scenario -name ${mode2}_${corner2} ...
read_parasitic_tech -tlup ...Cmin...
set_parasitic_parameters ...
set_scenario_status func_fast ...
```

Operating conditions

```
set_operating_conditions -max_library ...ss0p75v125c.db -min_library ...ff0p85v125c.db
```

---

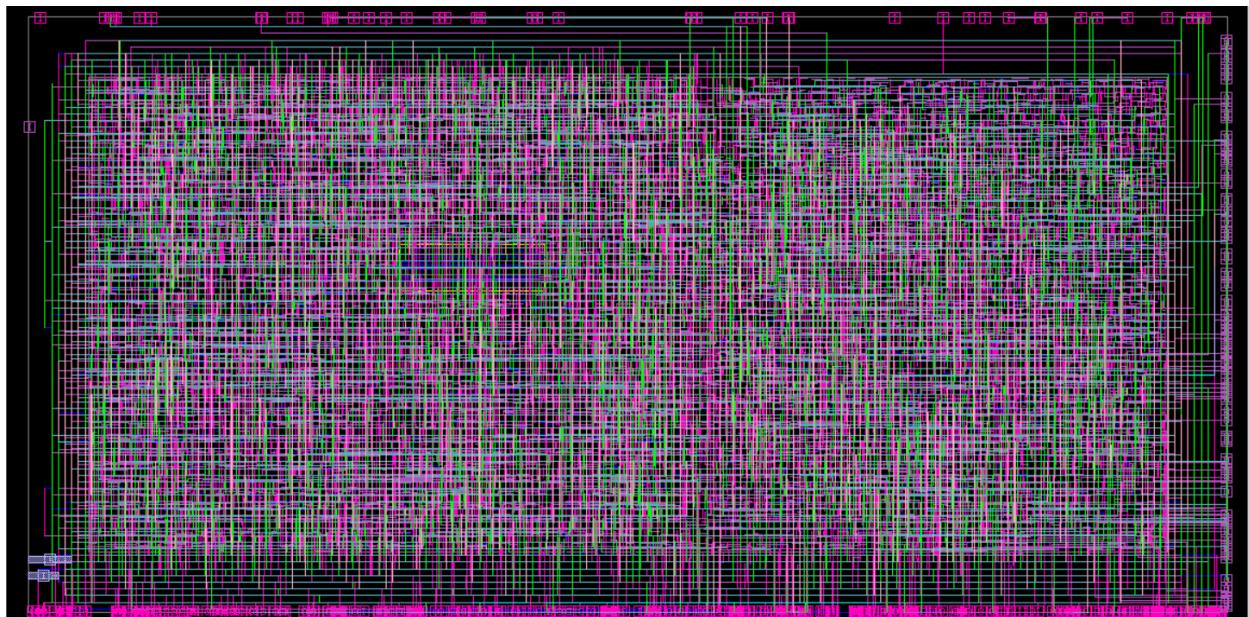
## CTS (Clock Tree Synthesis)

```
set_clock_routing_rules -min_routing_layer M3 -max_routing_layer M4 -default_rule
synthesize_clock_trees
clock_opt
```

- Performs **clock tree synthesis and optimization**, using M3–M4



Signal route track:



## 5.1 Routing of CTS TASK 1

### ROUTING

```
set_app_options -name route.global.timing_driven -value true
...
route_global
route_track
route_detail
```

- Enables timing/crosstalk-driven global, track, and detailed routing.
- Also enables **antenna diode fixing**.

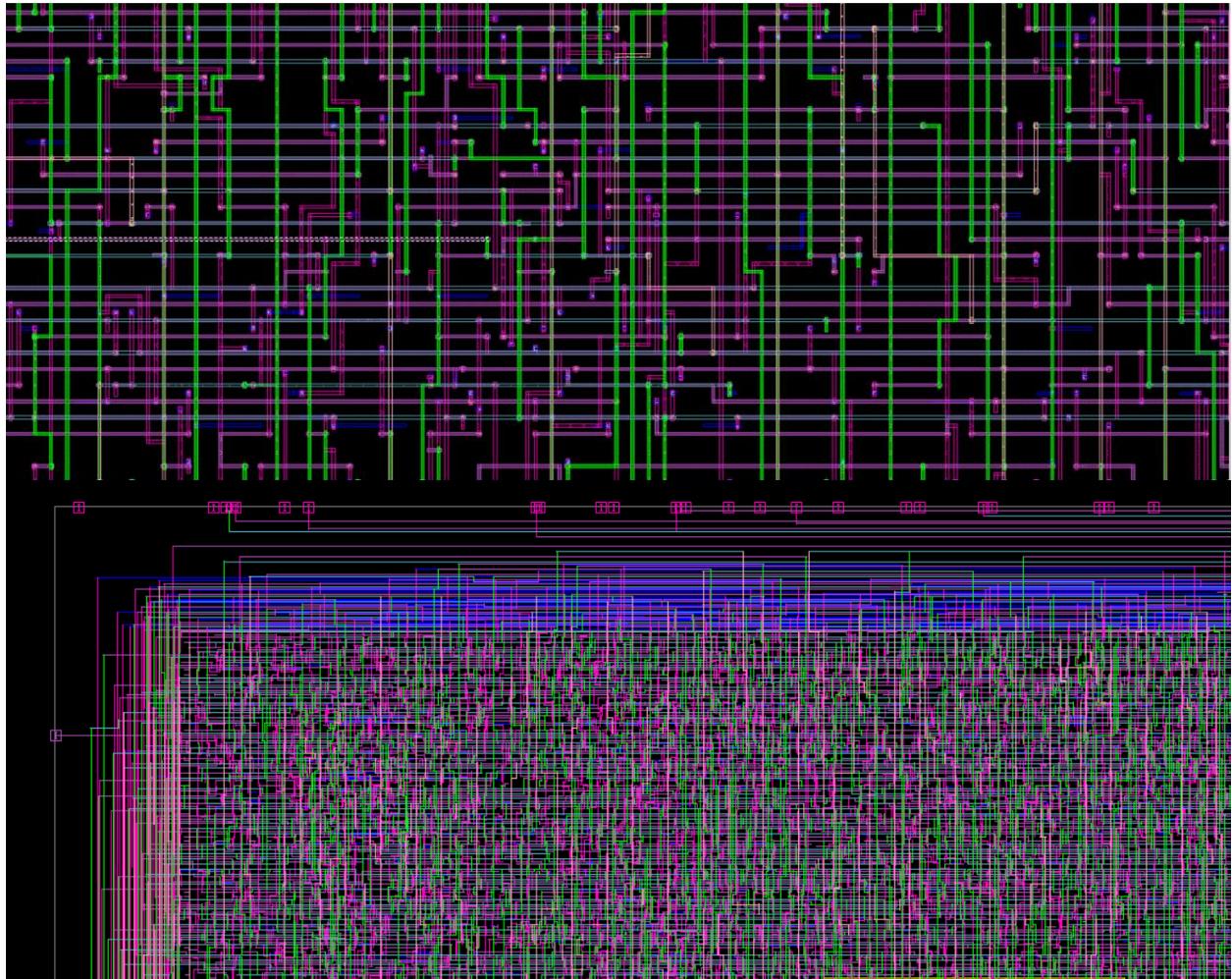
```
set_app_options -block [current_design] -name
route.detail.diode_libcell_names -value {*ANTENNA_RVT*}
```

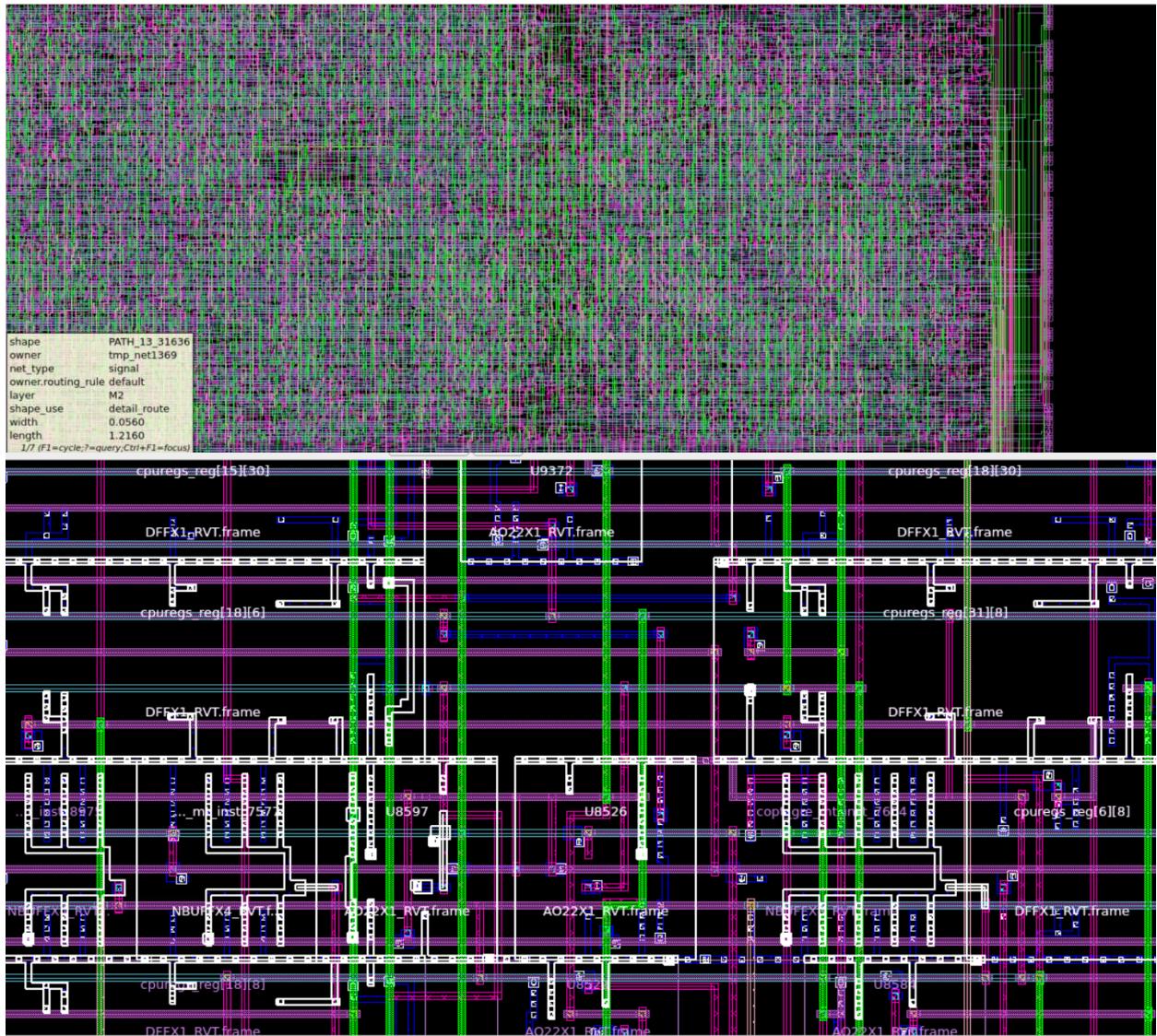
- Tells the tool to use specific **antenna diode cells**.
- 

## ROUTE OPTIMIZATION

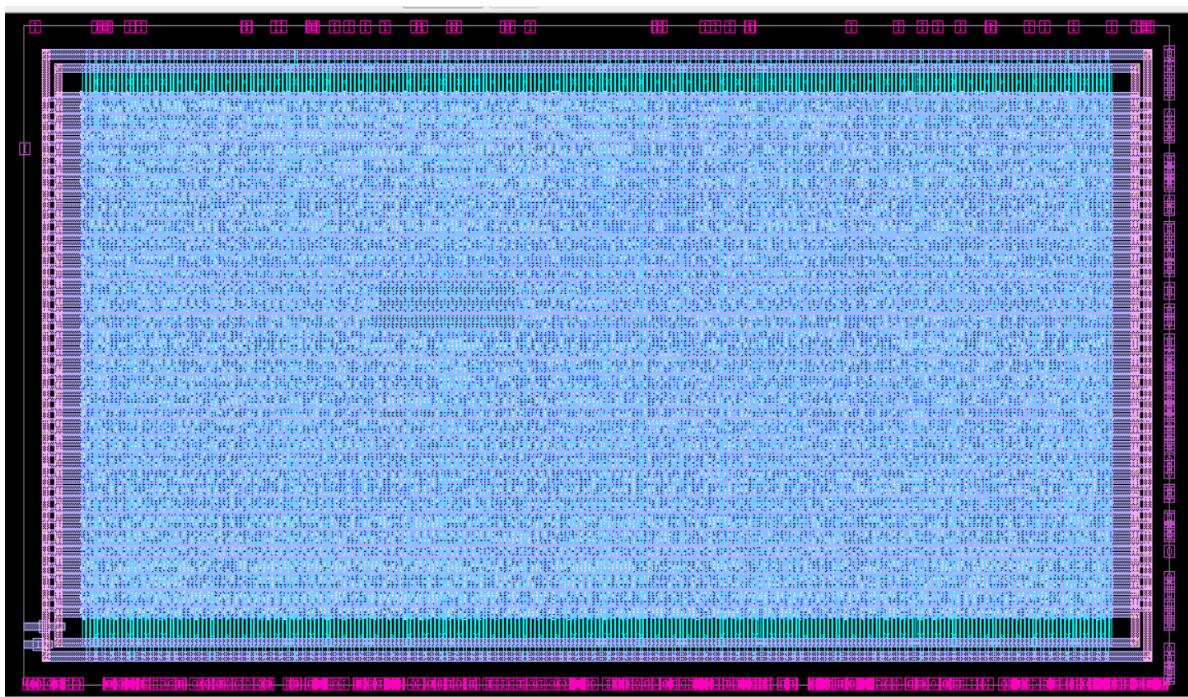
```
set_app_options -name route_opt.flow.enable_ccd -value true  
route_opt
```

- Performs post-route **route optimization** with CCD (congestion cost delay) enabled.





## Final View of Design:



**Reports : Setup Timing report Func\_slow :**

```

Startpoint: latched_store_reg (rising edge-triggered flip-flop clocked by clk)
Endpoint: reg_next_pc_reg[31] (rising edge-triggered flip-flop clocked by clk)
Mode: func
Corner: slow
Scenario: func_slow
Path Group: clk
Path Type: max

Point                                              Incr      Path
-----
clock clk (rise edge)                           0.00      0.00
clock network delay (propagated)                0.17      0.17

latched_store_reg/CLK (DFFX1_RVT)              0.00      0.17 r
latched_store_reg/Q (DFFX1_RVT)                0.09      0.25 r
U4591/Y (AND2X2_RVT)                          0.05      0.30 r
HFSINV_1119_677/Y (INVX4_RVT)                 0.03      0.33 f
U4592/Y (OR2X2_RVT)                           0.04      0.37 f
HFSINV_1694_533/Y (INVX2_RVT)                 0.04      0.40 r
U4605/Y (A0222X1_RVT)                         0.08      0.49 r
U4606/Y (NAND2X0_RVT)                         0.04      0.53 f
U4482/Y (OAI21X1_RVT)                         0.08      0.61 r
ctmTdsLR_2_2492/Y (INVX0_RVT)                 0.01      0.62 f
ctmTdsLR_3_2493/Y (OA221X1_RVT)               0.06      0.68 f
ctmTdsLR_2_1548/Y (OAI221X2_RVT)              0.07      0.75 r
ctmTdsLR_2_2227/Y (INVX0_RVT)                 0.02      0.76 f
ctmTdsLR_3_2228/Y (OAI221X2_RVT)              0.06      0.82 r
U6477/C0 (FADDX1_RVT)                         0.05      0.88 r
U6472/C0 (FADDX1_RVT)                         0.05      0.93 r
U6434/C0 (FADDX1_RVT)                         0.05      0.98 r
U6470/C0 (FADDX1_RVT)                         0.06      1.04 r
U6468/C0 (FADDX1_RVT)                         0.05      1.10 r
U6466/C0 (FADDX1_RVT)                         0.06      1.15 r
U6464/C0 (FADDX1_RVT)                         0.06      1.21 r
U5283/C0 (FADDX1_RVT)                         0.06      1.27 r
U5291/C0 (FADDX1_RVT)                         0.05      1.32 r
U6462/C0 (FADDX1_RVT)                         0.05      1.38 r
U5332/C0 (FADDX1_RVT)                         0.06      1.44 r
U6460/C0 (FADDX1_RVT)                         0.06      1.49 r
U6458/C0 (FADDX1_RVT)                         0.05      1.55 r
U6456/C0 (FADDX1_RVT)                         0.05      1.60 r
U6454/C0 (FADDX1_RVT)                         0.06      1.66 r
U6452/C0 (FADDX1_RVT)                         0.06      1.72 r
U6450/C0 (FADDX1_RVT)                         0.05      1.77 r
U4510/Y (XOR2XI_RVT)                          0.04      1.81 r
ctmTdsLR_3_1426/Y (A0222X1_RVT)               0.05      1.86 r
reg_next_pc_reg[31]/0 (DFFX1_RVT)              0.00      1.86 r
data arrival time                                1.86

clock clk (rise edge)                           2.00      2.00
clock network delay (propagated)                0.16      2.16
reg_next_pc_reg[31]/CLK (DFFX1_RVT)             0.00      2.16 r
clock uncertainty                               -0.30     1.86
library setup time                            -0.02     1.83
data required time                            1.83
-----
data required time                            1.83
data arrival time                             -1.86
-----
slack (VIOLATED)                            -0.03

```

holdTiming report Func\_slow :

*****		
Startpoint: count_cycle_reg[0] (rising edge-triggered flip-flop clocked by clk)		
Endpoint: count_cycle_reg[0] (rising edge-triggered flip-flop clocked by clk)		
Mode: func		
Corner: slow		
Scenario: func_slow		
Path Group: clk		
Path Type: min		
Point	Incr	Path
-----		
clock clk (rise edge)	0.00	0.00
clock network delay (propagated)	0.16	0.16
count_cycle_reg[0]/CLK (DFFX1_RVT)	0.00	0.16 r
count_cycle_reg[0]/QN (DFFX1_RVT)	0.07	0.22 f
U7871/Y (AND2X2_RVT)	0.04	0.26 f
count_cycle_reg[0]/D (DFFX1_RVT)	0.00	0.26 f
data arrival time		0.26
clock clk (rise edge)	0.00	0.00
clock network delay (propagated)	0.16	0.16
count_cycle_reg[0]/CLK (DFFX1_RVT)	0.00	0.16 r
clock uncertainty	0.10	0.26
library hold time	-0.00	0.26
data required time		0.26
-----		
data required time		0.26
data arrival time		-0.26
-----		
slack (MET)		0.00

### Hold Timing report Func\_fast :

```

Report : timing
  -path_type full
  -delay_type min
  -max_paths 1
  -report_by design
Design : picorv32
Version: V-2023.12-SP4
Date   : Thu May  1 23:56:41 2025
xxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

Startpoint: count_cycle_reg[0] (rising edge-triggered flip-flop clocked by clk)
Endpoint: count_cycle_reg[0] (rising edge-triggered flip-flop clocked by clk)
Mode: func
Corner: fast
Scenario: func_fast
Path Group: clk
Path Type: min

Point                               Incr      Path
-----
clock clk (rise edge)              0.00      0.00
clock network delay (propagated)  0.14      0.14

count_cycle_reg[0]/CLK (DFFX1_RVT) 0.00      0.14 r
count_cycle_reg[0]/QN (DFFX1_RVT)  0.07      0.20 f
U7871/Y (AND2X2_RVT)              0.04      0.24 f
count_cycle_reg[0]/D (DFFX1_RVT)   0.00      0.24 f
data arrival time                 0.24

clock clk (rise edge)              0.00      0.00
clock network delay (propagated)  0.14      0.14
count_cycle_reg[0]/CLK (DFFX1_RVT) 0.00      0.14 r
library hold time                 -0.00     0.14
data required time                0.14

data required time                 0.14
data arrival time                 -0.24

slack (MET)                       0.10

```

### Congetion report :

Layer Name	overflow			# GRCs has	
	total	max	overflow (%)	max	overflow
Both Dirs	2650	3	2426 ( 7.61%)	12	
H routing	1047	2	1037 ( 6.51%)	10	
V routing	1603	3	1389 ( 8.72%)	12	

HFSNET_260	16.00	16.11	-0.11	(VIOLATED)
PIN : HFSBUF_339_283/Y	16.00	16.11	-0.11	(VIOLATED)
HFSNET_510	16.00	16.05	-0.05	(VIOLATED)
PIN : HFSBUF_1361_572/Y	16.00	16.05	-0.05	(VIOLATED)

-----

Number of max\_capacitance violation(s): 50

Mode: func Corner: fast  
Scenario: func\_fast

-----

Number of min\_capacitance violation(s): 0

Mode: func  
Corner: fast  
Scenario: func\_fast

-----

Number of min\_pulse\_width violation(s): 0  
Total number of violation(s): 57

mem_la_addr[7]	16.00	16.01	-0
PIN : U4389/Y	16.00	16.01	-0

-----

Number of max\_capacitance violation(s): 180

Mode: func Corner: slow  
Scenario: func\_slow

-----

Number of min\_capacitance violation(s): 0

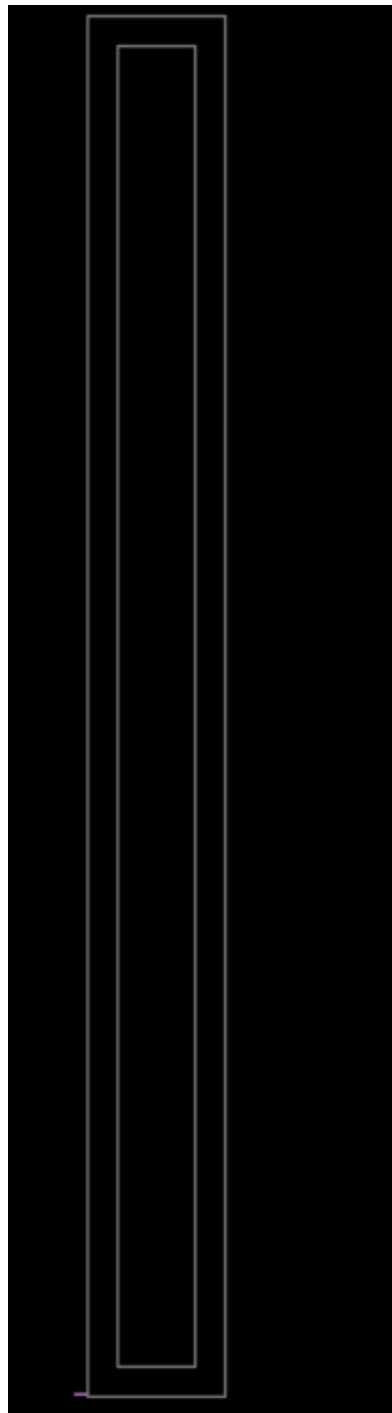
Mode: func  
Corner: slow  
Scenario: func\_slow

-----

Number of min\_pulse\_width violation(s): 0  
Total number of violation(s): 200

## 4.2 TASK 2 CTS :

```
initialize_floorplan -side_length {68 680 } -control_type die -core_offset 15
```



```
set_individual_pin_constraints -ports clk -sides {3}
```

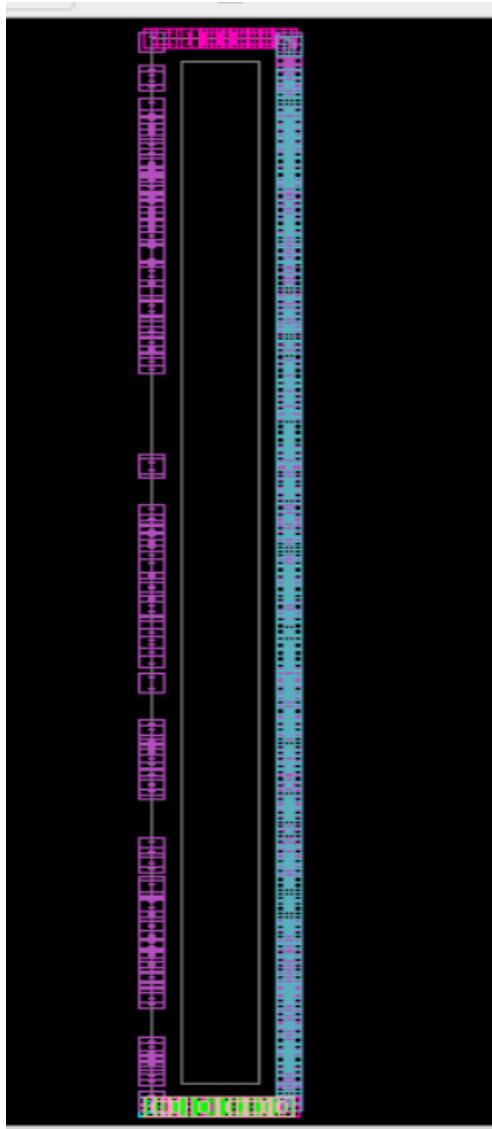
```
set_individual_pin_constraints -ports [remove_from_collection [all_inputs] clk] -sides {1 2 }

set_individual_pin_constraints -ports [all_outputs] -sides {3 4}

place_pins -ports [all_outputs]

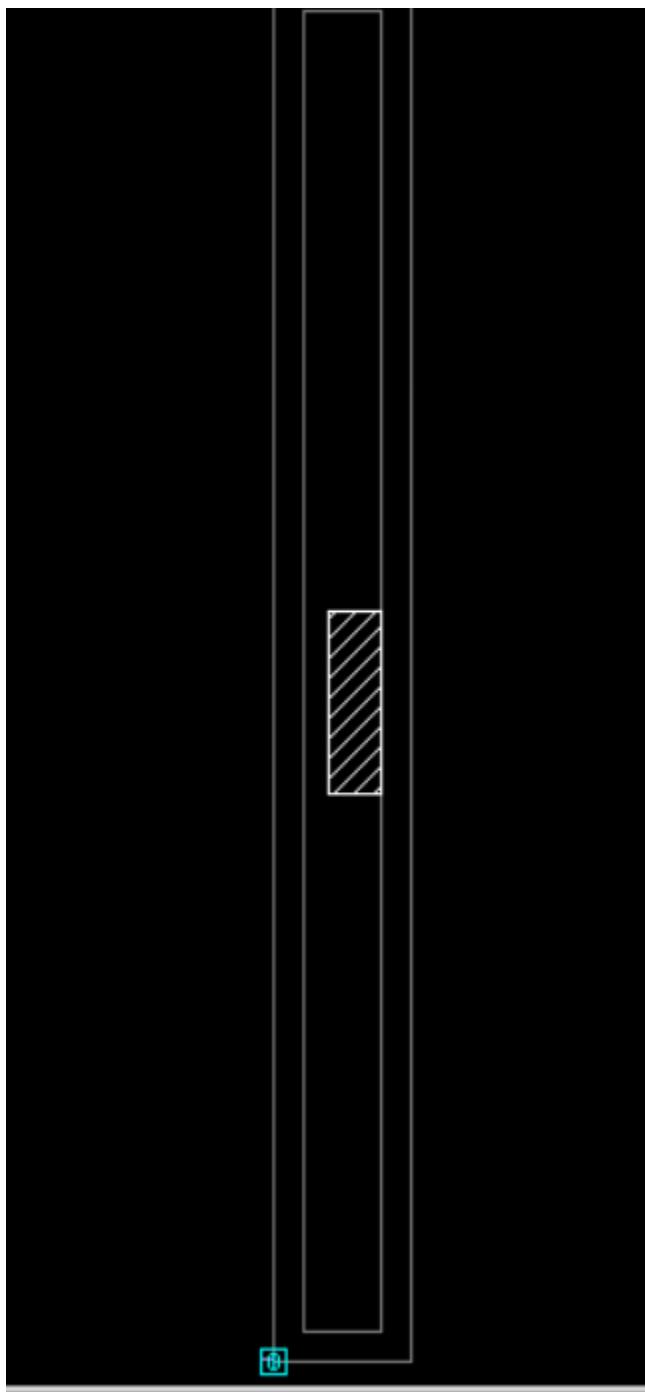
place_pins -ports [remove_from_collection [all_inputs] clk]

place_pins -ports clk
```



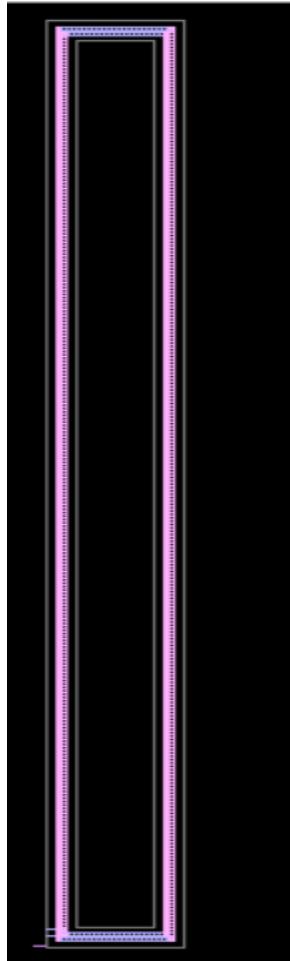
```
connect_pg_net -automatic -pg
```

#Create a partial blockage with 60 percent cell density



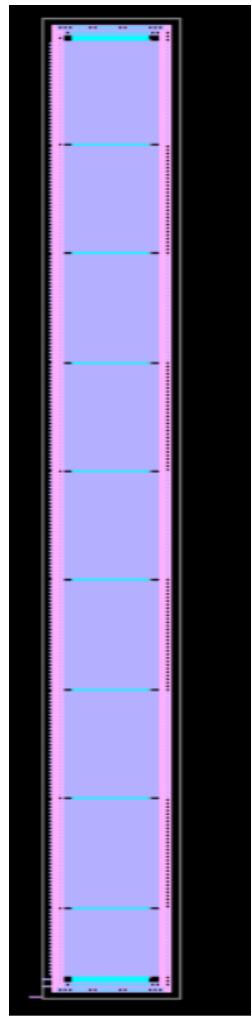
```
create_shape -shape_type rect -layer M8 -boundary {{0 8.299} {7.433 10.04}} -port VSS
```

```
create_shape -shape_type rect -layer M8 -boundary {{0 12.299} {10.89 14.089}} -port VDD  
create_pg_ring_pattern core_ring \  
-horizontal_layer M8 -horizontal_width 2 -horizontal_spacing 1. \  
-vertical_layer M9 -vertical_width 2 -vertical_spacing 1.2
```



```
set_pg_strategy ring_strategy -core -pattern {{name:core_ring} {nets:{VDD VSS}} {offset:{5  
4.5}}}  
compile_pg -strategies ring_strategy
```

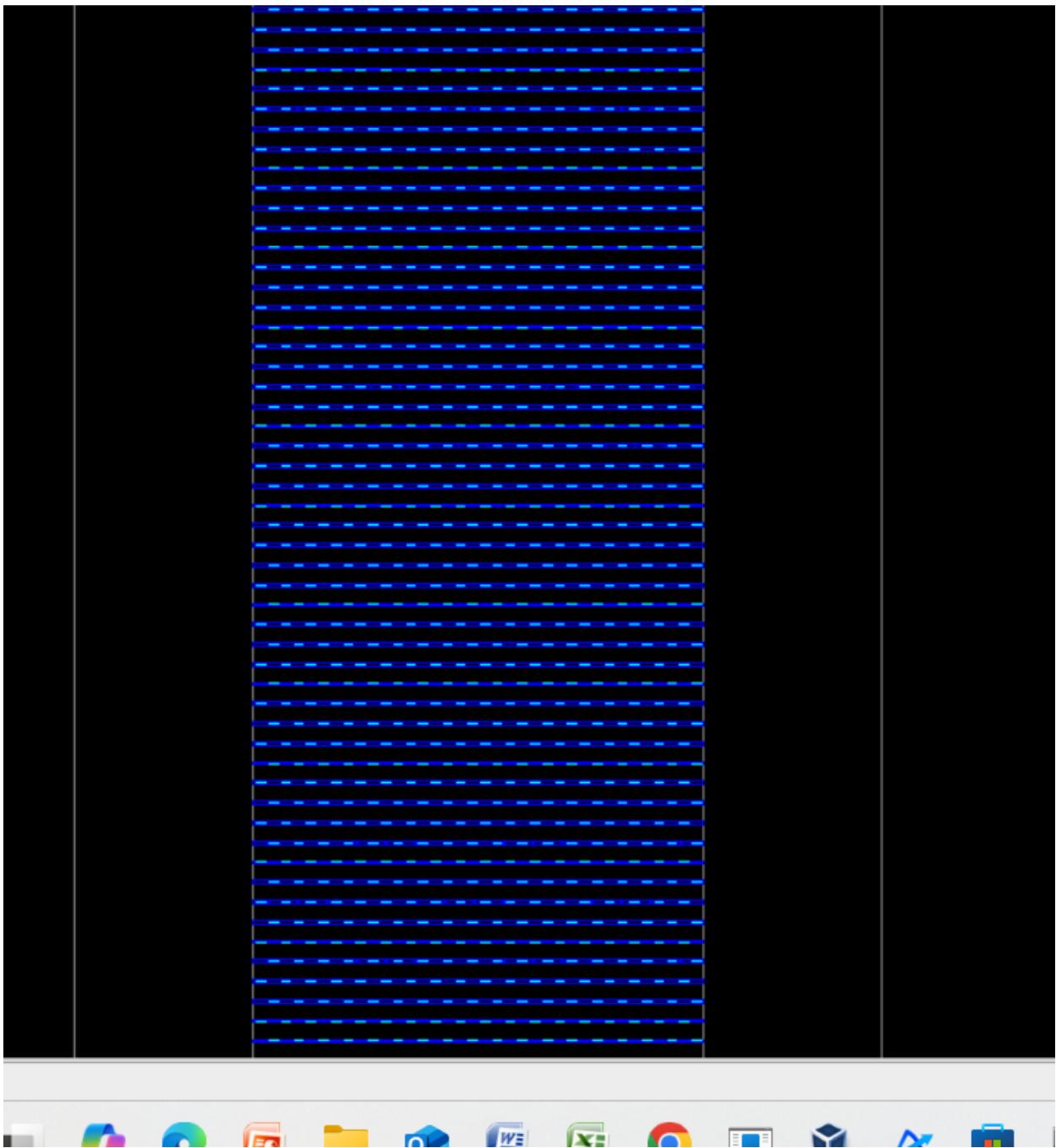
```
create_pg_mesh_pattern mesh -layers {{{vertical_layer:M7} {width:0.78}  
{spacing:interleaving} {pitch:2.1} {offset:0.7}} {{horizontal_layer:M8} {width:0.8}  
{spacing:interleaving} {pitch:2.5} {offset:0.8}}}  
  
set_pg_strategy core_mesh -pattern {{pattern:mesh} {nets:VDD VSS}} -extension {{direction:  
T L R B} {stop:innermost_ring}} -core  
  
compile_pg -strategies core_mesh
```



```
create_pg_std_cell_conn_pattern std_cell_rail -layers {M1} -rail_width 0.27
```

```
set_pg_strategy rail_stratery -core -pattern {{name:std_cell_rail} {nets:VDD VSS}}
```

```
compile_pg -strategies rail_stratery
```



```
read_sdc ./pico.sdc

set_app_options -name place.coarse.continue_on_missing_scandef -value true
```

```
create_mode func

create_corner slow

create_scenario -name func_slow -mode func -corner slow
```

```
read_parasitic_tech -tlup
"/data/pdk/pdk32nm/SAED32_EDK/tech/star_rcxt/saed32nm_1p9m_Cmax.tlupplus" -
layermap "/data/pdk/pdk32nm/SAED32_EDK/tech/star_rcxt/saed32nm_tf_itf_tlupplus.map"
-name p0

set_parasitic_parameters -late_spec p0 -early_spec p0
```

```
set_scenario_status func_slow -hold true -setup true -leakage_power true -max_capacitance
true -min_capacitance true -dynamic_power true -max_transition true -active true
```

```
read_sdc ./pico.sdc
```

```
create_mode func

create_corner fast

create_scenario -name func_fast -mode func -corner fast
```

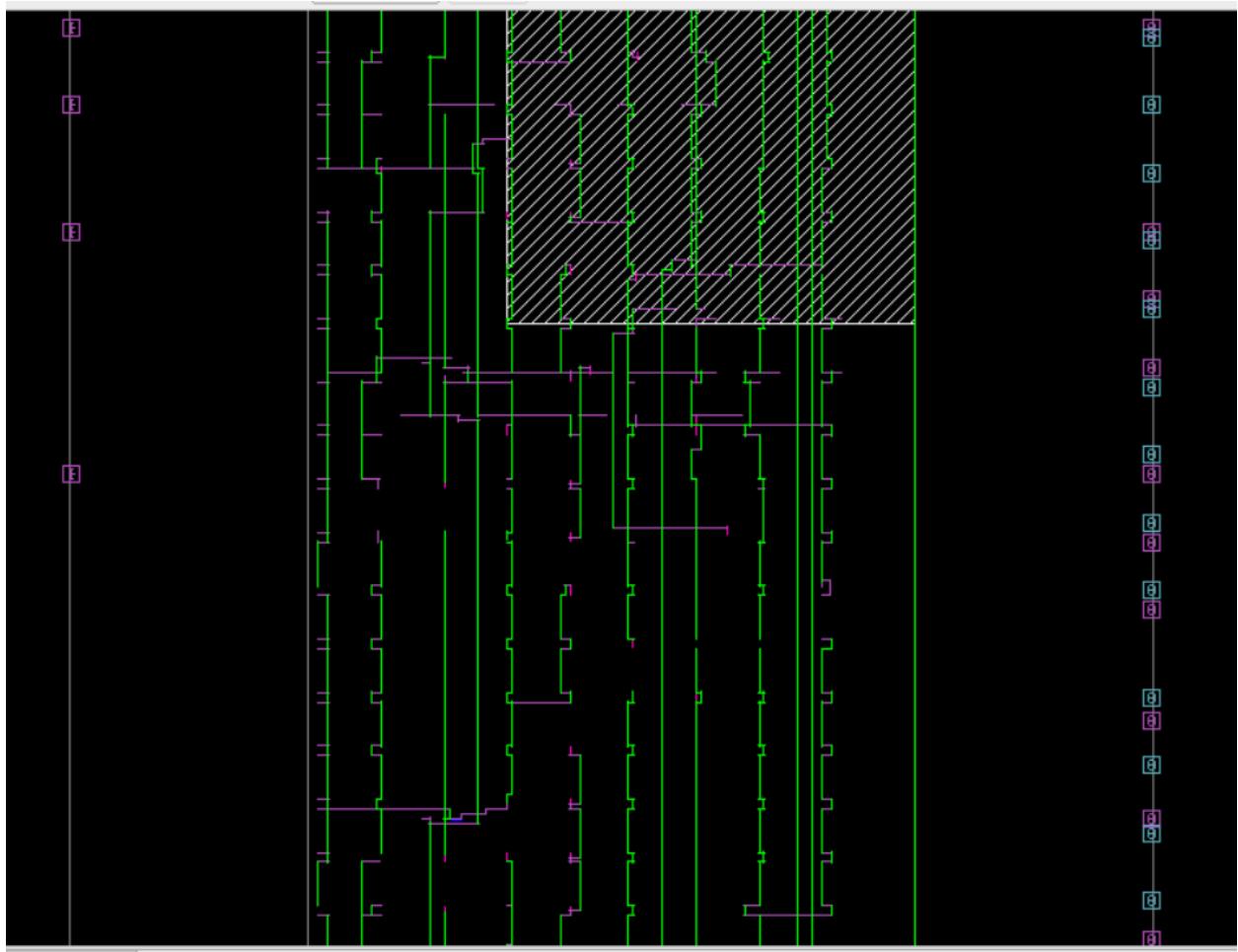
```
read_parasitic_tech -tlup
"/data/pdk/pdk32nm/SAED32_EDK/tech/star_rcxt/saed32nm_1p9m_Cmin.tlupplus" -
layermap "/data/pdk/pdk32nm/SAED32_EDK/tech/star_rcxt/saed32nm_tf_itf_tlupplus.map"
-name p1

set_parasitic_parameters -late_spec p1 -early_spec p1
```

```
set_operating_conditions -max_library  
"/data/pdk/pdk32nm/SAED32_EDK/lib/stdcell_rvt/db_ccs/saed32rvt_ss0p75v125c.db" -  
min_library  
"/data/pdk/pdk32nm/SAED32_EDK/lib/stdcell_rvt/db_ccs/saed32rvt_ff0p85v125c.db"
```

```
set_clock_routing_rules -min_routing_layer M3 -max_routing_layer M5 -default_rule  
read_sdc ./pico.sdc
```

```
set_scenario_status func_fast -hold true -setup true -leakage_power true -max_capacitance  
true -min_capacitance true -dynamic_power true -max_transition true -active true  
synthesize_clock_trees  
clock_opt
```



## 5.2 TASK 2 CTS ROUTING :

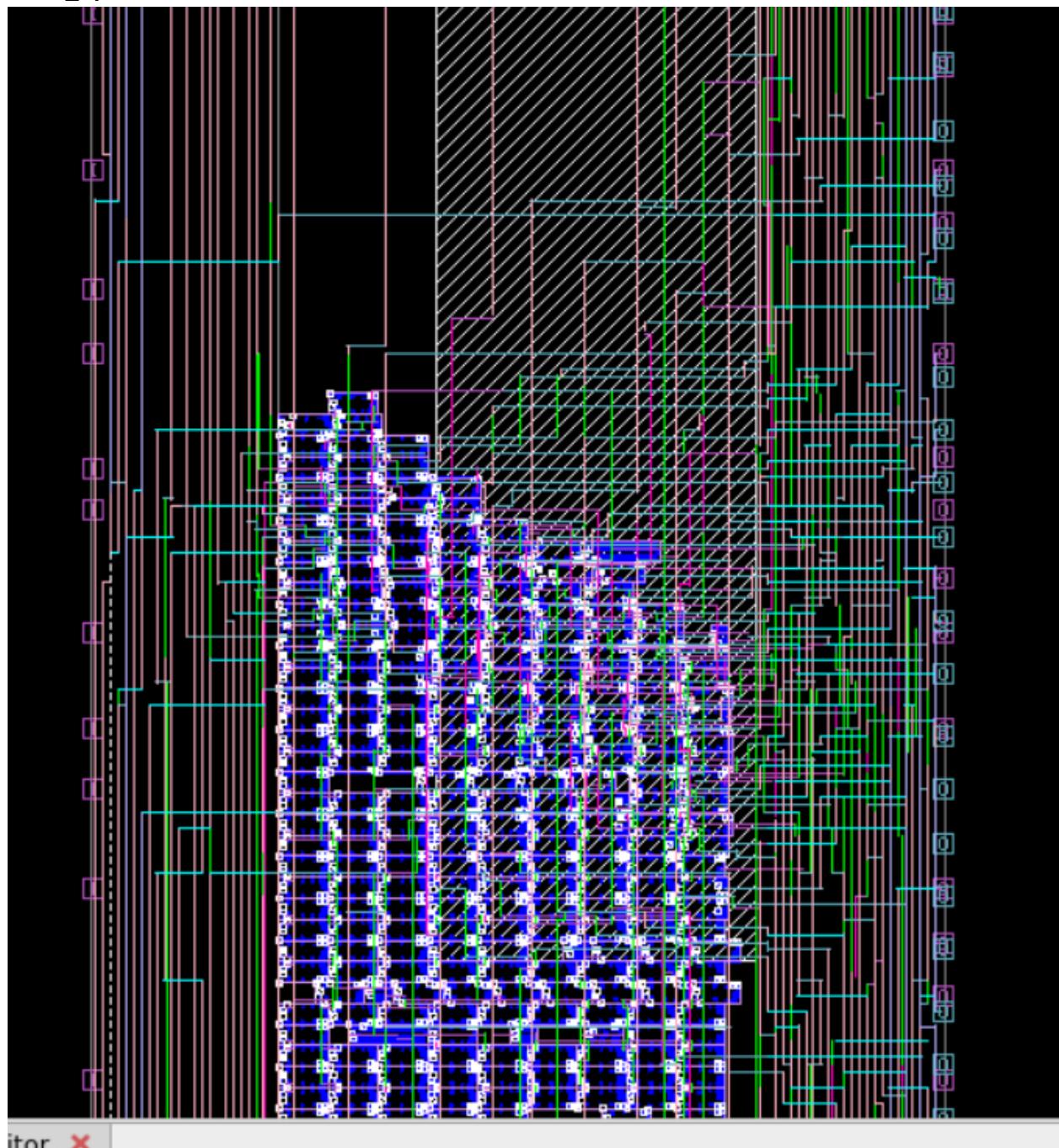
```
set_app_options -name route.global.timing_driven -value true  
set_app_options -name route.global.crosstalk_driven -value true  
set_app_options -name route.track.timing_driven -value true  
set_app_options -name route.track.crosstalk_driven -value true  
set_app_options -name route.detail.timing_driven -value true  
set_app_options -name route.detail.antenna -value true  
set_app_options -name route.detail.antenna_fixing_preference -value use_diodes  
set_app_options -block [current_design] -name route.detail.diode_libcell_names -value  
{/ANTENNA_RVT}  
route_global
```

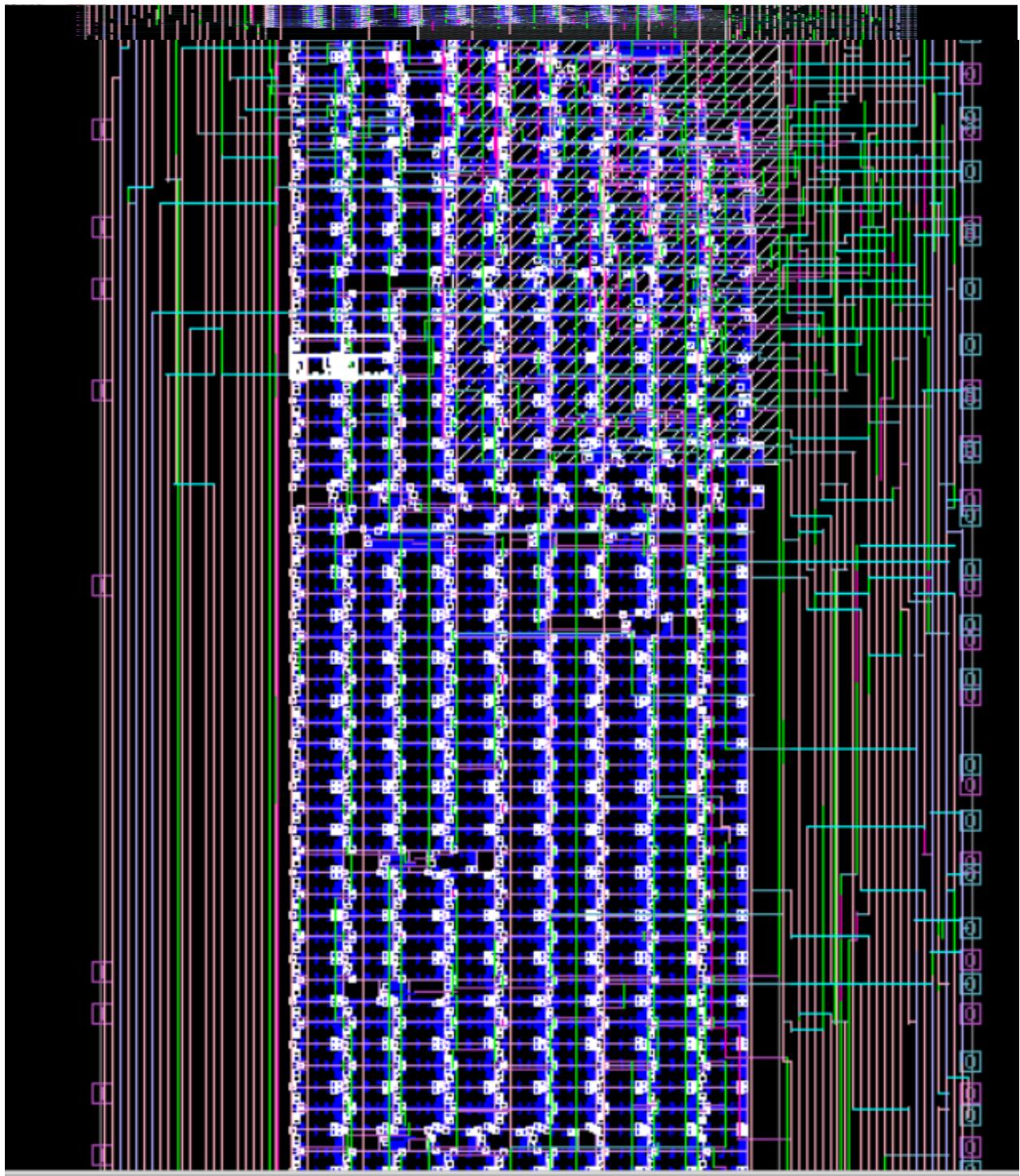
route\_track

route\_detail

```
set_app_options -name route_opt.flow.enable_ccd -value true
```

route\_opt





Startpoint: latched\_branch\_reg (rising edge-triggered flip-flop clocked by clk)  
 Endpoint: reg\_next\_pc\_reg[31] (rising edge-triggered flip-flop clocked by clk)  
 Mode: func  
 Corner: slow  
 Scenario: func\_slow  
 Path Group: clk  
 Path Type: max

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (propagated)	0.19	0.19
latched_branch_reg/CLK (DFFX1_RVT)	0.00	0.19 r
latched_branch_reg/Q (DFFX1_RVT)	0.23	0.43 f
U4591/Y (AND2X1_RVT)	0.10	0.53 f
U4297/Y (INVX1_RVT)	0.07	0.60 r
U4592/Y (NOR2X0_RVT)	0.07	0.67 f
U4585/Y (INVX1_RVT)	0.06	0.72 r
U4596/Y (NBUFFX2_RVT)	0.05	0.77 r
U4597/Y (OR2X1_RVT)	0.03	0.81 r
U4598/Y (OA21X1_RVT)	0.20	1.00 r
U4626/Y (NAND2X0_RVT)	0.01	1.01 f
U5115/Y (OAI21X1_RVT)	0.08	1.10 r
U5119/Y (AOI21X1_RVT)	0.05	1.14 f
U5120/Y (OAI21X1_RVT)	0.05	1.19 r
U5280/Y (AO21X1_RVT)	0.04	1.24 r
U6477/C0 (FADDOX1_RVT)	0.05	1.29 r
U6472/C0 (FADDOX1_RVT)	0.05	1.34 r
U6434/C0 (FADDOX1_RVT)	0.05	1.39 r
U6476/C0 (FADDOX1_RVT)	0.05	1.44 r
U6468/C0 (FADDOX1_RVT)	0.05	1.49 r
U6466/C0 (FADDOX1_RVT)	0.05	1.54 r
U6464/C0 (FADDOX1_RVT)	0.05	1.59 r
U5283/C0 (FADDOX1_RVT)	0.05	1.65 r
U5291/C0 (FADDOX1_RVT)	0.05	1.70 r
U6462/C0 (FADDOX1_RVT)	0.05	1.75 r
U5332/C0 (FADDOX1_RVT)	0.05	1.81 r
U6460/C0 (FADDOX1_RVT)	0.05	1.86 r
U6458/C0 (FADDOX1_RVT)	0.05	1.91 r
U6456/C0 (FADDOX1_RVT)	0.05	1.97 r
U6454/C0 (FADDOX1_RVT)	0.05	2.02 r
U6452/C0 (FADDOX1_RVT)	0.05	2.07 r
U6450/C0 (FADDOX1_RVT)	0.05	2.12 r
U4510/Y (XOR2X1_RVT)	0.06	2.18 f
U5334/Y (AOI22X1_RVT)	0.04	2.22 r
U4568/Y (OAI21X1_RVT)	0.15	2.41 f
reg_next_pc_reg[31]/D (DFFX1_RVT)	0.02	2.43 f
data arrival time		2.43
clock clk (rise edge)	2.00	2.00
clock network delay (propagated)	0.23	2.23
reg_next_pc_reg[31]/CLK (DFFX1_RVT)	0.00	2.23 r
clock uncertainty	-0.30	1.93
library setup time	-0.08	1.86
data required time		1.86
data required time		1.86
data arrival time		-2.43
slack (VIOLATED)		-0.57

```

-max_paths 1
-report_by design
Design : picorv32
Version: V-2023.12-SP4
Date   : Fri May  2 10:05:28 2025
*****



Startpoint: instr_jalr_reg (rising edge-triggered flip-flop clocked by clk)
Endpoint: mem_do_prefetch_reg (rising edge-triggered flip-flop clocked by clk)
Mode: func
Corner: slow
Scenario: func_slow
Path Group: clk
Path Type: min

Point                                Incr      Path
-----
clock clk (rise edge)                0.00      0.00
clock network delay (propagated)    0.18      0.18
                                         0.00      0.18 r
instr_jalr_reg/CLK (DFFX1_RVT)       0.00      0.18 r
instr_jalr_reg/QN (DFFX1_RVT)        0.11      0.29 r
U9556/Y (OA221X1_RVT)               0.07      0.37 r
mem_do_prefetch_reg/D (DFFX1_RVT)   0.00      0.37 r
data arrival time                   0.37

clock clk (rise edge)                0.00      0.00
clock network delay (propagated)    0.24      0.24
mem_do_prefetch_reg/CLK (DFFX1_RVT) 0.00      0.24 r
clock uncertainty                  0.10      0.34
library hold time                  -0.00     0.34
data required time                 0.34

data required time                  0.34
data arrival time                  -0.37
-----
slack (MET)                         0.03

```

Startpoint: instr\_jalr\_reg (rising edge-triggered flip-flop clocked by clk)  
 Endpoint: mem\_do\_prefetch\_reg (rising edge-triggered flip-flop clocked by clk)  
 Mode: func  
 Corner: fast  
 Scenario: func\_fast  
 Path Group: clk  
 Path Type: min

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (propagated)	0.18	0.18
instr_jalr_reg/CLK (DFFX1_RVT)	0.00	0.18 r
instr_jalr_reg/QN (DFFX1_RVT)	0.11	0.28 r
U9556/Y (0A221X1_RVT)	0.07	0.35 r
mem_do_prefetch_reg/D (DFFX1_RVT)	0.00	0.35 r
data arrival time		0.35
clock clk (rise edge)	0.00	0.00
clock network delay (propagated)	0.24	0.24
mem_do_prefetch_reg/CLK (DFFX1_RVT)	0.00	0.24 r
clock uncertainty	0.10	0.34
library hold time	-0.00	0.33
data required time		0.33
data required time		0.33
data arrival time		-0.35
slack (MET)		0.02

\*\*\*\*\*

Report : congestion

Design : picorv32

Version: V-2023.12-SP4

Date : Fri May 2 10:07:23 2025

\*\*\*\*\*

Layer	overflow			# GRCs has	
	Name	total	max	overflow (%)	max overflow
Both Dirs		9	1	9 ( 0.03%)	9
H routing		6	1	6 ( 0.04%)	6
V routing		3	1	3 ( 0.02%)	3

**Final View of design :**

